Scanning Test System Prototype of p/sFEB for the ATLAS Phase-I sTGC Trigger Upgrade

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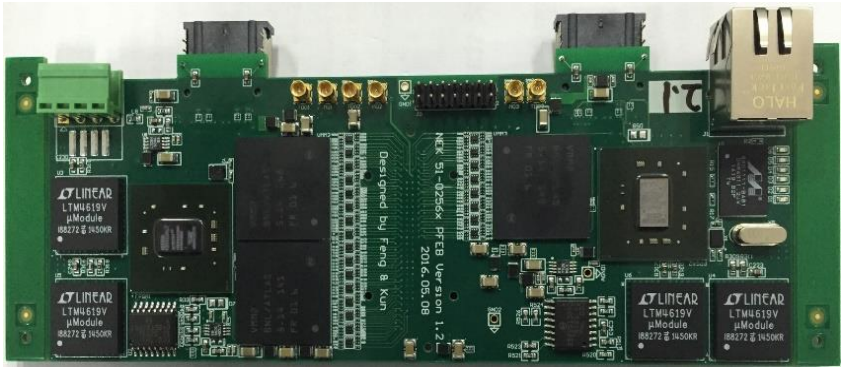
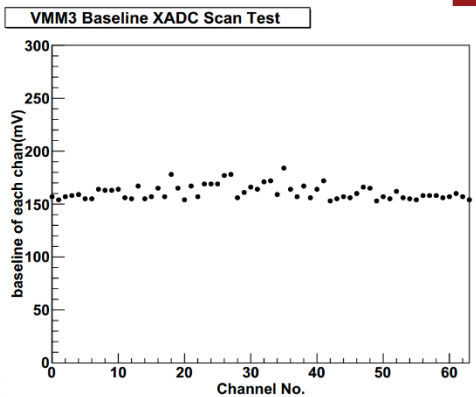
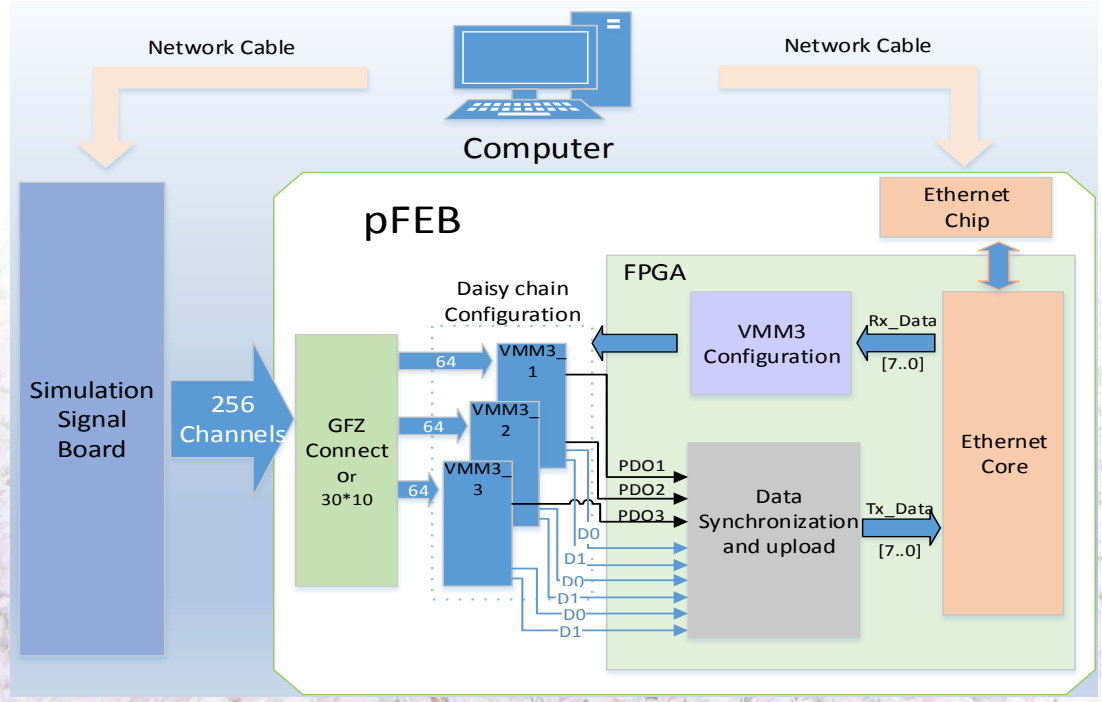
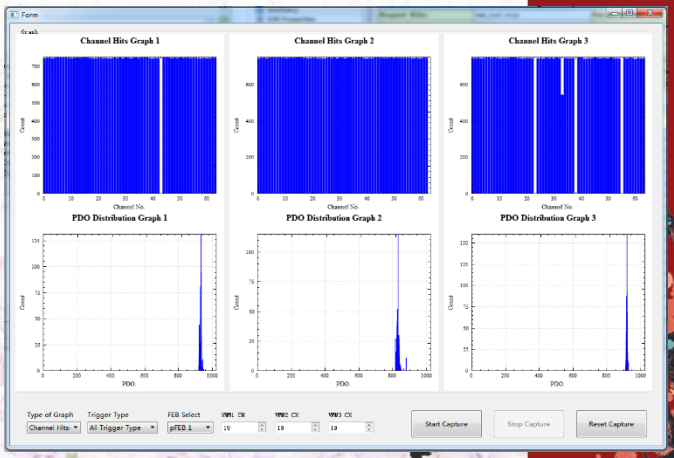


XADC Scan
baseline test
threshold DAC calibration
internal test pulse DAC calibration
Real time decode and display
dead channel test
gain test







Poster

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1.Introduction

ATLAS [1] detector which is one of the four experiments at Large Hadron Collider will fulfill Phase-I upgrade to extend the frontier of particle physics. The upgrade is going to replace the inner detector (Small Wheel, SW) [2] of the end-cap muon spectrometer with the "new small wheel" detector (NSW), which consists of the Small-strip Thin Gap Chamber (sTGC) [3] and Micromegas (MM).

STGC contains pad, wire and strip readout. The pads are used to identify muon tracks roughly pointing to the interaction point (IP) through a 3-out-of-4 coincidence and define which strips need to be readout to obtain a precise measurement in the bending coordinate for the event selection. The Pad Front End Board (pFEB) [4] is developed to readout pads signal to gather and analyze pads trigger. The Strip Front End Board (sFEB) [5] is developed to accept the pad trigger to define the regions-of-interest for strips readout. Both of pFEB and sFEB receive sTGC signals through the VMM3 [6],[7] ASIC which handles 64 input signals, and outputs the trigger data and raw data of hit events.

About 2000 p/sFEBs will be produced for final delivery and engineering backup. Before the p/sFEB are mounted on the detector, we need to confirm the performance of all the p/sFEBs. According to the function of p/sFEB in the whole system, the performance testing of each p/sFEB includes baseline test, threshold DAC calibration, internal test pulse DAC calibration, gain test and dead channel test.

We develop the scanning test system prototype of the p/sFEB. In this test system prototype , a simulation signal board is developed to generate different types of signal to the p/sFEB. PC software and FPGA XADC cooperate to achieve the scan test of analog parameter. The PC software is written based on Qt platform using the standard C++.

2.System Design

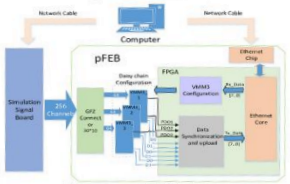


Fig.1 Block diagram of Test System Prototype

Fig. 1 is a block diagram of the test system. The p/sFEB includes three/eight VMM3 chips, one Kintex-7 FPGA for buffering VMM3 data, one Gigabit Ethernet Transceiver (GET), and connectors.The VMM3, which consists of 64 linear front-end channels, is an Application Specific Integrated Circuit (ASIC) for the detector. When the p/sFEB is connected to the sTGC detector, the analog signals from the sTGC detector are transmitted through the GFZ connector (10 * 30) to the p/sFEB and then into the three VMM3 chips via the protection circuit.

The simulation signal board [8] can be used to provide p/sFEB with 256/512 test pulses via the GFZ connector. In addition, the VMM3 chip can generate an adjustable amplitude test pulse signal internally. The pulse signal is sent to each linear front-end channel of the VMM3. The VMM3 chip outputs digital signal into the FPGA, and the FPGA completes the corresponding readout and analysis works. The FPGA communicates with a computer through the network cable, achieving the VMM3 initialization and data transmission.

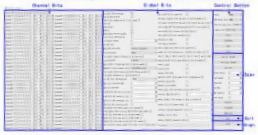


Fig.2 GUI of Test System Prototype

Each VMM3 chip requires 1728 configuration bits. Fig.2 shows the Qt-based GUI of the test system. The Qt-based GUI can complete the interaction between the computer and test board, automatic modification of parameters, issued commands and data acquisition. Pcap library is used to get access to Ethernet. In order to make the software run more smoothly and solve the problem of GUI stuck, the software uses a multi-threaded framework so that the data acquisition and user interface are built into different threads. Furthermore, this Qt-based GUI has the function of real-time data collection, analysis and display.

It is noteworthy that the outputs of 192/512 channels baseline test, threshold DAC calibration test, and internal test pulse DAC calibration test are analog signals. Without this scaning test system, an oscilloscope needs to be connected to the p/sFEB to read the analog value. Using an oscilloscope to test is very time-consuming and not easy to take multiple measurements on average due to the need of testing many channels. So our system uses XADC in FPGA for automatic scanning to complete these three tests, which can change the configuration bits and sampling by XADC automatically. Finally, the digital data outputs to the computer through the Ethernet, and then achieving the purpose of rapid

3.Test Result

Fig.3 is the construction of the test platform. After many tests, it is proved that the test system is reliable and can truly reflect the relevant characteristics of p/sFEB.

Fig.3 the Construction of Test System Prototype

The Qt-based GUI will collect the hit event raw data and decode them. Then display the corresponding information. Fig.4 shows the channel and amplitude test results for all the three VMM3s. In this GUI, the top three graphs displays hit event counts of VMM3 from channel 1 to channel 64, and the bottom three graphs display hits amplitude distribute information of one channel.We can find dead channels of each VMM from these graphs, and then further confirm this through another method to make the result more exactly.

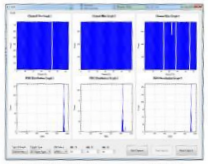
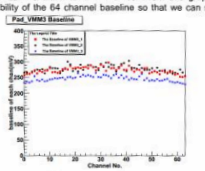


Fig.4 the real-time information display of VMM3

For the measurement of analog signals, we build the automatic scan test framework using some auxiliary analog inputs of the FPGA XADC. In this way, the analog signals can be measured several times to get the average value, which can increase the reliability and accuracy of the test result. Fig.5 and Fig.6 shows the result of baseline and threshold scan test of a VMM3 chip. Each channel tests 100 times. From this graph, we can get the consistency and variability of the 64 channel baseline so that we can set the threshold of VMM3 chip.



4.Conclusions

In this paper, we described the scanning test system prototype for p/sFEB in detail. In this test system prototype, a simulation signal board is developed to generate different typesof signals to the p/sFEB. PC software and FPGA XADC cooperate to achieve the scan test of analog parameter. With this system, we can test the circuit board quickly and reliably. In the early upgrade, the scanning test system is used for the p/sFEB performance test.

Introduction

System Design

Test Result

Conclusion

創寰宇學府
育天下英才
嚴濟慈題
一九八八年五月

中国科学技术大学
University of Science and Technology of China