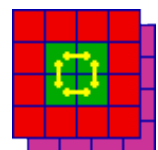
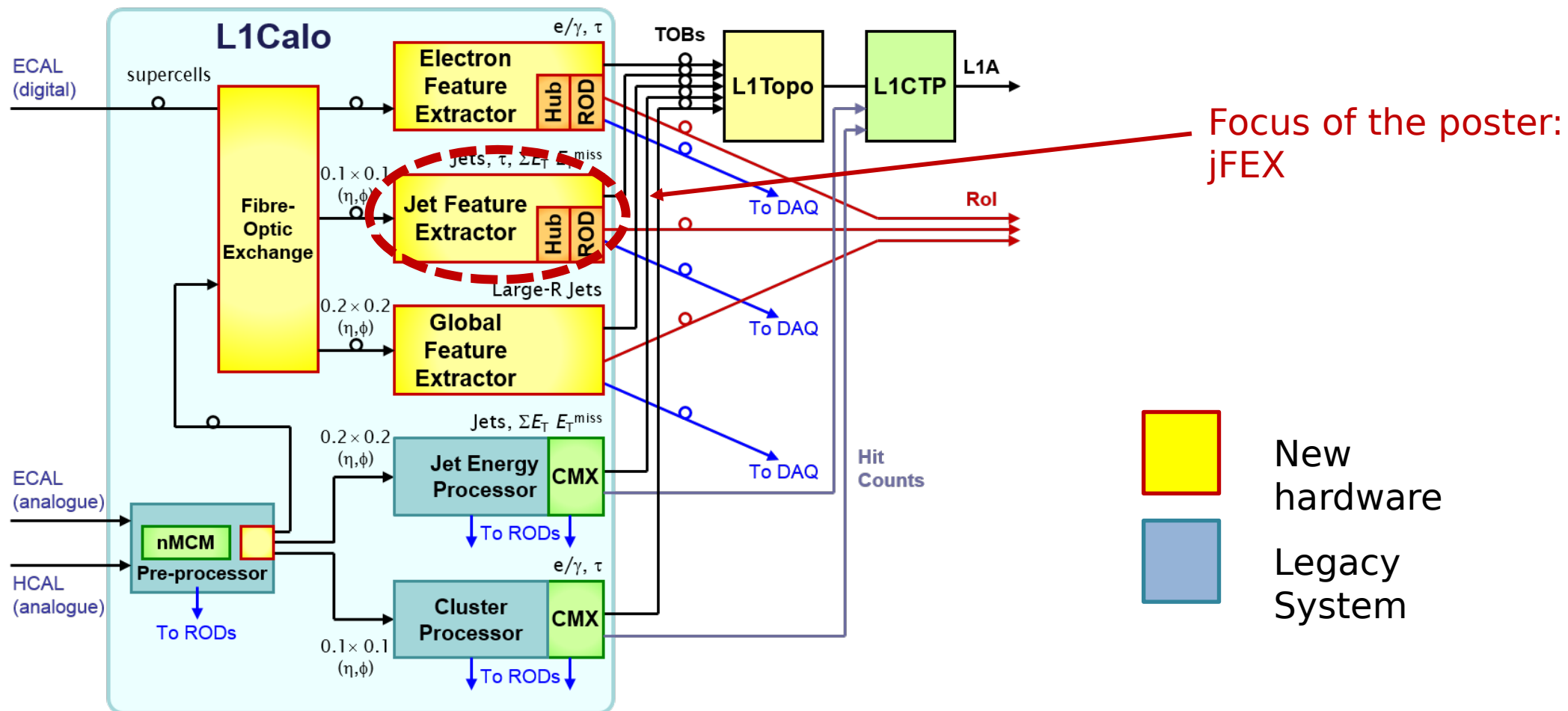


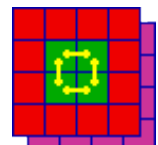
A new high speed, Ultrascale+ based board for the ATLAS jet calorimeter trigger system



PRiSMA
Cluster of Excellence

Phase-I ATLAS Level 1 Calorimeter Trigger system





GEFÖRDEBT VOM
Bundesministerium
für Bildung
und Forschung

A new high speed, Ultrascale+ based board for the ATLAS jet calorimeter trigger system

jFEX
DESCRIPTION

jFEX FIRMWARE

MOTIVATIONS

TEST RESULTS/
BOARD
CHARACTERISATION

The jFEX system will be produced by 2018 and installed and commissioned by start of Run3

Phase-I

The ATLAS experiment [1] has planned an upgrade to the LHC system for the Phase-I [2] period (from 2019 to 2023) to address the new challenging accelerator machine conditions, namely a luminosity $>2.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ and to maintain the sensitivity to electroweak physics without being affected by the increased number of pile-up events. The upgrade to the Level-1 Calorimeter (L1Calo) part of the system consists of three new Feature Extractor (FE) systems (electron FE (eFE), jet FE (jFE) and global FE (gFE)), which differ in the physics objects used for the trigger selection, which process digitised data from the calorimeters distributed by a new optical plant (FOK). At the start of LHC Run 3, during the commissioning of these new systems, the current legacy system will initially run in parallel before later being retired.

[1] ATLAS Collaboration, The ATLAS Experiment at the CERN Large Hadron Collider, JINST 3 (2008) S0903
[2] ATLAS TDAQ System Phase I Upgrade Technical Design Report arXiv:1404.0022

jFEX

Features: the jFEX consists of 6 modules with a η coverage of ± 4.9

Features:

- Modular design
- On-board duplication of input links using PMA loopback
- ATCA-based board
- 4 Xilinx Ultrascale+ (XC7U9P-2FLSA257T) per module
- 24 MiniPODs: 20 Rx + 4 Tx
- Control board on mezzanine
- Power on mezzanine
- Real-time data processing in fixed latency budget < 300 ns without any buffering

jFEX Characterisation

Characterisation of the Board B11000

JFEX measurement with Spectrum Analyser

Setup of the measurement with 240 inputs plus the 232 links with the PMA loopback for the data duplication on board. Electrical (dashed lines) and optical (solid lines) links.

Eye Diagrams of a single MGT link (worse case on the left, best case on the right). In both cases, **no link error was detected even for long measurement with BER < 10⁻¹²**.

Board	Subchannel	Current (A)	Temperature (°C)
U1	U1A	0.75	37.8
	U1B	0.85	38.2
	U1C	0.72	38.0
	U1D	0.80	38.1
U2	U2A	0.75	37.8
	U2B	0.85	38.2
	U2C	0.72	38.0
	U2D	0.80	38.1
U3	U3A	0.75	37.8
	U3B	0.85	38.2
	U3C	0.72	38.0
	U3D	0.80	38.1
U4	U4A	0.75	37.8
	U4B	0.85	38.2
	U4C	0.72	38.0
	U4D	0.80	38.1

Table of the board level voltage and PMA regulators with measured regulator temperatures.

Firmware

The jFEX identifies small/large area jets, jFEX tau, MET, ZE, using dedicated algorithms. Baseline versions of the algorithms have been implemented and successfully tested on hardware and integrated with R1DP infrastructure, with final versions implemented for large area jets and tau and for covering the full forward region.

The Trigger Objects (TOBs) are the algorithm results that will be sorted and then sent via optical links to the Level-1 Topological Processor (L1Topo), which will use these objects along with information from L1Muon to apply topological algorithms and kinematics cuts. The L1Topo results will be sent to the Central Trigger Processor (CTP) to build the overall L1 accept signal.

Step 1: Identification of local maxima. Done based on the 0.2 x 0.2 (x, y) granularity on the central region.

Step 2: Calculation of the Jet Energy Sum. Done based on the 0.2 x 0.2 (x, y) granularity on the central region.

Sorting: Local sorting of TOBs (FXGA core area) for each TOB type separately.

FPGA Resource Utilisation: Config: 104, DSP: 12, LUTs: 47, Forewarn: 121