The Design and Testing of the Address in Real Time Data Driver Card for the Micromegas Detector of the ATLAS New Small Wheel Upgrade

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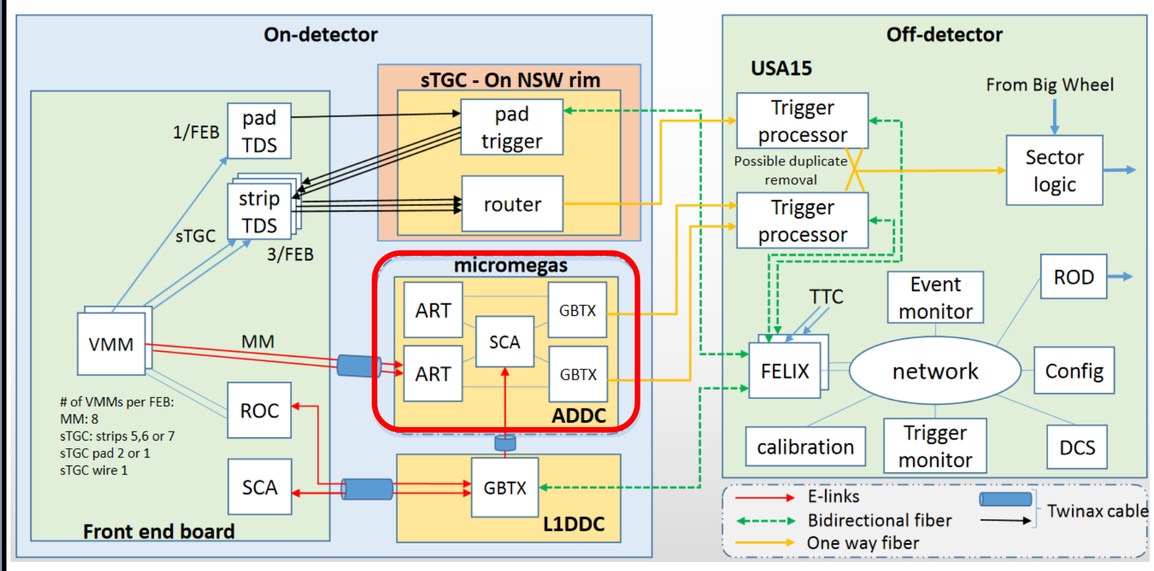
NSW Trigger and DAQ Electronics Scheme

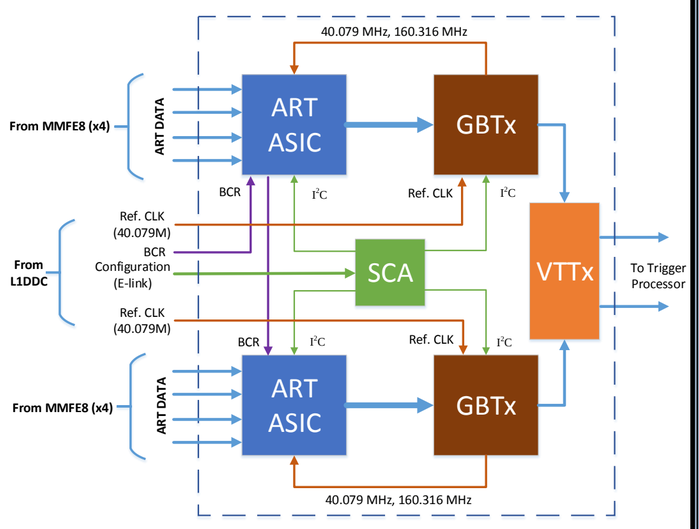
The scheduled ATLAS New Small Wheel(NSW) upgrade will be necessary to maintain high muon detection efficiency under the higher background radiation expected during Run-3 (2021-2023) and in HL-LHC (~2026). The NSW consists of two detectors, small Thin Gap Chamber (sTGC) and MicroMegas (MM) and both will contribute in the trigger decision. For the MicroMegas detector, the trigger primitive is the Address in Real Time (ART) signal, which is the 6-bit address of the strip with the earliest hit above a given threshold.



An important component of the trigger electronics is the ART Data Driver Card (ADDC), which interfaces with eight front-end boards, collects the produced ART data and process the hit selection. In total 512 ADDC boards will be mounted on the detector chamber along with the front-end electronics.

ADDC Structure and Functionality

The ADDC receives the ART signals from the front-end board, does a priority-based hit selection, and then sends the selected data to the back end trigger processor. The hit selection will be processed by a custom ASIC, the ART ASIC, within 1.25 bunch crossing (31.25 ns). Each ADDC has two ART ASIC to receive ART signals from 64 front end boards and the processed data will be sent to the GBTx serializer ASIC. The VTTx module collects the data from two GBTx ASICs and send them to the trigger processor through optic links. The CERN developed slow control ASIC, namely the SCA, is also used.



ADDC Block Diagram

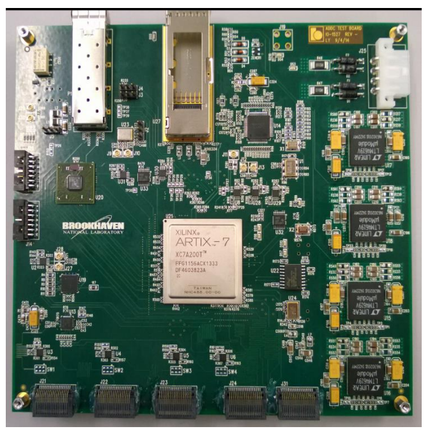
The main function of the ADDC is to:

- Receive ART data from up to 64 front end boards
- Achieve hit selection and send the selected data to MM trigger processor
- Receive the clock and configuration data from Level-1 Data Driver Card (L1DDC)

ADDC Prototypes

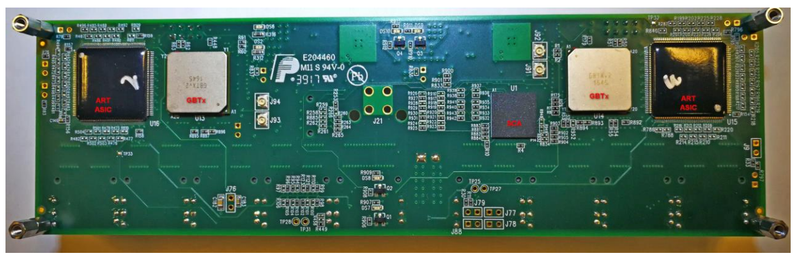
Before the ART ASIC is available, to evaluate the performance of the ADDC an FPGA-based prototype has been built at a smaller scale. It includes most of the major functional components while a Xilinx Artix-7 FPGA is used to emulate the ART ASIC. The HDL code of the ART ASIC has been ported to the FPGA for verification.

This prototype has half density of the final version ADDC, with one FPGA and one GBTx chip on board.



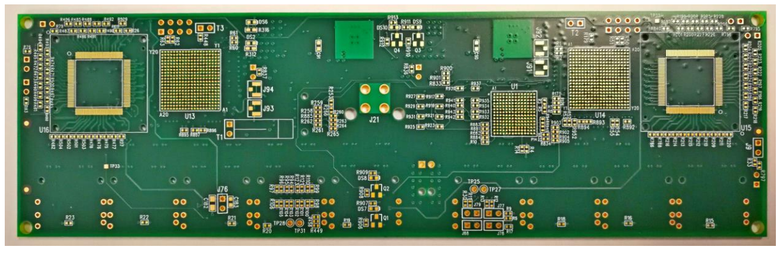
ADDC V1 Prototype (FPGA)

In the ADDC version 2 and version 3 prototypes, the dimensions are restricted and all the radiation-tolerant ASICs are evaluated. All the inductors and capacitors are carefully selected to ensure the performance under the radiation hard and strong magnetic field environment. These prototypes are also at the full scale to handle 64 channels of ART inputs. Several stand-alone and integration tests have been performed on these prototypes and the results are very positive.



ADDC Version 3 Prototype

In the version 2 and version 3 prototypes the ART ASIC uses the 144 pin LQFP package. However the yield rate of this package didn't not meet the expectation thus a 128 pin LQFP package is proposed as a replacement. The ADDC preproduction prototype design is revised to match the change of ART ASIC package. Various of tests are already planned for the preproduction prototype and once they are finished with positive results the massive production boards fabrication will start.



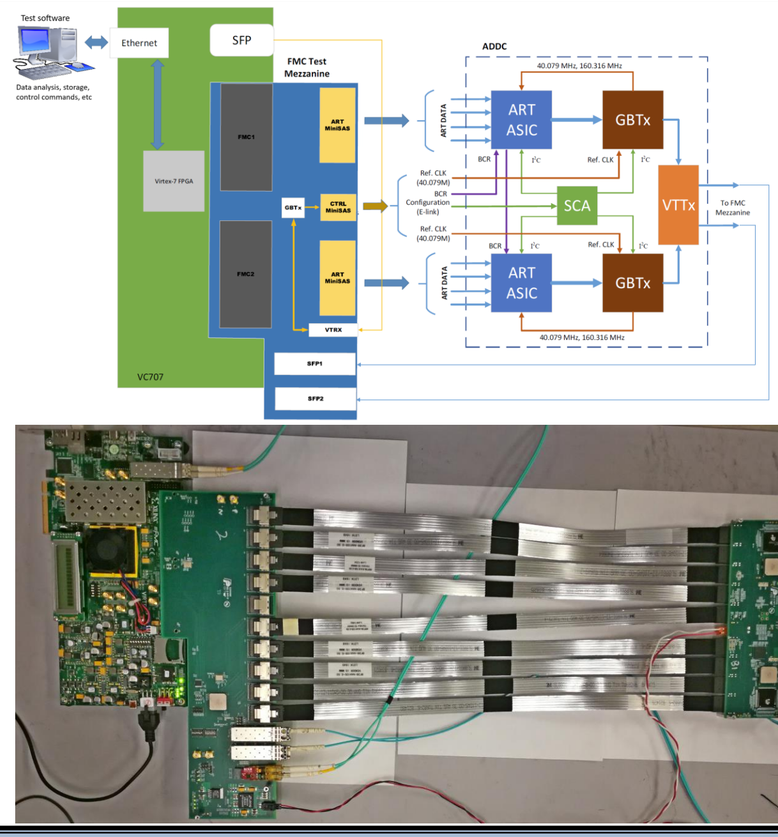
ADDC Preproduction Board Bare PCB

Testing of the ADDC

In the final stage more than 600 ADDC cards will be produced and tested. A FMC based test platform is designed to provide a complete test environment for the ADDC boards. This test platform works with the VC707 commercial develop kit, connects to the ADDC and will provide the simulated ART signals and configuration/clock signals to the ADDC board.

The Ethernet transmission and communication to the PC is achieved by the MicroBlaze soft microprocessor core. Another important component of the firmware is the customized GBT-FPGA module, which implements the configuration to the ADDC and also read the selected ART data for validation. On the computer side, a test software based on Python has been developed to communicate to the VC707 board through Ethernet. It provides fully automated configuration and testing of ADDC in order to minimize possible human errors.

This test platform has been used in the tests of the ADDC prototypes. The ART signal sending rate of the Virtex-7 FPGA to the ADDC is every three bunch crossing periods (75 ns) on all ART channels, which is much higher that the expected ART signal rate from the MicroMegas detectors. The test platform performs very well during these tests and with its help some defective engineering samples of the ART ASIC are recognized. When the final production of the ADDC is finished this platform will be used to guarantee the boards quality.



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