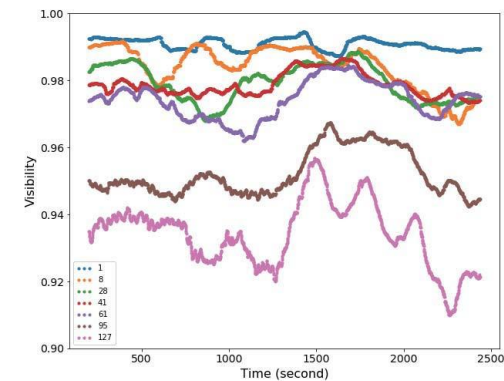
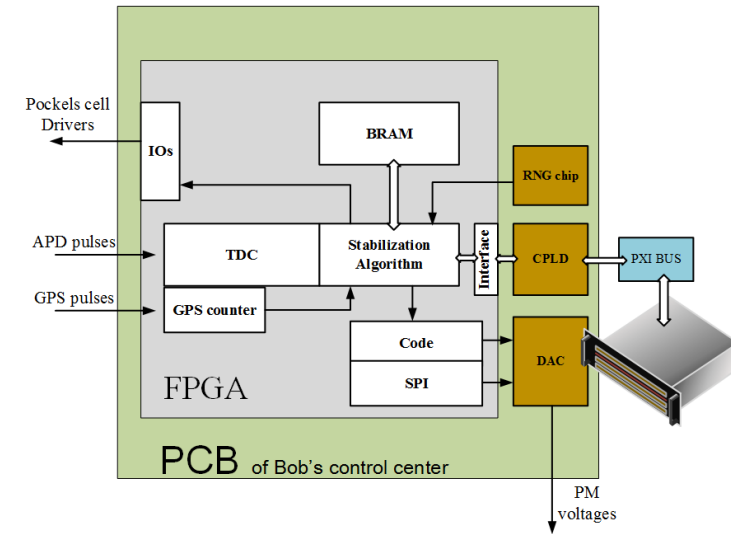
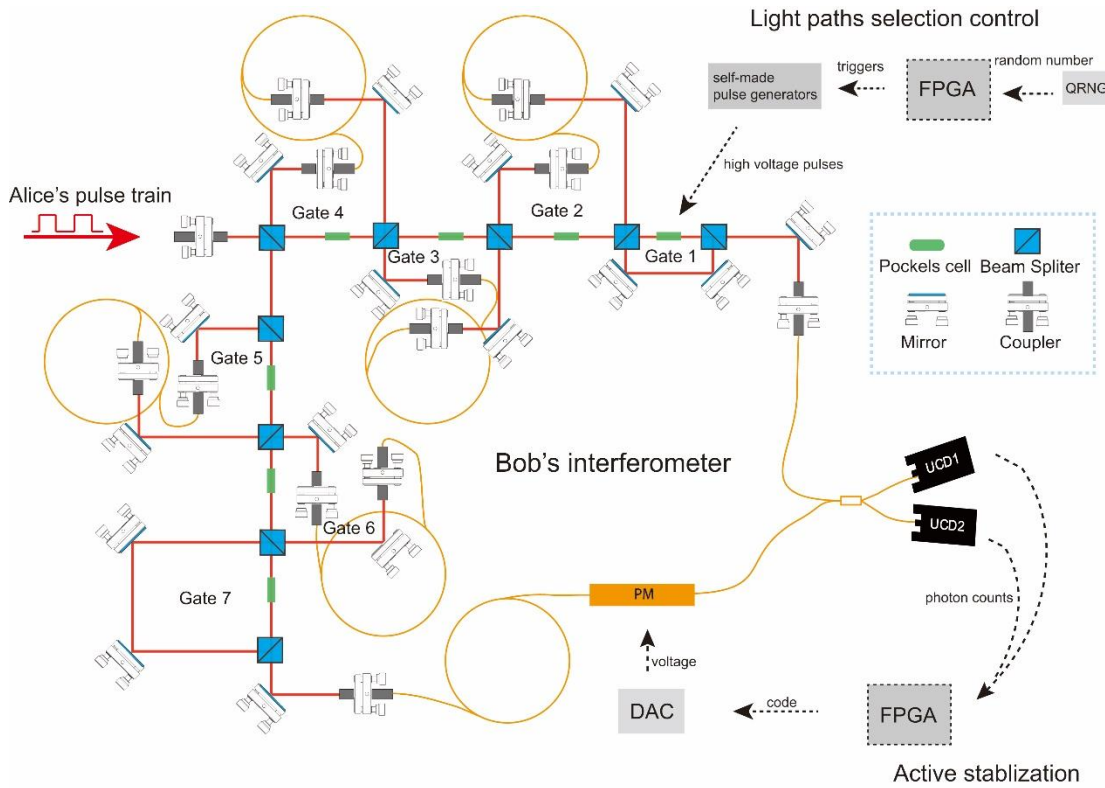


Technique of active phase stabilization for the interferometer with 128 actively selectable paths



No.468 Poster



Technique of active phase stabilization for the interferometer with 128 actively selectable paths



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1. Introduction

RRDPS QKD has advantage over the traditional Bennett, Brassard 1984 (BB84) protocol in terms of eliminating the fundamental, irreducible bit error rate of 1/4 [1]. The RRDPS protocol has a better tolerance of bit errors, which makes it easier to accomplish QKD in high noise background[2], such as the application of long distance free-space communication.

However, the implementation of the RRDPS scheme relies on the realization of a variable delay Mach-Zehnder interferometer, which is extremely sensitive to the mechanical and acoustic vibrations, temperature drift, etc. other disturbances [3]. These disturbances lead to phase imbalances between two arms of the interferometer. Although a few active stabilizing materials have been employed to envelop the interferometer as a passive protection, we still need a solution to eliminate the residual phase instabilities caused by the drift of the optical wavelength of the laser or other low frequency disturbances. Besides, a suitable phase should be maintained on PM immediately when a new light path is selected. Therefore, a system of active phase control with closed feedback loop is designed and put into use.

2. Experiment Design

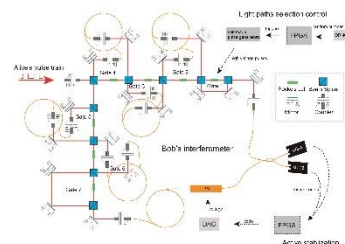


FIG. 1. 128 actively selectable Mach-Zehnder interferometer with active phase control.

168's choice 128 delays

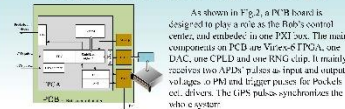
Because...in the RRDPS-QKD protocol, key rate is given by the formula:

$$R = \sum_{l=1}^L \sum_{m=1}^M \sum_{n=1}^N \sum_{k=1}^K \sum_{j=1}^J \sum_{i=1}^I \sum_{h=1}^H \sum_{g=1}^G \sum_{f=1}^F \sum_{e=1}^E \sum_{d=1}^D \sum_{c=1}^C \sum_{b=1}^B \sum_{a=1}^A$$

Where R is the final key bit per L -pulse train, larger L means higher tolerance of bit errors. For example, for $L = 128$, R is positive to $\alpha_{max} = 0.811$ [1].

128 light paths of different lengths should be prepared so as to achieve a discrete delay values $\tau = (0 \text{ ns}, 2 \text{ ns}, 4 \text{ ns}, 6 \text{ ns}, \dots, 254 \text{ ns})$ precisely. Seven delay gates access to seven optical fibers of different lengths are embedded in Bob's interferometer. Each gate switches under the control of a Pockels cell. A Pockels cell behaves like a half-wave plate at the half-wave voltage, in order to achieve fast switching between 0 V and half-wave voltage, which is around 2100 V in experiment, seven custom-built Ru-MgSiO₄ Li based high-voltage generators are employed to supply the square-shaped 2 kV pulses with repetition rate of 0 MHz. These generators are triggered by an FPGA Virtex-6 embedded in the Bob's control system. The trigger sequence are extended by a 7-bit random number generated by a RNG chip SNOW on-board during QKD process. As shown in Fig.1, thanks to the Bob's control system as well as the high voltage generators, the whole interferometer can transform into any one of the 128 light paths as soon as the random number changes, whose switching rate reaches 10 kHz.

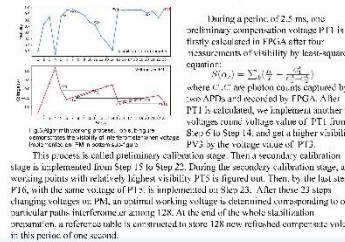
3. Hardware and logic Design



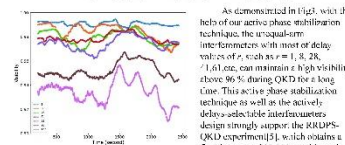
4. Stabilization Preparation

In order to realize real-time phase stabilization, Bob's control system is designed to refresh the optimal data for phase stabilization in first 340 ns of every second, which is named stabilization preparation stage. For each cycle t , an optimal composition voltage of PM, which is determined to adjust the relative phase between two arms of the interferometers, should be measured and recorded.

5. Stabilization Algorithm



6. Stabilization Result



References

[1] H. K. Lo, and J. Pook, Physical Review Letters, vol. 85, pp. 4411-4414, 2000.
 [2] Y. Zhang, W. H. Bao, C. Du, S. W. Li, S. Wang, and S. J. Han, Optics Express, vol. 24, pp. 2602-2607, 2016.
 [3] J. Lin, C. Z. Peng, and Y. Xu, Chinese Science Bulletin, vol. 61, pp. 111-114, 2016.
 [4] J. Lin, C. Z. Peng, and Y. Xu, Chinese Science Bulletin, vol. 61, pp. 111-114, 2016.

Introduction



Application



Hardware and algorithm design



Results

