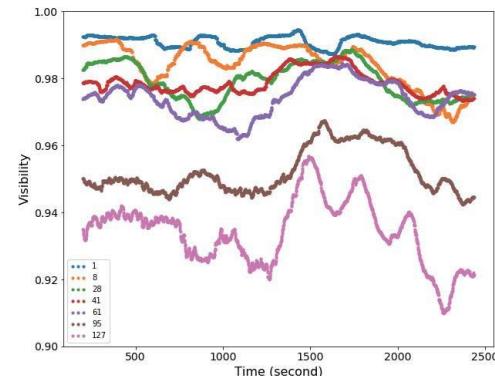
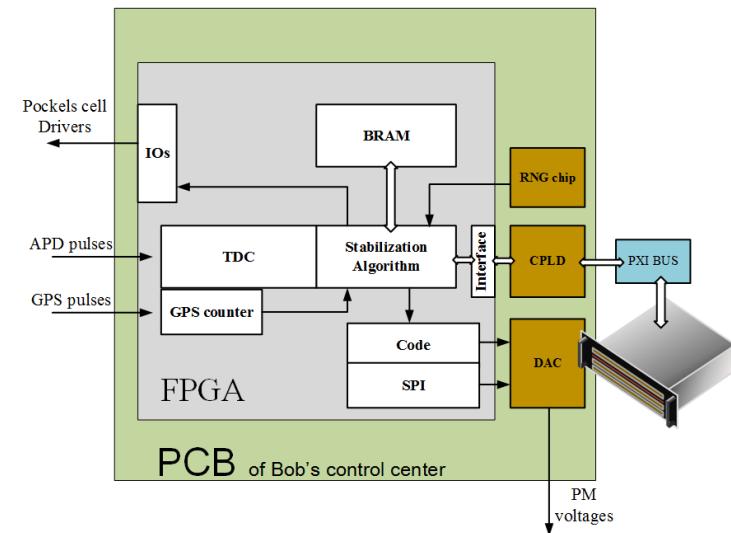
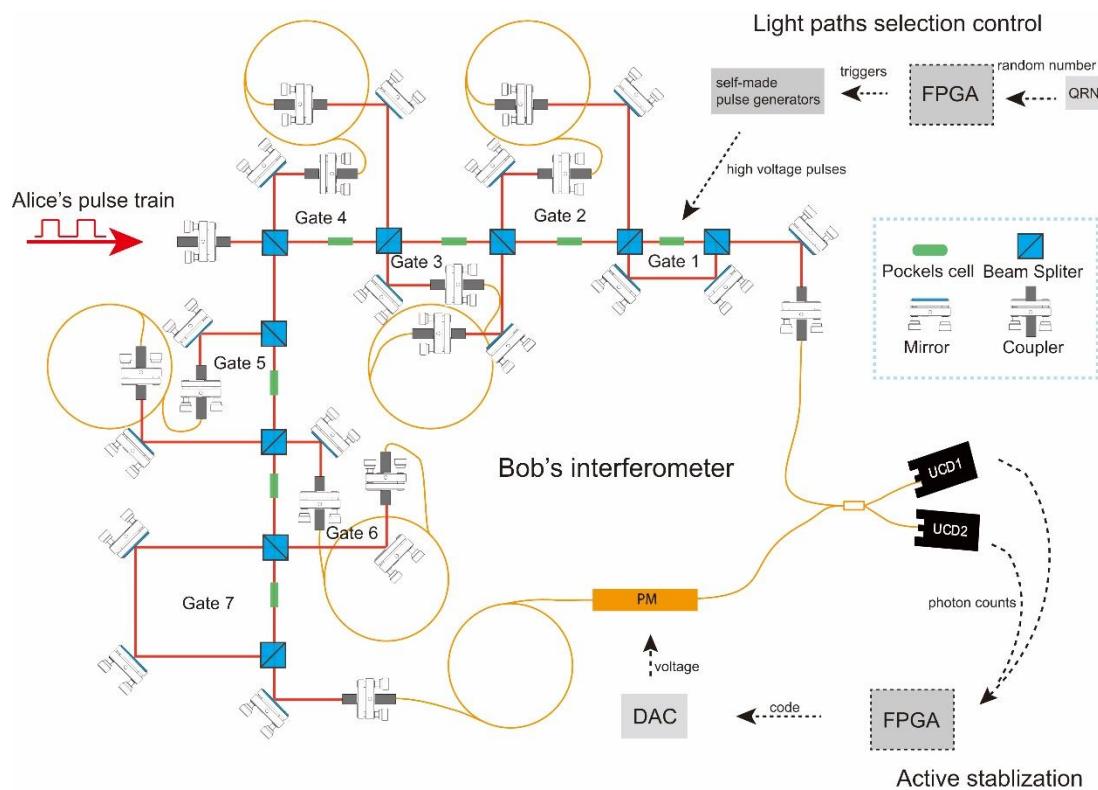




Technique of active phase stabilization for the interferometer with 128 actively selectable paths





No.468 Poster

Introduction →

Technique of active phase stabilization for the interferometer with 128 actively selectable paths

Yu Xu^{1,2}, Jin Lin^{1,2}, Yu-huai Li^{1,2}, Hui Dai^{1,2}, Sheng-Kai Liao^{1,2*}, Cheng-Zhi Peng^{1,2}
 (1) Hefei National Laboratory for Physical Sciences at the Microscale and Department of Modern Physics,
 University of Science and Technology of China, Hefei, 230026, China
 2. Chinese Academy of Sciences (CAS) Center for Excellence and Synergetic Innovation Center in Quantum Information and Quantum Physics,
 University of Science and Technology of China, Shanghai 201315, China

1. Introduction

BRDPS-QKD has advantages over the traditional BB84 protocol. Decohered BB84 protocol in terms of maintaining the fundamental threshold of bit error rate of 1/2 [1]. The BRDPS protocol has a better tolerance of bit errors, which makes it easier to accomplish QKD in high noise background[2], such as the application of performing distance free-space communications.

Jitter and drift of the 10Gb/s source clock, the influence of a variable delay of Mach-Zehnder interferometer, which is induced by the mechanical vibrations, temperature shift, etc. other factors, etc. [3]. These disturbances lead to phase imbalances between two arms of the interferometer. Although a series of high-damping materials have been employed to envelop the interferometer as a passive protection, we still need a solution to eliminate the residual phase instability caused by the drift and the external environment of the fiber or other laser frequency components. Recently, a suitable phase should be introduced in PMI immediately when a new light path is selected. Therefore, a system of active phase control with closed feedback loop is designed and put into use.

2. Experiment Design

Fig. 1 shows the schematic diagram of the 128 actively selectable path interferometer with Bob's control system.

3. Hardware and logic Design

As shown in Fig. 2, a PCB board is designed to play a role as the Bob's control center, and embedded in one PXIe slot. The main components on PCB are Virtex-6T FPGA, one DAC, one CPLD and one RNG chip. It mainly receives the APD pulses as input and outputs voltage to PMI and trigger pulses for Pockels-cell driver. The GPS pulse synchronizes the whole system.

4. Stabilization Preparation

In order to realize real-time phase stabilization, Bob's control system is designed to refresh the optimal data for phase stabilization in first 340 ms of every second, which is named stabilized preparation stage. First, calculate an optimal compensation voltage of PMI, which is dug up to adjust the relative phase between two arms of the interferometers, should be measured and recorded.

5. Stabilization Algorithm

During a period of 2.2 ms, one stability compensation voltage P11 is firstly calculated in FPGA after four measurements of visibility by least-squares equation:

$$S(\alpha_1) = \sum_i (y_i - \frac{1}{2})^2$$

where y_i are photon counts captured by two APDs and recorded by FPGA. After P11 is calculated, the average compensation voltage value of P11 from Step 6 to Step 14, and get a higher visibility P13 by the voltage value of P12.

This process is called pre-measurement calibration stage. Then a secondary calibration stage is performed in Step 15 to Step 22. In the second calibration stage, a working point with relatively highest visibility P15 is figured out. Then, by the last step, P16, with the same voltage of P12, is implemented on Step 23. After these 22 steps, changing voltages on PMI, an optimal working voltage is determined corresponding to one particular path interferometer among 128. At the end of the whole stabilization preparation, a reference table is constructed to store 128 new refreshed compensation voltage in this period of one second.

6. Stabilization Result

As demonstrated in Fig.3, with the help of our active phase stabilization technique, the visibility of the 128 paths can be maintained at a level of about 95% for a long time. This active stabilization technique is very useful for the design of delay-selectable fiber interferometers, design support the BRDPS-QKD experiments[3] which contains a fine key rate of 15.52 bits with total loss of 16dB and an error rate of 8.7%

Fig. 1. 128 actively selectable path interferometer with Bob's control system

Fig. 2. Choose 128 delays

Recall... in the RRDPS-QKD protocol, key rate is given by the formula:

$$R = Q[1 - h(\omega_0) - h(\frac{\omega_0}{\omega_1})]$$
 Where R is the final key bit per t -pulse train, larger t ensures higher tolerance of bit errors. For example, for $t=128$, R is positive to $\lambda \omega_0 = 0.33$ [1].

128 "light paths" of different lengths should be prepared in advance. A discrete delay values of 0 to 127 are used in this poster. Several delay gates access to several types of different lengths are realized in Bob's interferometer. Each gate switches under the control of a Pockels cell. A Pockels cell behaves like a half-wave plate at the half-wave voltage. In order to achieve fast switching between two half-wave voltages, which is around 2100 V in experiment, seven custom-built RI-MOSFET U1 homojunction diodes are used to switch the voltage of the Pockels cell at a rate of 1000 pulses with repetition rate of 16 kHz. These generators are triggered by an FPGA system embedded in Bob's control system. The trigger sequence are encoded by a 7-bit random number generated by a RXC chip WNG8 on board during QKD process. As shown in Fig. 1, thanks to the Bob's control system as well as the high voltage generators, the whole interferometer can transform any one of the 128 light paths as soon as the random number changes, whose switching time reader 100 ns.

References

[1] W. Ren, J. G. Fossel. Physical review letters, 96, 040502
 [2] Y. Zhang, W. S. Bao, C. Bai, B.W. Li, T. Wang, and M.S. Jiang. Optics express, 24, 20–39 (2016).
 [3] J. Xu, Y. Zhang, and M. Guo. Nature Sci. Discov., 1(1), 1–10 (2013).

←
Hardware and
algorithm design

Application →

← Results

Yu Xu