

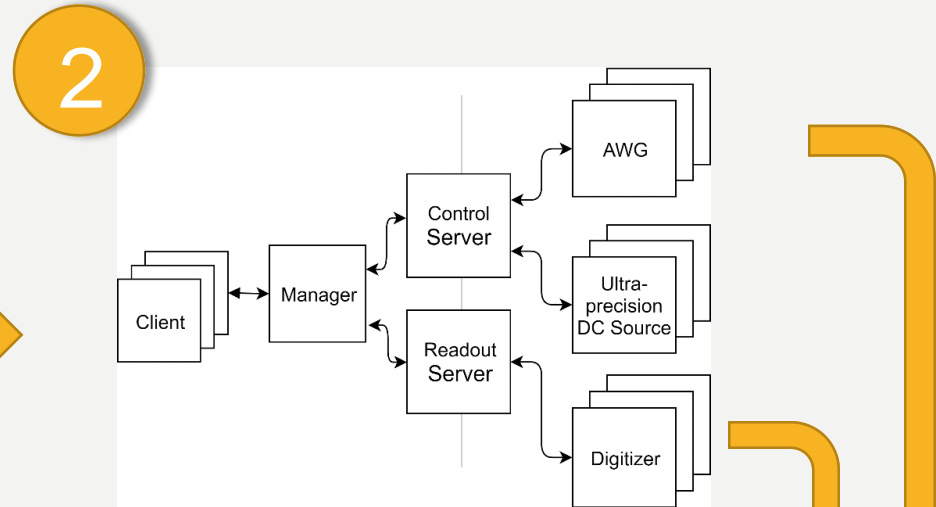
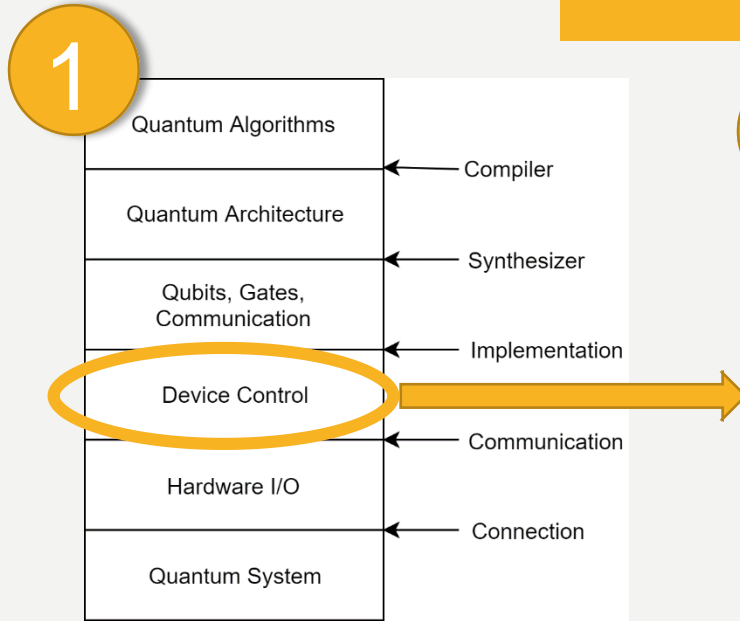
# Control and Readout Software in Superconducting Quantum Computing



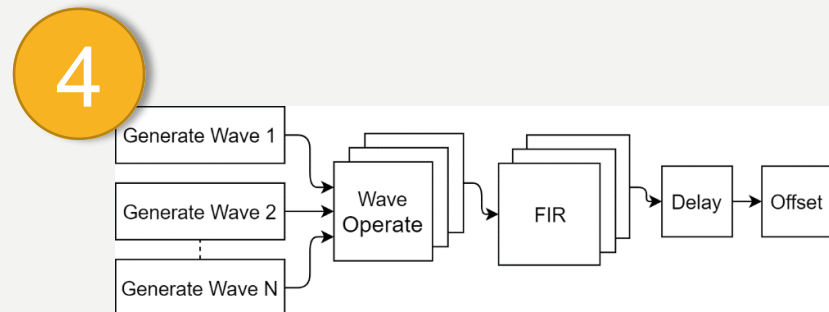
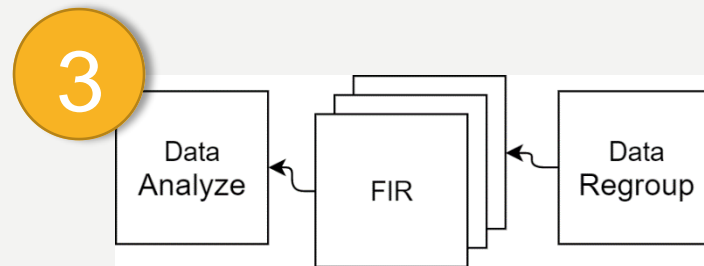
**Author: Cheng Guo**

**Speaker: Jin Lin**

# The Software Architecture



- 1) Layering of quantum computer
- 2) The structure of Device Control layer
- 3) Managing the readout signal from digitizers
- 4) Managing the waveform for AWGs



# The Poster



## Control and Readout Software in Superconducting Quantum Computing

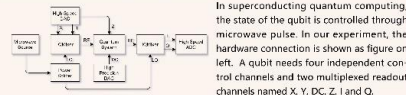


Cheng Guo<sup>1,2</sup>, Fu Tian Liang<sup>1,2</sup>, Jin Lin<sup>1,2</sup>, Yu Xu<sup>1,2</sup>, Li Hua Sun<sup>1,2</sup>, Sheng Kai Liao<sup>1,2</sup>, Cheng Zhi Peng<sup>1,2</sup>

1. Hebei National Laboratory for Physical Sciences at the Microscale and Department of Modern Physics, University of Science and Technology of China, Hefei 230026, China  
2. Chinese Academy of Sciences (CAS) Center for Excellence and Synergetic Innovation Center in Quantum Information and Quantum Physics, University of Science and Technology of China, Shanghai 201310, China

### I Introduction

Quantum computers can solve the problem that classical computers can not accomplish attributable to its parallel acceleration characteristics. Benefit from same manufacturing process used in the traditional semiconductor industry, superconducting quantum chips have good scalability and show promise in achieving a high degree of integration. Recently, high level quantum programming languages have been developed, QCL, Quipper, OpenQASM, the advent of these quantum programming languages, sketched out a picture of the quantum computer. However the underlying control of superconducting quantum computing has not been well studied due to device correlation.



In superconducting quantum computing, the state of the qubit is controlled through microwave pulse. In our experiment, the hardware connection is shown as figure on left. A qubit needs four independent control channels and two multiplexed readout channels named X, Y, DC, Z, I and Q.

The Z and DC are used to provide the bias condition of the qubit. The X and Y are IF signal directly synthesised by High speed DAC. IQMixer acts as a man-in-the-middle to upconvert controlling IF signals and downconvert RF readout signal. The bias of X and Y will lead to the leakage of local frequency. The imbalance of gain and phase will lead to the leakage of image frequency. The accuracy of the control signal is related to the microwave detuning which determines the upper limit of fidelity. The imbalance of IQ conversion is an issue that must be considered. As qubit experiments scale from single to multi-qubit, the complexity of channel control increases rapidly. Manipulating these signals is an important part of making a real quantum computer. We design the device control layer which focuses on automatic parameter calibration, equipment resources management and high-speed communication.

### III Readout and Control Server

In order to provide a consistent interface, we abstract a logic DAC with corresponding hardware resources regardless of the fact that the boards are physical independent. The logic DAC device have configurable coherent waveform output channels, trigger output channels and DC output channels, each channel can be configured individually. Control server is used to manage all available resources. The server will be responsible for maintaining the balance and coherent among the different channel.



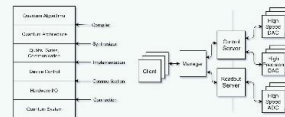
The control server can store a fixed number of waveforms, and we use the index number to address the waveform. Like the ALU in CPU, the waveform processing engine can generate sine, gauss, flattop, etc and provide addition, multiplication, integration, differential and so on. As left top figure show, after the waveform operations, there are several steps required before outputting the wave, which are designed to overcome the defects of hardware. Z square pulse signal is used to control flux bias of SQUID (superconducting quantum interference device). The sharp raise edge is important in this scenario and we can use a high bandwidth low pass filter to optimize the raise edge. For X and Y signals, they are connected to the IQ mixer to acquire a higher frequency, and the signals need to be calibrated to suppress local frequency and image frequency. For this application we can configure delay and offset to solve the problem. By individually configuring FIR filter, offset and delay of each channel, we can use channels for different purposes. The readout server is used to acquire and analysis data. Just like the control server, the logic ADC device have configurable coherent signal input channels and trigger input channels. As right top figure show, the readout server firstly combines the data frames captured from the Ethernet and then filters noise or equalizes frequency-domain, finally analyzes data and give the result.

### V Conclusion

Superconducting quantum computing requires a large number of AWGs. The high price of commercial AWGs limits its use on a large scale. In addition, commercial AWGs cannot meet the requirements of customization and rapid application change. It is a general trend to use cheap AWG. In recent years, some instrument companies have also joined in the development of new control devices for superconducting quantum computing. Keysight introduced M3202A/M3102A PXIe cards for synchronous control of ADC and DAC, BBN based on X6-1000M developed dedicated hardware for fast closed-loop feedback, Zurich Instrument launched UHF DigiDziber/HDAWG. Development of supporting software also has important value. This paper briefly introduced the layering stack of superconducting quantum computing and developed readout and control server for device control. We explained the application in quantum randomized benchmarking in the end. In the future, the software needs to be further expanded in terms of functions and layers. For functions, rapid closed-loop feedback is an important direction. As for layering, from device control to gate operation is an inevitable change.

### II Layering and Modularization

Considering bunch of instruments involved in superconducting quantum computing. It is necessary to develop a software platform for quantum computing. Layering and modularization have proven to be an effective way to overcome software development difficulties in the past. In our design, the layering stacks shown as figure on left bottom. The compiler is responsible for transforming the high level quantum algorithm to proper code in specified architecture. The function of synthesizer is making architecture specified code to logic qubit operation. Just like FPGA, the implementation act like a bridge of qubit operation to hardware control under the constraint of resources. The communication is used to maximize the data transmission efficiency of device. As for hardware connection, which is used to optimize the quality of the signal.



Modularization makes it available for different developers to independently maintain the corresponding code. We design two stand-alone servers based on modular concept in device control layer called readout server and control server as shown in top right figure. The waveform generation, calculation and analysis are deployed on the server. The client can easily access the service with the RPC protocol. Transmitting only instructions and calculation results can avoid massive data exchange, reducing the data forwarding pressure of the manager. The control server and readout server also separate the network.

### IV Randomized Benchmarking

The randomised benchmarking can be used to characterise the gate fidelity of qubit. As below figure show, in the reference test, the waveform engine produces  $m$  random sequences of gate operations from Clifford group, and then appending the unique recovery Clifford ( $C_r$ ) that inverts the sequence. For the interleaved test, each Clifford followed a gate operation to measure the extra error rate. At perspective of waveform manipulation, firstly the client randomly selects a qubit Clifford, then calculates parameters such as phase, amplitude, etc at a specific time, and next sends the command to the control server. The control server will generate corresponding waveform and store in a waveform register. The client continues to send instruction to generate and merge waveforms. After  $m$  cycle of operation then append a revert gate at the end. Secondly, After control server and the readout server is properly configured, the client sends a trigger command to launch the experiment. Finally, the giving DAC channels output the specified waveform synchronously and ADC channel estimates the state of qubit. Repeating the above procedure we can get error rate by counting the results and the operation fidelity can be calculated from the error rate.

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