Clock Distribution and Readout Architecture for the ATLAS Tile Calorimeter at the HL-LHC

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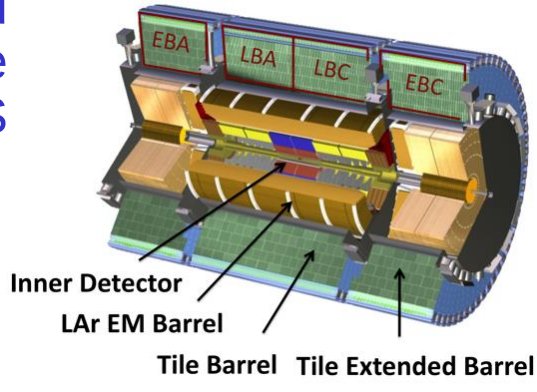
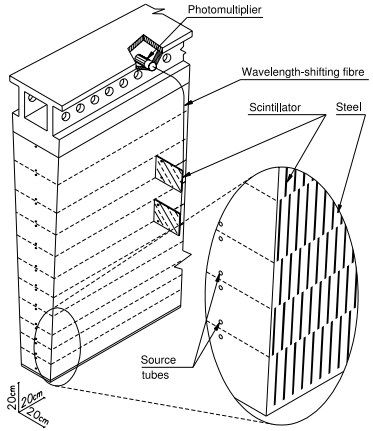
Introduction

- The Tile Calorimeter is a segmented calorimeter made of steel plates and plastic scintillator which covers the most central region of the ATLAS experiment
  - 4 partitions: EBA, LBA, LBC, EBC
  - Each partition has 64 modules → each module hosts up to 45 Photo Multiplier Tubes (PMTs)





	Present	Phase II
Total BW	**~205 Gbps**	**~40 Tbps**
N. fibers	256	4096
BW/module	800 Mbps	160 Gbps
Nb. boards	32	32
Nb. crates	4 (VME)	4 (ATCA)
In BW/board	6.4 Gbps	625 Gbps
Out BW/board$_{DAQ}$	3.2 Gbps	40 Gbps
Out BW/board$_{L0/L1}$	Analog	500 Gbps

- The LHC plans a major upgrade around 2024 → increase the instantaneous luminosity by a factor 7.5
  - Complete redesign of the detector electronics with a new readout strategy
  - All detector data will be transmitted to the off-detector electronics for every bunch crossing
  - Full granularity and digital inputs to the ATLAS trigger system

Demonstrator Upgrade project

- Evaluation the new readout architecture and trigger system interfaces before the HL-LHC
- One Demonstrator module equipped with the upgraded electronics and operated and read out with the PreProcessor module (TilePPr)
  - Upgraded readout architecture but keeping backward compatibility with the current DAQ system