Scalable Self-Adaptive Synchronous Triggering System in Superconducting Quantum Computing

Lihua Sun[1], Futian Liang[1,2], Jin Lin[1,2], Cheng Guo[1], Yu Xu[1], Shengkai Liao[1,2], Chengzhi Peng[1,2]

1.Hefei National Laboratory for Physical Sciences at the Microscale and Department of Modern Physics, University of Science and Technology of China, Hefei 230026, China

2. Chinese Academy of Sciences (CAS) Center for Excellence and Synergetic Innovation Center in Quantum Information and Quantum Physics, University of Science and Technology of China, Shanghai 201315, China

Abstract—Superconducting quantum computing (SQC) can solve some specific problems which are deeply believed to be intractable for classical computers. Synchronizing trigger is essential for SQC where the control and measurement of qubits can't go on without the synchronous operation of digital to analog converter array and the controlled sampling of analog to digital convertor. In this paper, a scalable self-adaptive synchronous triggering system is proposed to ensure synchronized operation among different qubits of SQC.

Introduction

As a distributed data converters array, superconducting quantum computing needs to solve the problem of synchronous operation of multiple qubits. Meanwhile, because the state of qubit is very sensitive to its microwave control signal, the signal must be stable and controllable, that is to say, the phase noise should be as small as possible.

Control and Measurement System of SQC

A quantum processor chip made from superconducting qubits works at an ambient temperature below 10mk provided by dilution refrigerator. The modulating signal from room temperature is transmitted to the chip after multistage refrigeration, attenuation and filtering . These modulating signals can be obtained by mixing up the microwave signals generated by the DAC-based arbitrary waveform generator(AWG) with the RF signals provided by the microwave sources.

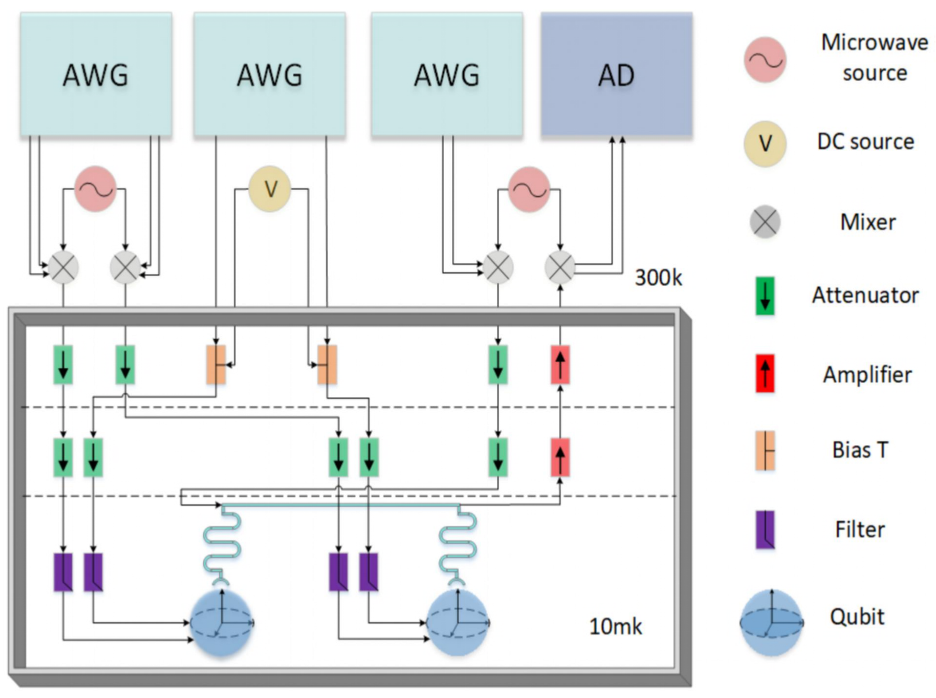

Fig 1. The Experiment Equipment of SQC

In the process of reading, a modulating signal is first input into the resonant cavity coupled with the qubits. Different states of qubits correspond to the different amplitudes and phases of the modulating microwave signal on the resonator. The state information of qubits can be obtained from the demodulated results of ADC after collecting the feedback microwave signal from the resonator.

The Design of Synchronizing Trigger System

A. The High-profermance Clock System

We design a scalable clock tree system in which a 10 MHz Rubidium clock is deployed as the root of the clock tree. The rubidium clock has multiple coherent 10MHz outputs, which is mainly used in three aspects: the first one is locked to 250 MHz by a clock gengertor HMC7044 and fan out to 56 by fan-out bufers HMC7043 to every AWG as the synchronous reference clock.

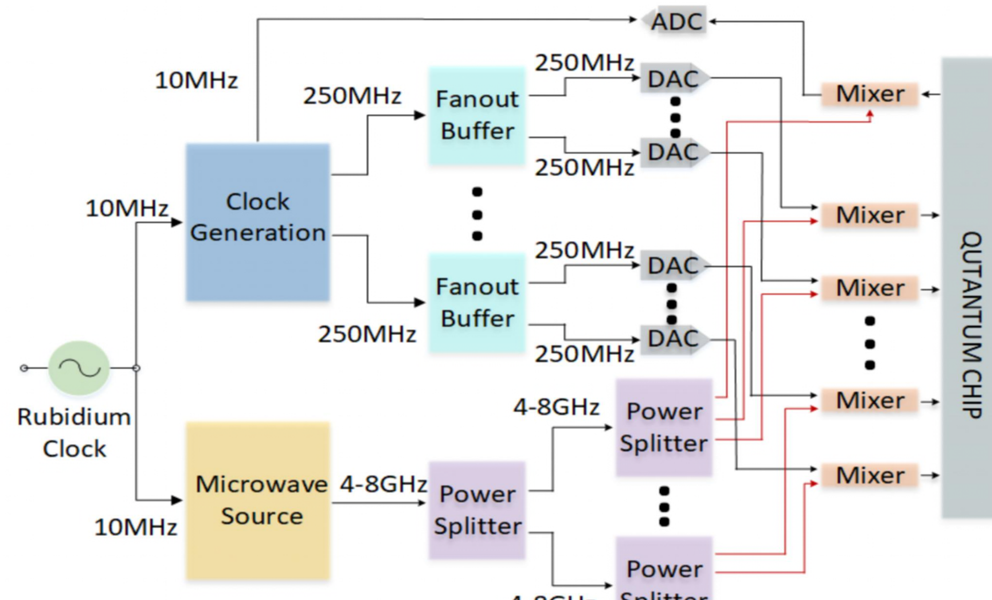

Fig 2. The Structure of Clock Tree

The second one is used as the reference clock of microwave source which is used to generate the 4-8GHz RF signal. Similarly, the RF signal is divided into multiple channels as the local signal of IQ mixer through the power splitter of multi-level tree struture. The last one is used as the clock source of ADC acquision board.

B. The Star-like Trigger Design

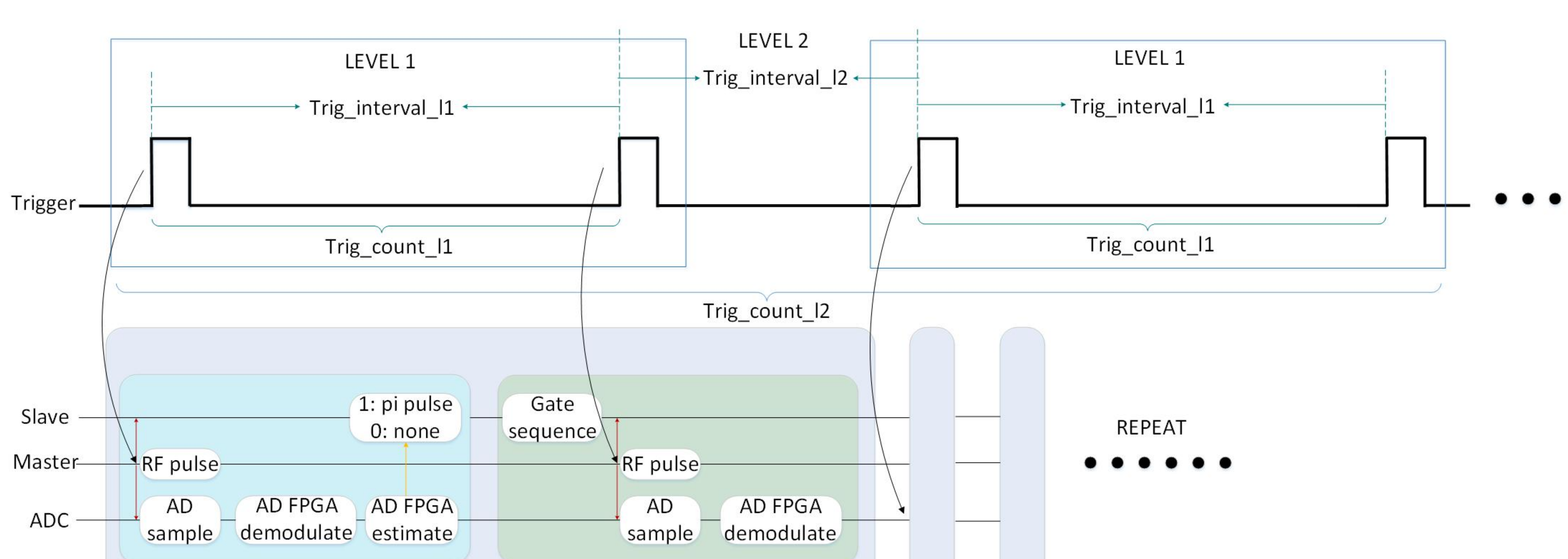

Fig 3. The Timing Diagram of Trigger Mechanism

Based on the Field Programmable Gate Array(FPGA) in self-developed AWG, we design a two-level trigger generation gateware elaborately that can support the qubit reset. It is a star-like structure based on the master-slave model, in which one of the AWG is set as master device and the others are slaves. When master receives a 'run' instruction from control-computer, it outputs a series of triggers with configurable counts and intervals(figure 3). These triggers are fanned out into multiplexed synchronous triggers to each AWG through the fan-out module shown in figure 4.

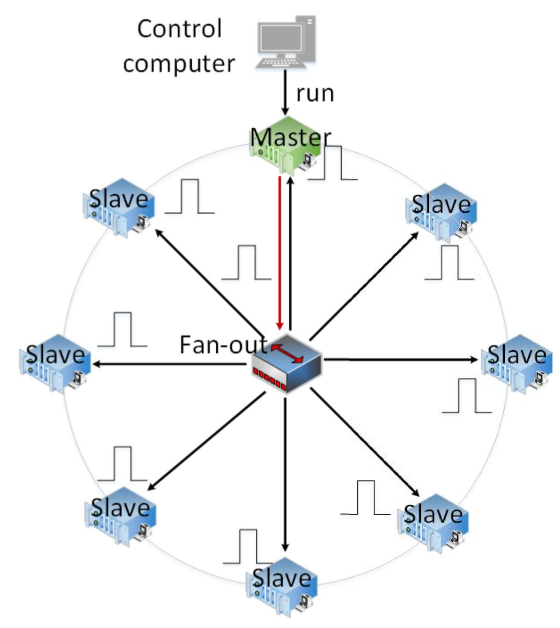

Fig 4. The Star-like Fanning Out Structure

The first trigger in level 1 instructs that the ADC reads the initial state of qubit and feeds it back to AWG. At the second trigger moment in level 1, the AWG decides whether to emit a pi pulse for qubit reset based on the state of qubit. This is a complete operation with a qubit reset. Level 2 is the repetition of operation in level 1.

C. The Self-adaptive Design

Under the master-slave trigger mechanism, the metastable phenomena is aninevitable problem. Based on the IDELAY/ODELAY resouces in FPGA, we proposed a self-adaptive method which can detect the meta-stability and calibrate it.

A cascade chain of up to 8 ns with 2 ODELAYE3 and 2 IDELAYE3 is designed to realize the delay adjustment of at least two 250M clock cycles. By adjusting the output delay of the trigger from master, we can find a stable region away from the metastability.

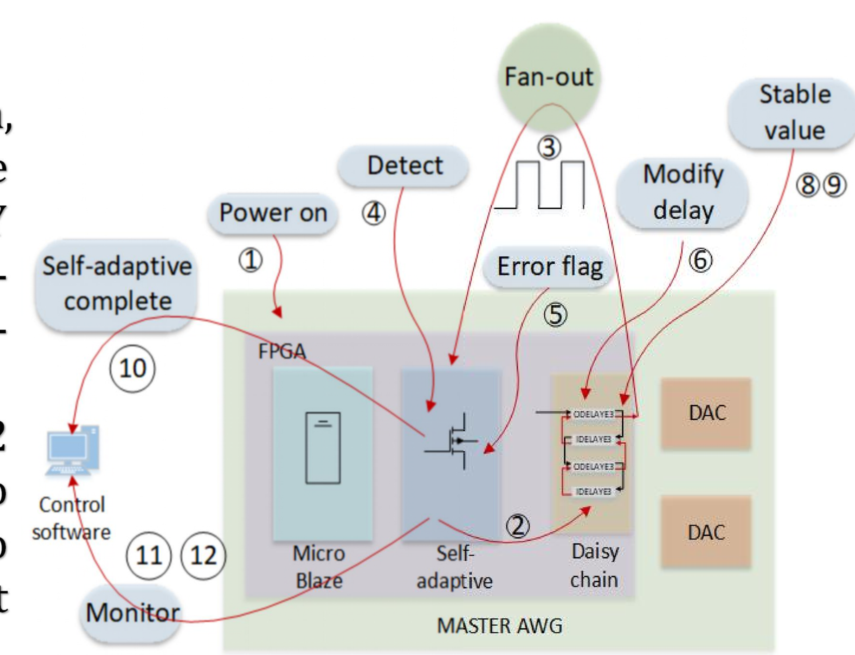

Fig 5. The Process of Self-adaption

Test Results and Analysis

A. The Test of Clock System

We carry out a comparison test using the original ordinary clock design and the proposed high-performance clock solution, which is shown in figure 6. The curren design can bring an improvement of about 15dB in phase noise of DAC output and an improvement of about 6 dB in phase noise of RF signal in an offset range of 1k to 2MHz.

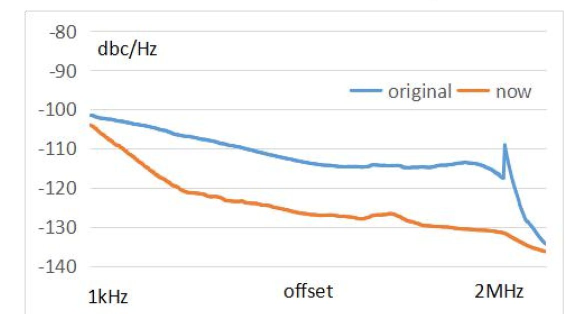

Fig 6.a Phase Noise Comparision of DAC Output

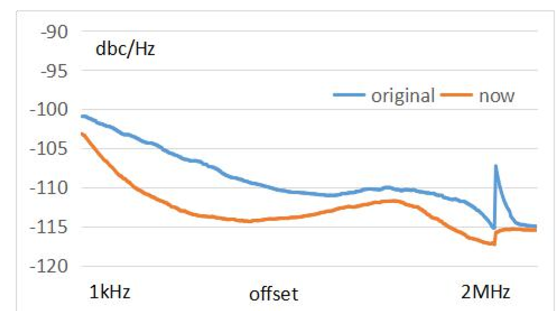

Fig 6.b Phase Noise Comparision of RF Output

B. The Test of Self-adaption

We record the probability of metastable phenomena for each modification of the trigger output delay. The results show that traversing a 4 ns clock cycle needs a modification of about 215 times, 6 of which are companied by a high probability of metability.Therefore, there are about 111 ps unstable interval in this system.

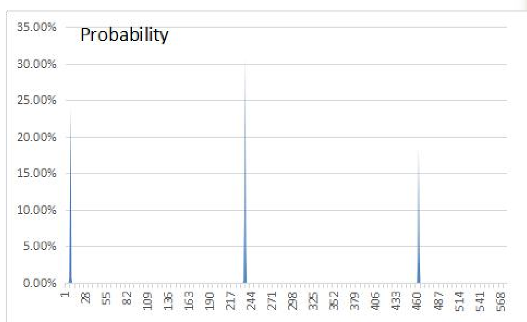

Fig 7 The Probability of Metability

C. The Test of Synchronization

A synchronization test with 10 AWGs is present in figure 8. Results show that a synchronization of less than 25 ps is achieved without addition adelay adjustment.

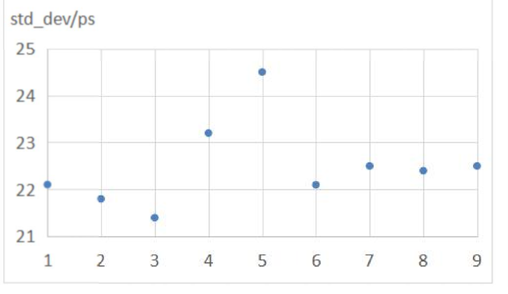

Fig 8 Skew Between 10 AWGs

Conclusion

In this paper, a scable synchronous trigger system is proposed to ensure synchronized operation of qubits in SQC. First, a high-performacne clock system is designed to serve as a physical structure of the proposed two-level trigger method. This clock scheme can bring about a phase noise improvement of about 15 dB for AWG output and an improvement of about 6 dB for the RF control clock of qubits. Then a scalable master-slave star-like trigger method is proposed, which can realize the synchronization of dozens or hundreds of qubits with the synchronization precision lesson than 25ps. Finally, an self-adaptive solution is proposed to detect and calibrate the metastability that ensure the synchronization of multiple AWGs.