Development and Characterization of a 3.2 Gb/s Serial Link Transmitter for CMOS Image Sensors

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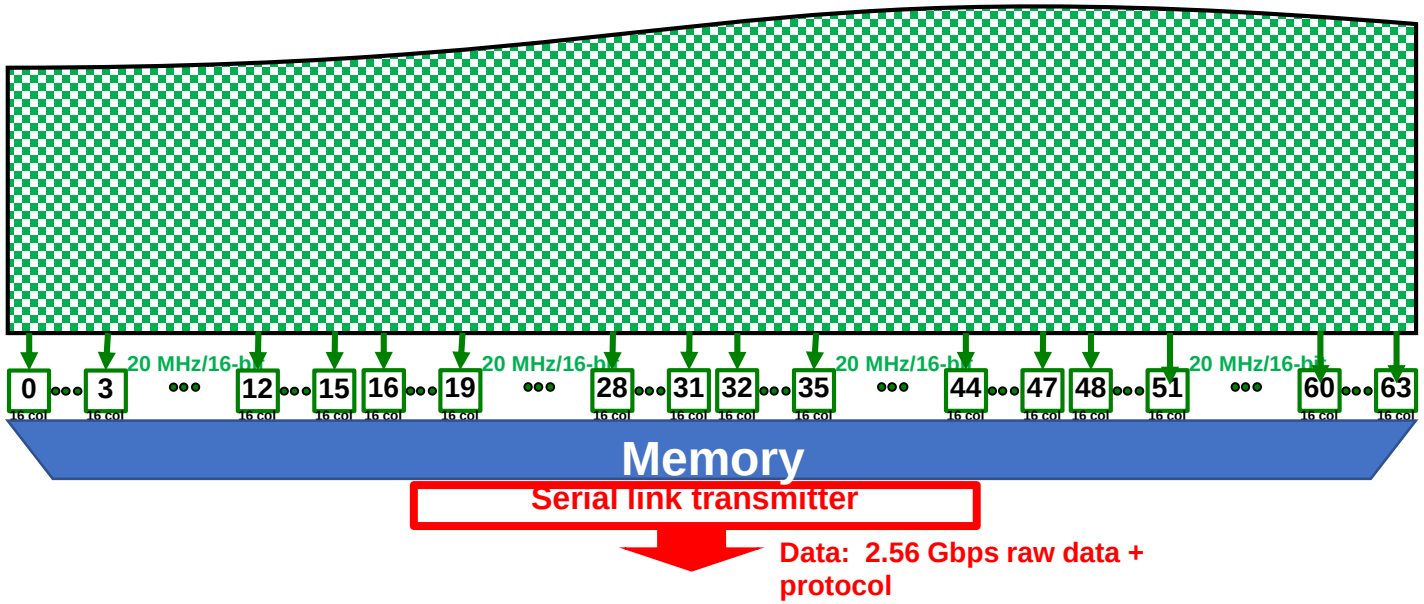
SMU

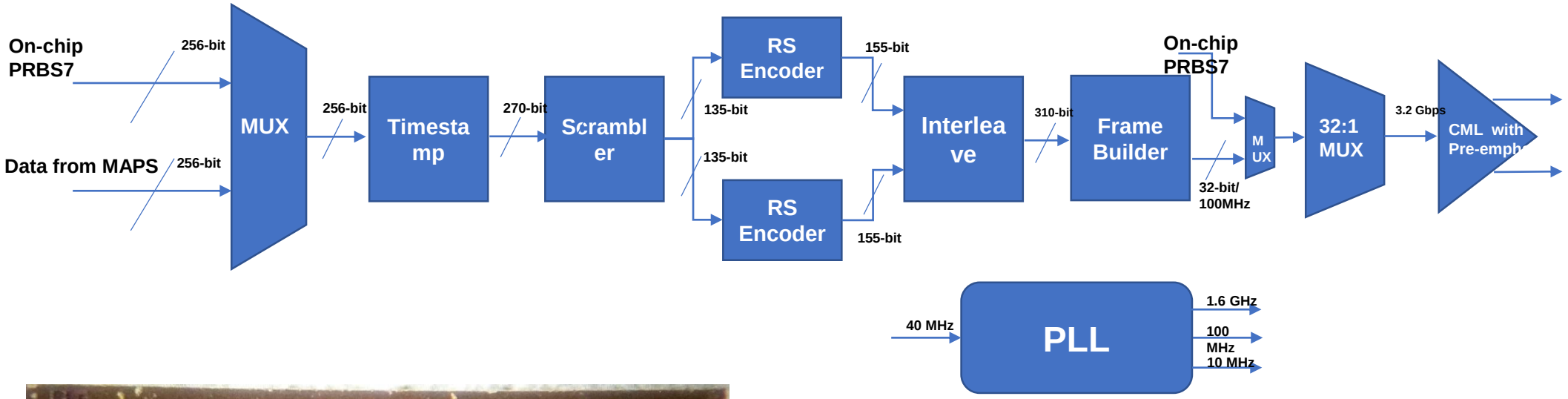
Data transmission for MAPS

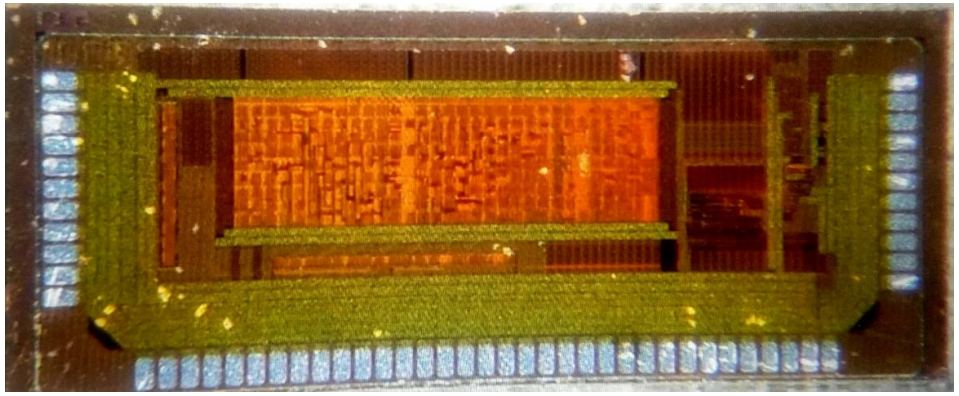


	Current Parallel Data Transmission(8 X 320 Mbps, LVDS)	Serial Data Transmission
Cables	18 (16 of them for data and other 2 for clock)	2
Clock Skew	Yes	No
Error Correction	No error correction	Up to 20 bits in a frame

- **CMOS monolithic active pixel sensors (MAPS) have demonstrated their potential for future subatomic physics experiments, due to trade-off among:**
  - **granularity, material budget and readout speed**
- **Parallel data links are pervasively used in MAPS due to their simplicity. However, parallel links suffer from**
  - **Material penalty**
  - **Clock skew as data rate increasing**
- **We proposed a 3.2 Gbps serial link transmitter for MAPS applications.**

Architecture





- 256-bit raw data at 10 MHz
- 14-bit timestamp
- Scrambler provides DC-balanced data
- Error correction with FEC encoder
- Full-custom serializer working at half-rate
- CML with pre-emphasis
- On-chip PLL for clock generation