Study of Retina Algorithm on FPGA for Fast Tracking

Wendi Deng and Zixuan Song
Université libre de Bruxelles(ULB) & Central China Normal University(CCNU)

21st IEEE Real Time Conference -Colonial Williamsburg

Zixuan.Song@ulb.ac.be , dengdandan@mails.ccnu.edu.cn

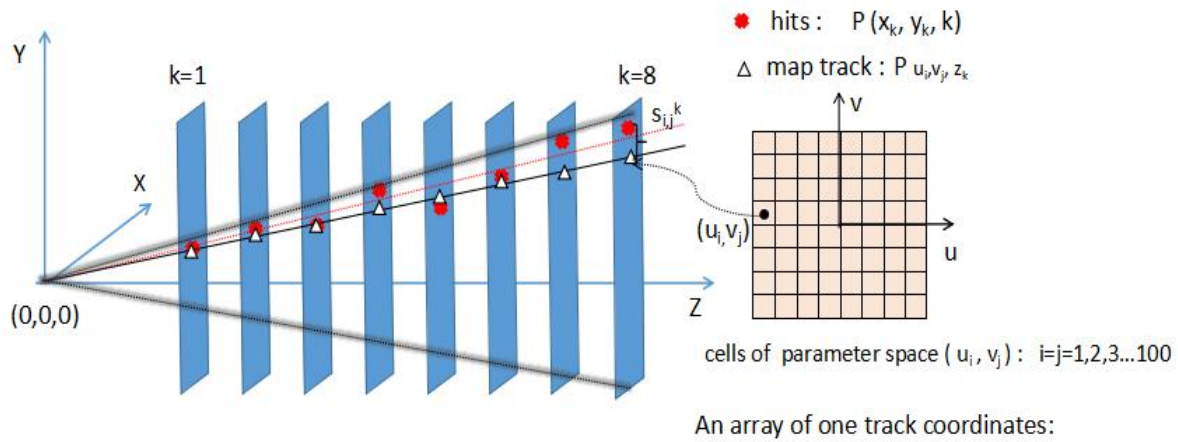
Retina algorithm & Simulation

Retina Algorithm formula：

$$\text{Reina Output} = Max\left(\sum_{k} \exp\left(-\frac{s_{i,j}^{k\ 2}}{2\sigma^2}\right)\right)$$

σ is a adjusted parameter for optimal response

Case1： RECO straight track with Retina



An array of one track coordinates:

...8

Case2： RECO track in strong magnetic field with Retina

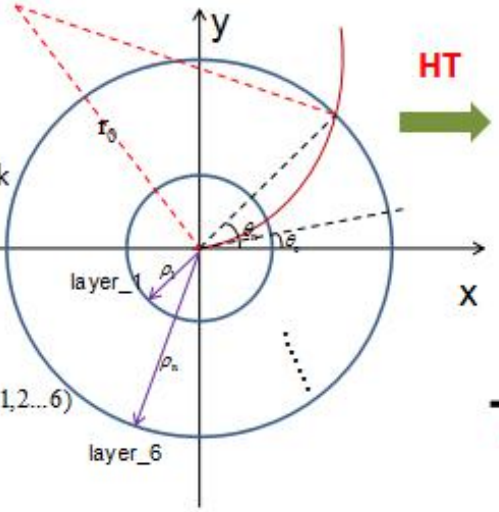
$$\theta_i = \frac{\rho_i}{2r_0} + \theta_0 \quad 0 \le \theta_0 \le 2\pi$$

r_0 :the radius of particle's track

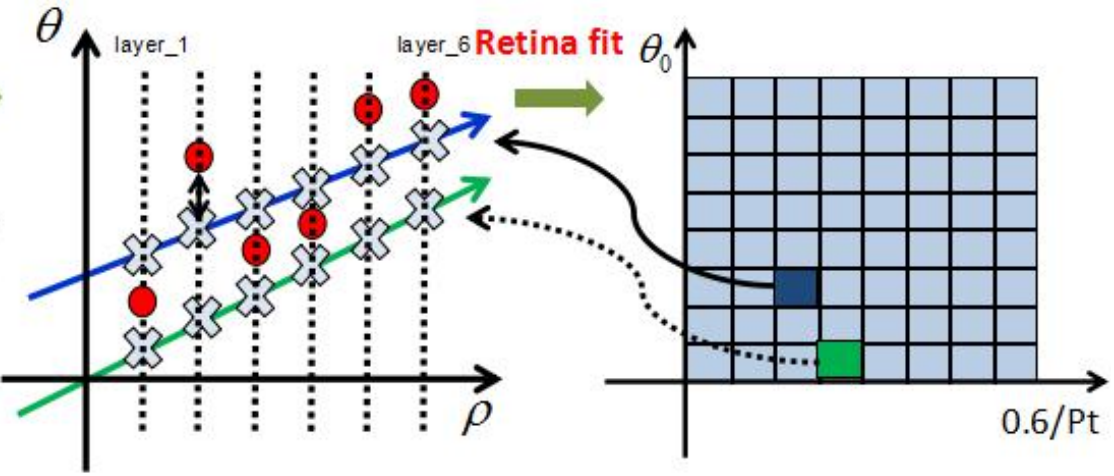
$$P_T = 0.3BQr_0 \rightarrow r_0 = \frac{P_T}{0.3BQ}$$

Set $B=4T$, $Q=+1$:

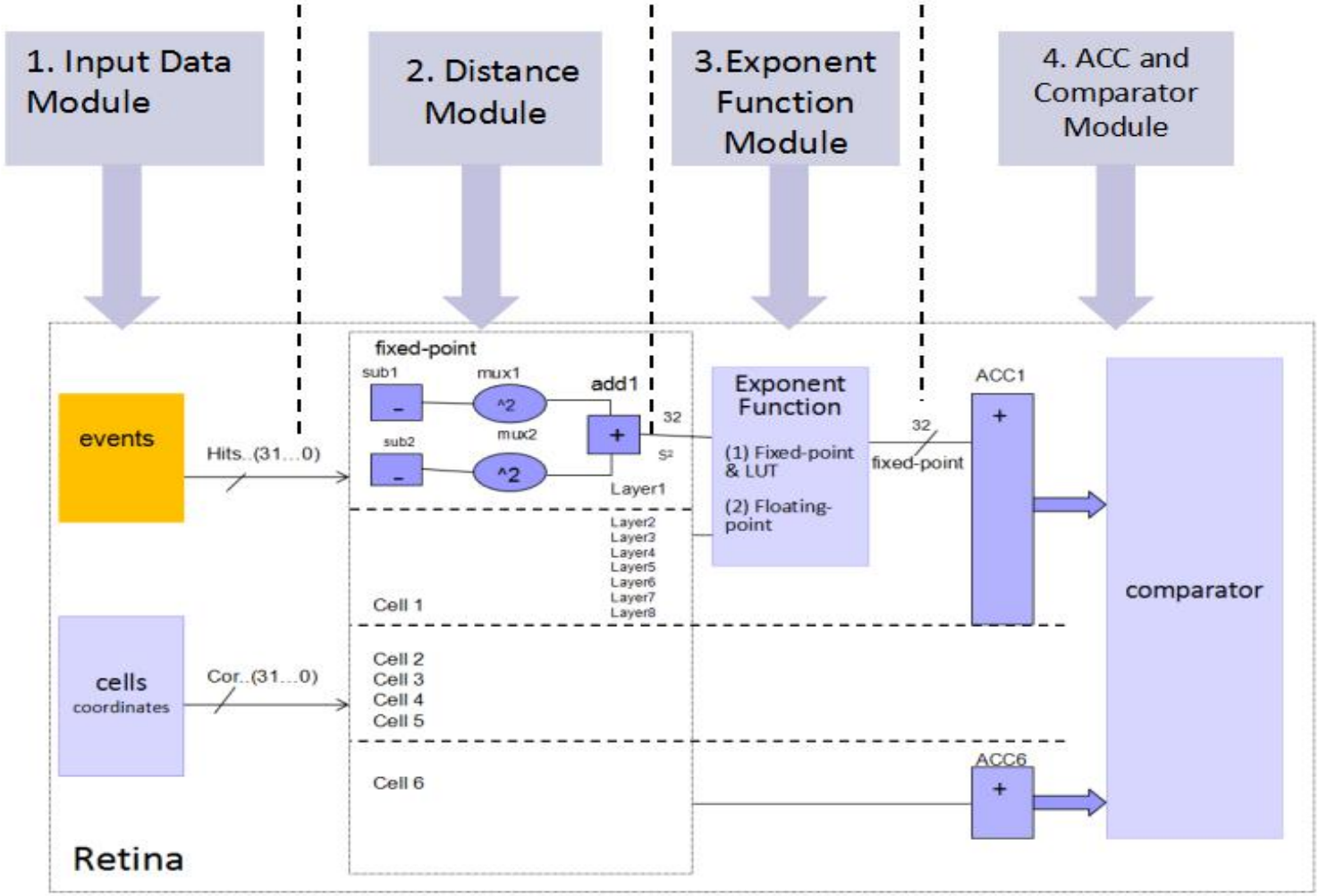
$$\theta_i = \frac{0.6}{P_T} \cdot \rho_i + \theta_0 \rightarrow \theta_i = m \cdot \rho_i + \theta_0 (i = 1,2...6)$$



HT



Firmware design of retina algorithm



Two approaches of Retina computing implementation:

-Float point-32bits (standard IP core)

-Fixed point-12bits (LUT made up mainly by BRAM)

Clock (Hz)	Firmware Design	DSP (%)	LUT (%)	LUTRAM (%)	BRAM (%)	FF (%)	Latency (Cycles) /μs
100M	Floating-point	17.14	70.72	15.24	3.03	42.32	156/1.56
100M	Fixed-point and LUT	11.43	7.25	8.46	33.48	9.8	68/0.68