Radiation-Tolerant, High-speed Serial Link Design with SRAM-based FPGAs

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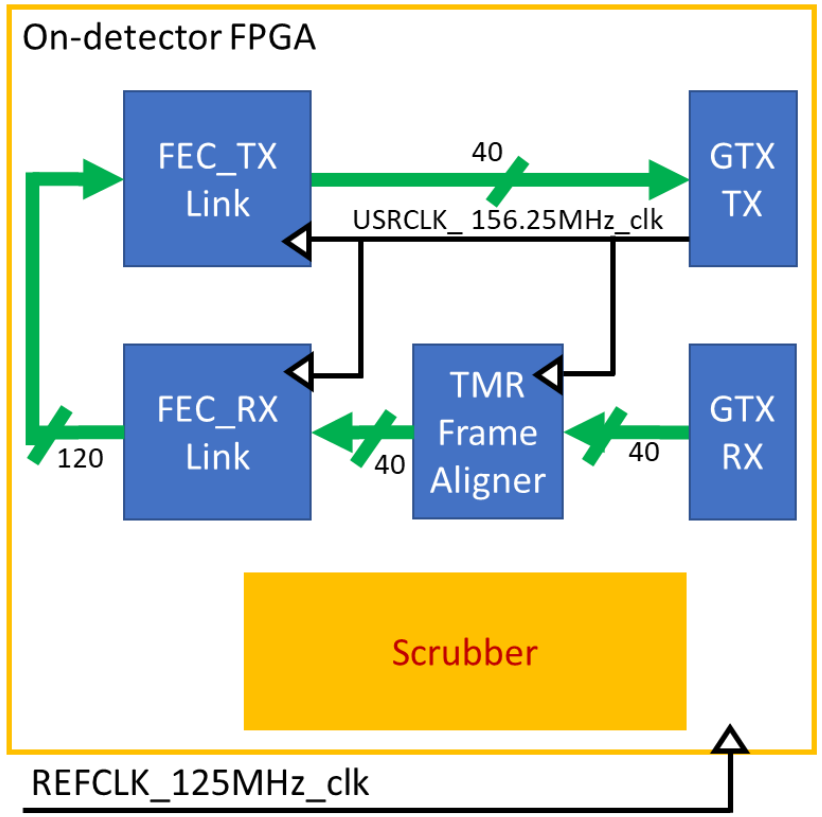
- High-speed serial links implemented by means of SRAM-based FPGAs usually used only off-detector
  - mostly due to FPGA sensitivity to radiation-induced single event effects
- This work is about a radiation-tolerant link running @6.25 Gbps in a Xilinx 7-Series FPGA
  - Adaptive, FEC line code protects data
  - Triple Modular Redundancy protects critical logic blocks
  - Scrubber protects configuration



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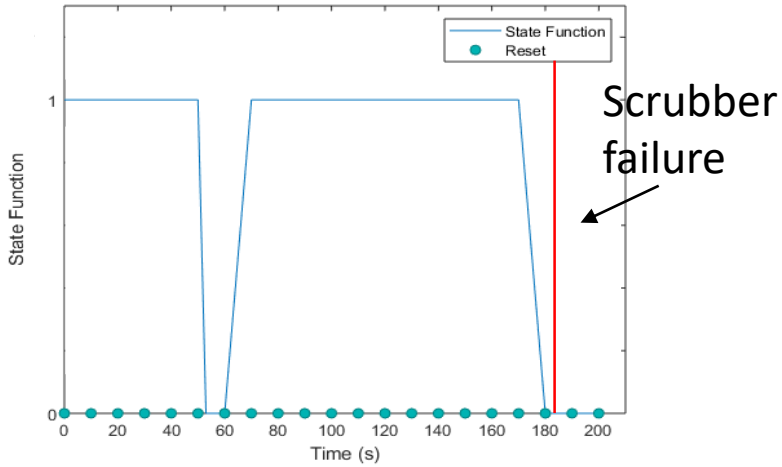
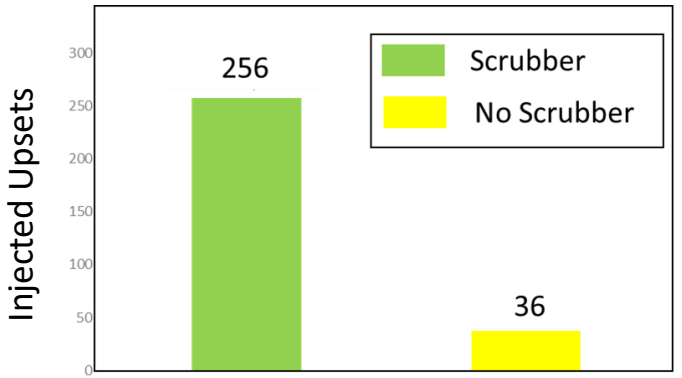
- Results from a fault-injection test
  - The link corrects the maximum burst-errors compatible with the line code protection level
  - The link recovers from losses of locks in spite of the injected errors when the scrubber is active
  - # of injected upsets before failure is 7x higher when the scrubber is operating





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Motivation and Overview of the Radiation-Tolerant Link

Details on System and its implementation on Xilinx FPGAs

Description of the fault injection test and of preliminary results

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Summary

In the field of High Energy Physics experiments, high-speed serial links implemented on SRAM-based FPGAs have been extensively used in the trigger and data acquisition systems. Their application has been usually limited to the off-detector electronics, due to SRAM-based FPGA susceptibility to ionizing radiation effects.
However, in order to use these devices in radiation environments, dedicated mitigation techniques can be adopted:
- information redundancy (typical of error correcting codes)
- hardware redundancy, such as triple modular redundancy (TMR)
- configuration scrubbing.

In this paper, we present a serial link running at 6.25 Gbps implemented in a Xilinx Kintex-7 FPGA which is protected against radiation effects by means of all the above-mentioned methods (Fig. 1).

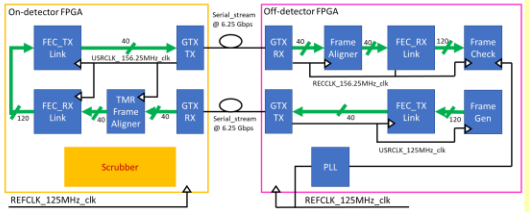


Fig. 1 Simplified Block Diagram of the Radiation Tolerant Link.

1. Link Architecture

- Self-synchronizing scrambler for data randomization.
- Reed-Solomon encoder/decoder, whose error correction capability is increased adopting the Interleaving technique.
- Adaptive Reed-Solomon code to cope with different rates of radiation-induced faults, trading the available bandwidth for data redundancy.
- TMR replicas (Synplify Premier tool [1]) of alignment circuit for masking error before scrubbing correction.
- Scrubber for repairing corrupted configuration frames in real-time [2,3].

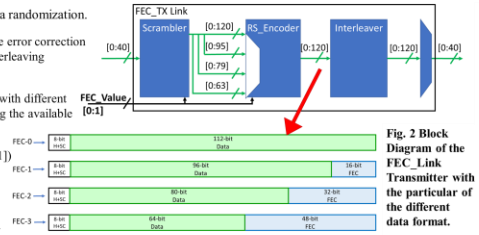


Fig. 2 Block Diagram of the FEC_Link Transmitter with the particular of the different data format.

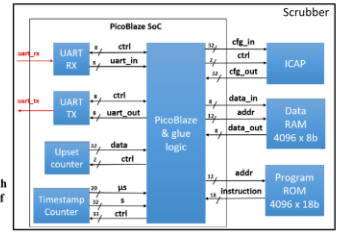


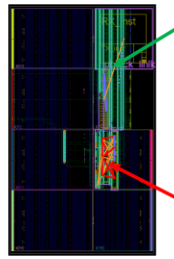
Fig. 3 Block Diagram of the Scrubber.

2. Implementation & Replication

- Both the on-detector and the off-detector Link have been implemented in Xilinx Kintex-7 FPGAs whose embedded GTX transceivers support data rates up to 10.3125 Gbps.
- The configuration of the on-detector link node (i.e. intended to be used in radiation areas) has been protected.
- The project summary of the resources utilization is shown in Table 1.
- The project occupation on the FPGA device is shown on in Fig. 5
- In Fig. 7 the configuration occupation of the project before and after the replication of the configuration frames.

	Slice LUTs (41000)	Slice Registers (82000)	Slice (10250)	BUFG (32)	IOB (285)
TMRLinkScrubber	7057 (17.2%)	3450 (4.2%)	2091 (20.4%)	4(12.5%)	5 (1.8%)
Link	5460 (13.3%)	1970 (2.4%)	1481(14.5%)	2(6.3%)	3 (1%)
GTX	261 (0.6%)	310 (0.4%)	132 (1.3%)	1 (3.1%)	0 (0%)
FEC_TX_Link	1396 (3.4%)	367 (0.5%)	139 (1.9%)	0 (0%)	0 (0%)
FEC_RX_Link	3032 (7.4%)	730 (0.9%)	799 (7.8%)	0 (0%)	0 (0%)
TMR_Frame_Aligner	774 (1.9%)	558 (0.7%)	217 (2.1%)	0 (0%)	0 (0%)
Scrubber	1597(3.9%)	1480(1.8%)	610 (6%)	2(6.3%)	2(0.8%)

Table 1 Resources Utilization.



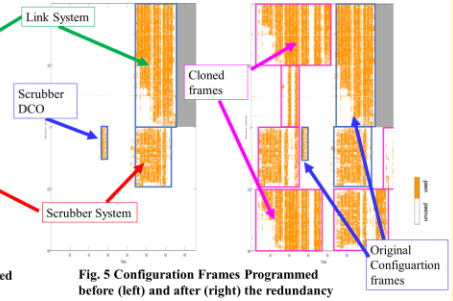


Fig. 4 Layout of the implemented design (Off-detector FPGA).

Fig. 5 Configuration Frames Programmed before (left) and after (right) the redundancy (on-detector FPGA)

3. Fault InjectionTest

- Test with a Fault Injector software.
- Custom DUT board FPGA loaded with Remote Link firmware.
- Tester board (Xilinx KC705) with the Local link firmware with a frame checker for the verification of the DUT output
- Multichannel Power Analyzer (PA) powers DUT board.
- Test controller logs upsets from scrubber, functionality test results from tester board and power logs from PA.
- PC inject error on essential bits via JTAG.

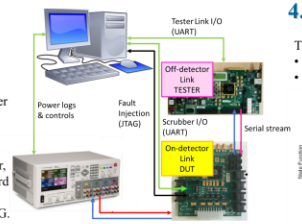


Fig. 6 Test Setup.

4. Test Results

The Link has been tested with or without scrubbing
- Fig. 7 shows the state function of the link when scrubber is active.
- In Fig. 8 the upsets injected in the configuration before failure w/ and w/out scrubbing.

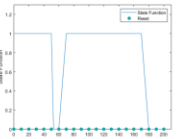


Fig. 7 State Function of the on-detector link.

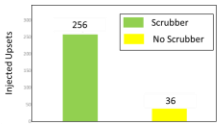


Fig. 8 Upsets injected in the firmware by the firmware before failure.

References

[1] Synplify Pro and Premier. Synopsys, Inc. Mountain View, Calif. (USA), 2015 [Online]. Available:https://www.synopsys.com/content/dam/synopsys/implementation&signoff/datasheets/synplify-pro-premier.pdf.
[2] R. Giordano et al. IEEE Trans. on Nucl. Sci., vol. 64, no. 9, pp. 2497-2504, Sept. 2017
[3] R. Giordano et al. "Self-Contained Configuration Scrubbing in Xilinx FPGAs for On-detector Applications" PM2018, Conference Proceeding, Pisa, 2018. [4] R. Giordano et al. IEEE Trans. on Nucl. Sci., vol. 64, no. 9, pp. 2497-2504, Sept. 2017

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