

DE LA RECHERCHE À L'INDUSTRIE



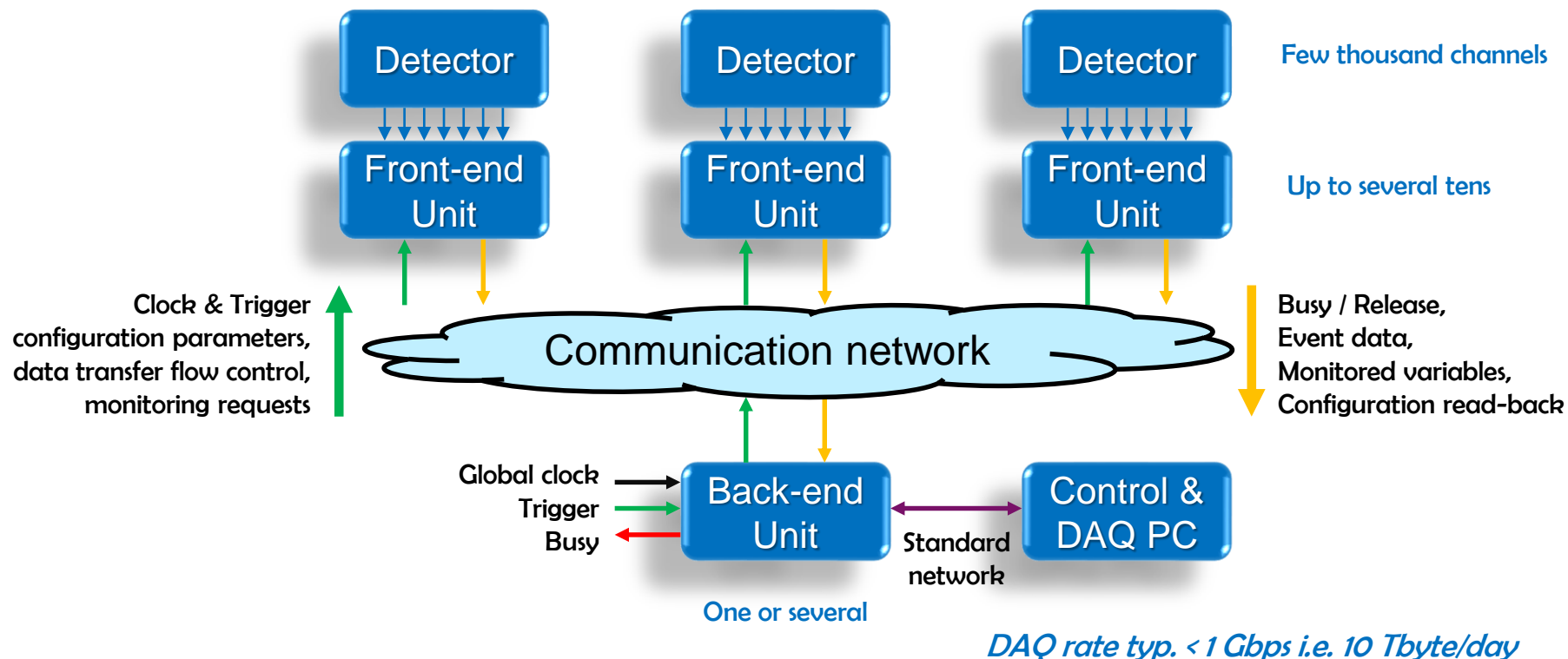
BACK-END ELECTRONICS FOR LOW BACKGROUND AND MEDIUM SCALE PHYSICS EXPERIMENTS BASED ON AN ASYMMETRIC NETWORK

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Proposed concept

- A fanout structure in the back-end to front-end direction
→ *natural choice for deterministic latency clock and trigger distribution*
- A set of medium-speed point-to-point links in the opposite direction
→ *bandwidth per link = DAQ bandwidth / Number of front-ends = typ. ~100 Mbps only*

BACK-END UNIT DESIGNED



Use the few available multi-Gbps capable FPGA SERDES where high bandwidth is needed

Control & DAQ,
Board cascading

Trigger Clock input,
LEDs, buttons, etc



Multi-gigabit
SERDES

Low speed I/O's

Custom
Made
Carrier

System-On-
Chip
FPGA + CPU

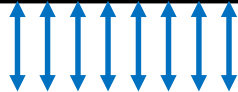
Use a commercial SoC module for a fast, cheap and lower risk development

Use regular FPGA user I/O pins to build several tens of multi 100 Mbps capable serial links

Regular LVDS I/O's

Physical Layer
Mezzanine Card

Physical Layer
Mezzanine Card



Links to/from Front-End Units