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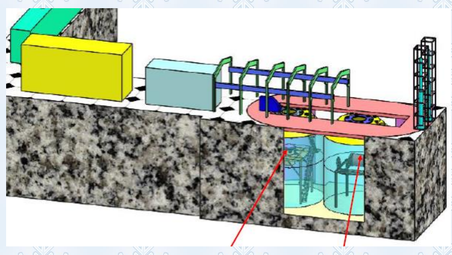
Back-end Electronics for Low Background and Medium Scale Physics Experiments Based on an Asymmetric Network

D. Calvet,
IRFU, CEA Université Paris-Saclay F-91191, Gif-sur-Yvette FRANCE

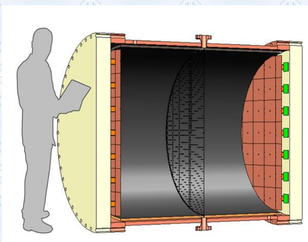
DIRECTION DE LA RECHERCHE FONDAMENTALE
INSTITUT DE RECHERCHE SUR LES LOIS FONDAMENTALES DE L'UNIVERS
CENTRE DE SACLAY

Application Context

PandaX-III – Searching ^{136}Xe neutrinoless $\beta\beta$ decay



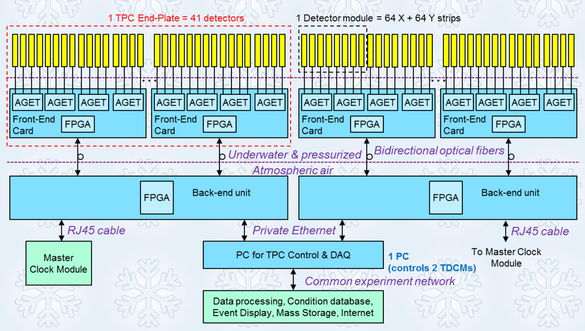
PandaX-III and PandaX-4T in their water tank shield



PandaX-III TPC vessel and detection planes

Detector features

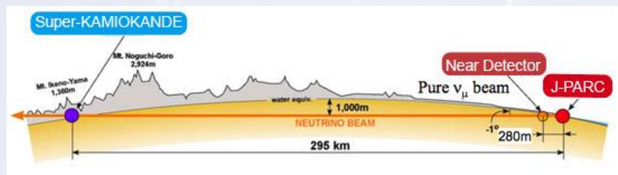
- 10 bar pressure ^{136}Xe TPC
- 41 Microbulk Micromegas detectors per TPC end-plate
- Ultra-low background radioactivity



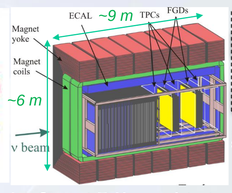
Readout electronics at a glance

- 10 K channels total
- Based on 64-channel AGET chip
- 256 channels per Front-End Unit (= Cards)
- 21 Front-end Units for each TPC end-plate
- Typical trigger rate: ~10 Hz
- Expected data throughput: <20 MB/s
- Front-end: 10 bar operating pressure + lowest possible background radioactivity

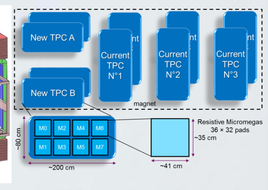
T2K-II – Unveiling the mysteries of neutrino oscillations



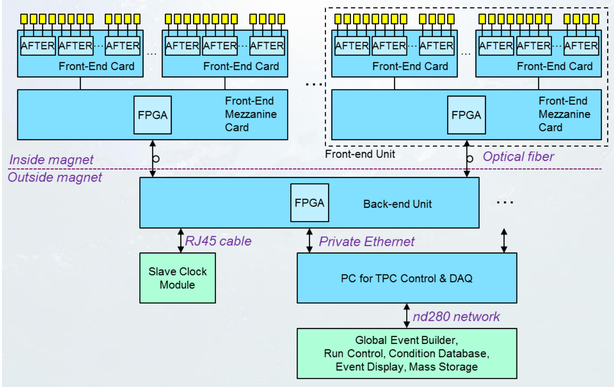
T2K long baseline neutrino oscillation experiment



Current T2K near detector



TPCs in proposed upgrade



Electronics for new TPCs

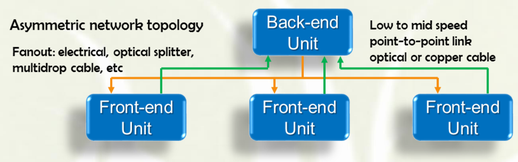
- 36 K channels total
- Based on 72-channel AFTER chip
- 1152 channels per Front-End Unit (2 Front-end Cards + 1 Front-End Mezzanine)
- 16 Front-end Units for each of 2 TPCs
- Max. trigger rate: ~10 Hz
- Expected data throughput: <10 MB/s
- Front-end: 0.2 T magnetic field tolerance

Architecture Concepts Questions and Answers

What link bandwidth is really needed?

- Back-End to Front-end: few KB config. (once) + monitoring every few seconds + trigger at few 10 Hz = no more than 1 Mbps total!
- Opposite link direction: DAQ bandwidth / Number of Front Ends + trigger ack. + config. read back + monitoring = only few 10 Mbps!

Solution: fanout BE to FE + return p-to-p links



What is needed for deterministic latency low/mid speed optical links? A good CDR chip

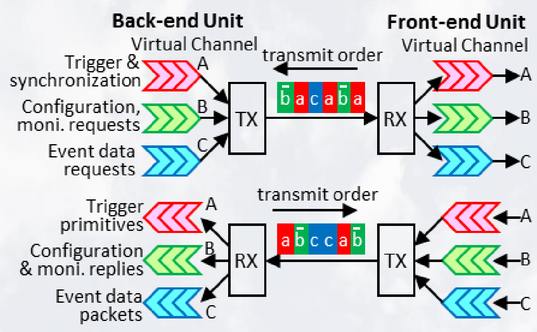
Continuous Rate 10 Mb/s to 1.25 Gb/s Clock and Data Recovery IC
ANALOG DEVICES ADN2815
MICREL 3.3V 28Mbps to 1.3Gbps
SY87701AL AnyRate® Clock and Data Recovery

- Found fixed delay over power-cycling
- Low part-to-part dispersion observed
- Stable for power in 3V-3.6V. 600 ps drift for 50°C change (Test sample: 4 ADN2815)

How to exchange simply several classes of messages over one media?

- Deterministic latency trigger information, configuration and monitoring requests and responses, acquired event data

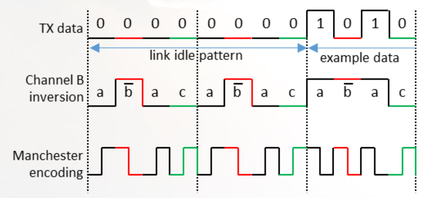
Solution: fixed cycle time division multiplexing



Link encoding properties of BE to FE fanout?

- DC-balanced; easy frame delineation
- Receiver synchronization without interrupting the transmitter

Solution: invert 1 bit in frame and Manchester encode



Other properties

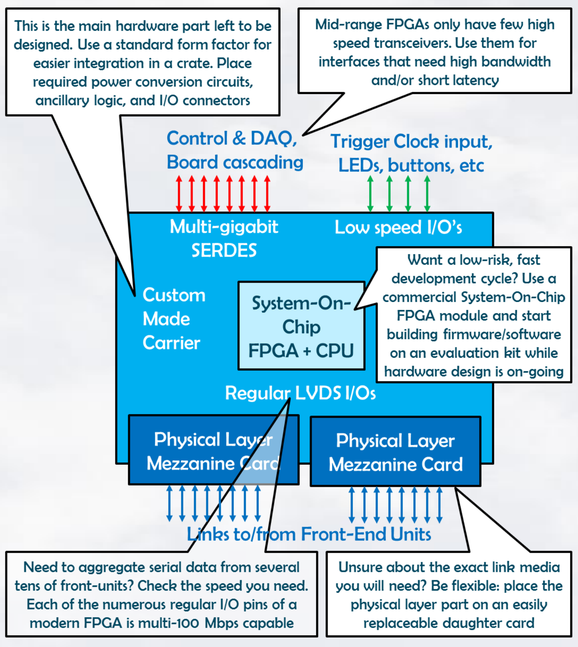
- Easy to built
- 1 transition per cycle (low jitter clock distribution)
- Error detection: if a bit is not followed by its inverse

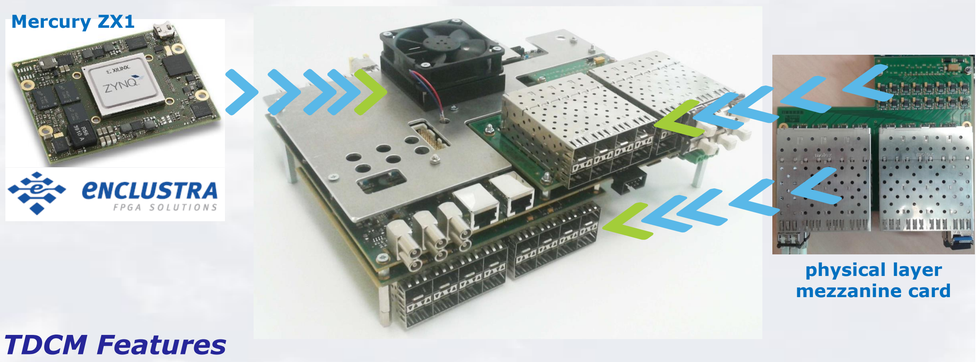
Same encoding for FE to BE links?

- DC-balanced; easy frame delineation; low overhead, simple

Solution: self-synchronizing scrambler 1 + x^{43}

The Trigger and Data Concentrator Module - TDCM

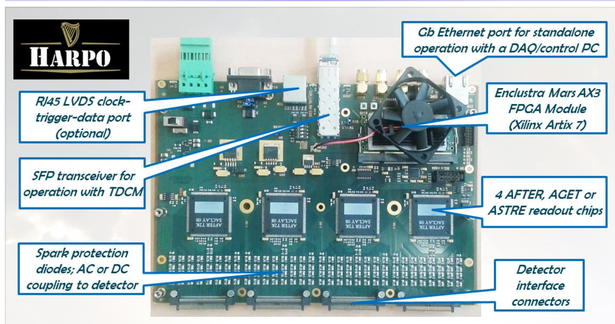




TDCM Features

- 6U form factor card, single 12 V input, commercial Enclustra ZX1 Xilinx Zynq SoC
- Controls up to 32-link to front-end units (680 Mbps capable links; 500 Mbps tested)
- 2 replaceable 16-port physical layer mezzanine cards – current model: 16 optical SFP
- 3 user defined GTP, 2 GbE ports, 1 PCI Express Gen 2 x 4 cable interface (to be tested)
- 2 RJ45 LVDS for connection to master clock & trigger unit or multi-TDCM cascading
- 6 NIM and 6 TTL I/Os for simple clock and trigger interface (Trigger IN, Busy OUT)
- Bare metal configuration and readout interpreter program on ARM CPU core

A Readout Card - ARC

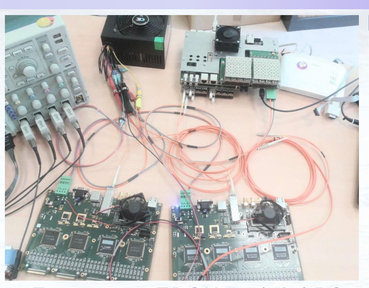


ARC Features

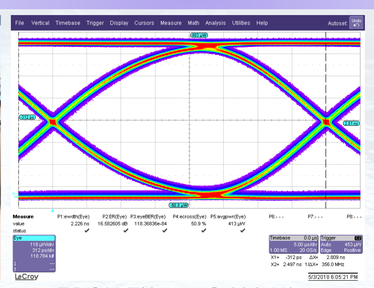
- 256-channel generic detector readout card
- Compatible with AFTER, AGET and ASTRE chips
- 120 fC-10 pC range, 100 ns to 8 µs peaking time
- 512-time bucket SCA; 100 MHz max. sampling
- External or self trigger (AFTER, or AGET-ASTRE)

The ARC is not intended for PandaX-III. See instead: D. Zhu, "Development of the Front-End Electronics for PandaX-III Prototype TPC", in this conference

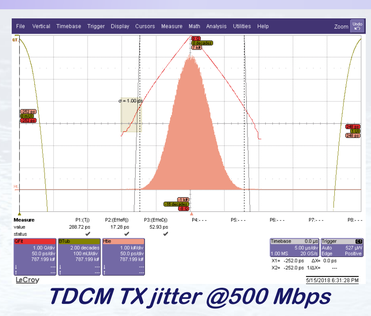
Performance Evaluations



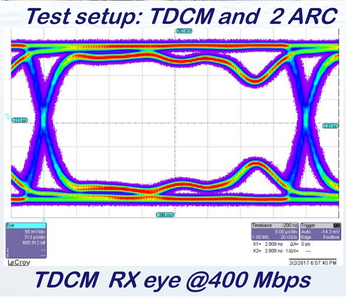
Test setup: TDCM and 2 ARC



TDCM TX eye @400 Mbps



TDCM TX jitter @500 Mbps

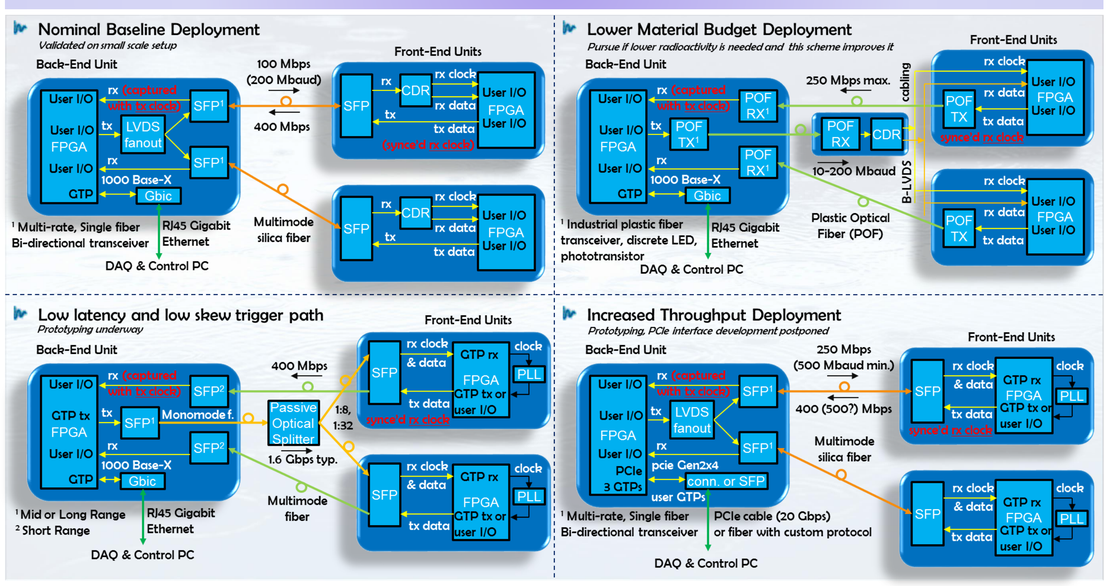


TDCM RX eye @400 Mbps

Results

- BER tester PRBS7/15/23/31 in FPGA logic. Measured link BER: $<10^{-12}$ @ 200 Mbps FE RX and $2*10^{-13}$ @ 400 Mbps BE RX (95% C.L.)
- Correct PRBS reception with TX user I/O pin 500 Mbps to GTP RX
- Configuration, data taking and readout tested with 1 and 2 ARC
- Local event builder and DAQ transfer at up to 120 MB/s (GbE limit) tested with data generator in FPGA emulating up to 32 front-ends

TDCM Use-case Scenarios



CEA - Saclay

université PARIS-SACLAY

- Concept: a readout system with asymmetry in network topology, link encoding, speed and possibly media
- Recipe: use regular FPGA I/O pins for multi-100 Mbps serial links; CDR chip on front-end for fixed latency
- Product: a 32-port 12.8 Gbps bandwidth clock/trigger distributor & data aggregator from commercial SoC
- Companion: a 256-channel front-end card for a generic detector readout system scalable to 8K channels

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