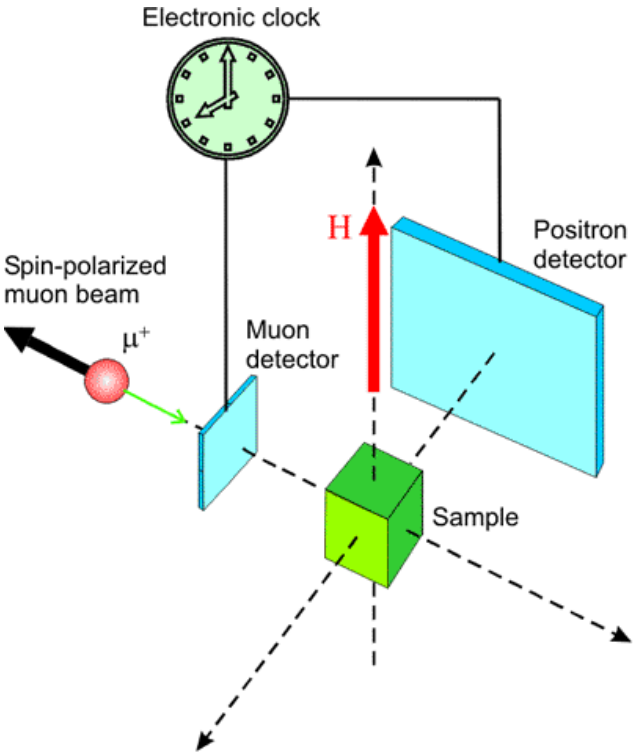
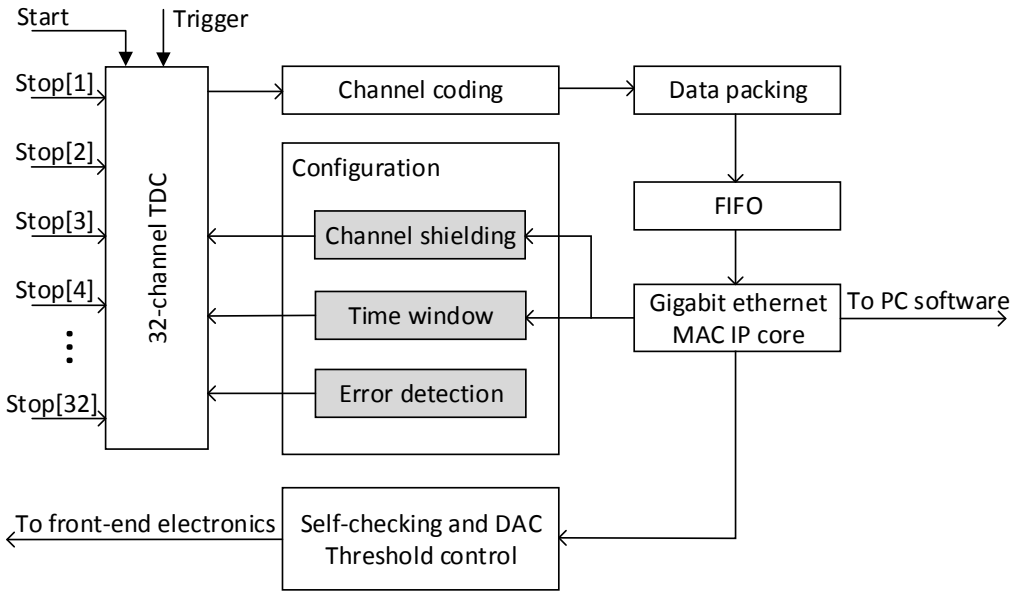
Design of 32-channel TDC Based on Single FPGA for μSR Spectrometer at CSNS





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I. Introduction

The use of muon's spin properties to study the properties of materials is called Muon Spin Rotation, Relaxation and Resonance (μSR) technology. μSR technology has an irreplaceable role in studying the microstructure and properties of materials, especially micro-magnetic properties. An experimental muon source is being built in China Spallation Neutron Source (CSNS) now. At the same time, a 128-channel μSR spectrometer as China's first μSR spectrometer is being developed.

This μSR spectrometer uses a double ring structure with 64 detectors placed in front of and behind the sample. Muon's lifetime can be obtained by measuring the positron's flight time. The time spectrum of μSR can be obtained by fitting the curve of positron count rate with time and then can reveal the internal physical structure of the sample information. In order to measure the positron's flight time, a 32-channel Time-to-Digital Converter (TDC) is implemented in a Xilinx Virtex-6 Field Programmable Gate Array (FPGA).

II. Design and Implementation

A. Design Method

This TDC uses Shifted-phase Clock Sampling(SCS) method. The external clock is multiplied by two PLLs to generate eight 200MHz clocks that have the same frequency but a difference of 22.5 degrees between the two adjacent clocks. the input signal can be routed to 16 flip-flops, with 8 flip-flops being activated by 8 clock rising edge and the other 8 flip-flops being activated by 8 clock falling edge.

The most significant effect on the linearity of TDC bins is the time skew of input signal routing to flip-flops. In order to minimize time skew, the Look-Up Tables(LUT) in FPGA are used as shown in Fig. 1. The input signal is routed to 16 flip-flops after four stages of LUTs and these LUTs are placed symmetrically in the same slice column. After sufficient area constraints and timing constraints, the time skew can be reduced to a few picoseconds.

B. TDC Design

Figure 2 is the schematic of one TDC channel. The input signal is routed to 16 flip-flops driven by 16 shifted-phase clocks with minimal time skew, the value of flip-flops is encoded into a 4-bit binary code as a fine count and then the fine count is sent to the hit-buffer with coarse count. The data is finally stored in the readout FIFO after passing through the trigger counter. Because the time measurement range is required to reach hundreds of microseconds, the coarse counter is a 16-bit counter driven by 200MHz clock, so the time measurement range is up to 327us. The single-channel detector may receive multiple positrons in a short time, so the TDC is designed to be multi-stop and it has a deep hit-buffer up to 512. The trigger counter can be configured as external trigger or internal self-trigger to decide whether the data is reserved and to record the number of trigger signals. The time tag is used to record the moment when the hit signal is detected.

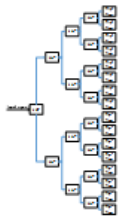

Fig.1 Time skew is minimized by inserting LUTs.

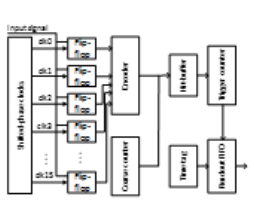

Fig.2 Schematic of one TDC channel.

C. FPGA Implementation

This TDC contains a start channel and 32 stop channels. Schematic of 32-channel TDC and control logic in a single FPGA is shown in Fig. 3. 54bit data of each TDC, including 20bit time data, 26bit time tag and 8bit trigger count, is packaged into 64bit after channel coding and then stored in the FIFO, and finally uploaded to data acquisition system (DAQ) through Gigabit Ethernet. A 7-bit channel coding is used as the identification number for each channel. TDC's configuration section includes channel shielding, time window setting and error detection. Channel shielding, time window are used to select the channel and time range of interest to the user. Error detection is used to reset the entire TDC logic when an error occurs.

This FPGA is also responsible for controlling the front-end electronics, including the self-checking and Digital to Analog Converter (DAC) threshold for each channel. The front-end electronics periodically simulate the detector signals and the FPGA also generates periodic pulse signals when self-checking. On the one hand, the entire electronics system can be tested whether it can work normally without the detector connected, on the other hand, the delay of each channel can be calibrated. TDC and control logic can be configured in real time by DAQ.

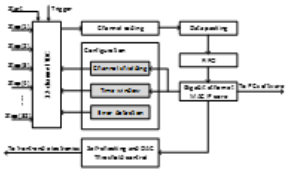

Fig.3 Schematic of 32-channel TDC and control logic in a single FPGA.

III. Test Results

We tested the time measurement performance between the start channel and one of the stop channels. The test method is to generate the periodic start signal and stop signal by generator. Test results are shown in Fig. 4, the FWHM precision is equal to 368.1ps. Change the time interval to do multiple measurements in 200 ps steps. After 27 times measurements, the worst is 385.8ps. So the FWHM precision of single channel is better than $385.8/\sqrt{2}$=273ps. The fitting curve of expectation with input time interval is shown in Fig. 5, the correlation coefficient R^2 is close to 1.0000 (0.99999989).

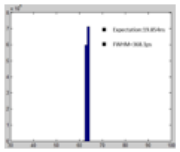

Fig 4 Measured FWHM precision of TDC channel

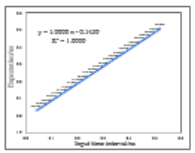

Fig.5 Fitting curve of expectation with input time interval.

IV. Conclusion

In this paper, a 32-channel TDC is implemented in a single Xilinx Virtex-6 FPGA to measure the positron's flight time of μSR Spectrometer at CSNS. This TDC has a dead time of 5ns and has the ability to store multiple hit signals in a short time and the measuring range is up to 327us. The FWHM precision is better than 273ps and the linearity is pretty.

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