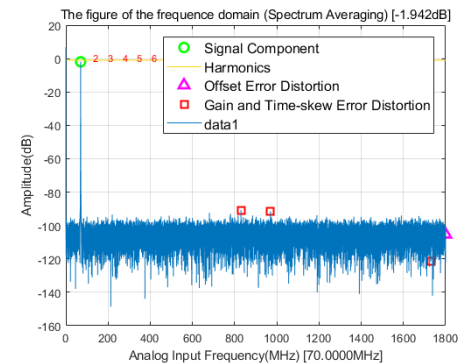
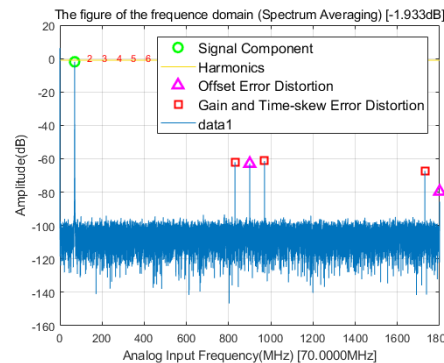
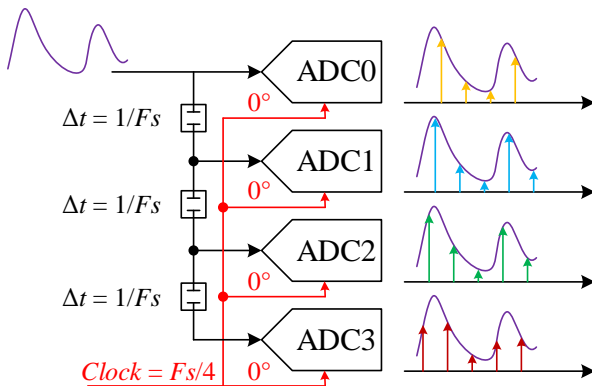
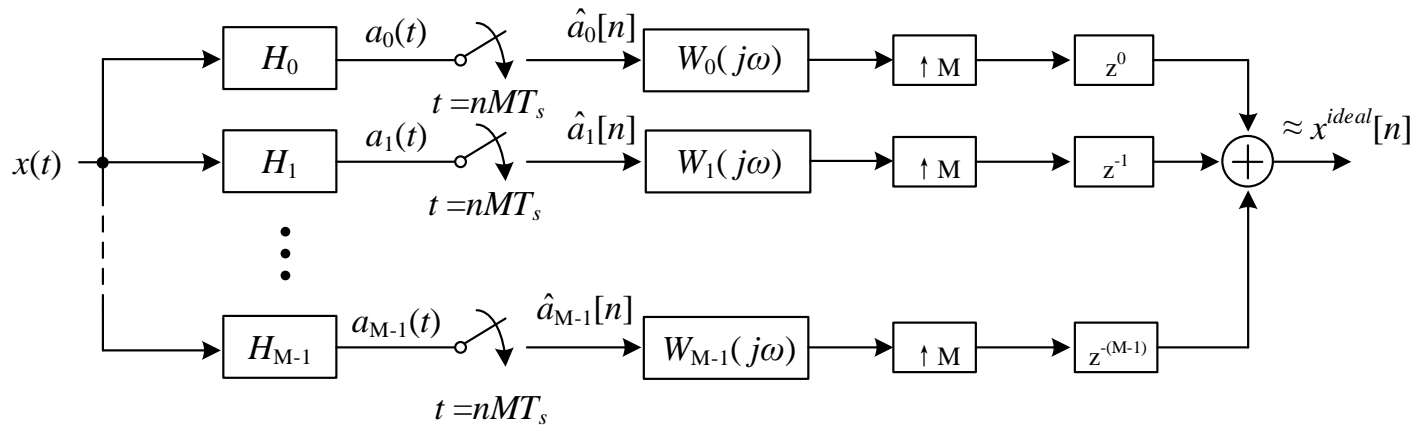


A new all-digital background calibration technique for time-interleaved ADC using first order approximation FIR filters

Jiadong Hu





A new all-digital background calibration technique for time-interleaved ADC using first order approximation FIR filters

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Introduction

Proposed Calibration Technique

Simulation Results

1. Introduction

To achieve high-speed, high-resolution signal sampling, time-interleaved analog-to-digital converter (TIADC) is proposed to be an effective architecture, by combining several slow but accurate sub-ADCs in parallel, as Fig. 1 shows.

However, due to discrepancies among the sub-ADCs, channel mismatches including offset, gain and sample-time mismatches distort the sampled signal and degrade the SNDR/SFDR performance of the TIADC significantly.

This paper presents a new all-digital background calibration technique for the TIADC, consuming few hardware resources while compensating channel mismatches. Moreover, this method is not limited by the number of TIADC channels.

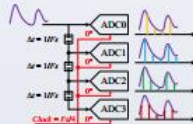


Fig. 1. A four-channel TIADC structure.

2. Proposed Calibration Technique

In all-digital background calibration technique, offset mismatches can be simply calibrated by subtracting a certain constant, so the proposed calibration technique assumes that the offset mismatches do not exist in formula derivation.

Suppose first order approximation FIR filters

$$w_m[n] = \begin{cases} \frac{(-1)^{n+1}}{n} \frac{\Delta t_m}{M}, & n \neq 0, n \in \mathbb{Z} \\ 1 - \Delta t_m \text{ or } \frac{1}{1 + \Delta t_m}, & n = 0 \end{cases}$$

$$\xrightarrow{DFT} W_m(j\omega) = 1 - \Delta t_m \sum_{k \neq 0} \frac{1}{k} j(\omega - 2\pi k) \frac{\Delta t_m}{M} \Phi(\omega - 2\pi k)$$

$$\text{or } \frac{1}{1 + \Delta t_m} \sum_{k \neq 0} j(\omega - 2\pi k) \frac{\Delta t_m}{M} \Phi(\omega - 2\pi k) \quad (1)$$

then

$$\hat{a}_m[n] * w_m[n] \approx \hat{a}_m^{ideal}[n] \xrightarrow{DFT} \hat{A}_m(j\omega) \cdot W_m(j\omega) \approx \hat{A}_m^{ideal}(j\omega) \quad (2)$$

Fig. 2 shows the overall architecture of the proposed calibration technique. It can be seen that the proposed technique is not limited by the number of sub-ADC channels.

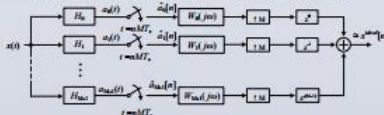


Fig. 2. The overall architecture of the proposed calibration technique.

3. Simulation Results

To verify the efficiency of the proposed technique, simulations are carried out on a four-channel 12-bit TIADC clocked at $f_{clk}=3.6\text{GHz}$. Unless otherwise noted, the analog input signal is 70MHz, the number of FIR taps is 30, FIR coefficient word length is 30, no offset mismatch, gain mismatch is within 1% but random, and sample-time mismatch is within 1% of $1/f_s$ but random. The simulation results are statistically averaged.

Fig. 3(a) shows spectra before calibration. After using the calibration technique, the spectra are shown in Fig. 3(b). The frequency spectra of mismatches are canceled after calibration, and the SINAD of signal is improved from 52 dB to 59 dB.

Fig. 4(a) shows SINAD versus input frequency with and without calibration. Fig. 4(b) shows SINAD versus FIR coefficient word length with and without calibration. Fig. 4(c) shows SINAD versus FIR taps with and without calibration when sample-time mismatch is within 10% of $1/f_s$. Fig. 4(d) shows SINAD versus FIR taps with and without calibration when sample-time mismatch is within 1% of $1/f_s$.

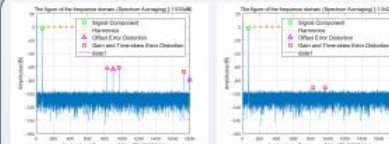


Fig. 3. TIADC simulation output spectra: (a) w/o and (b) with calibration.

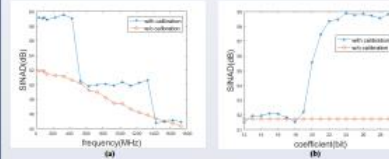


Fig. 4. SINAD versus simulation parameters. (a) SINAD versus frequency; (b) SINAD versus FIR coefficient word length; (c) SINAD versus FIR taps when sample-time mismatch is within 10% of $1/f_s$; (d) SINAD versus FIR taps when sample-time mismatch is within 1% of $1/f_s$.

4. Measured data Validation

In addition, measured data from ADC12D1800 chips, tested under the same conditions as simulation of Fig. 3, is carried out calibration. Fig. 5(a) shows spectra before calibration. After using the calibration technique, the spectra are shown in Fig. 5(b). The frequency spectra of mismatches are canceled after calibration, and the SINAD of signal is improved from 49 dB to 53 dB.

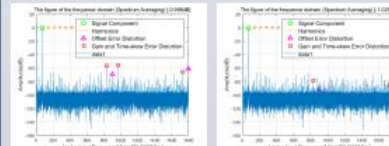


Fig. 5. TIADC measured data output spectra: (a) w/o and (b) with calibration.

5. Conclusion

This paper has described a new area-efficient all-digital technique for calibration of the mismatches in TIADCs. The proposed technique uses first order approximation FIR filter banks which do not need large number of FIR taps. This technique is not limited by the number of sub-ADC channels. In case of the four-channel 12-bit TIADC, the proposed technique improves SINAD of simulated data from 52dB to 59dB, and improves SINAD of measured data from 49dB to 53dB, while the number of FIR taps is only 30.

Measured data Validation

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