A Design of FPGA Based Small Animal PET Real Time Digital Signal Processing and Correction Logic

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- 32-channel in a single Xilinx Artix-7 family of FPGA
- 2D raw position calculation, crystal identification, events energy filtering, several online corrections, flood map and energy spectrum real time histogram

- A technical design of Crystal Look-up Table applied to reduce logic consumption
- 1,000,000 events/s rate, ≤1.5% RMS position precision, ≤118ps RMS timing precision, ≤2.4‰ energy precision
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**Introduction**
- Background
- General Introduction

**System Design**

**Logic Design**
- Digital Signal Processing Logic Design

**Design of the CLT**
- The transformation from the typical CLT to the new-designed boundary CLTs

**Testing**
- Position precision
- Timing precision
- Energy precision
- The Flood Map and Energy Spectrum Histogram
- The Energy online Calibration to 511 keV