A Design of FPGA Based Small Animal PET Real Time Digital Signal Processing and Correction Logic

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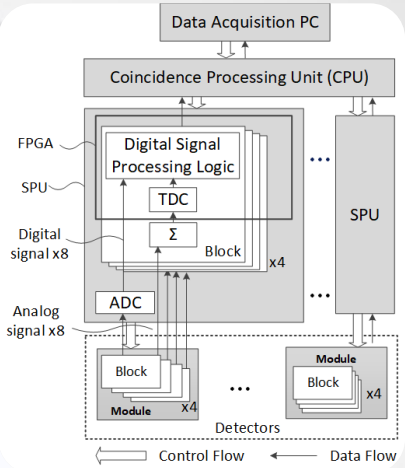
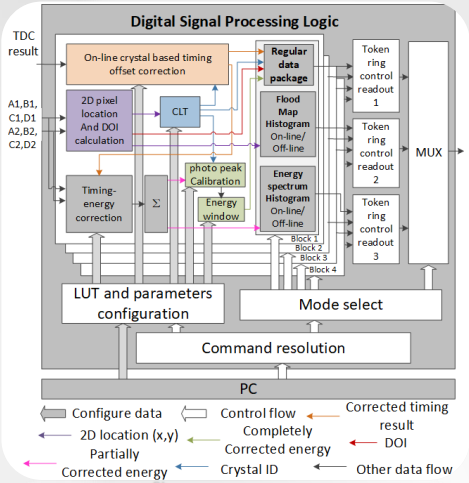
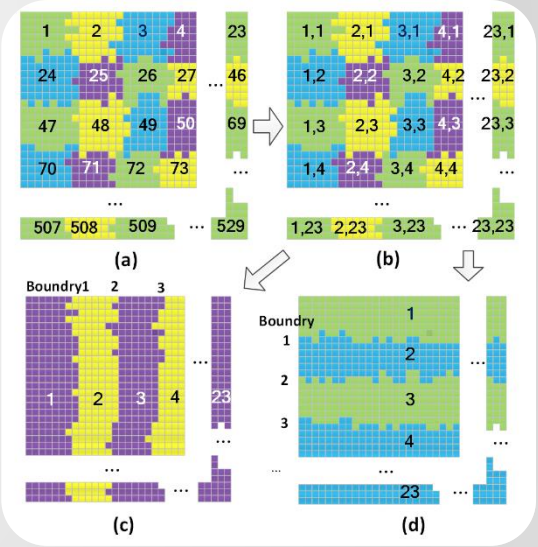




- **32-channel in a single Xilinx Artix-7 family of FPGA**
- **2D raw position calculation, crystal identification, events energy filtering, several online corrections, flood map and energy spectrum real time histogram**

- **A technical design of Crystal Look-up Table applied to reduce logic consumption**
- **1,000,000 events/s rate, ≤1.5‰ RMS position precision, ≤ 118ps RMS timing precision, ≤ 2.4‰ energy precision**



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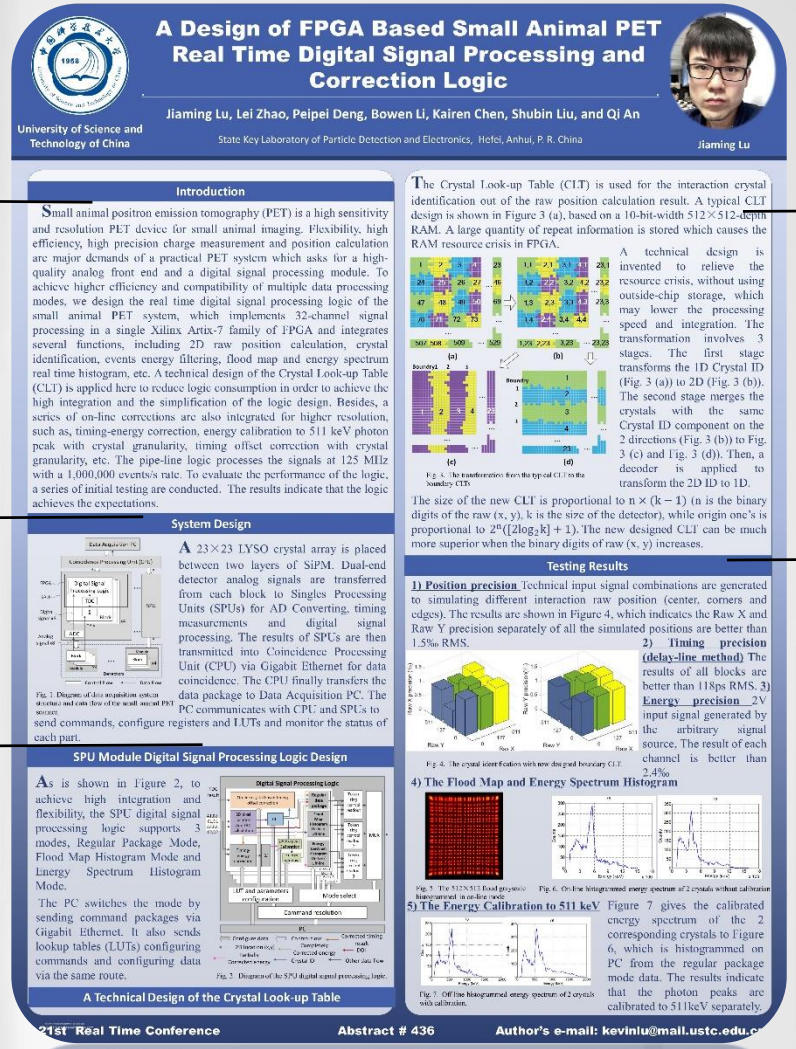
Introduction

- Background
- General Introduction

System Design

Logic Design

- Digital Signal Processing Logic Design



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Introduction

Small animal positron emission tomography (PET) is a high sensitivity and resolution PET device for small animal imaging. Flexibility, high efficiency, high precision charge measurement and position calculation are major demands of a practical PET system which asks for a high-quality analog front end and a digital signal processing module. To achieve higher efficiency and compatibility of multiple data processing modes, we design the real time digital signal processing logic of the small animal PET system, which implements 32-channel signal processing in a single Xilinx Artix-7 family of FPGA and integrates several functions, including 2D raw position calculation, crystal identification, events energy filtering, flood map and energy spectrum real time histogram, etc. A technical design of the Crystal Look-up Table (CLT) is applied here to reduce logic consumption in order to achieve the high integration and the simplification of the logic design. Besides, a series of on-line corrections are also integrated for higher resolution, such as, timing-energy correction, energy calibration to 511 keV photon peak with crystal granularity, timing offset correction with crystal granularity, etc. The pipe-line logic processes the signals at 125 MHz with a 1,000,000 events/s rate. To evaluate the performance of the logic, a series of initial testing are conducted. The results indicate that the logic achieves the expectations.

System Design

A 23×23 LYSO crystal array is placed between two layers of SiPM. Dual-end detector analog signals are transferred from each block to Singles Processing Units (SPUs) for AD Converting, timing measurements and digital signal processing. The results of SPUs are then transmitted into Coincidence Processing Unit (CPU) via Gigabit Ethernet for data coincidence. The CPU finally transfers the data package to Data Acquisition PC. The PC communicates with CPU and SPUs to send commands, configure registers and LUTs and monitor the status of each part.

Fig. 1. Diagram of the acquisition system structure and data flow of the small animal PET scanner.

SPU Module Digital Signal Processing Logic Design

As is shown in Figure 2, to achieve high integration and flexibility, the SPU digital signal processing logic supports 3 modes, Regular Package Mode, Flood Map Histogram Mode and Energy Spectrum Histogram Mode.

The PC switches the mode by sending command packages via Gigabit Ethernet. It also sends lookup tables (LUTs) configuring commands and configuring data via the same route.

Fig. 2. Diagram of the SPU digital signal processing logic.

A Technical Design of the Crystal Look-up Table

The Crystal Look-up Table (CLT) is used for the interaction crystal identification out of the raw position calculation result. A typical CLT design is shown in Figure 3 (a), based on a 10-bit-width 512×512-depth RAM. A large quantity of repeat information is stored which causes the RAM resource crisis in FPGA.

A technical design is invented to relieve the resource crisis, without using outside-chip storage, which may lower the processing speed and integration. The transformation involves 3 stages. The first stage transforms the 1D Crystal ID (Fig. 3 (a)) to 2D (Fig. 3 (b)). The second stage merges the crystals with the same Crystal ID component on the 2 directions (Fig. 3 (b)) to Fig. 3 (c) and Fig. 3 (d)). Then, a decoder is applied to transform the 2D ID to 1D.

Fig. 3. The transformation from the typical CLT to the boundary CLTs

The size of the new CLT is proportional to $n \times (k-1)$ (n is the binary digits of the raw (x, y), k is the size of the detector), while origin one's is proportional to $2^n([2\log_2 k]+1)$. The new designed CLT can be much more superior when the binary digits of raw (x, y) increases.

Testing Results

1) Position precision Technical input signal combinations are generated to simulating different interaction raw position (center, corners and edges). The results are shown in Figure 4, which indicates the Raw X and Raw Y precision separately of all the simulated positions are better than 1.5‰ RMS.

Fig. 4. The crystal identification with new designed boundary CLT.

2) Timing precision (delay-line method) The results of all blocks are better than 118ps RMS. **3) Energy precision** 2V input signal generated by the arbitrary signal source. The result of each channel is better than 2.4‰

4) The Flood Map and Energy Spectrum Histogram

Fig. 5. The 512×512 flood map in histogrammed in on-line mode.

Fig. 6. On-line histogrammed energy spectrum of 2 crystals without calibration.

5) The Energy Calibration to 511 keV Figure 7 gives the calibrated energy spectrum of the 2 corresponding crystals to Figure 6, which is histogrammed on PC from the regular package mode data. The results indicate that the photon peaks are calibrated to 511keV separately.

Fig. 7. Off line histogrammed energy spectrum of 2 crystals with calibration.

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Design of the CLT

- The transformation from the typical CLT to the new-designed boundary CLTs

Testing

- Position precision
- Timing precision
- Energy precision
- The Flood Map and Energy Spectrum Histogram
- The Energy online Calibration to 511 keV

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