Prototype of Front-end Electronics for PandaX-4ton Experiment

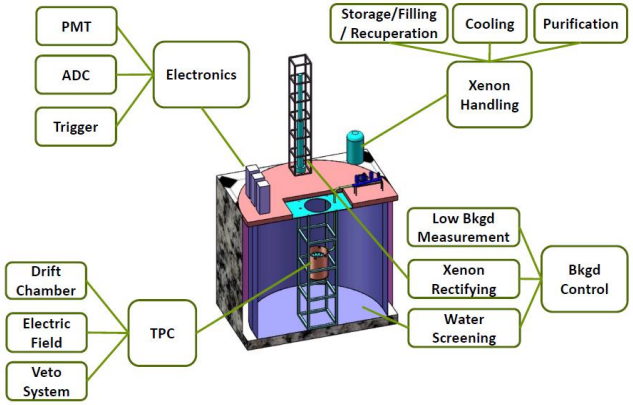

Fig. 1. PandaX-4ton Experiment Design

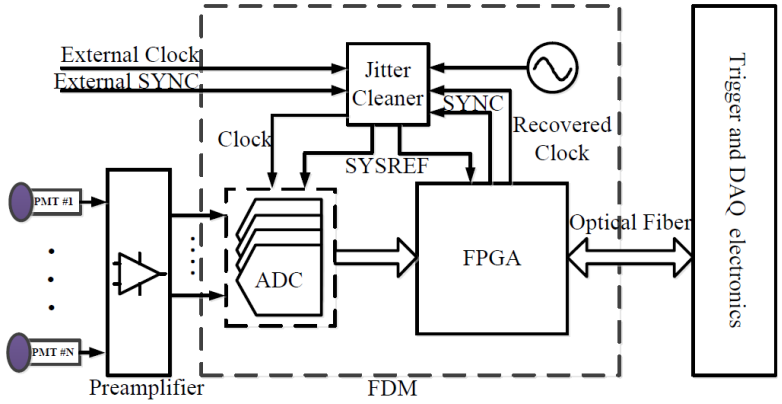

Fig. 2 Front-end electronics system schematic

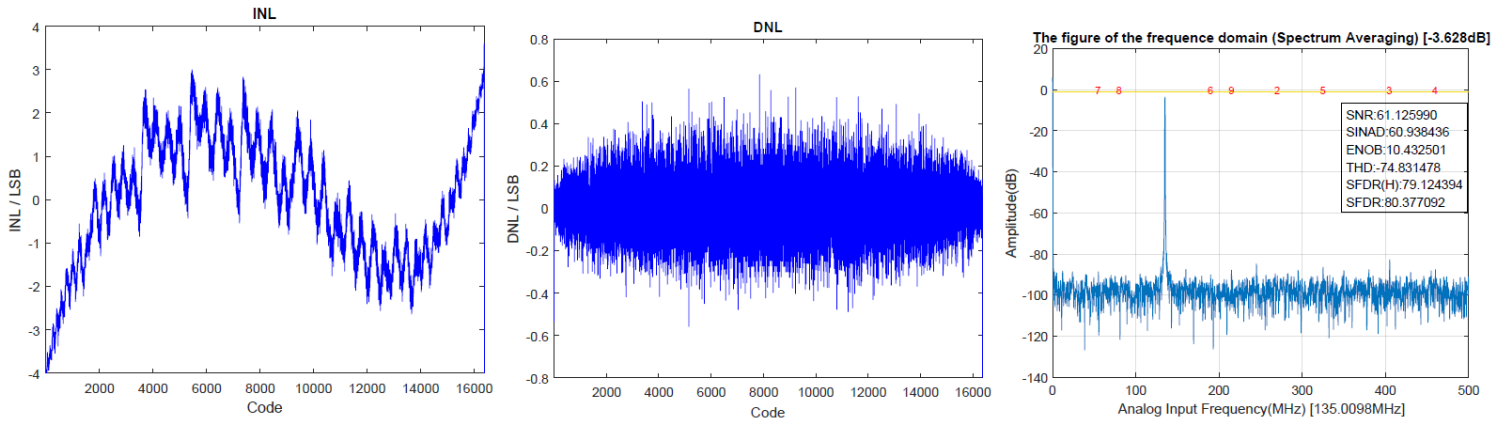

Fig. 3. The test results of front-end digital module

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Poster

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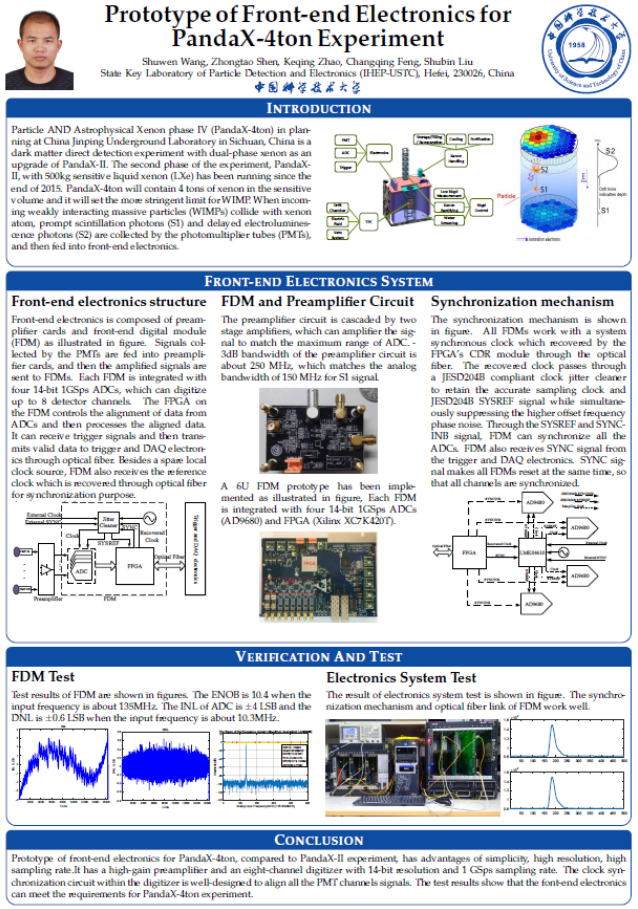

Prototype of Front-end Electronics for PandaX-4ton Experiment

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INTRODUCTION

Particle AND Astrophysical Xenon phase IV (PandaX-4ton) in planning at China Jinping Underground Laboratory in Sichuan, China is a dark matter direct detection experiment with dual-phase xenon as an upgrade of PandaX-II. The second phase of the experiment, PandaX-II, with 500kg sensitive liquid xenon (LXe) has been running since the end of 2015. PandaX-4ton will contain 4 tons of xenon in the sensitive volume and it will set the more stringent limit for WIMP. When incoming weakly interacting massive particles (WIMPs) collide with xenon atom, prompt scintillation photons (S1) and delayed electroluminescence photons (S2) are collected by the photomultiplier tubes (PMTs), and then fed into front-end electronics.

FRONT-END ELECTRONICS SYSTEM

Front-end electronics structure

Front-end electronics is composed of preamplifier cards and front-end digital module (FDM) as illustrated in figure. Signals collected by the PMTs are fed into preamplifier cards, and then the amplified signals are sent to FDMs. Each FDM is integrated with four 14-bit 1GSps ADCs, which can digitize up to 8 detector channels. The FPGA on the FDM controls the alignment of data from ADCs and then processes the aligned data. It can receive trigger signals and then transmits valid data to trigger and DAQ electronics through optical fiber. Besides a spare local clock source, FDM also receives the reference clock which is recovered through optical fiber for synchronization purpose.

FDM and Preamplifier Circuit

The preamplifier circuit is cascaded by two stage amplifiers, which can amplifier the signal to match the maximum range of ADC. -3dB bandwidth of the preamplifier circuit is about 250 MHz, which matches the analog bandwidth of 150 MHz for S1 signal.

A 6U FDM prototype has been implemented as illustrated in figure. Each FDM is integrated with four 14-bit 1GSps ADCs (AD9680) and FPGA (Xilinx XC7K420T).

Synchronization mechanism

The synchronization mechanism is shown in figure. All FDMs work with a system synchronous clock which recovered by the FPGA's CDR module through the optical fiber. The recovered clock passes through a JESD204B compliant clock jitter cleaner to retain the accurate sampling clock and JESD204B SYSREF signal while simultaneously suppressing the higher offset frequency phase noise. Through the SYSREF and SYNC~INB signal, FDM can synchronize all the ADCs. FDM also receives SYNC signal from the trigger and DAQ electronics. SYNC signal makes all FDMs reset at the same time, so that all channels are synchronized.

VERIFICATION AND TEST

FDM Test

Test results of FDM are shown in figures. The ENOB is 10.4 when the input frequency is about 135MHz. The INL of ADC is ±4 LSB and the DNL is ±0.6 LSB when the input frequency is about 10.3MHz.

Electronics System Test

The result of electronics system test is shown in figure. The synchronization mechanism and optical fiber link of FDM work well.

CONCLUSION

Prototype of front-end electronics for PandaX-4ton, compared to PandaX-II experiment, has advantages of simplicity, high resolution, high sampling rate.It has a high-gain preamplifier and an eight-channel digitizer with 14-bit resolution and 1 GSps sampling rate. The clock synchronization circuit within the digitizer is well-designed to align all the PMT channels signals. The test results show that the font-end electronics can meet the requirements for PandaX-4ton experiment.

← Front-end electronics system

← Conclusion

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