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Quality Evaluation Electronics for CBM-TOF Super Module

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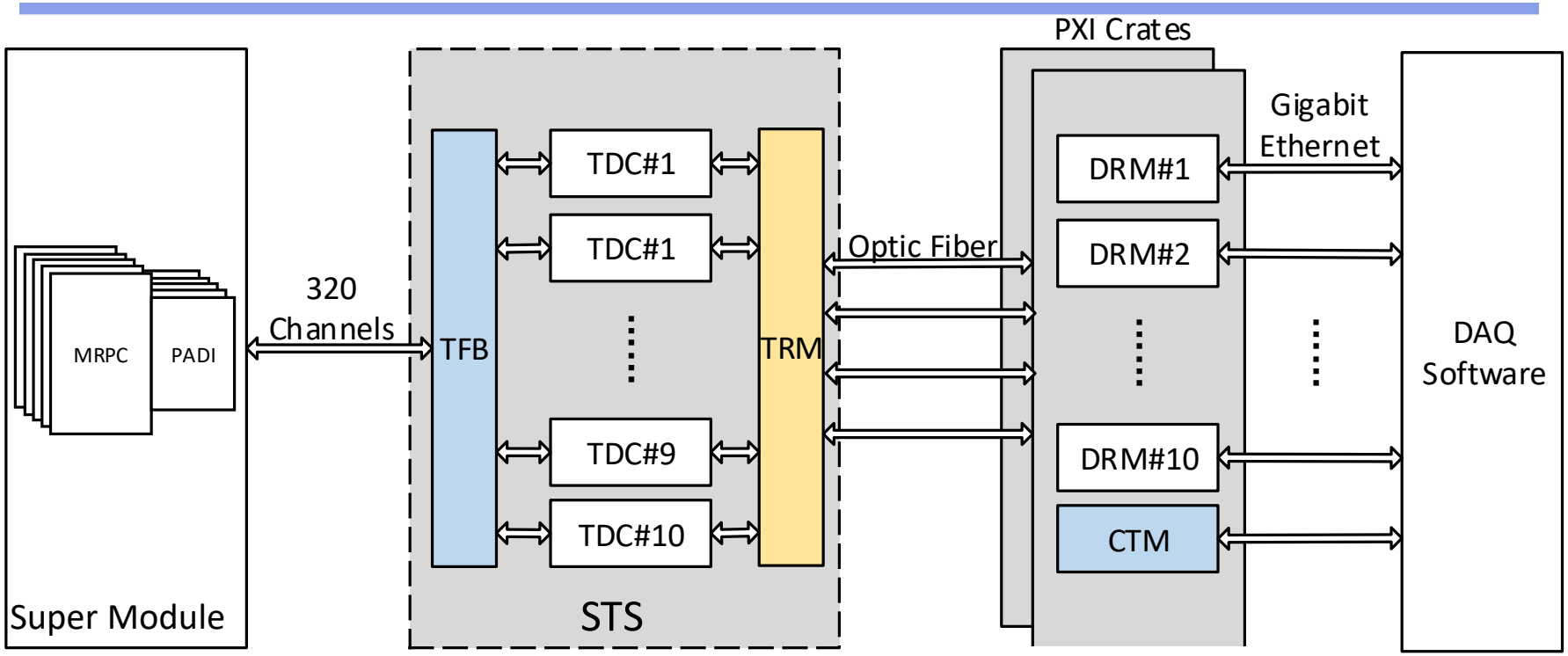
Architecture of quality evaluation electronics



- Time digitizer
  - 10 TDC for 320-channel time digitizing
  - Each TDC has 32 electronic channels with TOT measurement
- Readout modules
  - TDC Readout Motherboard (TRM) for reading out multiple TDC
  - data readout module (DRM) for sending data to the DAQ system

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Introduction

System Design

Implementation of the time digitizer

Implementation of readout modules

Time resolution of TDC: 15 ps (RMS)

Time resolution of MRPC: 60 ps (RMS)

Quality Evaluation Electronics for CBM-TOF Super Module

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1. Introduction

The main purpose of the Compressed Baryonic Matter (CBM) experiment at the Facility for Antiproton and Ion Research (FAIR) is to study fundamental properties of the strong interaction. The Time-of-Flight (TOF) system is used for charged hadron identification, which is composed of 6 different types of super module detector assemblies named M1 to M6. Each M5 or M6 type of super module comprises 5 high resolution multi-gap Resistive Plate Chambers (MRPCs) and provides up to 320 electronic channels for high-precision time measurements. During mass production of the MRPCs, it is necessary and important to do quality control work to ensure that the detectors achieve the targeted performance. In this paper, the readout electronics based on the PXI platform is described. It has time resolution better than 20 ps and can read data out data from one super module at the rate of 6 Gbps.

2. System architecture

The quality evaluation system has a distributed architecture, as shown in Figure 1, including sandwich TDC station (STS), data readout module (DRM), synchronous clock and trigger network.

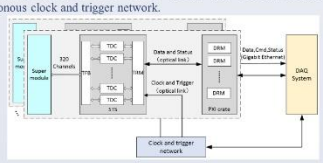

Figure 1. Architecture of readout electronics system

For the convenience of testing and analyzing the MRPCs, the system runs in the conventional frontend triggered mode. In this triggered system, the discriminated MRPC signals passing the frontend thresholds are digitized and buffed by the Time-to-Digital Converter (TDC). Around the same time, the dedicated trigger decision is generated and distributed to the TDC for selection of the effective time data from the buffer according to the arrival time. Then, the matched time data are transmitted to the TDC readout motherboard (TRM) for aggregation. In the end, the data readout module (DRM) exports the merged time data from the TRM though optical links to the data acquisition (DAQ) system through the Ethernet. In order to simplify the readout structure, the sandwich TDC station (STS) is proposed, each of which consists of 10 TDC boards and 1 TRM, serving as frontend electronics. Since the STS is placed near the super module detector, the DRM allocated in the PXI-6U crate in the electronics room is tens of meters away from the STS. Optical links are used to connect the DRM to the frontend electronics.

3. Time digitizer

As aforementioned, the time digitizer is one crucial parts of the readout electronics, which is aimed for acquiring the arriving time of particles and the charge information. A prototype of high resolution and density FPGA TDC board is designed, as showed in Figure. 2, which can supports up to 32 digitizing channels with a time resolution better than 20 ps and TOT measurement. For the sake of reducing cost, a low-end Xilinx (XC7A100T-1FGG484) FPGA is selected.

Both time digitizing and readout logic are implemented inside the FPGA. Time digitizing is fulfilled in two stages combing coarse time measurement with fine time measurement. Coarse time is provided by a circular counter which is controlled by the clock with a 4 ns period, and fine time is provided by using tapped delay line (TDL) to perform time interpolation within a coarse clock period. The dedicated fast lookahead carry logic in Xilinx FPGA called CARRY4 is used to construct a long delay chain for time interpolation. Each channel can save time information for up to 63 hits per trigger and can cope with burst hit rates of up to 100 MHz.

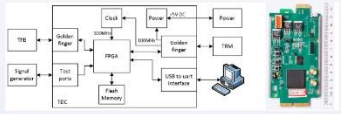

Figure 2. Left: Block diagram of the TDC. Right: Photo of the TDC board

4.Readout module

In order to export numerous data from the TDC to the backend DAQ, two type readout module called the TRM and the DRM are designed, which compose the second and third level of the readout system.

In consideration of reducing the output link of the frontend electronics and simplifying the readout structure, the TRM is designed for readout multiple TDC boards, as shown in Figure. 3. The main functions of the TRM are data aggregation, TDC configuration, and clock and trigger synchronization. There are two Xilinx Kintex-7 series FPGA (XC7K70T-1FFG676) in the TRM. Each FPGA aggregates time data from 5 TDC boards concurrently and transmits the data to the backend readout electronics as fast as possible with 2 optical uplinks, forming the second level of the readout system.

As shown in Figure. 4, a prototype of the DRM is proposed for delivering data from the TRM to the DAQ system, acting as the third level of the readout system. And it is also responsible for transferring the command from the DAQ system to the frontend readout electronics reversely. The DRM is designed as a standard PXI 6U plugin, mainly containing one FPGA, one SFP connector, two LEMO connectors and two Gigabit Ethernet boards (GEB). A Cyclone IV GX series FPGA (EP4CGX30CF23C8) with 4 integrated 3.125 Gbps transceivers (GXB) is adopted as the readout controller.

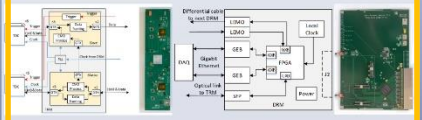

Figure 3. Photograph of TRM Figure 4. Photograph of DRM

5.Conclusion

To confirm the performance of the readout electronics, several tests were conducted both in the laboratory and with the detectors, including time measurement test, the clock performance test and cosmic ray test.

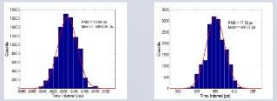

Figure 5. Left: Time measurement results of two channels from same TDC. Right: Time measurement of two channel from two separate TDC boards.

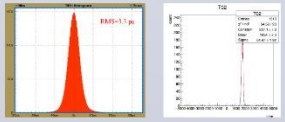

Figure 6. Left: Results of clock performance. Right: Results of cosmic ray test.

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