

A Zynq-based flexible ADC architecture combining real-time data streaming and transient recording

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Abstract

The RFX-mod2 Nuclear Fusion experiment is an upgrade of RFX-mod, that was shutdown in 2016. Among the other improvements in machine structure and diagnostics, a larger number of electromagnetic probes (EMs) is foreseen to provide more information about plasma instabilities and to allow an improved real-time plasma control. An Analog to Digital Converter (ADC) architecture able to provide both transient recording and real-time streaming is foreseen in RFX-mod2. Transient recording provides full speed data acquisition by recording data in local memory and reading memory content after the plasma discharge. Real-time streaming of sub-sampled data is required for active control. The chosen technology is based on the XILINX Zynq architecture that provides in the same chip a multi-core ARM processor tightly coupled to an FPGA.

Time critical functions carried out by the FPGA in this context are:

- 1) The management of a circular data buffer and the DMA transfer in RAM of pre and post trigger samples after the trigger has been received;
- 2) Antialiasing filtering and subsampling of the samples to be streamed. The resulting samples are enqueued in a FIFO accessed by the processor.

The functions carried out by the processor are:

- 1) The management of the configuration setting, received via TCP/IP or HTTP. The processor validates the configuration and write the appreciate registers in the FPGA;
- 2) Offline data readout of acquired samples in transient recording;
- 3) Network data streaming of subsampled data read from the FIFO and sent in UDP packets to the active plasma control system.

Numerical integration of EM probes for RFX-mod2

RFX-mod [1] is a toroidal plasma machine $R = 2.0\text{m}$, $a = 0.46\text{m}$. Works in 2 MA current (RFP) or 0.5 T (Tokamak). The experiment was shut down in 2016 and is now being upgraded as RFX-mod2 [2]. A major foreseen development is a **substantial improvement of the magnetic measurement system**.

EM feedback changes:

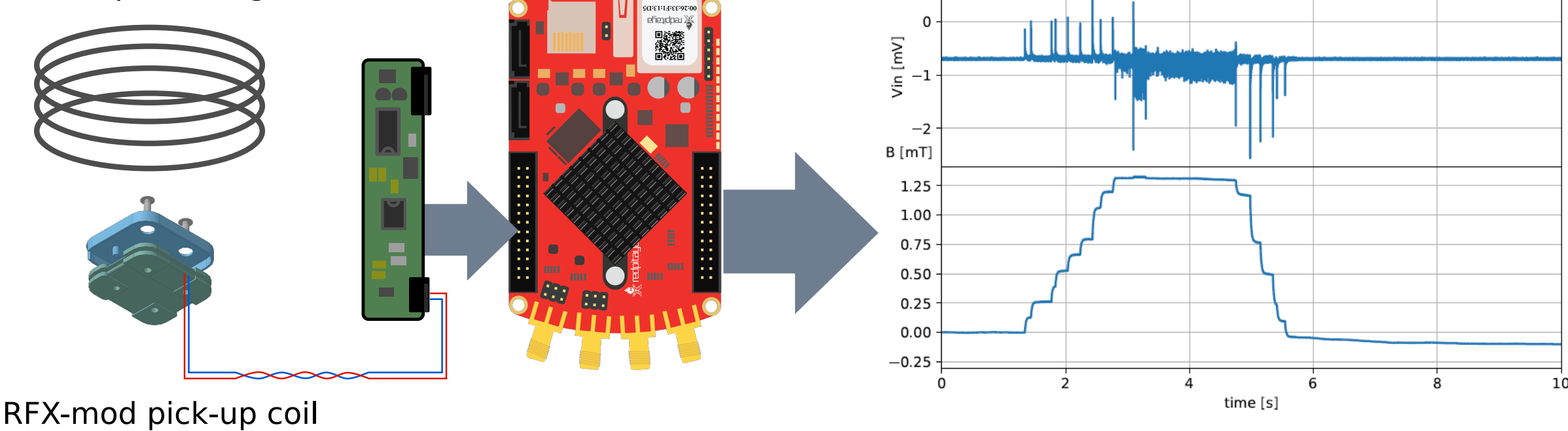
- 1) Sensors moved inside the vacuum vessel widening usable **signal bandwidth up to 200 kHz**.
-> better plasma control.
- 2) Total number of pick-up coils will be increased
-> improved spatial resolution [3].

We need a device with strong electrical insulation. In addition, the possibility of a fast data acquisition, together with the local numerical integration requires for a device with high bandwidth, sensitivity and SNR.

To match the these characteristics a compact and cost effective solution has been investigated based on the ATCA-MIMO-ISOL [9] architecture developed for the plasma column vertical stabilization at JET tokamak experiment. The ADC module is composed by a plug-in component mounting a 18-bit SAR converter from Analog Devices (AD7641) that acquires signals from a fully differential input in the range 2.048 V at a maximum rate of 2 MSamples/s.

A proper logic interface has been built in FPGA to talk with the serial 4-wire LVDS protocol. A simulated mock-up experiment was set to test the correct module acquisition.

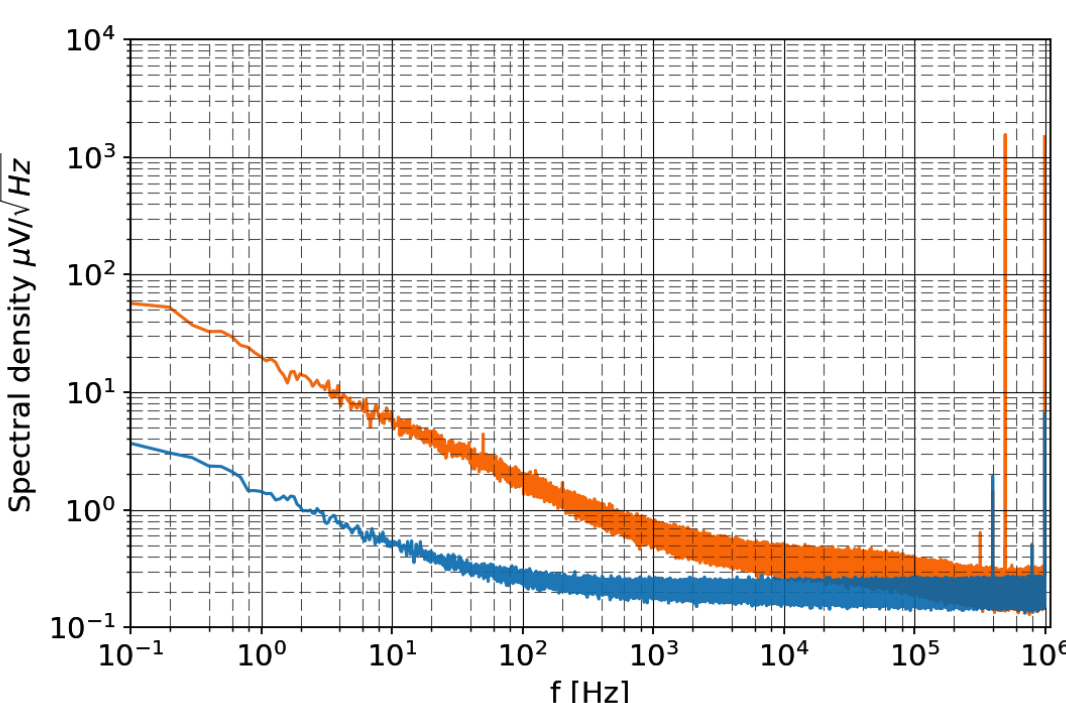
Mock-up B field gen.



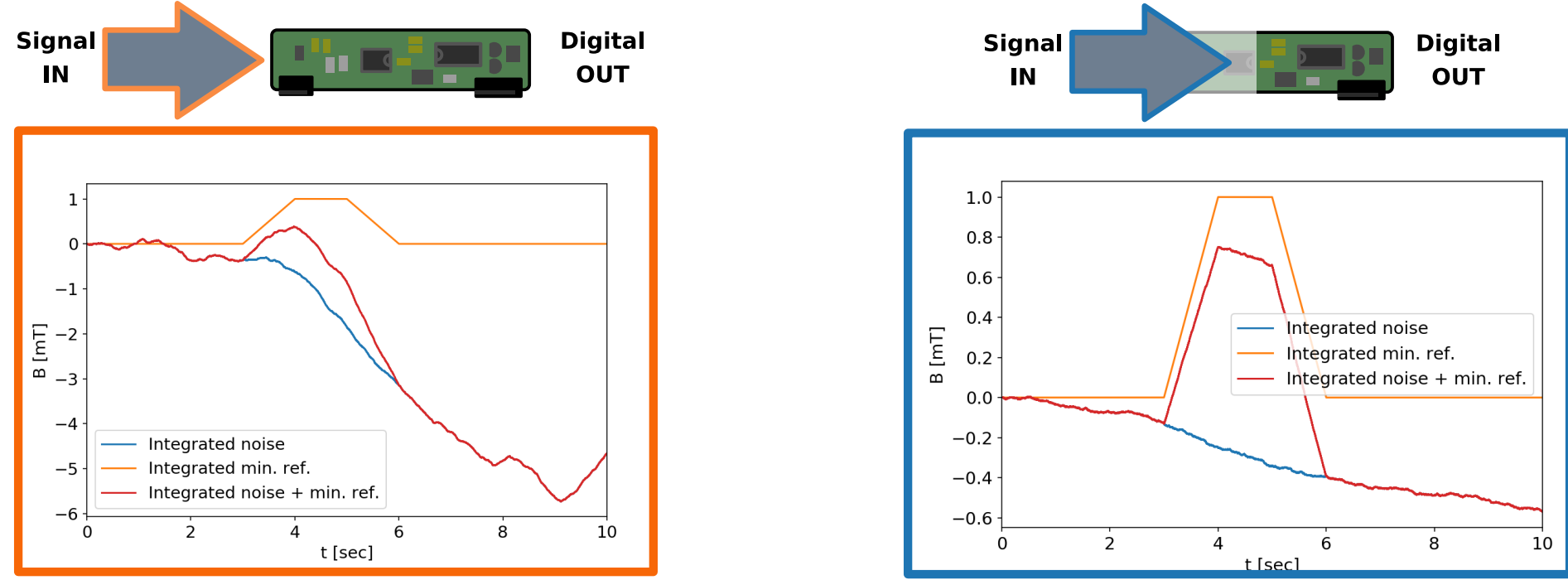
Noise requirements in ADC stage for digital integration

If we try to extend the acquisition over a simulated RFX-mod2 long pulse signal the **natural flickering 1/f noise** that comes from the electrical components [11] dominates the final result making the use of direct acquisition non feasible for numerical integration. A detailed characterization of the noise has been studied [5] proving that a possible solution could come from the careful selection of components.

In the image the two curves represent the noise spectra of the entire module acquisition in red, showing the $1/f$ behavior with a very high cut-off freq; and the noise of the sole ADC component in blue with the expected cut-off.



The effect of the $1/f$ noise introduces a drift in the integration. Two instances of the integrated noise are shown in the figures below compared with a **10s** signal of **1 mT** for the two noise spectra:



Flexible ADC SoC implementation

The RFX-mod2 improved controllability will require the design of a **new ADC architecture** able to provide both the transient recording and the streaming of data for the control of the experiment.

The **transient recorder** functionality will provide full speed data acquisition (up to $1 \approx 2$ MSample/s) by recording data in local memory and reading back the memory content after the plasma discharge.

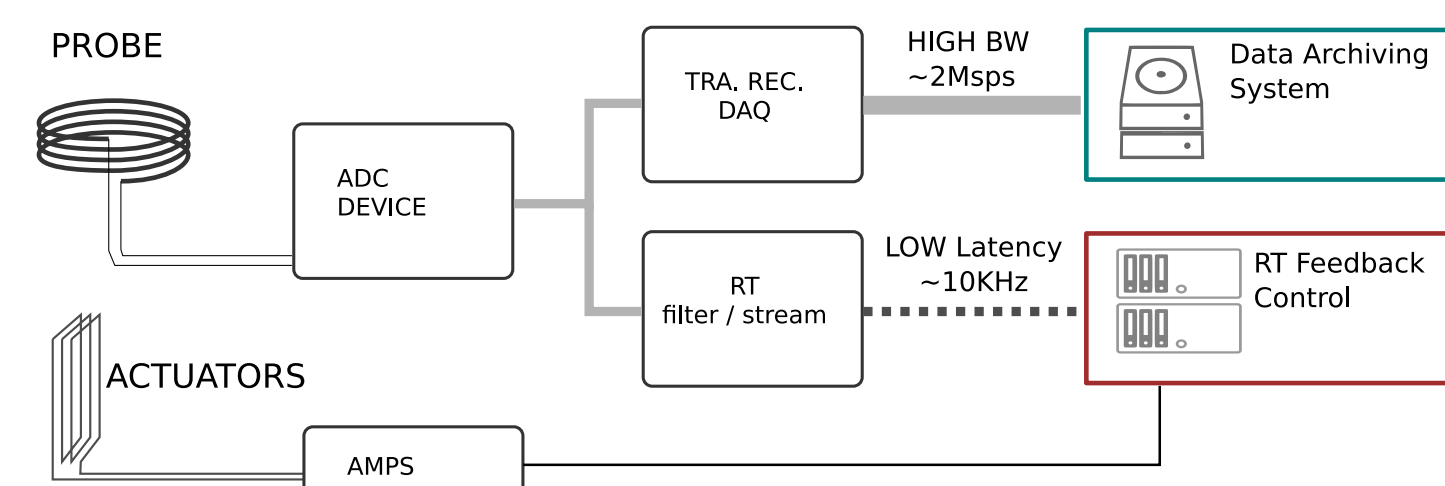
At the same time the **real-time streaming** functionality is required when the target signal is used in active control because such data must be promptly available in the closed loop feedback. In this case a 10 kHz sub-sampled version is streamed out toward the control units.

The solution proposed comes from the adoption of the technology based on the **XILINX Zynq** architecture that provides in the same chip a multi-core ARM processor tightly coupled to an FPGA. The critical functions implemented inFPGA are:

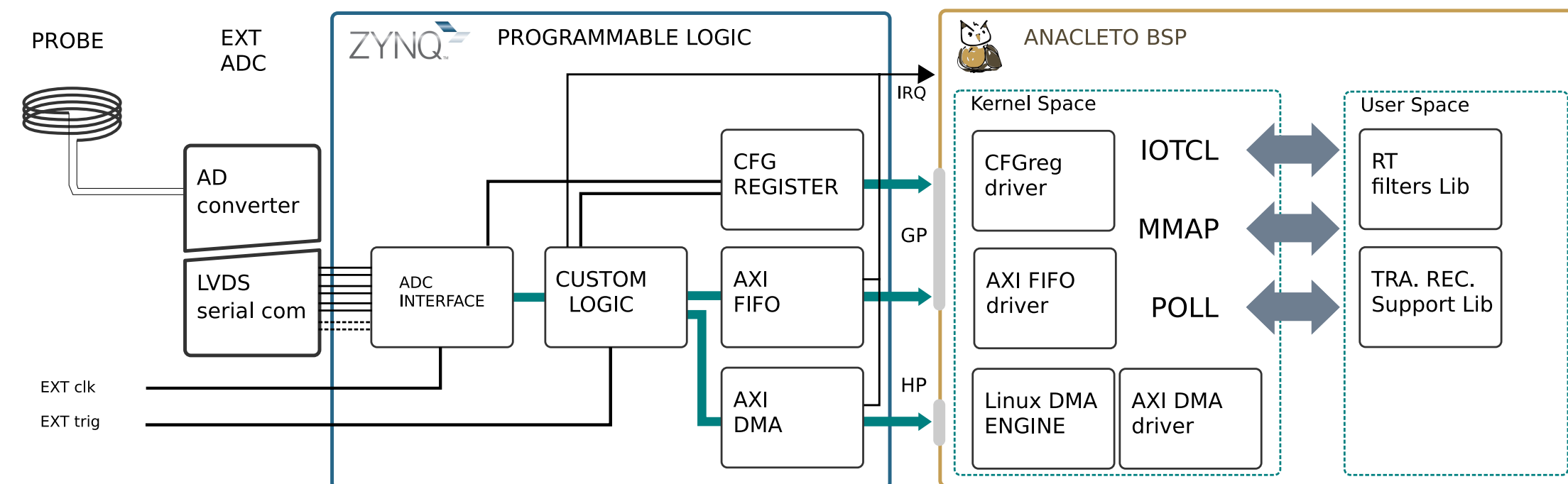
- The management of a circular data buffer and the DMA transfer in RAM of pre and post trigger samples after the trigger has been received;
- anti-aliasing filtering and sub-sampling of the signal data to be streamed.
- digital integration for deriving magnetic field measurements from EM probe signals
- ROI detection in case ADC triggers are derived from the signal itself (e.g. over a given signal level threshold)
- Clock and trigger extraction in case a highway signal is provided by the timing system, encoding both clock and triggers.

The less critical functions that will be carried out by the processor unit are:

- The management of the configuration setting, received via TCP/IP or HTTP.
- off-line data readout of acquired samples in transient recording;
- network data streaming of sub-sampled data read from the FIFO and sent in UDP packets to the active plasma control system.



Developing critical and non critical functions requires HDL development for the first ones, and C or C++ code development for the others. In addition, a Linux driver must be written, acting as a bridge between the FPGA functions and the outside world. The ANACLETO framework provides an effective solution by transparently orchestrating the download and the installation of the required components and toolchain, letting the developer concentrate on the specific aspects of his/her project.



The following communication media are supported by ANACLETO:

- I/O registers
- Input and/or output FIFOs
- Input and/or output DMA channels

ANACLETO recognizes the I/O registers, FIFOs and DMA controllers defined in the FPGA project (available as IPs in the XILINX toolbox), modifies the device tree produced by VIVADO and produces the corresponding source code driver template.

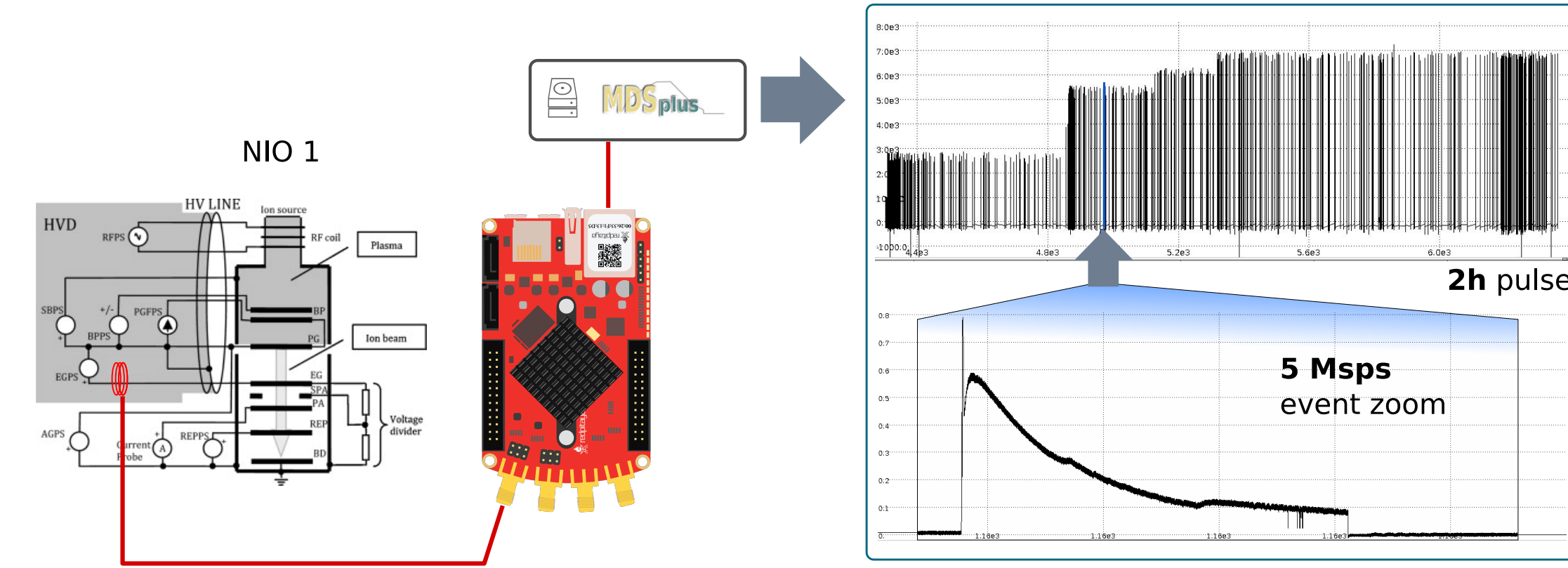
Starting from the template, the developer will implement the specific functions, but he can ignore to a large extent the intricacies required for the I/O data transfer such as Interrupt handler programming and DMA engine configuration.

Working example for event triggered acquisition for NIO1

Another desired topics for a DAQ device is the possibility to increase the level of detail during acquisition based on particular events. Indeed is not uncommon to have an observed quantity that changes rapidly in time and than last steady or possibly in a non interesting state for long periods.

As real case scenario this acquisition technique has been applied to Nio experiment [11] a small radio frequency negative ions beam source with a high voltage electrostatic particle accelerator stage composed of grids. In certain conditions breakdown events [12] appear on the high voltage gaps of the grids causing a high current discharges of the power supply feeding the accelerator.

A current probe has been placed around the wire connecting the extraction grid to power supplies (ESPS) before the protection units. A break-down event discharging the grid causes a sudden current flowing in that circuit that depends on the charge of the grid itself. The first plot shows a dense sequence of these events occurring during 2h NIO operation with different setting parameters. One of the events is plotted deep zooming into the same signal revealing the shape of the current at a rate of **5 Msps** for a total event duration of **20us**



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Acknowledgments:

The authors would express their gratitude to all the people from RFX, from the technicians to the administrative employees, that directly or indirectly took part in this work with their useful ideas, suggestions and support.

A special thanks to all the NIO1 experiment crew in the person of Gianluigi Seriani.

<https://github.com/mildstone/anacleto>

fork Anacleto here ! ->

Thanks for your attention to this work,
if I'm not next to this poster please find me around the session.

I am very willing to interact.
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