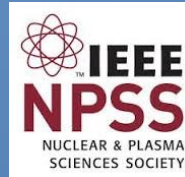




21th Real Time Conference 2018



General purpose readout board

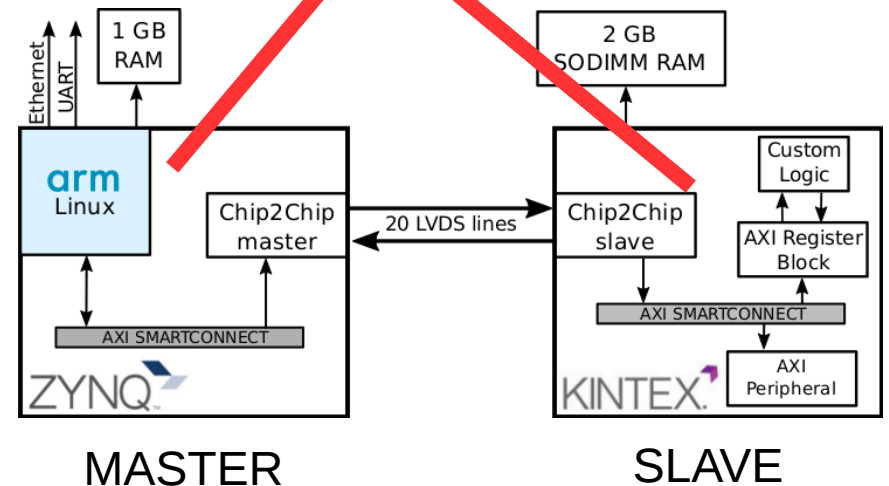
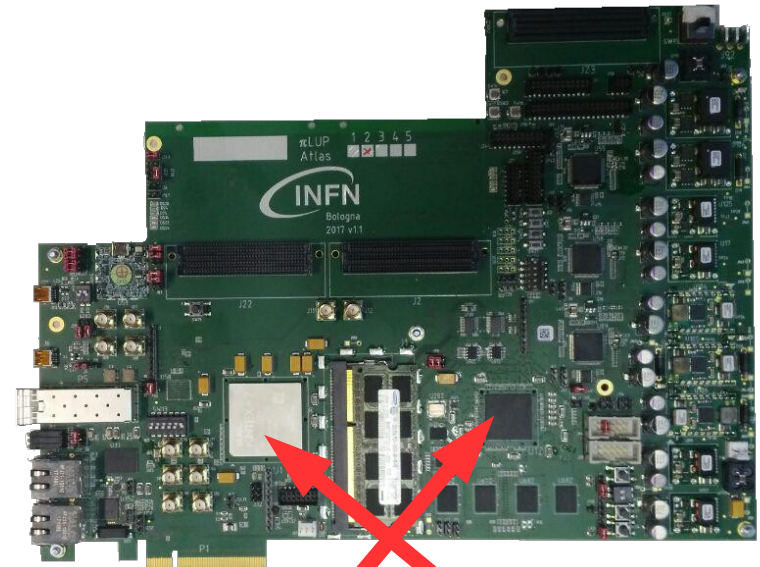
π LUP:

overview and results.

Nico Giangiacomi, Fabrizio Alfonsi, Gabriele
d'Amen, Gabriele Balbi, Davide Falchieri,
Alessandro Gabrielli, Giuseppe Gebbia, Giuliano
Pellegrini, Davide Soverini
University and INFN Bologna

Why you should be interested

- **PCIe** Readout board
- **80 Gbps** max bandwidth
- Two FPGAs architecture:
Xilinx **ZYNQ 7 (MASTER)**
Xilinx **KINTEX 7 (SLAVE)**
- **PetaLinux** kernel on **ARM core**
- Different applications
 - **Readout** system
 - Data **generator**
 - System **interface**
- Interface with **FELIX**
- Highly versatile



General purpose readout board π LUP: overview and results.

Nico Giangiacomi^{1,2}, Francesco S. Biondi¹, Roberto di Loreto¹, Roberto Belli², Danilo Fabiani¹, Alessandro Galassi¹, Giuseppe Galbiati¹, Claudio Pellegrini¹, Danilo Veronesi¹

NPSS 21th Real Time Conference 2016
Theoretical Physics Institute, INFN Bologna, www.giangiacomi.org

This report gives an overview of the π LUP Express based π LUP focusing on the motivation that led to its development, the technology choices adopted and its performance. The π LUP board was designed by INFN and University of Bologna as a general readout solution to be used after the upgrade of the Pixel Detector of the ATLAS and CMS experiments at LHC. The same team at Bologna also designed and commissioned the Read Out Driver (ROD) board, recently implemented in all the two layers of the ATLAS Pixel Detector (see table II, Layers Layer 2 and Layer 3), and used in the past years together with the ATLAS readout chain and the publications arising in each experiment as follows. The π LUP was designed to be a general purpose, i.e. highly versatile readout for a variety of applications, several of which will be discussed in this work. The π LUP operation will be discussed in this document as follows: a description of the board architecture and a description of the hardware and software. The hardware and software protocols have been tested at different speeds. The hardware of π LUP boards have been fabricated and tested: two boards in the first batch (version 1.0) and four boards in the second batch (version 1.1), comprising all the patterns required for the readout system.

π LUP: READOUT BOARD PROPOSAL

- The Bologna π LUP cards is a 16 layers PCI Express board capable of interfacing to several different other boards or front-ends and processing data at high speed. Main components:
 - 7 series Xilinx FPGAs
 - 16 steps of Xilinx 40100 for trigger and data processing at 100 MHz with high speed dual core ARM Cortex-A9
 - 1 x PCIe Express interface (AGB) towards the PC memory
 - 16 external signals:
 - 4 x SPD connectors
 - 4 x SMI connectors
 - 4 x IFC SMI connectors
 - 4 x LFC SMI connectors
 - 1 x HPC (40 pins) FMC
 - 2 x LPC (160 pins) FMC
 - DDR3 2x67 MHz
 - ARM Dual-Core A9
 - 16 layers - stacking



Version 1.0 (2 boards produced)

Version 1.1 (4 boards produced)

π LUP applications

- The main applications for the π LUP board are:
 - Kernel on control systems: front-end triggers, online data processing, fast triggering and data transfer via PCIe bus. Max bandwidth: 4 GB/s (8 lanes PCIe gen 2 max speed) or 7.9 GB/s (8 lanes PCIe gen 3 max speed)
 - Data generator front-end emulator. Max throughput: 10 GB/s (8x 10 Gbps transceivers)
 - Bridge between two different systems: connection between two different readout systems that use different protocols or different communication physical layers.

π LUP application: Protocol Converter

- Collaboration started between FELIX group and Bologna π LUP group
- Target: interface the new KODIA read-out chip (CEFN project for the ATLAS and CMS's Pixel Detectors upgrade)
- Protocol Converter to transform 4rd 28 Gbps Aurora 64000 Protocol to 9.6 Gbps PCIe Protocol
- KODIA Emulators only fitted in π LUP

π LUP OVERVIEW

APPLICATIONS

SOFTWARE ARCHITECTURE

RD53A READOUT SYSTEM

RESULTS

EYE DIAGRAM SCANS

- π LUP Results
- All 16 Gbps transceivers tested
- Several Protocols Tested:
 - GBT (4.8 Gbps)
 - PCIe Mode (9.6 Gbps)
 - Aurora 64k/64k (4.128 Gbps, 1x 5.12) Gbps
- PCI Express tested:
 - Gen2: max user payload: 31 GB/s
 - Gen3: under development

Protocol	Line Rate (Gbps)	Line Rate (MBps)
GBT	4.8	600
PCIe Mode	9.6	1200
Aurora 64k/64k	4.128	516
Aurora 64k/64k	5.12	640
GBT	4.8	600
PCIe Mode	9.6	1200
Aurora 64k/64k	4.128	516
Aurora 64k/64k	5.12	640

XILINX IBERT TEST (Feedback)

