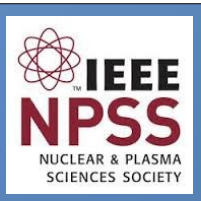
21th Real Time Conference 2018



General purpose readout board πLUP: overview and results.

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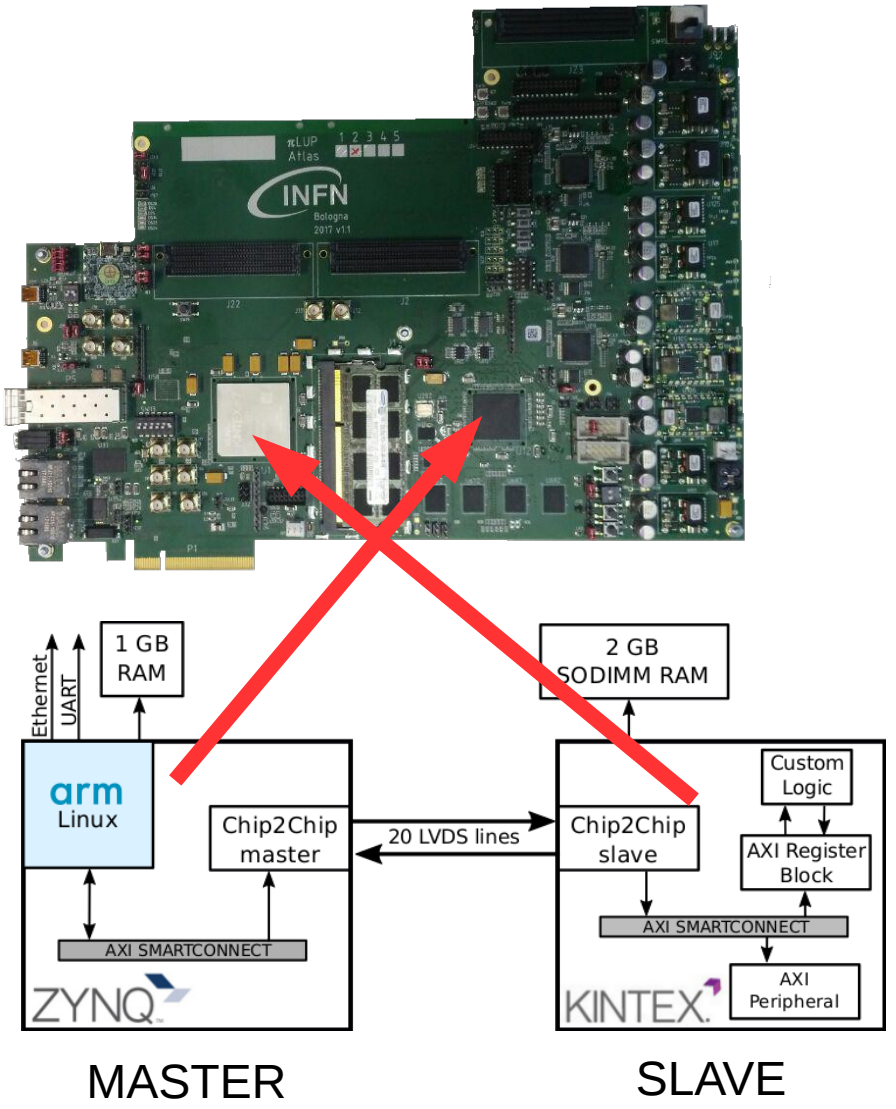
Why you should be interested

- **PCIe** Readout board
- **80 Gbps** max bandwidth
- Two FPGAs architecture:
  Xilinx ZYNQ 7 (**MASTER**)
  Xilinx KINTEX 7 (**SLAVE**)
- **PetaLinux** kernel on ARM core
- Different applications
  - **Readout** system
  - Data **generator**
  - System **interface**
- Interface with **FELIX**
- Highly versatile



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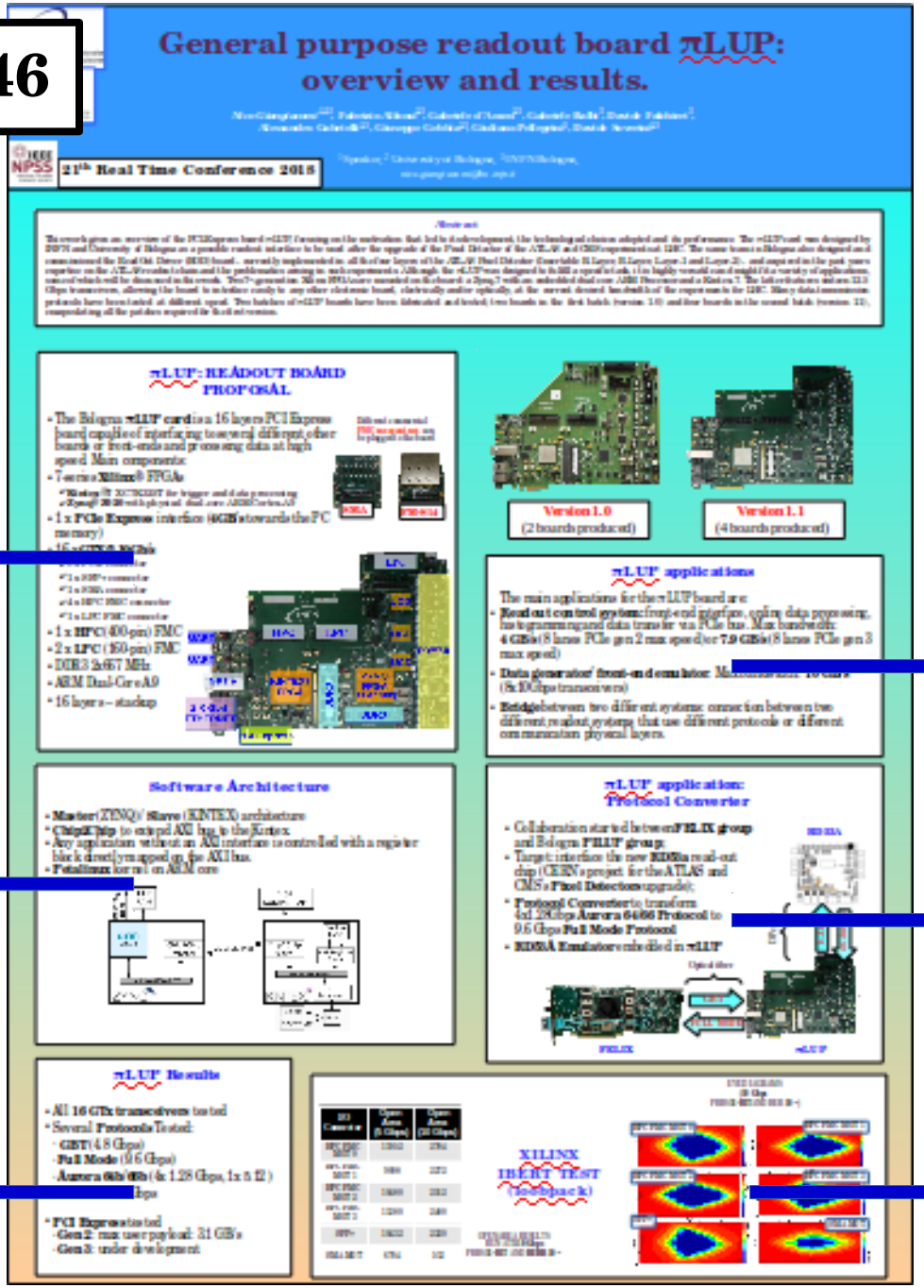

πLUP OVERVIEW

APPLICATIONS

SOFTWARE ARCHITECTURE

RD53A READOUT SYSTEM

RESULTS

EYE DIAGRAM SCANS