21st IEEE Real Time Conference - Colonial Williamsburg

Friday 15 June 2018

Front End Fast Detectors 2 (11:10-12:50)

-Conveners: Jinyuan Wu

time	[id] title	presenter
11:10	[411] A 3.8ps RMS time synchronization implemented in a 20 nm FPGA	Mr XIE, HongBo
11:30	[439] FPGA Based Pico-second Time Measurement System for a DIRC-like TOF Detector	Mr CAO, Qiang
11:50	[444] Preliminary Design of Integrated Digitizer Base for Photomultiplier Tube	Mr ZHU, Jinfu
12:10	[582] Development of a multichannel FPGA based high resolution Time-to-Digital Converter	TAKAHASHI, Tomonori
12:30	[437] A 5.5 ps Time-interval RMS Precision Time-to-Digital Convertor Implemented in Intel Arria 10 FPGA	Mr KUANG, Jie Prof. WANG, Yonggang