

# MicroTCA.4 Communication Links

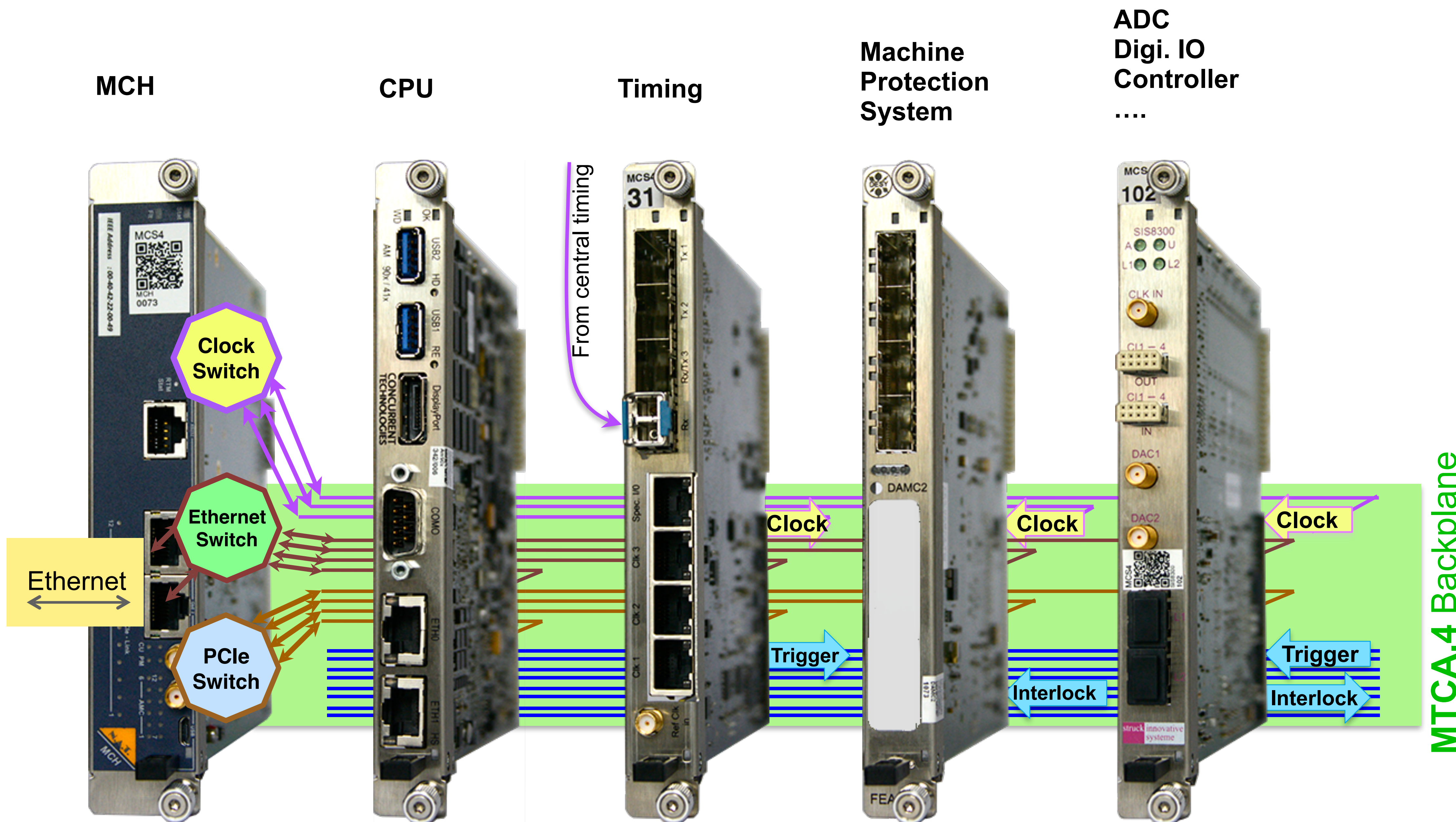
Kay Rehlich, DESY MicroTCA Technology Lab

Backplane MTCA.0 & MTCA.4  
Ethernet, PCIe, SATA  
Clocks, Triggers, interlocks  
Point-to-point

# MicroTCA Crate Backplane Communication

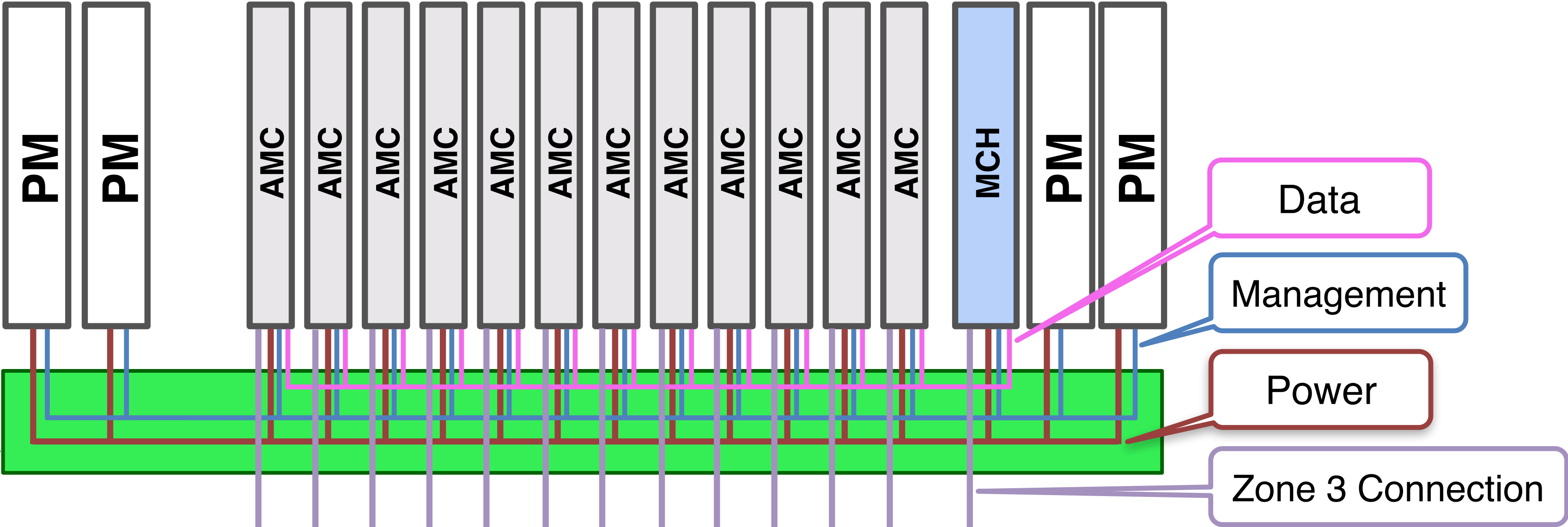
Common modules

Application modules



# MTCA.4 Backplane

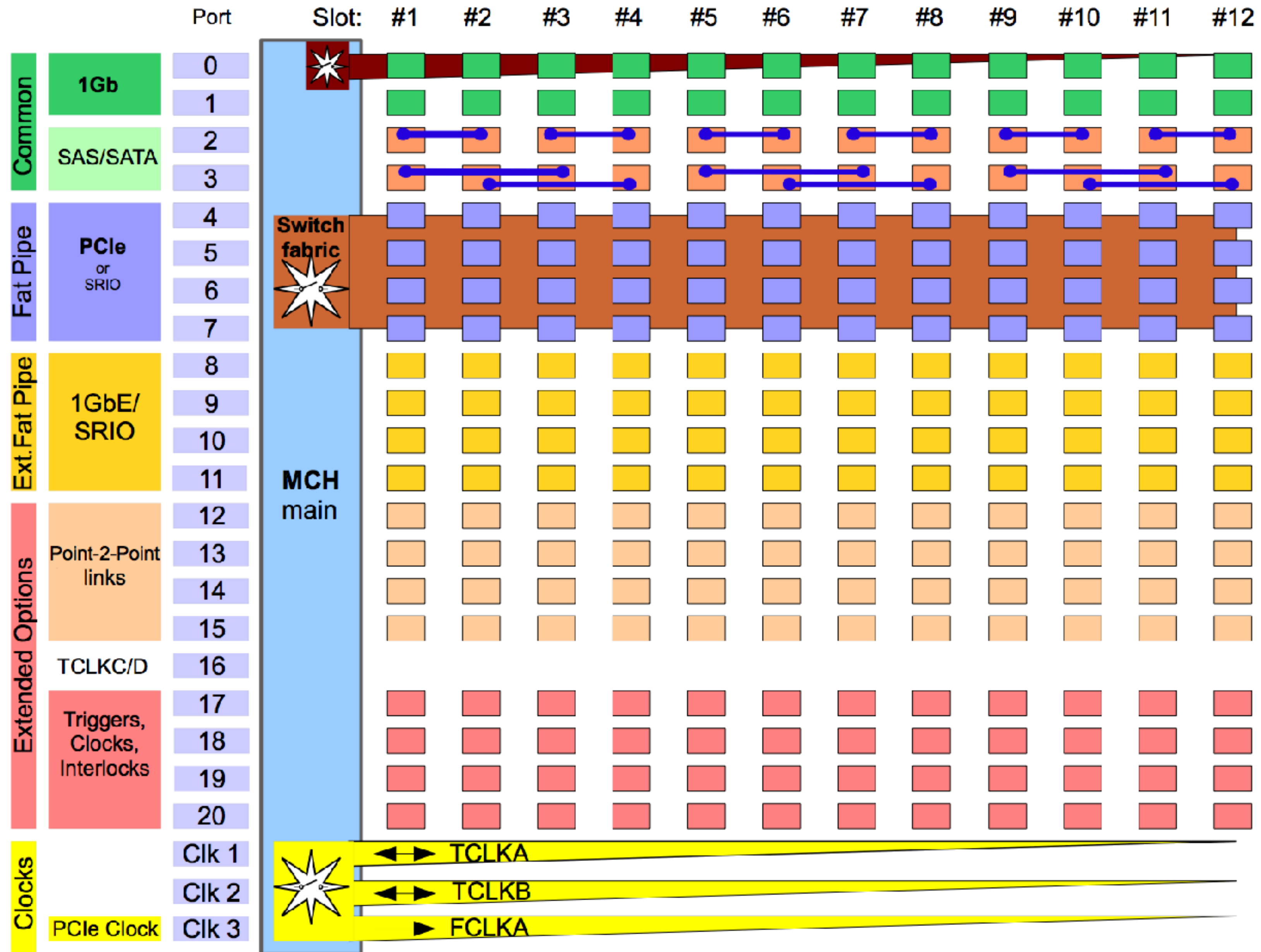
Front Side



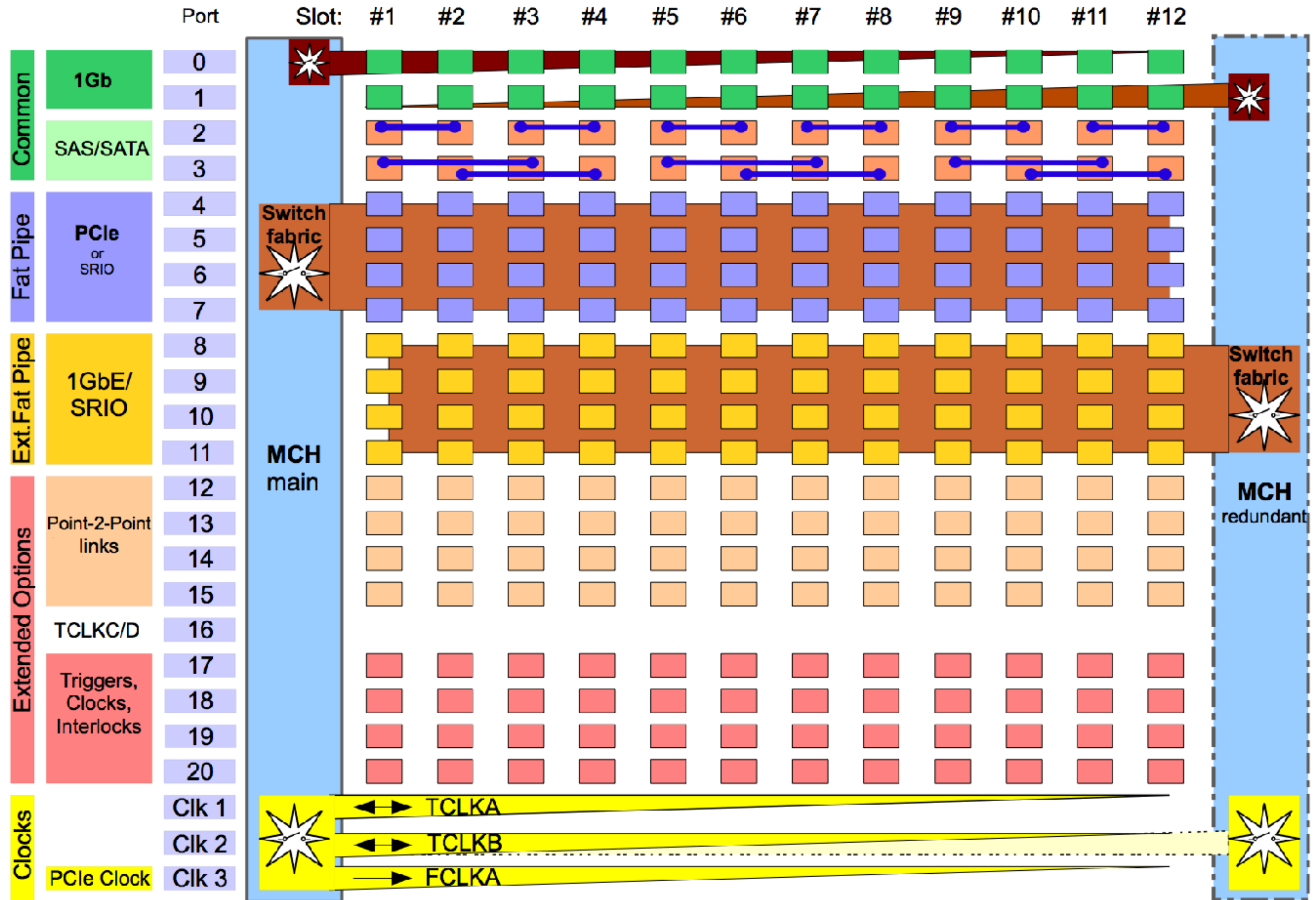
Rear Side



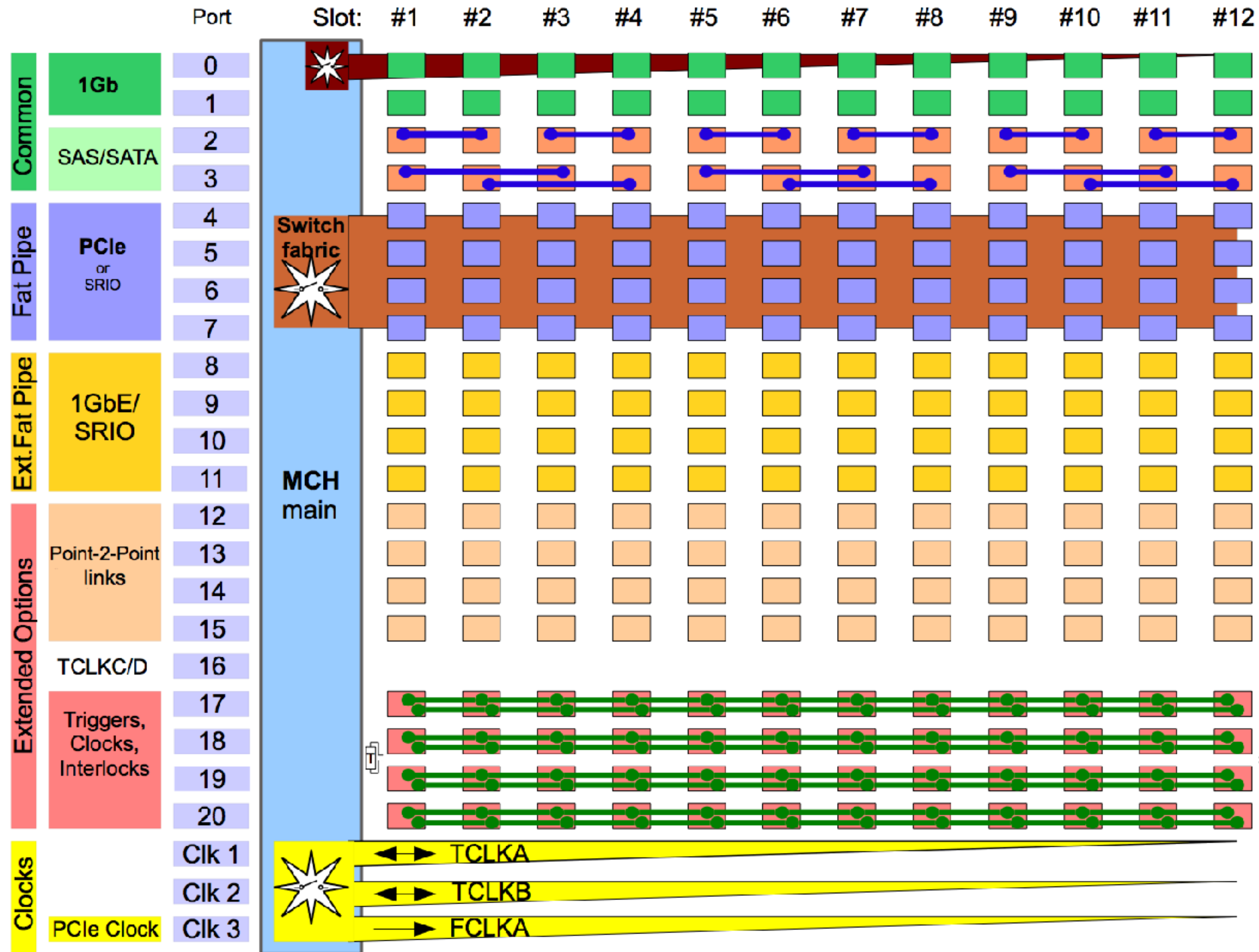
# Basic MTCA.0



# MTCA.0 with Redundancy

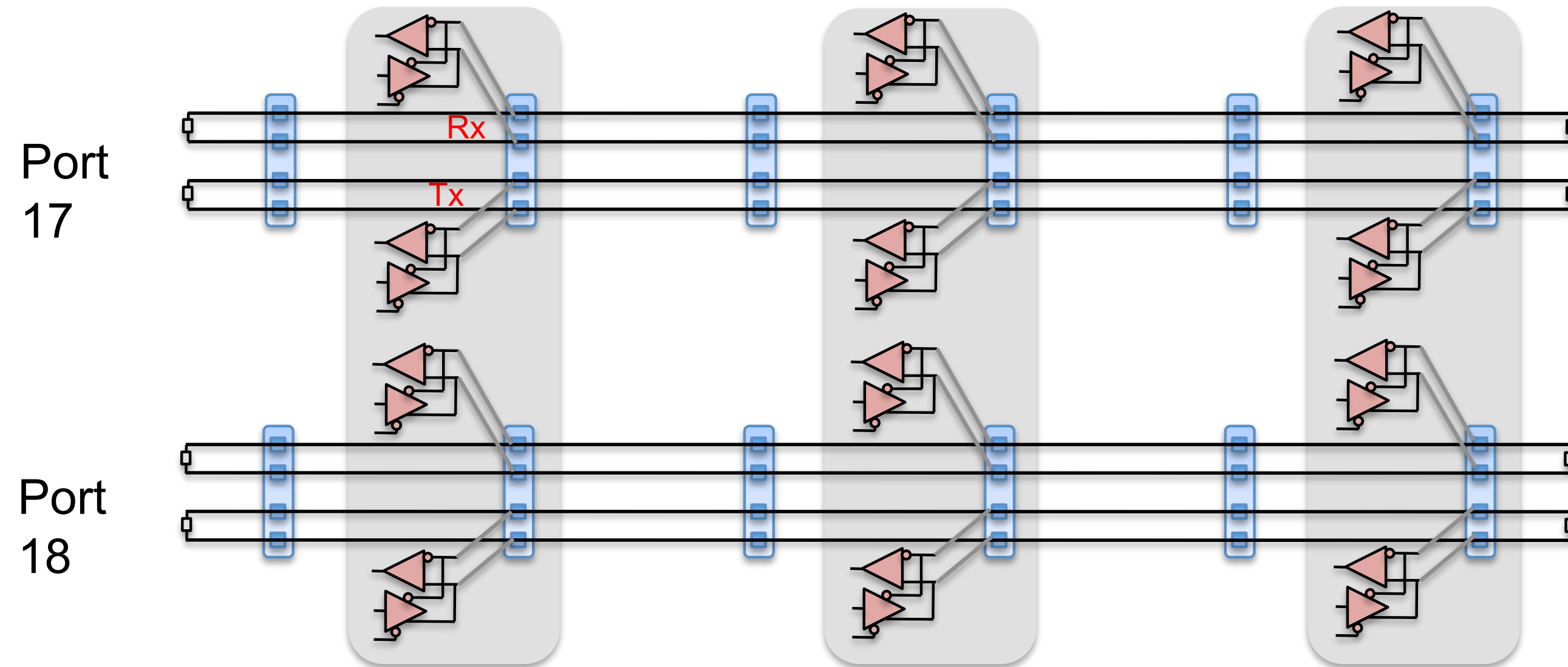


# MTCA.4: MLVDS Bus



8 MLVDS lines:  
 • FPGA-2-FPGA  
 • Triggers  
 • Clocks  
 • Interlocks  
 • ...

# Port 17 ... 20 Used as Wired-OR for Interlocks



**M-LVDS** Type-2 receivers (SN65MLVD082) implement a **failsafe** by using an offset threshold. In addition, the driver rise and fall times are between 1 and 2.0 ns to provide operation at **250 Mbps** while also accommodating stubs on the bus.

Outputs are **slew rate controlled** to reduce EMI and crosstalk effects associated with large current surges.

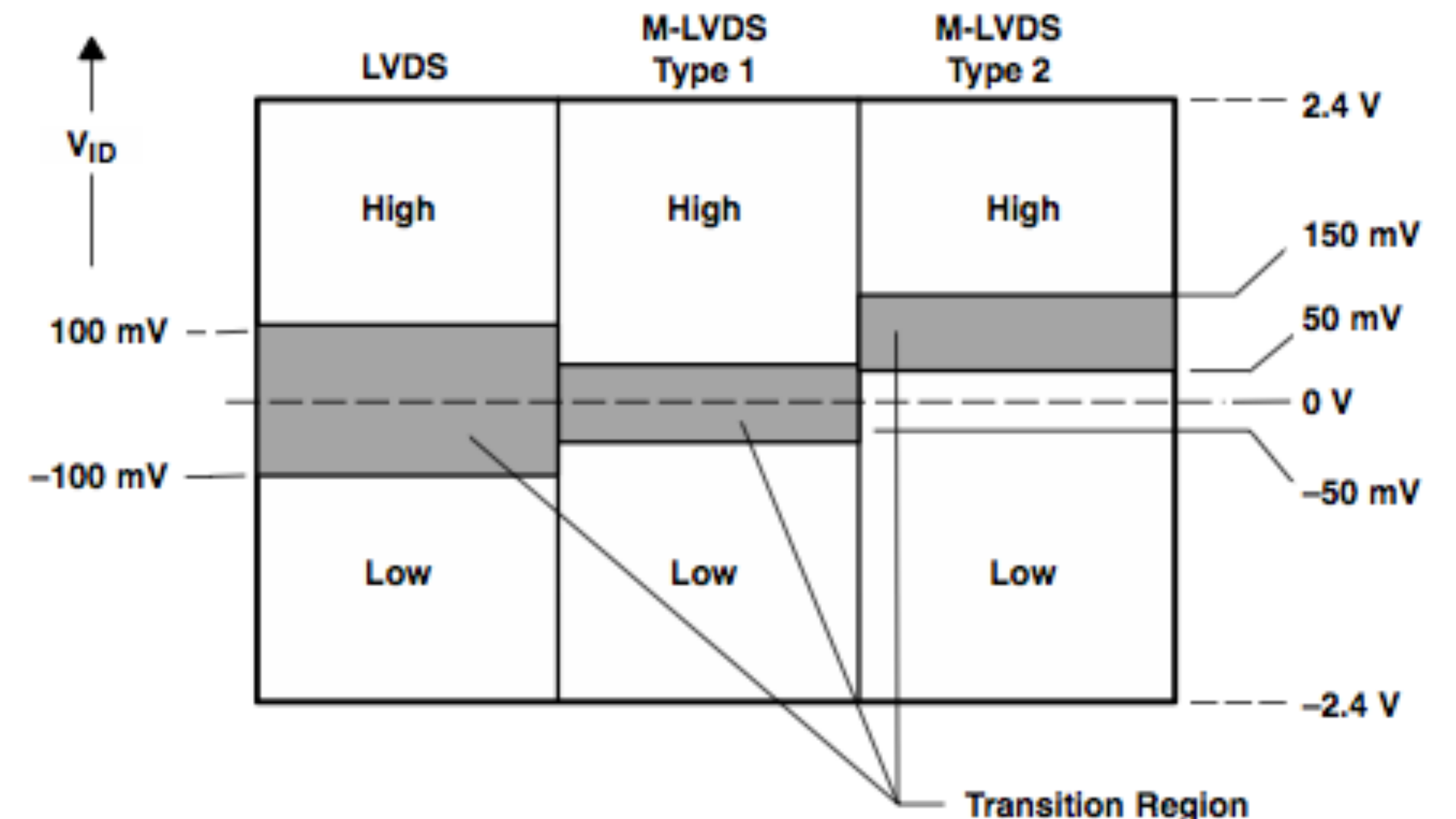
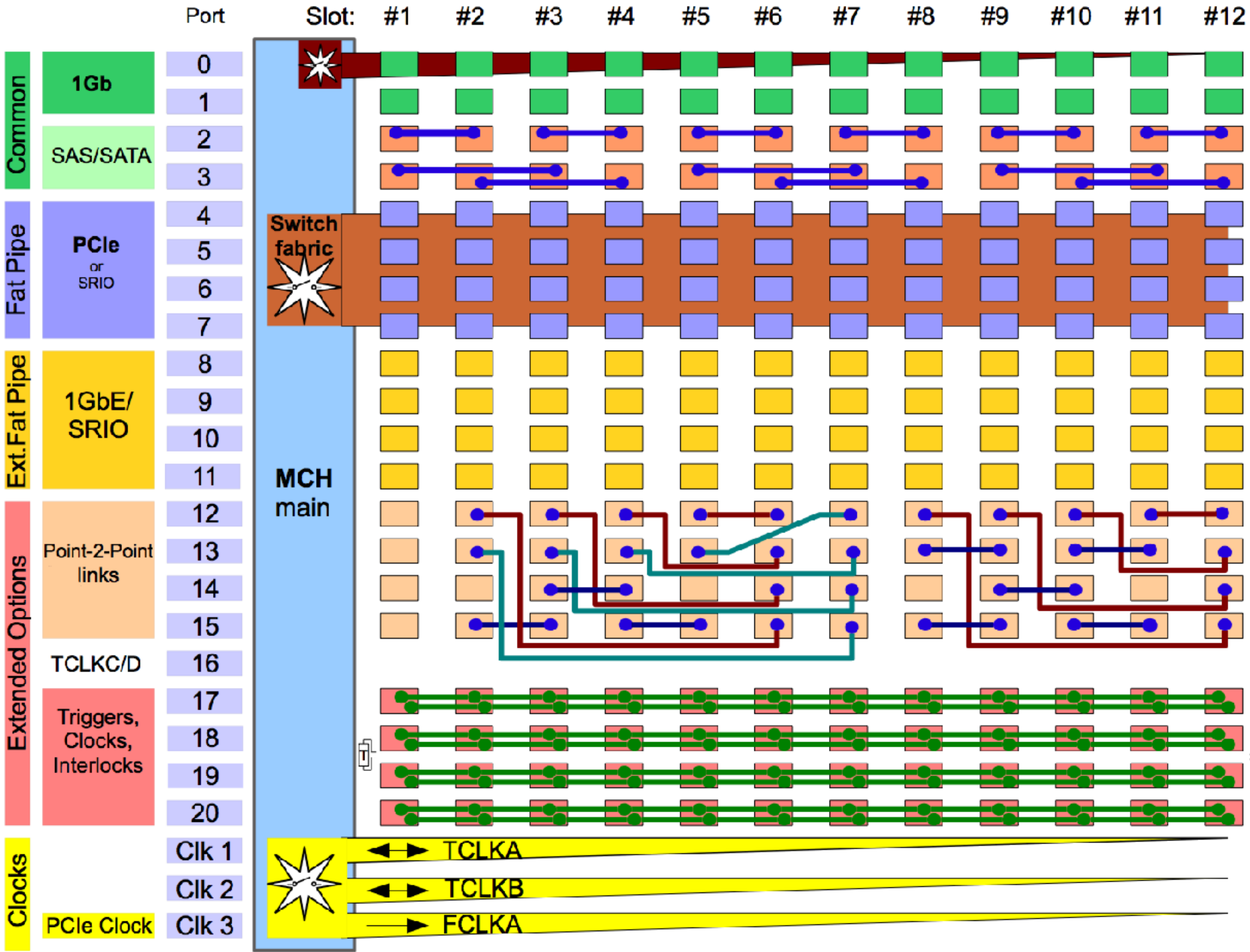


Figure 2-3. LVDS and M-LVDS Differential Input Voltage Thresholds

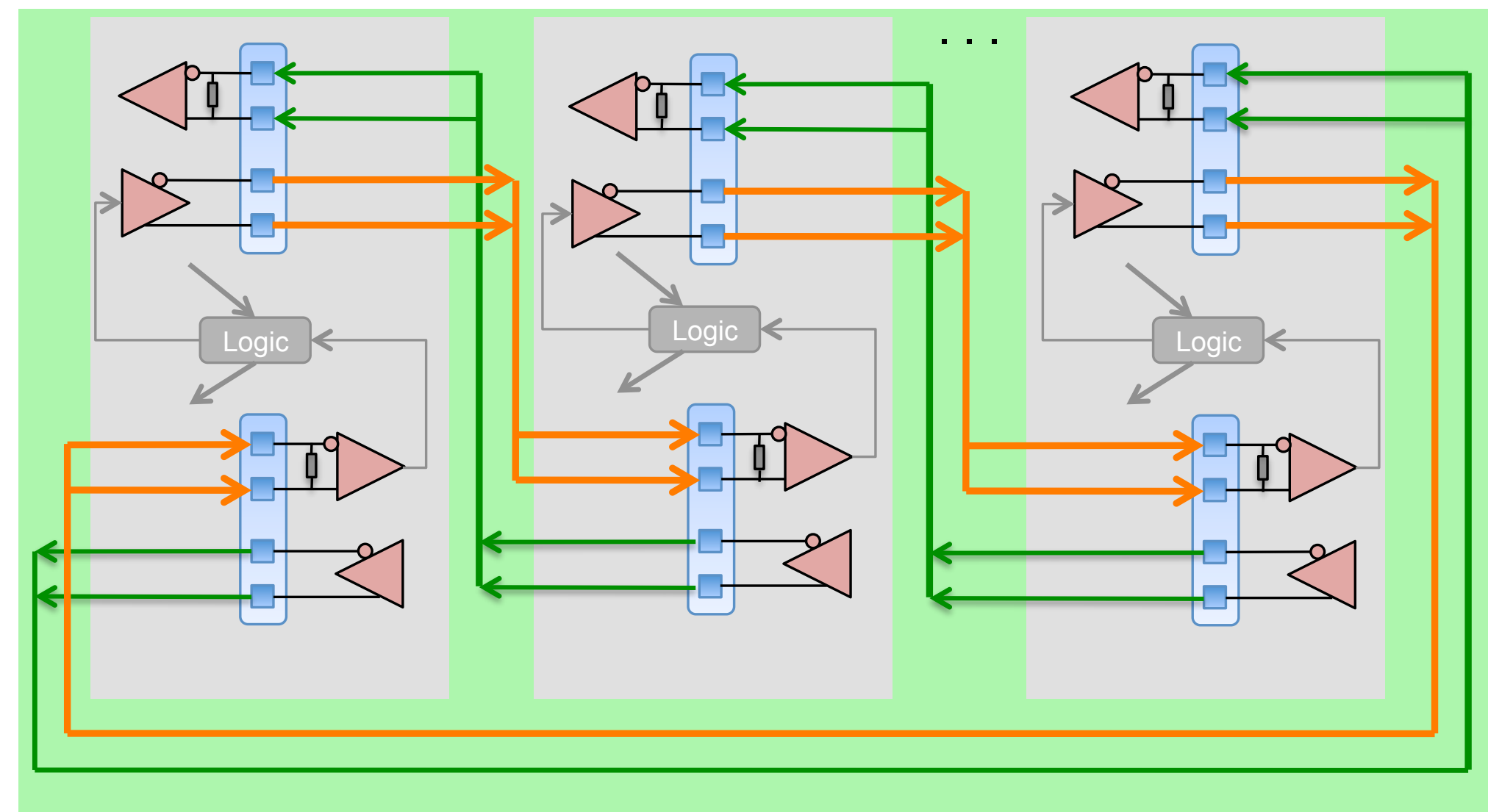
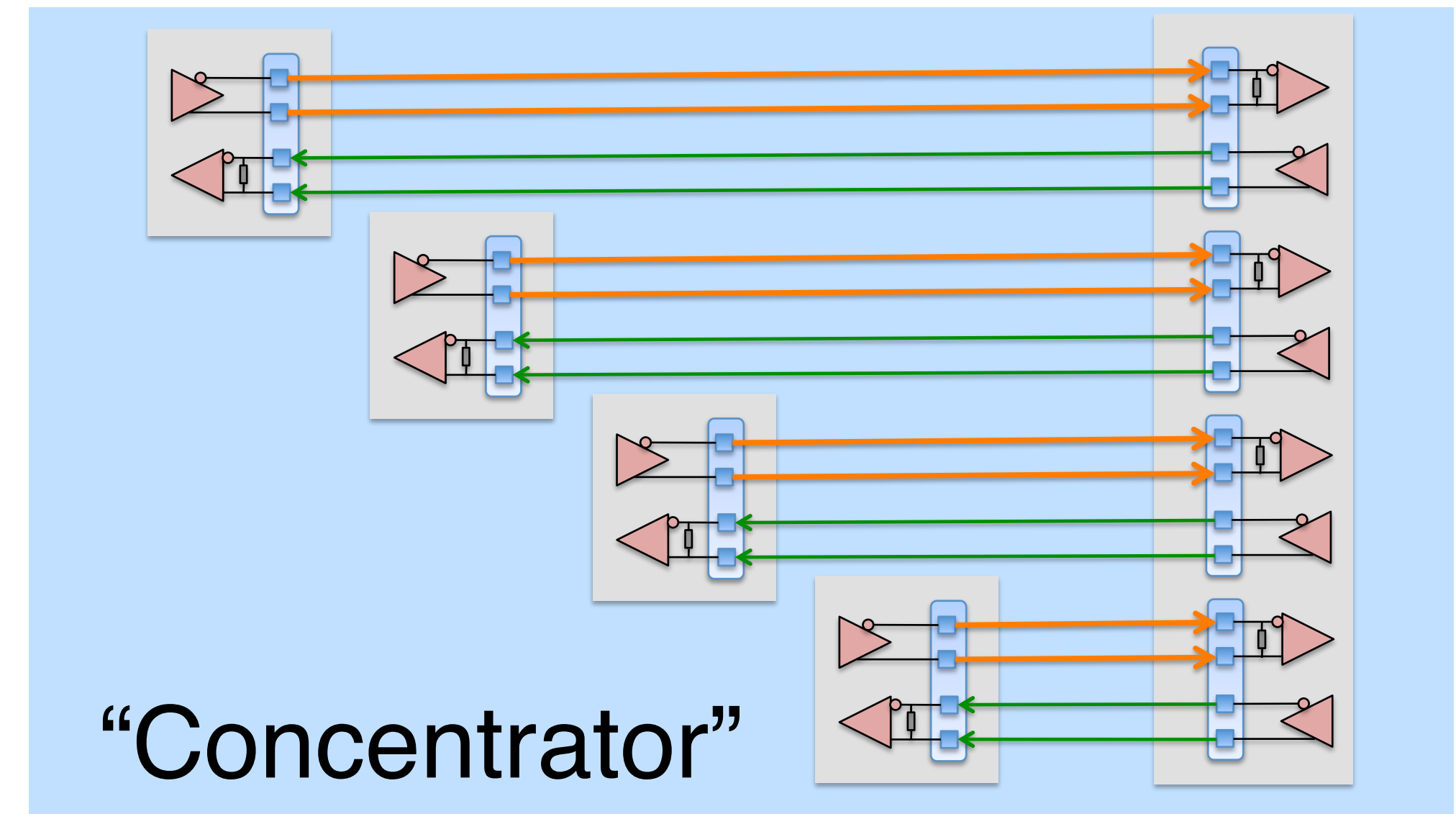
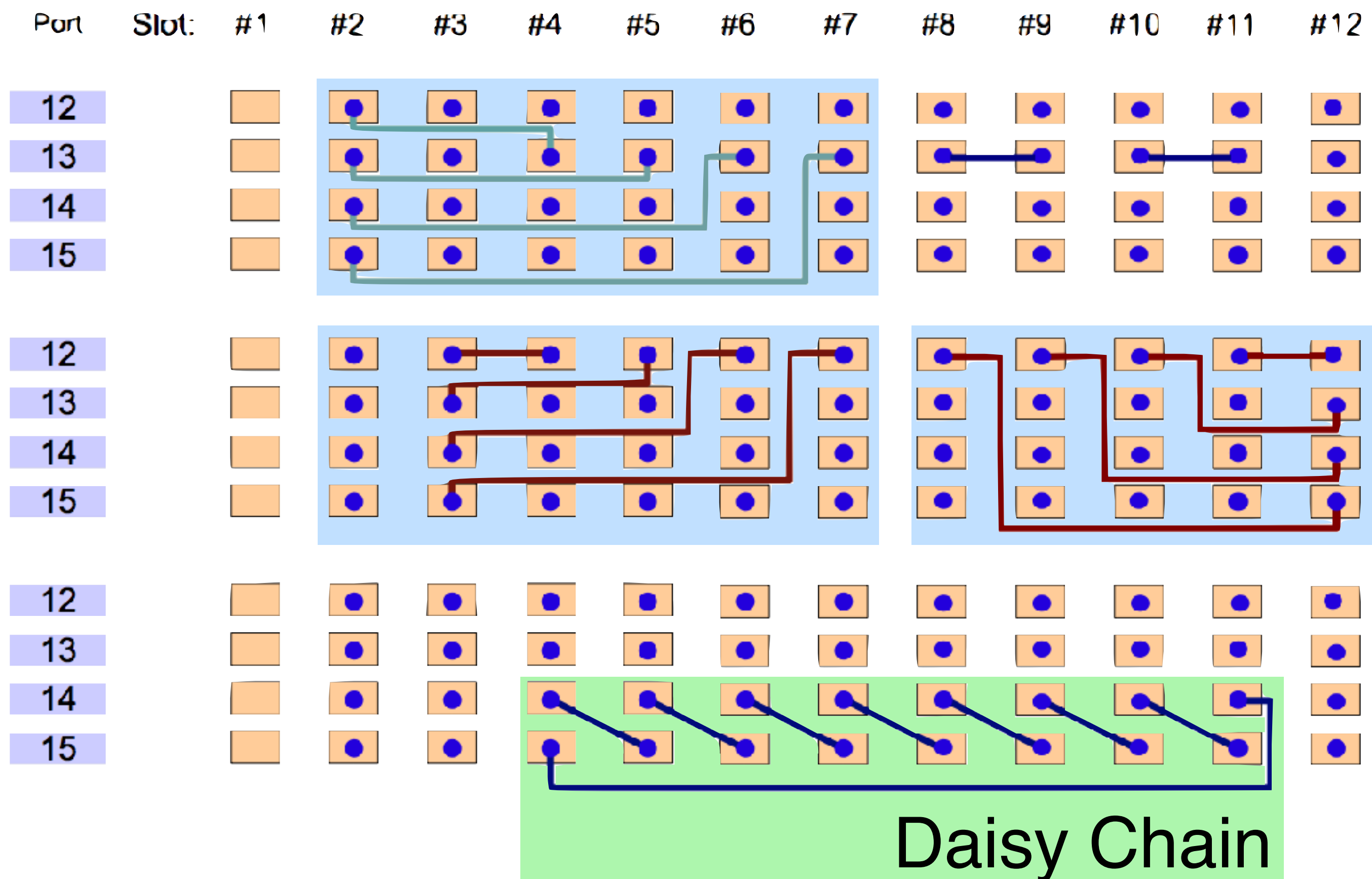
# MTC.A.4 with Point-2-Point Links



4 bi-directional LVDS lines:  
FPGA-2-FPGA communication

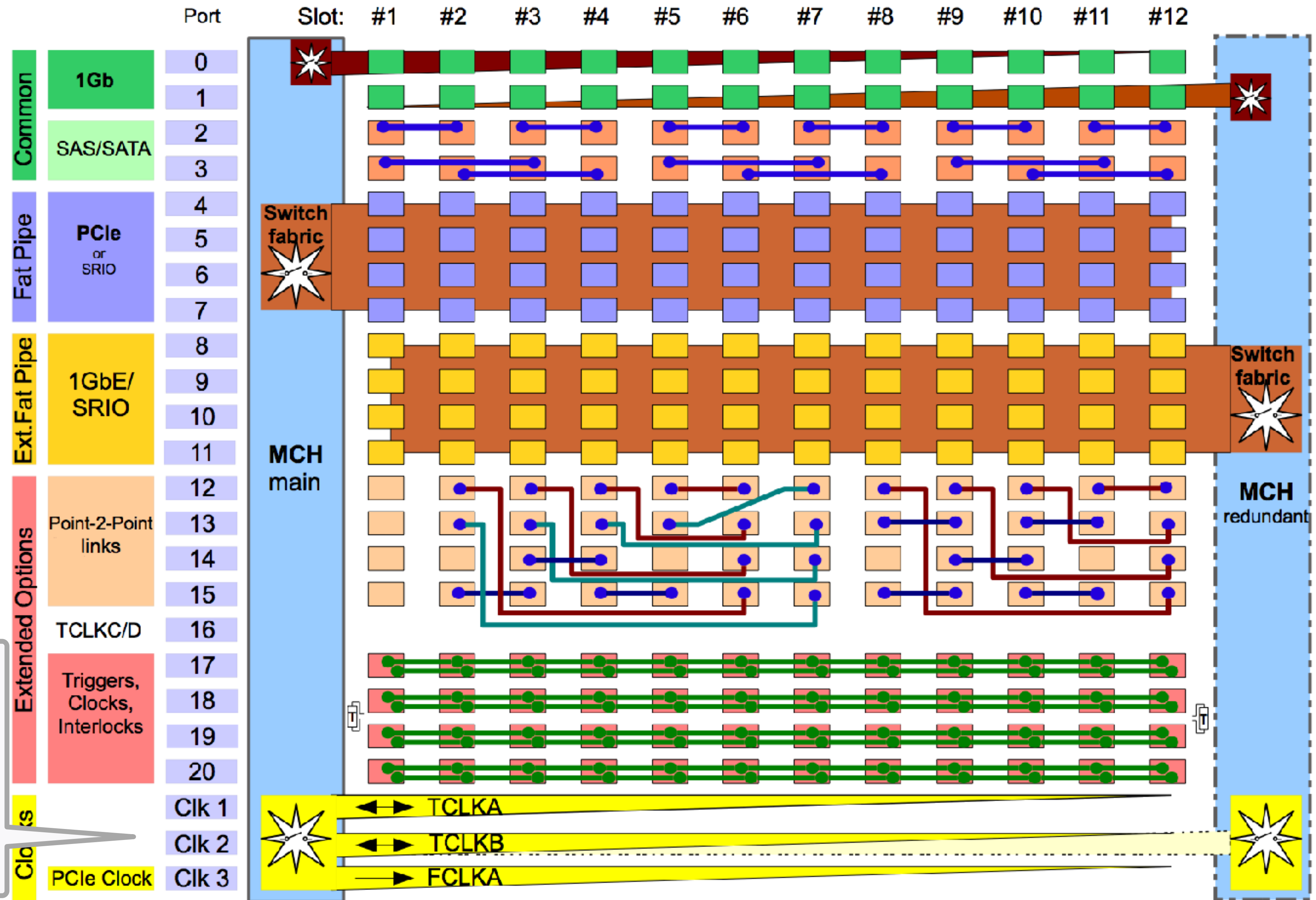


# Point-2-Point Topologies

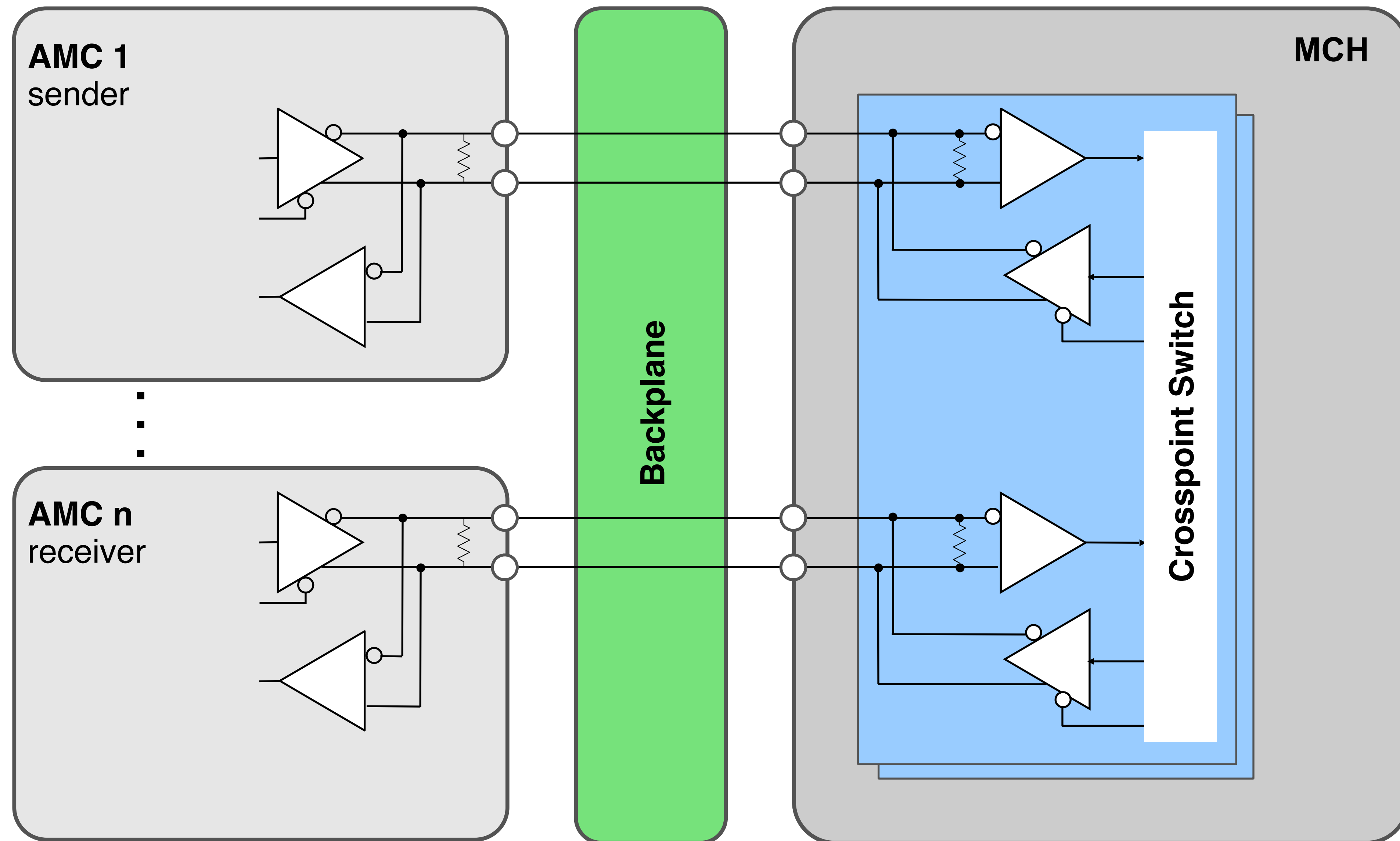


**Other topologies are possible by modifying the backplane**

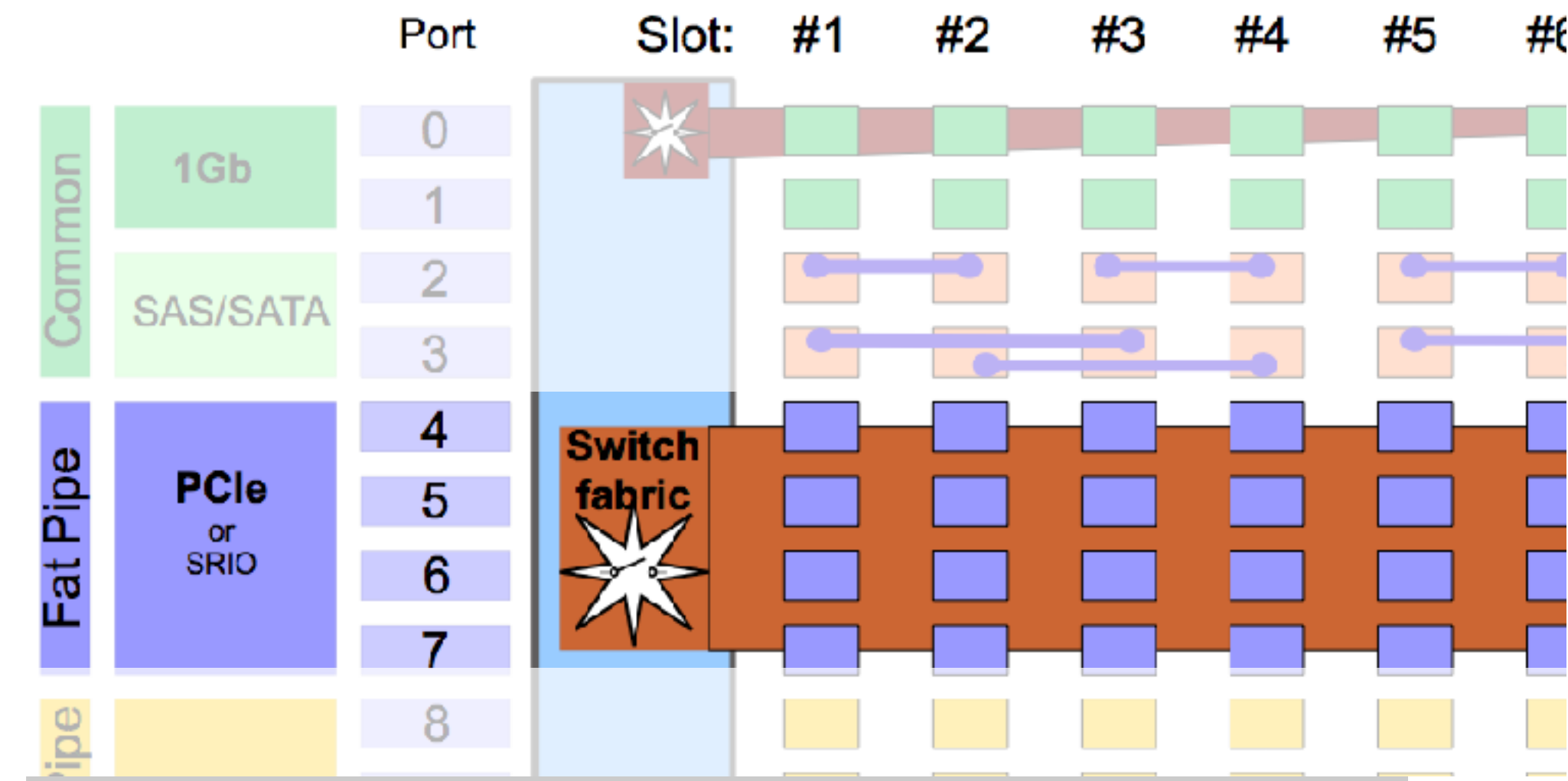
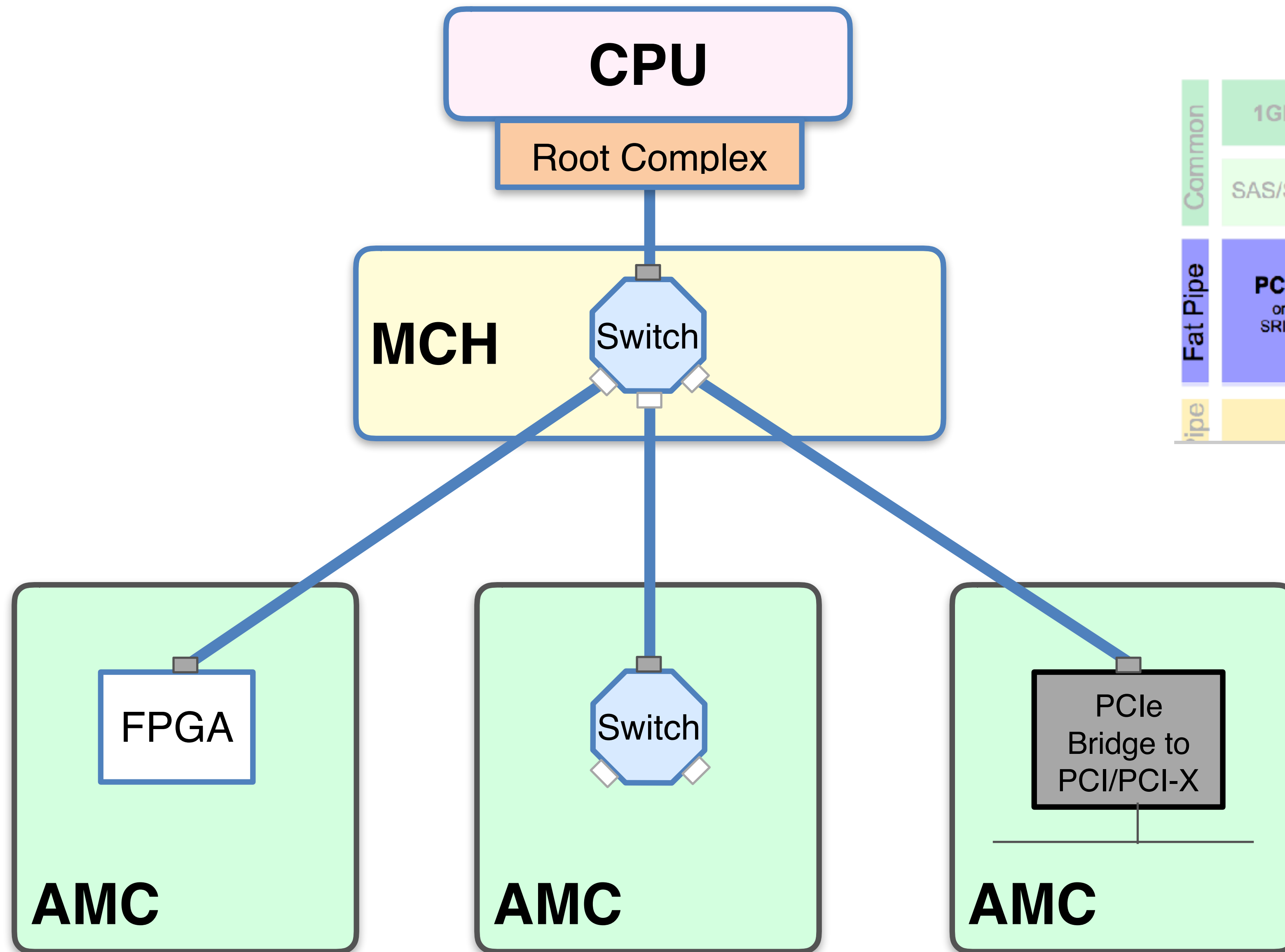
# MTCA.4 Clocks: MTCA.0 Compatible



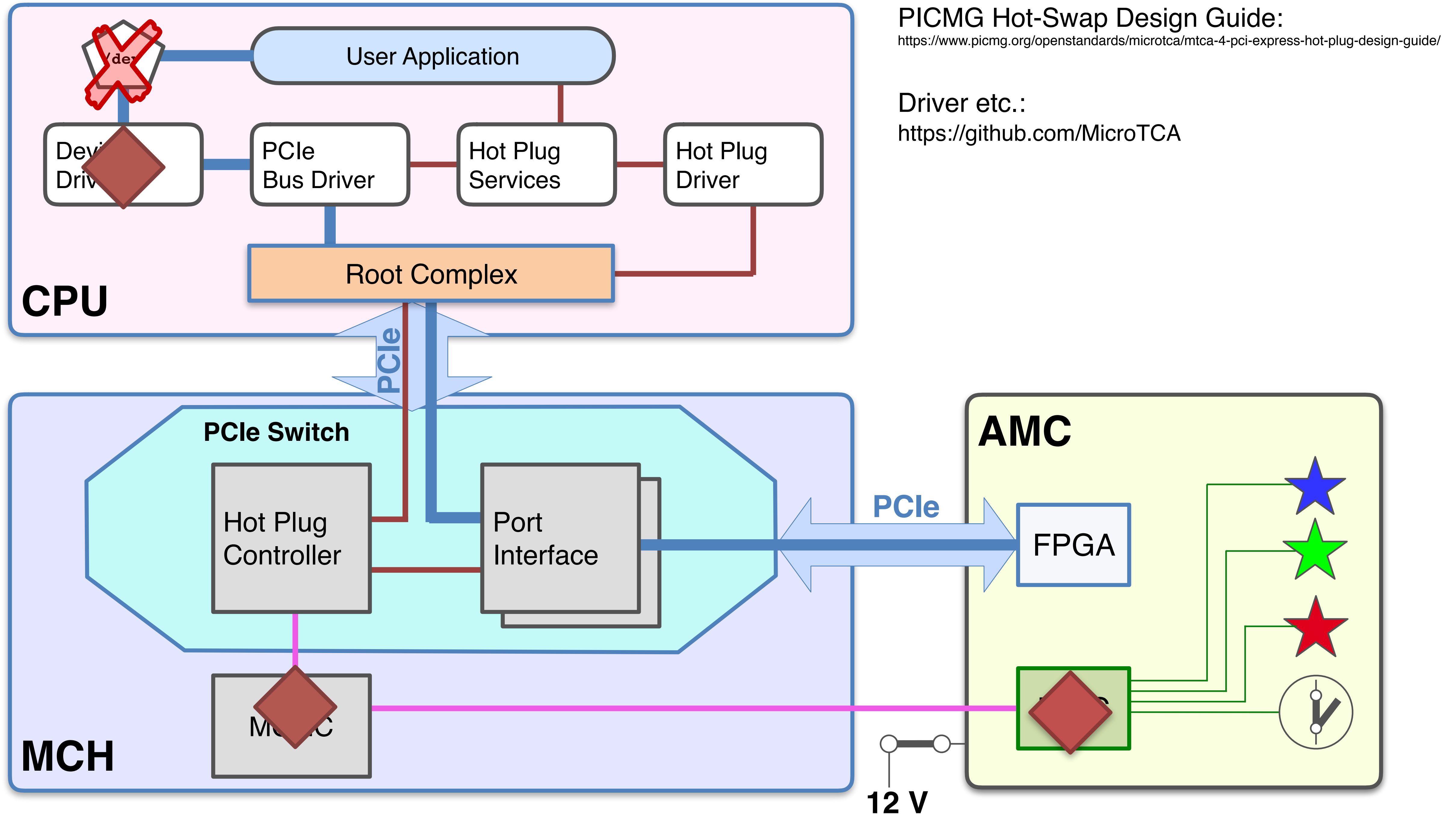
# Low Jitter Clock Distribution: Bi-directional LVDS



# PCIe Topology



# Architecture : PCIe with Hot-Swap



# MicroTCA.4 Communication Links

