MicroTCA.4 Communication Links

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Backplane MTCA.0 & MTCA.4
Ethernet, PCIe, SATA
Clocks, Triggers, interlocks
Point-to-point
MicroTCA Crate Backplane Communication

**Common modules**

- **MCH**
  - Clock Switch
  - Ethernet Switch
  - PCIe Switch

- **CPU**
  - From central timing
  - Clock
  - Ethernet Switch

- **Timing**
  - Clock

**Application modules**

- **Machine Protection System**
  - Trigger
  - Interlock

- **ADC**
  - Digi. IO Controller
  - …

- **Controller**

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Basic MTCA.0

![Diagram of MTCA configuration with labels for Port, Slot, 1Gb, SAS/SATA, Fat Pipe, Ext Fat Pipe, MCH main, TCLKC/D, Triggers, Clocks, and PCIe Clocks.]
MTCA.0 with Redundancy

[Diagram of MTCA.0 with Redundancy]
MTCA.4: MLVDS Bus

8 MLVDS lines:
- FPGA-2-FPGA
- Triggers
- Clocks
- Interlocks
- …
Port 17 ... 20 Used as Wired-OR for Interlocks

**M-LVDS** Type-2 receivers (SN65MLVD082) implement a **failsafe** by using an offset threshold. In addition, the driver rise and fall times are between 1 and 2.0 ns to provide operation at **250 Mbps** while also accommodating stubs on the bus. Outputs are **slew rate controlled** to reduce EMI and crosstalk effects associated with large current surges.
MTCA.4 with Point-2-Point Links

4 bi-directional LVDS lines:
FPGA-2-FPGA communication
Point-2-Point Topologies

Other topologies are possible by modifying the backplane
MTCA.4 Clocks: MTCA.0 Compatible

Point-2-Point Clocks:
- Low jitter
- Flexible configuration
Low Jitter Clock Distribution: Bi-directional LVDS
PCle Topology

CPU

Root Complex

MCH

Switch

FPGA

AMC

Switch

AMC

AMC

Phys

PCIe Bridge to PCI/PCI-X

1.0
8b/10b
2.5
GT/s
250
MB/s
1.0
GB/s

2.0
8b/10b
5.0
GT/s
500
MB/s
2.0
GB/s

3.0
128b/130b
8.0
GT/s
985
MB/s
3.9
GB/s

PCIe or SRIO

Fat Pipe

Common

1Gb
0
1
2
3
4
5
6
7
8

Switch fabric

Port
Slot:

#1
#2
#3
#4
#5
#6
Architecture: PCIe with Hot-Swap

PICMG Hot-Swap Design Guide:
https://www.picmg.org/openstandards/microtca/mtca-4-pci-express-hot-plug-design-guide/

Driver etc.:
https://github.com/MicroTCA

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MicroTCA.4 Communication Links

- PCIe
- Gb Ethernet
- Clock
- P-2-P
- MLVDS Bus
- CPU
- Timing
- Machine Protection System
- I/O