High Bandwidth Data Acquisition (HBDQ) MTCA.4.1 Platform

Let Your Application benefit

www.nateurope.com
About **N.A.T.**  
**Network and Automation Technology**

- Founded in 1990, privately owned
- Hard- and Software design and manufacturing
- Focus on *innovation in communication*
- International and worldwide operations
- Headquarters
  
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  53227 Bonn  
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- **MTCA.4 Instructors:**
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  - Dipl. Phys. Heiko Körte, heiko@nateurope.com
About **N.A.T.**

Core competences and capabilities

- **Functions:**
  - Interfaces for LAN, WAN/MAN, RAN, GPIO
  - Communication and processing boards hosting GPU, NPU, DSP, FPGA
  - System controllers and intelligent switches for SRIO, PCIE, 1/10/40GbE
  - Carriers, converters, adapters and extenders

- **Form factors and standards:**
  - VME, cPCI, PCI/PCIe, PMC, XMC, FMC, AMC, MTCA, custom

- **Technologies:**
  - FPGA: Altera, Xilinx, Lattice
  - DSP: Analog Devices, Texas Instruments, Octasic
  - CPUs: NXP, ARM, MicroBlaze, NIOS
  - Switches (Broadcom, IDT, PLX, Fulcrum, Vitesse)

- **Software/firmware:**
  - Board Support Packages and host drivers: Linux, OK-1; OSE, vxWorks, QNX on request
  - Protocol stacks: telecom (ISDN, SS7, mobile), IP related, custom
  - Applications and APIs

**NX on request**
Agenda

- Motivation
- Building Blocks: Chassis, MCH, Power, Timing
- HBDQ: High Bandwidth Data Acquisition Platform based on MTCA.4.1 standard
- JTAG debugging multiple FPGAs
- Summary
1U, 2 single, mid/full-size Slots or 1 double, mid/full-size Slot
Motivation for
High Bandwidth Data Acquisition Platform

- IO move from PCIe-Gen1 to -Gen2 to nowadays -**Gen3**
  - SIS8300-KU: new ADC/DAC using Ultrascale FPGAs, 4 lanes PCIe-Gen3
- AMC CPU become bottleneck
  - already offer 8 PCIe lanes, but can only use 4 lanes in standard MTCA.4 crates
- Technology Evolution
  - AMC-CPU do not follow **Intel-CPU technology quick enough** (Intel Gen1, Gen3, Gen6)
  - Upcoming request for using beside FPGAs oder **GP-GPU** (general purpose graphic processing units) -> AMC-GPU or NVIDIA-PCIe cards
  - Latest COMexpress modules require **more than 30 Watts**
- Latest requirements (FAIR, ESS, ...)
  - less slots but distributed IO, 10G Ethernet too long latency
  - Redundancy on crate level, not board level

- **Goal**
  - Take MTCA.4 systems to the next level of performance taking advantage of the upcoming MTCA.4.1 standard -> HBDQ Platform
About N.A.T.
Markets and Applications

- Automation
- Communication
- Defense & Aerospace
- Energy
- Industrial Control
- Infotainment
- Medical
- Test & Measurement
- Transportation
Agenda

• Motivation
• **Building Blocks: Chassis, MCH, Power, Timing**
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## NATIVE Overview

<table>
<thead>
<tr>
<th>Standard</th>
<th>Name</th>
<th>Size</th>
<th>AMC Slots</th>
<th>µRTM Slots</th>
<th>MCH Slots</th>
<th>Cooling Unit Slots</th>
<th>Power module Slots</th>
<th>JSM</th>
<th>Fat-Pipe Size</th>
<th>Comment</th>
<th>Dust Filter</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>NATIVE-mini</td>
<td>1U</td>
<td>2 sm or 2 sf or 1 df</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td></td>
<td>x8</td>
<td>eMCH, Cooling unit, power module</td>
<td>1</td>
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<tr>
<td>MTCA.0</td>
<td>NATIVE-C1</td>
<td>19&quot;, 1U</td>
<td>6 sm or 3 sf or 2 sm + 4dm</td>
<td>-</td>
<td>1 sf</td>
<td>2</td>
<td>1 sf</td>
<td>soon</td>
<td>x8</td>
<td>redundant x4</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>NATIVE-C2</td>
<td>19&quot;, 2U</td>
<td>12 sm or 6 sf or 4 sm + 4dm or ...</td>
<td>-</td>
<td>2 sf</td>
<td>2</td>
<td>2 sf</td>
<td>soon</td>
<td>redundant x4</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>NATIVE-C5</td>
<td>5U</td>
<td>6 dm + 1 df or 7 dm or single/double mix</td>
<td>-</td>
<td>1 df</td>
<td>1</td>
<td>1 df</td>
<td>no</td>
<td>x4</td>
<td>Cooling Unit, Power Module</td>
<td>1</td>
</tr>
<tr>
<td>MTCA.1</td>
<td>NATIVE-SX</td>
<td>3U</td>
<td>3 sm + 2 sf</td>
<td>-</td>
<td>1 sf</td>
<td>-</td>
<td>-</td>
<td></td>
<td>x4</td>
<td>redundant x4 direct replacement for IPC</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>NATIVE-IPC</td>
<td>19&quot;, 4U</td>
<td>12 sm (pluggable from Rear)</td>
<td>-</td>
<td>2 sf</td>
<td>1</td>
<td>2 sdf</td>
<td></td>
<td>x4</td>
<td></td>
<td>no</td>
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<tr>
<td>MTCA.4</td>
<td>NATIVE-R2</td>
<td>2U</td>
<td>5 dm + 1 df</td>
<td>4 dm + 1 dm(if no JSM)</td>
<td>1 df + RTM</td>
<td>1</td>
<td>1 df</td>
<td>yes</td>
<td>x8</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>NATIVE-R5</td>
<td>5U</td>
<td>6 dm + 1 df or 7 dm or single/double mix</td>
<td>6 dm + 1 df or 7 dm</td>
<td>1 df + RTM</td>
<td>1</td>
<td>1 df</td>
<td>no</td>
<td>x4</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>NATIVE-R9</td>
<td>19&quot;, 9U</td>
<td>12 dm or 6 df or single/double mix</td>
<td>12 dm or 6 df or combination</td>
<td>2 df + 2RTM</td>
<td>2</td>
<td>4 df or 2 ddf</td>
<td>yes</td>
<td>redundant x4</td>
<td></td>
<td>1</td>
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<tr>
<td>MTCA.2</td>
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<td></td>
<td></td>
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<td></td>
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<tr>
<td>MTCA.3</td>
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</tbody>
</table>
## Power Modules for MTCA.0 and MTCA.4

<table>
<thead>
<tr>
<th>INPUT</th>
<th>PAYLOAD</th>
</tr>
</thead>
<tbody>
<tr>
<td>NAT-PM-DC420 DC -48V</td>
<td>420W</td>
</tr>
<tr>
<td>NAT-PM-DC840 DC -48V</td>
<td>840W</td>
</tr>
<tr>
<td>NAT-PM-AC600 AC 110-265</td>
<td>600W</td>
</tr>
<tr>
<td><strong>NAT-PM-AC600D AC 110-265V</strong></td>
<td><strong>600W (double width)</strong></td>
</tr>
<tr>
<td>NAT-PM-AC1000 AC 110-265V</td>
<td>1000W (double width)</td>
</tr>
<tr>
<td>NAT-RPM-PSC AC 110-265V</td>
<td>600W (double width)</td>
</tr>
<tr>
<td>NAT-PM-DC600LV DC 24V</td>
<td>ad: 300W/600W</td>
</tr>
<tr>
<td>NAT-RPM-PSC AC 110-265V</td>
<td>+/-VV (variable Voltages)</td>
</tr>
</tbody>
</table>

![Image of power modules]
NAT-MCH-PHYS80

- Low Cost (1GbE)
- Telecom Clock and FCLK
- Serial Rapid I/O Gen 2 + FPGA
- Serial Rapid I/O Gen 2
- 10GbE (XAUI)
- PCI Express Gen 3
- Physics Clock + SSD
- Ruggedized
New MCH-RTM
NAT-MCH-RTM-BM-FPGA: Front Side

Multiple COMexpress-CPU-Modules

RTM Power connector
RTM Control&Data connector
Second Zone3 connector
New MCH-RTM
NAT-MCH-RTM-BM-FPGA: Block Diagram
NAMC-psTimer
Synchronisation simplified
Need of Timing/Triggering Hardware
Installation Example XFEL
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Put things into NATIVE-R2
6 AMCs, 5 µRTMs, PM, JSM, MCH, MCH-RTM

- 2U MTCA.4 chassis for AMCs and µRTMs and JTAG Switch Module

AMCs with up to 3 sub-modules or big heatsinks

1x Fieldbus e.g. EtherCAT
4x USB3.0 Dev. e.g. Cameras
2x Displays (4k)
MTCA.4.1 Defines
µRTM Backplane, Zone-2 Connector, Zone-3 Classes RPM, eRTMs, MCH-RTM, x16 Fat-Pipe
NATIVE-R2
Data stream from DSP/FPGA or FPGA/GPU to Displays

μRTM

CPU

ADC

FPGA

FPGA

DSP+FPGA

FPGA

FPGA

DIO

CPU

MCH

FPGA

GPU

DSP+FPGA

Switch

DSP+FPGA

x4 optical PCIe or x8 or x16

MultiCore CPUs with GPU NVIDIA Graphic Card with 100s of Cores

DISPLAY
3 + 4

local CPU

external CPU+GPU

DISPLAY
1 + 2 or more

Input

PCIe Gen3

PCIe Gen3

PCIe Gen3

PCIe Gen3
NATIVE-R2
Trigger and Clocks combined with High Bandwidth

1x Ref-Clock-In
1x or 2x Trigger-In
3x to 12x Clock-Out
3x to 12x Trigger-Out
Special IO

MultiCore CPUs with GPU
NVIDIA Graphic Card with 100s of Cores
NATIVE-R2
Low Latency Cascading of Systems
NATIVE-R2
Clustering, Uplink, Cascading of systems

Optical PCIe Uplink
16 PCIex Lanes

MCH-RTM:
Local Root Complex
16 PCIex lanes

PCI Express Switch
128 Gb/s

AMC PCIe lanes
x1
x4
2 x4
1 x8
PCIe Gen1, 2 or 3

AMC6

µRTM1
AMC1

µRTM2
AMC2

µRTM3
AMC3

µRTM4
AMC4

µRTM5
AMC5

2.5 – 32 Gb/s
or 64 Gb/s
JTAG Switch Module by N.A.T.
NAT-JSM: compact, versatile, flexible
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