

High Bandwidth Data Acquisition (HBDQ) MTCA.4.1 Platform



Let Your **Application** benefit

www.nateurope.com

About N.A.T.

Network and Automation Technology



- Founded in 1990, privately owned
- Hard- and Software design and manufacturing
- Focus on **innovation in communication**
- international and worldwide operations
- Headquarters

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- MTCA.4 Instructors:
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 - Dipl. Phys. Heiko Körte, heiko@nateurope.com



About N.A.T.

Core competences and capabilities



Innovation
Communication

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The brain of your MTCA.4 system

Higher bandwidth for Physics: the new NAT-MQH-PHY580

Key features:

- 10Gbps SerDes uplink at front panel
- 10Gbps link to local CPU host console
- special low latency and low jitter QM module
- fully open accessible quad core Intel QM Core 0
- 16GB RAM for UEFI bootplane
- complete product line

Let Your **Application** benefit

The brain of your MTCA system [read more ...](#)

Accelerate Media Processing
[read more ...](#)

The brain of your MTCA system
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The QorIQ Family
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Board Level Products	System Solutions	Upcoming Events	Latest News
		<ul style="list-style-type: none">▶ MTCA Workshop at DESY Dec 5th-8th, 2016, Hamburg▶ 10th NGMN 2016 Oct 12-13, Frankfurt, Germany▶ 20th IEEE RTC 2016 June 4th-10th, Padova, Italy	<ul style="list-style-type: none">▶ AMC module NAMC-SDR New Radio Head for Software Defined Radio▶ Bandwidth Upgrade for CPRI Links N.A.T. and RHI demonstrate EQ-Compression▶ New product NAT-3SM Open JTAG switch module in AMC form factor▶ AMC module NAMC-ODSP-M New Media Acceleration Engine based on 6x OCT2324M DSPs

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NX on request



Agenda

- Motivation
- Building Blocks: Chassis, MCH, Power, Timing
- HBDQ: High Bandwidth Data Acquisition Platform based on MTCA.4.1 standard
- JTAG debugging multiple FPGAs
- Summary

1U, 2 single, mid/full-size Slots or 1 double, mid/full-size Slot



Motivation for High Bandwidth Data Acquisition Platform



- IO move from PCIe-Gen1 to -Gen2 to nowadays -**Gen3**
 - SIS8300-KU: new ADC/DAC using Ultrascale FPGAs, 4 lanes PCIe-Gen3
- AMC CPU become bottleneck
 - already offer 8 PCIe lanes, but can only **use 4 lanes** in standard MTCA.4 crates
- Technology Evolution
 - AMC-CPU do not follow **Intel-CPU technology quick enough** (Intel Gen1, Gen3, Gen6)
 - Upcoming request for using beside FPGAs oder **GP-GPU** (general purpose graphic processing units) -> AMC-GPU or NVIDIA-PCIe cards
 - Latest COMexpress modules require **more than 30 Watts**
- Latest requirements (FAIR, ESS, ...)
 - less slots but distributed IO, 10G Ethernet too long latency
 - Redundancy on crate level, not board level
- **Goal**
 - Take MTCA.4 systems to the next level of performance taking advantage of the upcoming MTCA.4.1 standard -> HBDQ Platform



About N.A.T. Markets and Applications



- Automation
- Communication
- Defense & Aerospace
- Energy
- Industrial Control
- Infotainment
- Medical
- Test & Measurement
- Transportation

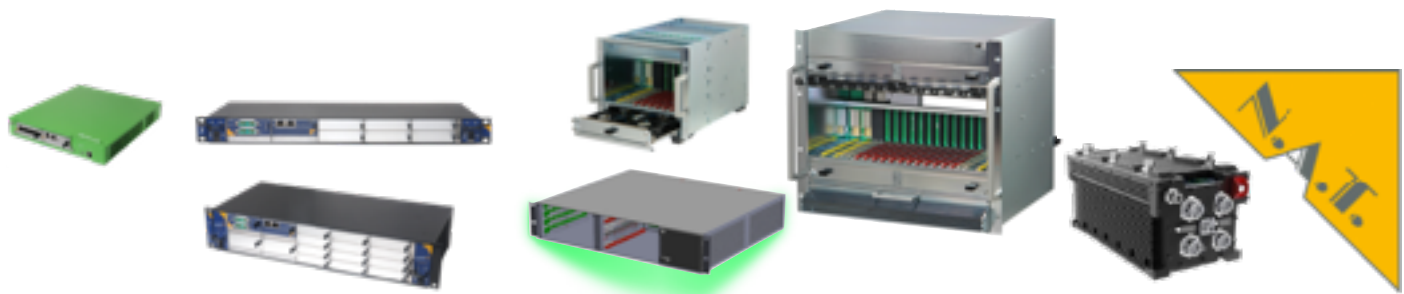




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NATIVE Overview



Standard	Name	Size	AMC Slots	µRTM Slots	MCH Slots	Cooling Unit Slots	Power module Slots	JSM	Fat-Pipe Size Comment	Dust filter
	NATIVE-mini	1U	2 sm or 2 sf or 1 df	-	-	-	-	-	x8 eMCH, Cooling unit, power module	1
MTCA.0	NATIVE-C1	19", 1U	6 sm or 3 sf or 2sm+4dm	-	1 sf	2	1 sf	soon	x8	1
	NATIVE-C2	19", 2U	12 sm or 6 sf or 4sm+4dm or ...	-	2 sf	2	2 sf	soon	redundant x4	1
	NATIVE-C5	5U	6 dm +1 df or 7 dm or single/double mix	-	1 df	1	1 df	no	x4	1
MTCA.1	NATIVE-SX	3U	3 sm + 2 sf	-	1 sf	-	-	-	x4 Cooling Unit, Power Module	no
	NATIVE-IPC	19", 4U	12 sm (pluggable from Rear)	-	2 sf	1	2 sdf	-	redundant x4 direct replacement for IPC	1
MTCA.4	NATIVE-R2	2U	5 dm + 1 df	4 dm + 1 dm(if no JSM)	1 df + RTM	1	1 df	yes	x8	1
	NATIVE-R5	5U	6 dm +1 df or 7 dm or single/double mix	6 dm + 1 df or 7 dm	1 df + RTM	1	1 df	no	x4	1
	NATIVE-R9	19", 9U	12 dm or 6 df or single/double mix	12 dm or 6 df or combination	2 df + 2RTM	2	4 df or 2 ddf	yes	redundant x4	1
MTCA.2 MTCA.3	on request									

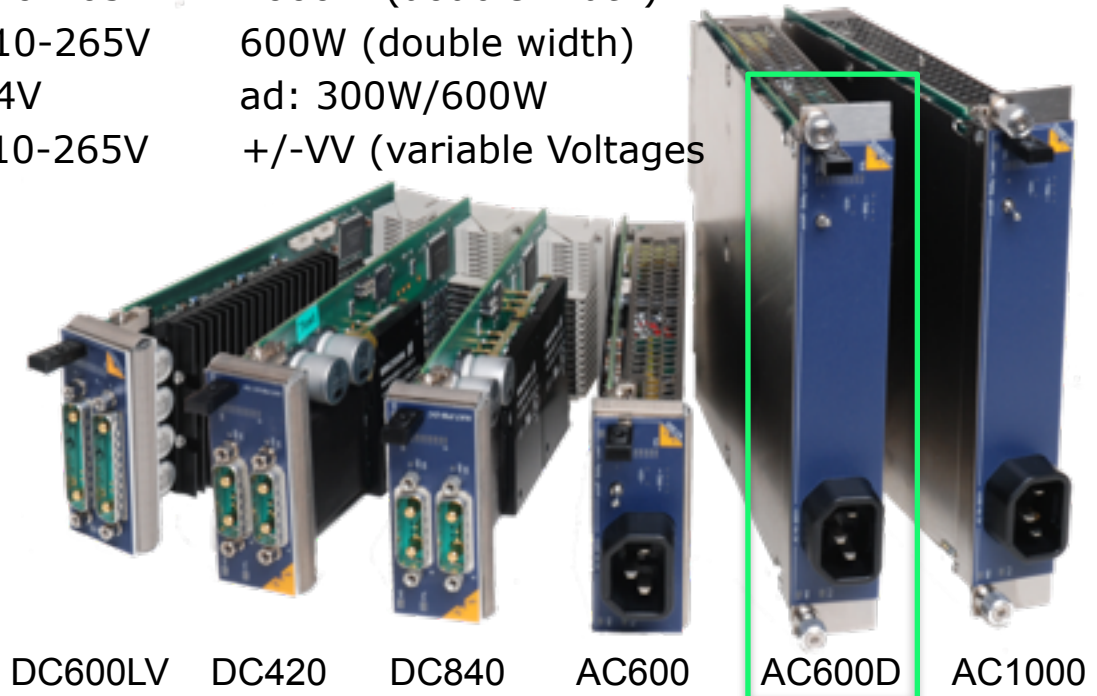


sm single width, mid-size
sf single width, full-size
dm double width, mid-size
df double width, full-size
ddf double width, double-full-size

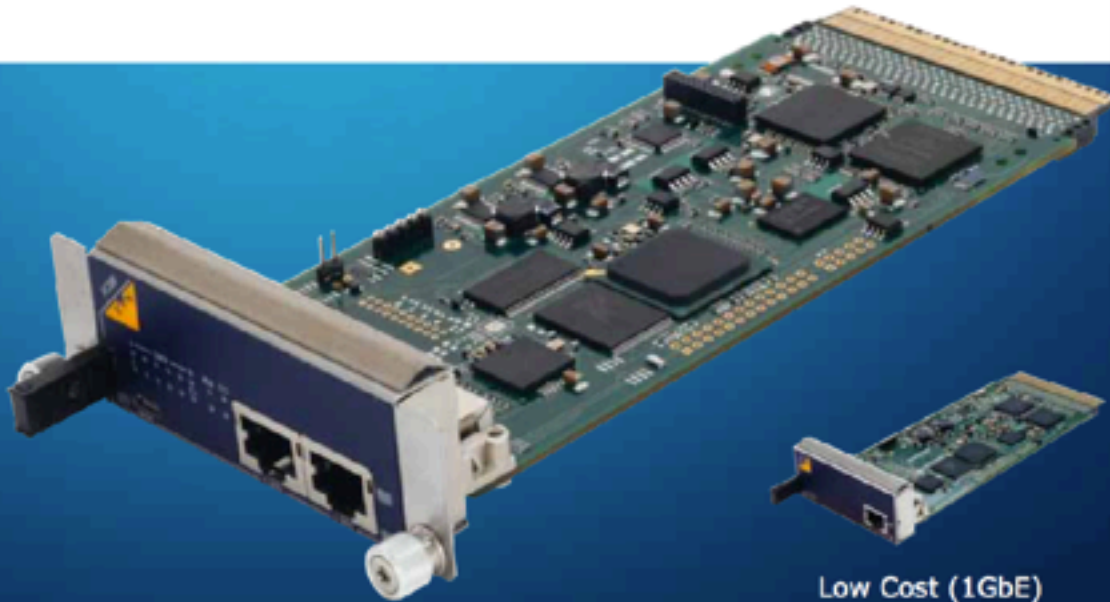
Power Modules for MTCA.0 and MTCA.4



	INPUT	PAYLOAD
• NAT-PM-DC420	DC -48V	420W
• NAT-PM-DC840	DC -48V	840W
• NAT-PM-AC600	AC 110-265	600W
• NAT-PM-AC600D	AC 110-265V	600W (double width)
• NAT-PM-AC1000	AC 110-265V	1000W (double width)
• NAT-RPM-PSC	AC 110-265V	600W (double width)
• NAT-PM-DC600LV	DC 24V	ad: 300W/600W
• NAT-RPM-PSC	AC 110-265V	+/-VV (variable Voltages)



NAT-MCH-PHYS80



Low Cost (1GbE)



Telecom Clock and FCLK



Serial Rapid I/O Gen 2
+ FPGA



Serial Rapid I/O Gen 2



10GbE (XAUI)



PCI Express Gen 3



Physics Clock +
SSD



Ruggedized

New MCH-RTM

NAT-MCH-RTM-BM-FPGA: Front Side

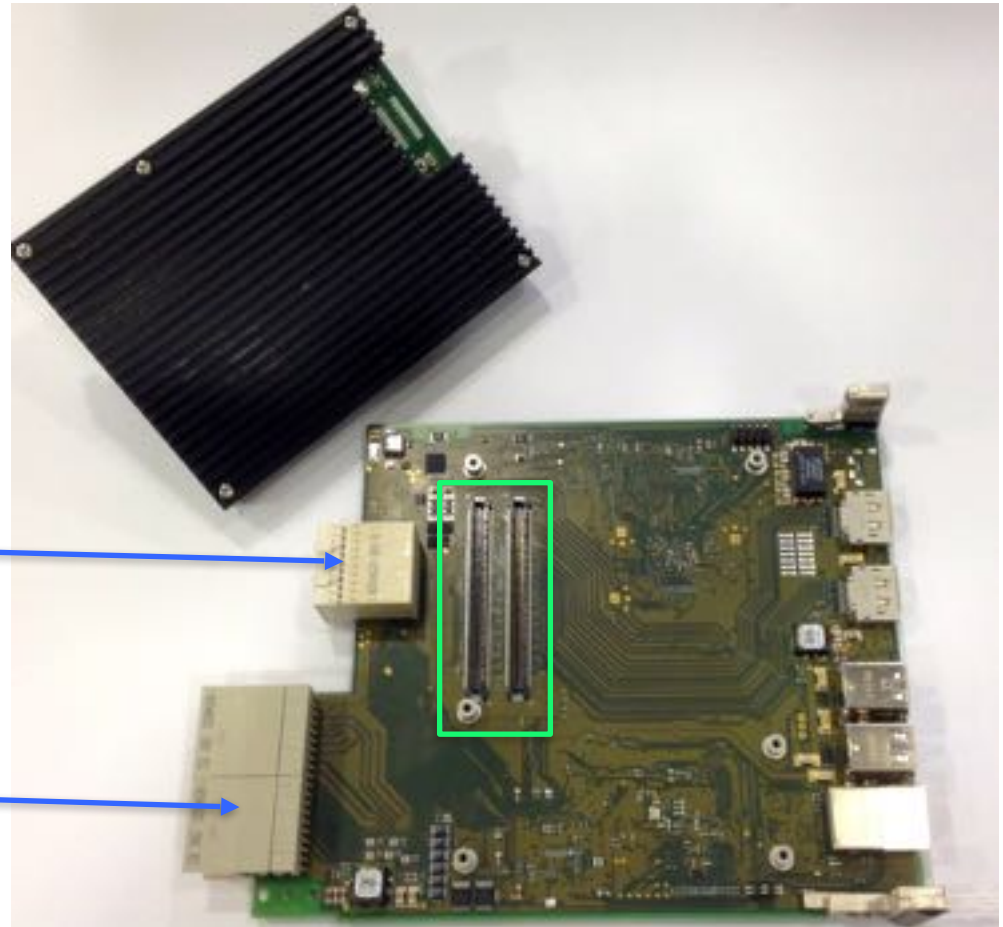


Multiple
COMexpress-CPU-Modules

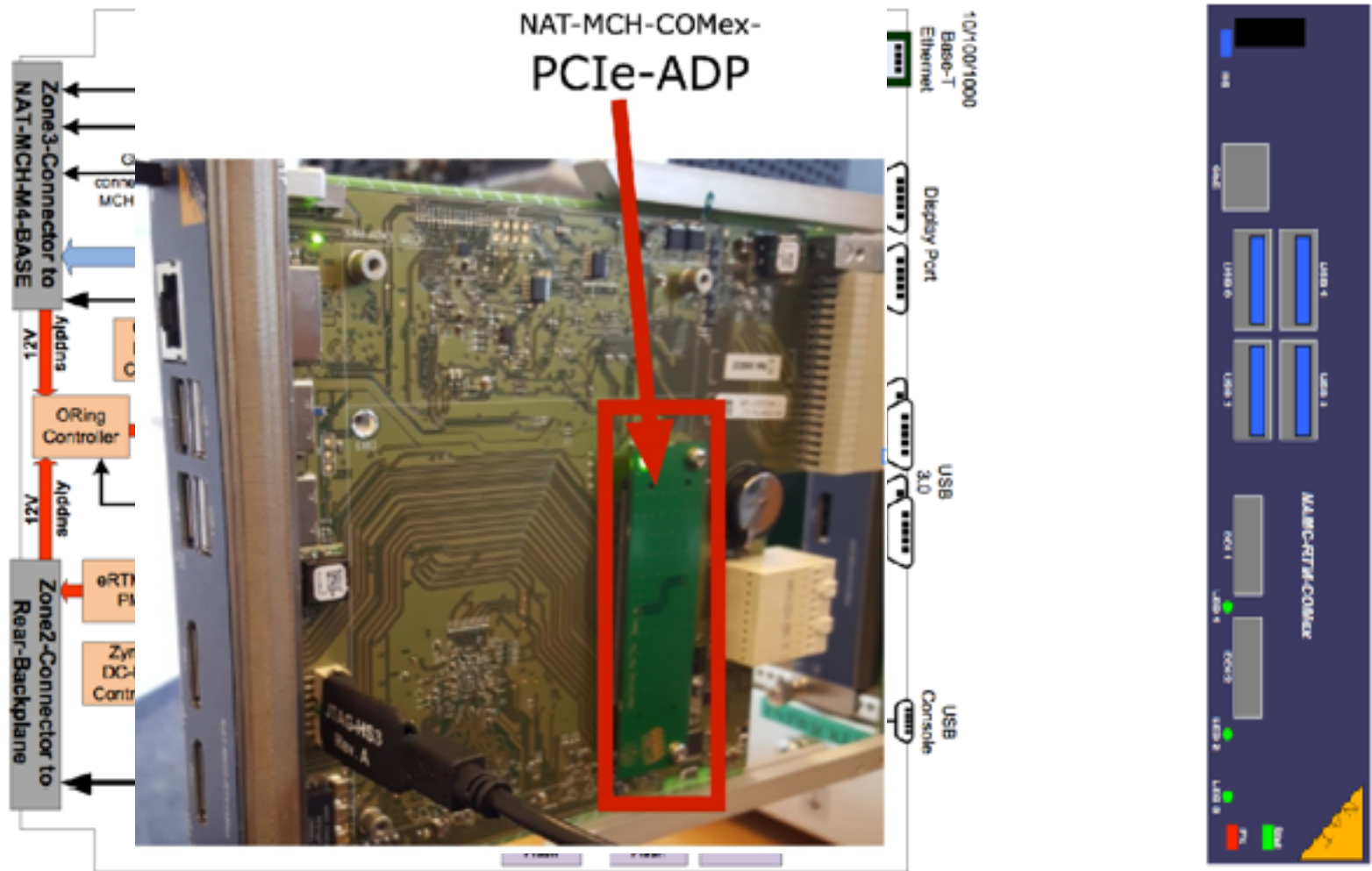
RTM Power connector

RTM Control&Data connector

Second Zone3 connector

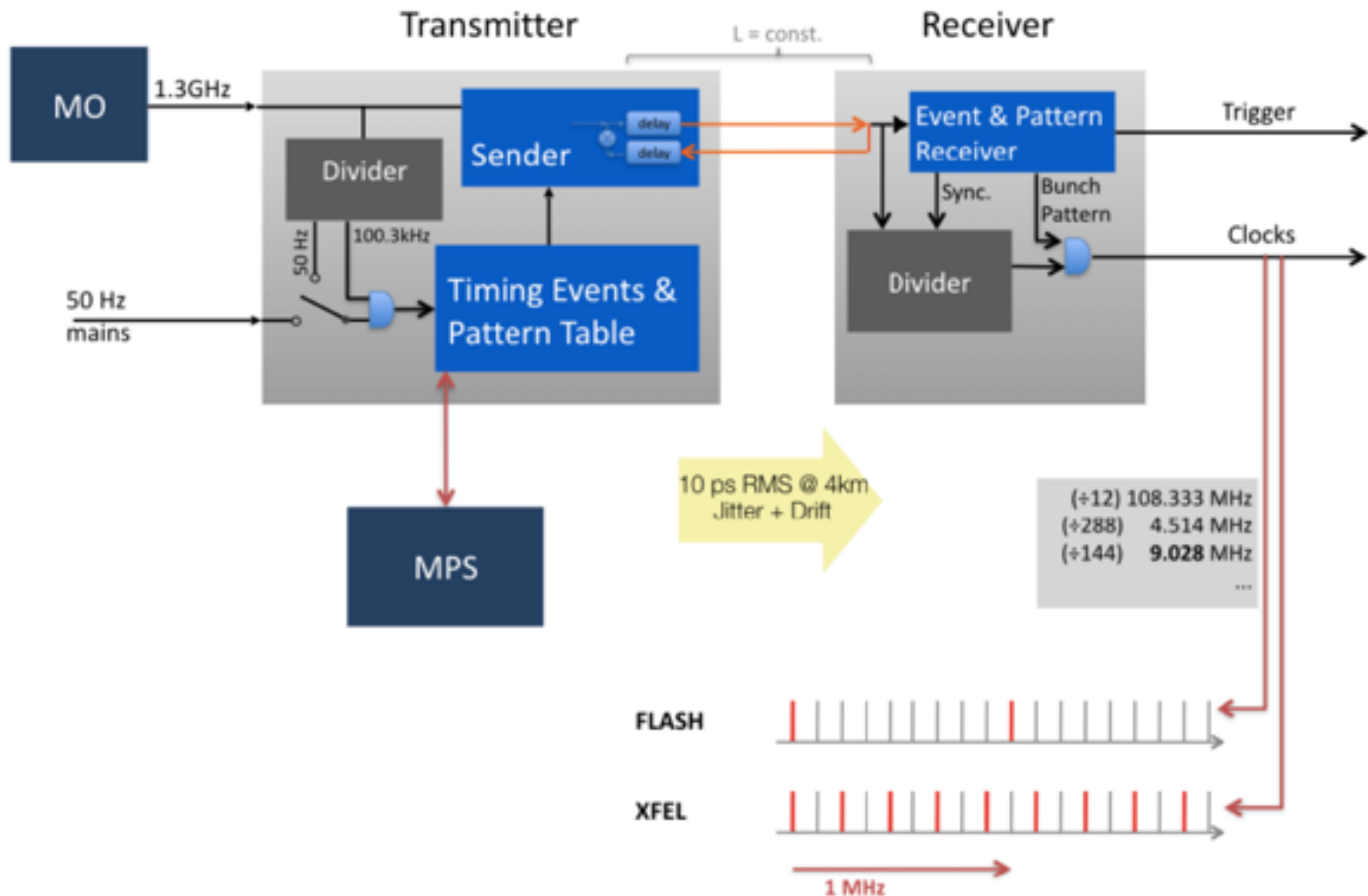


NAT-MCH-RTM-BM-FPGA: Block Diagram



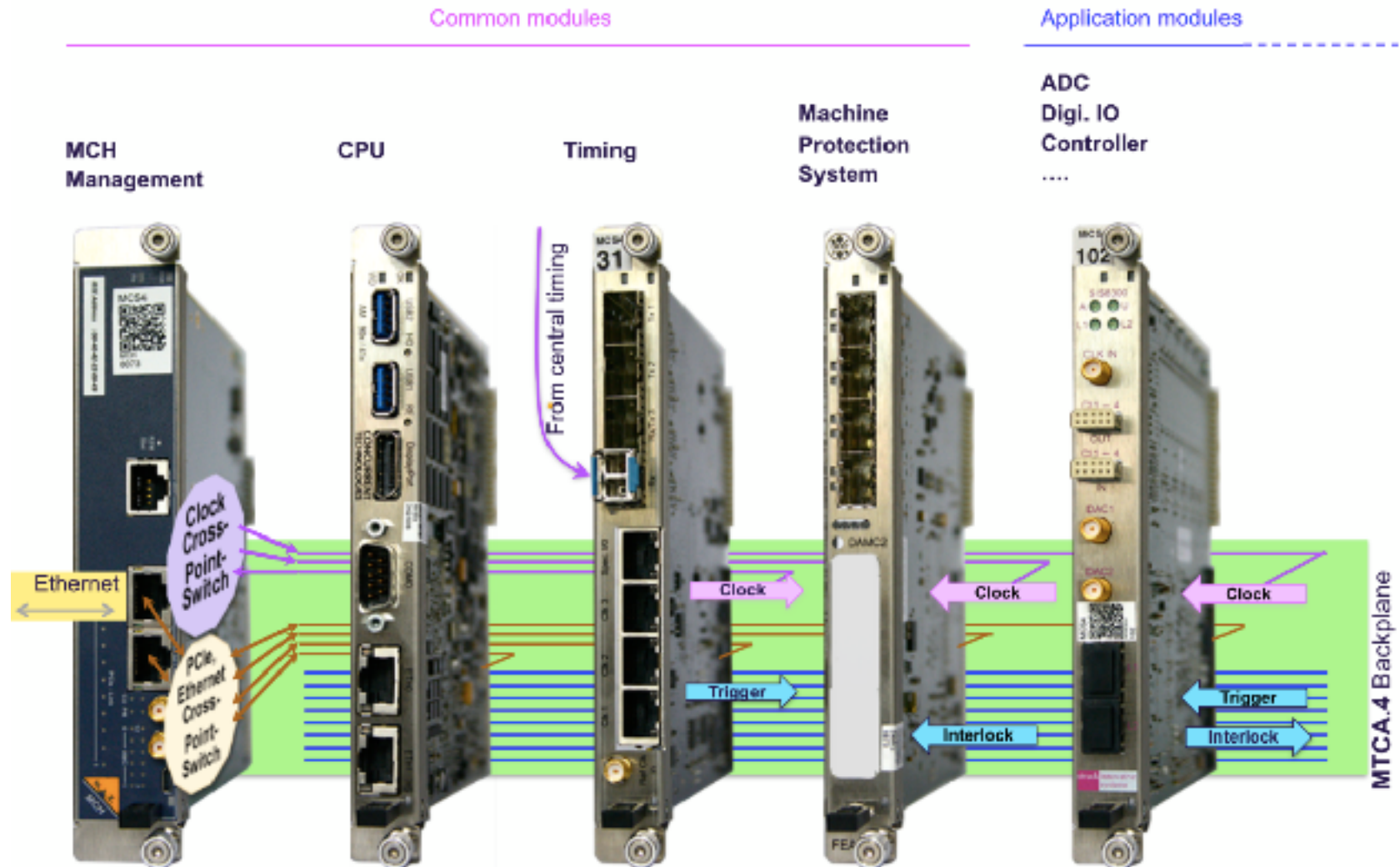
NAMC-psTimer

Synchronisation simplified



Need of Timing/Triggering Hardware

Installation Example XFEL





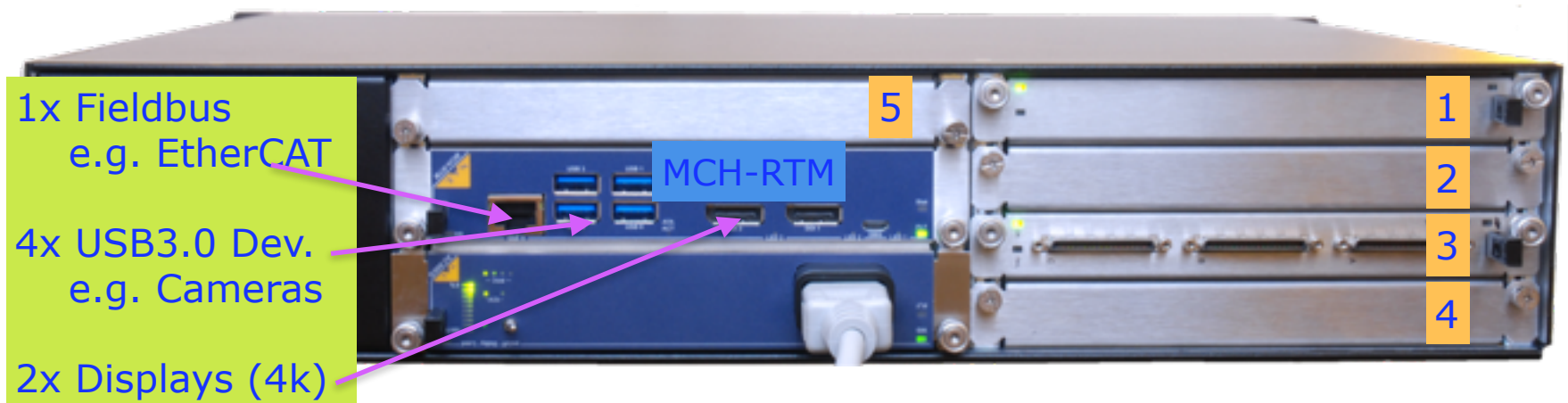
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Put things into NATIVE-R2

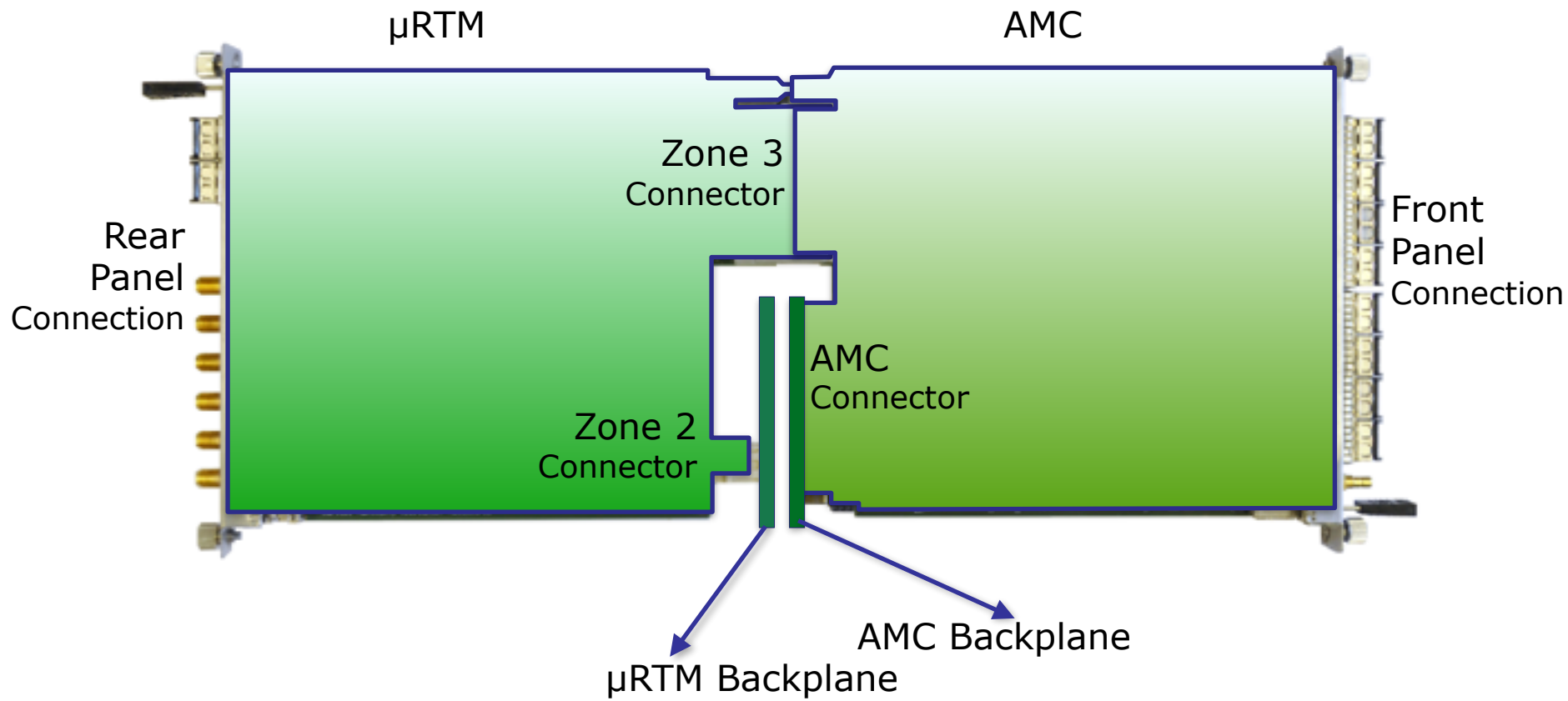
6 AMCs, 5 μ RTMs, PM, JSM, MCH, MCH-RTM

- 2U MTCA.4 chassis for AMCs and μ RTMs and JTAG Switch Module



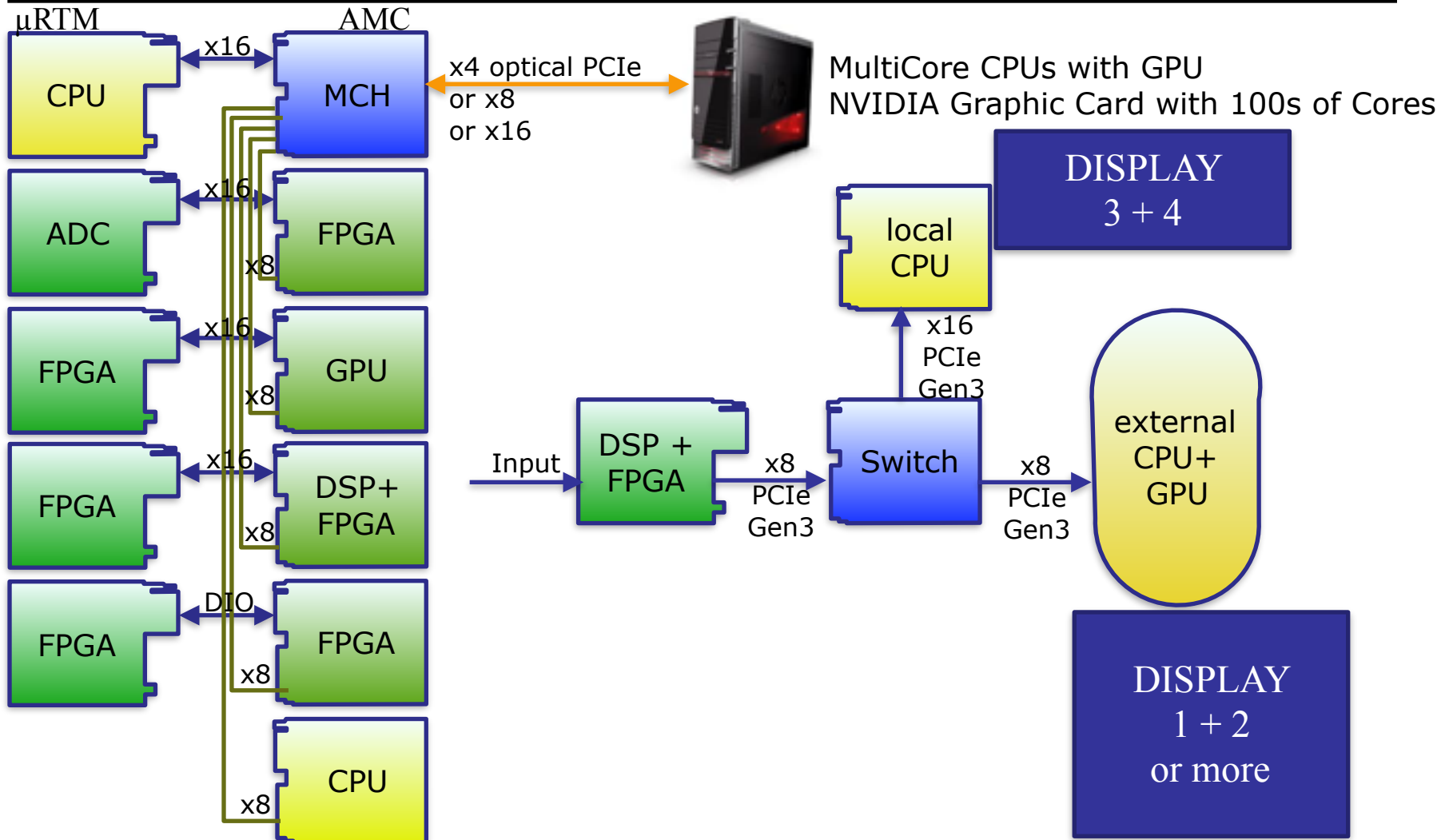
MTCA.4.1 Defines

μRTM Backplane, Zone-2 Connector, Zone-3 Classes
RPM, eRTMs, MCH-RTM, x16 Fat-Pipe



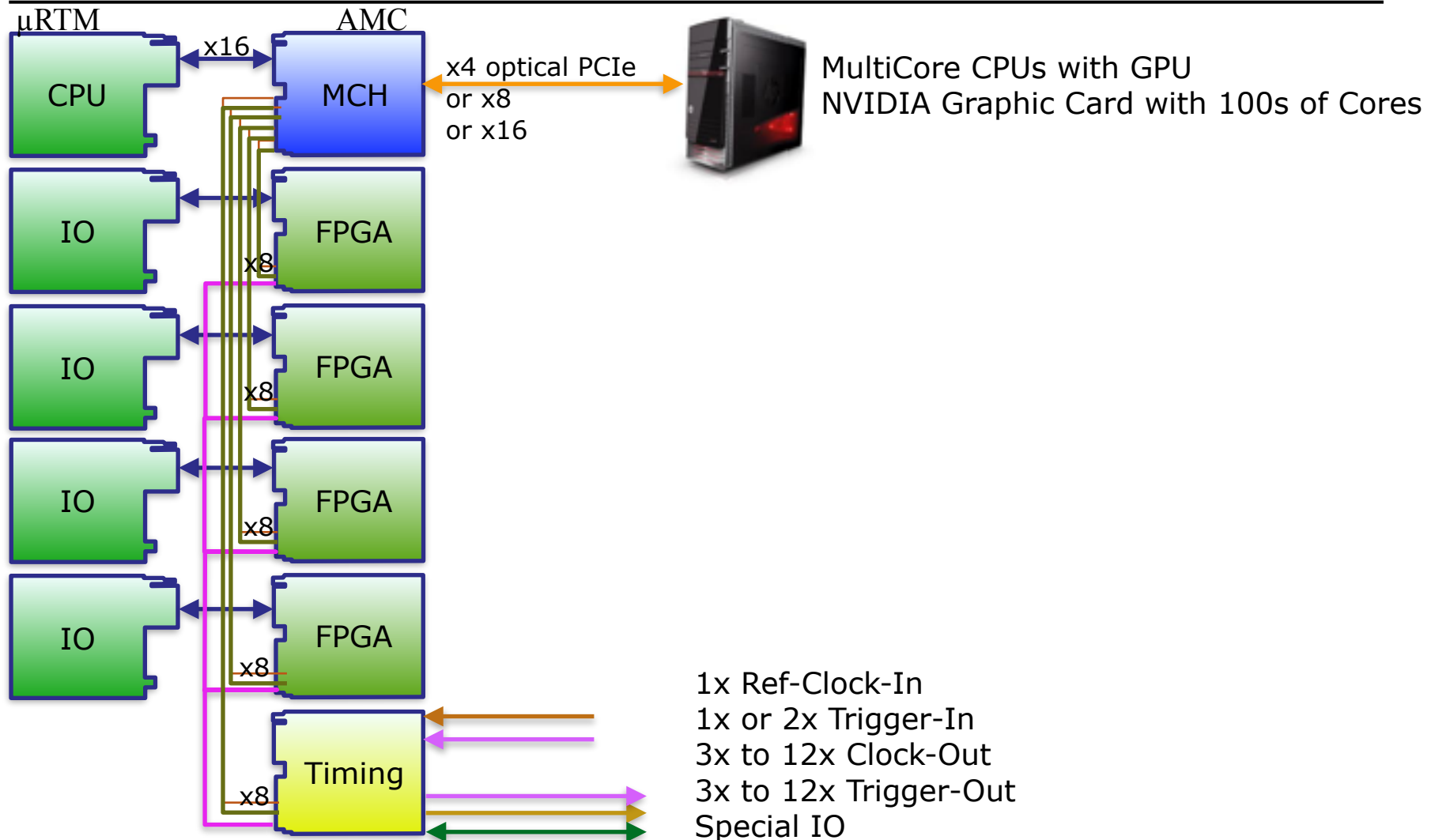
NATIVE-R2

Data stream from DSP/FPGA or FPGA/GPU to Displays



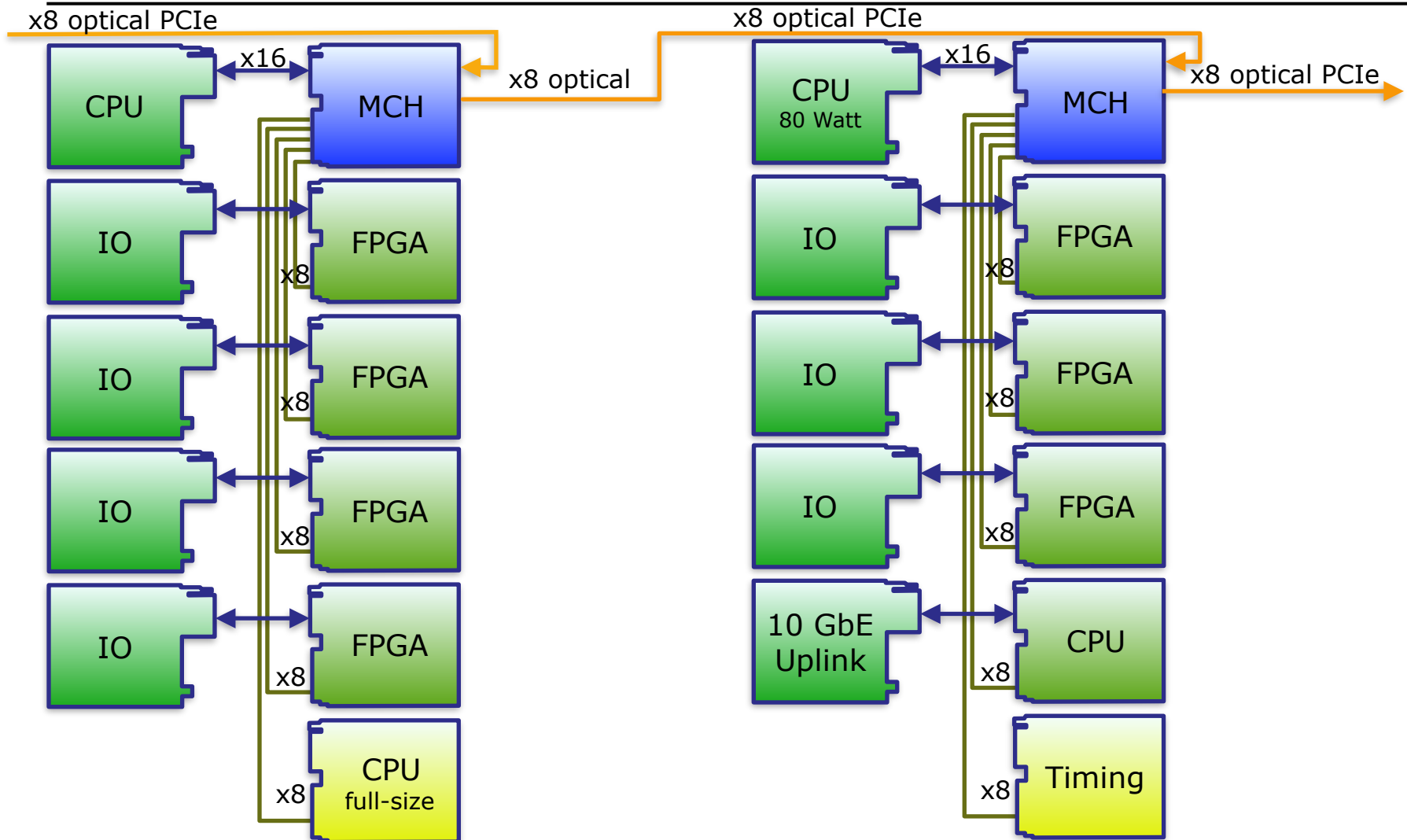
NATIVE-R2

Trigger and Clocks combined with High Bandwidth



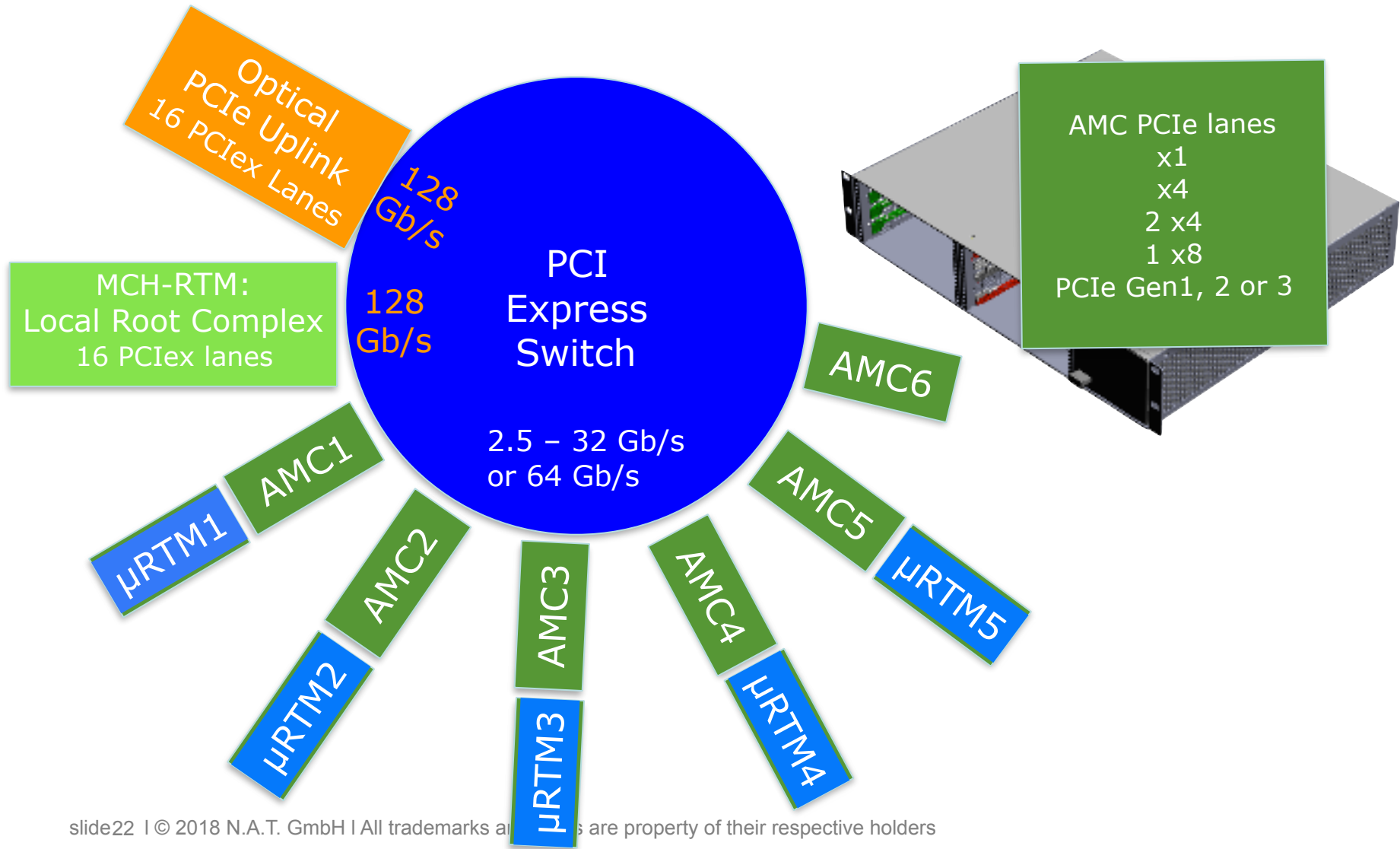
NATIVE-R2

Low Latency Cascading of Systems



NATIVE-R2

Clustering, Uplink, Cascading of systems





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