HIE-Isolde Low Level RF *proposal*

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BE/RF/FB

Outline

- 1. New LLRF developments in the BE/RF/FB section
- 2. LHC LLRF
- 3. Linac4 LLRF and SPL studies
- 4. HIE-Isolde LLRF *proposal*

1. BE/RF/FB section

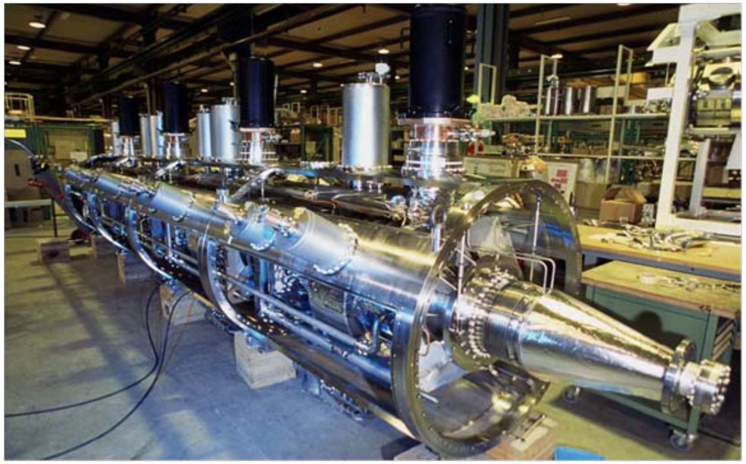
LLRF in the BE/RF/FB section

- RF operation of six machines
  - PSB, PS, SPS, LHC
  - LEIR
  - AD
- Fourteen staff members
- Ongoing LLRF projects
  - LHC re-start
  - PSB
  - Linac4
  - SPL studies

2. LHC LLRF

LHC LLRF

- Super Conducting Standing Wave Cavities, single-cell, R/Q = 45 ohms, 6 MV/m nominal
- Movable Main Coupler $10000 < Q_L < 180000$
- Mechanical Tuner range = 100 kHz
- 1 klystron per cavity
  - 330 kW max (58 kV, 8.4 A)
  - In operation < 200 kW CW
- 0.5 A DC current

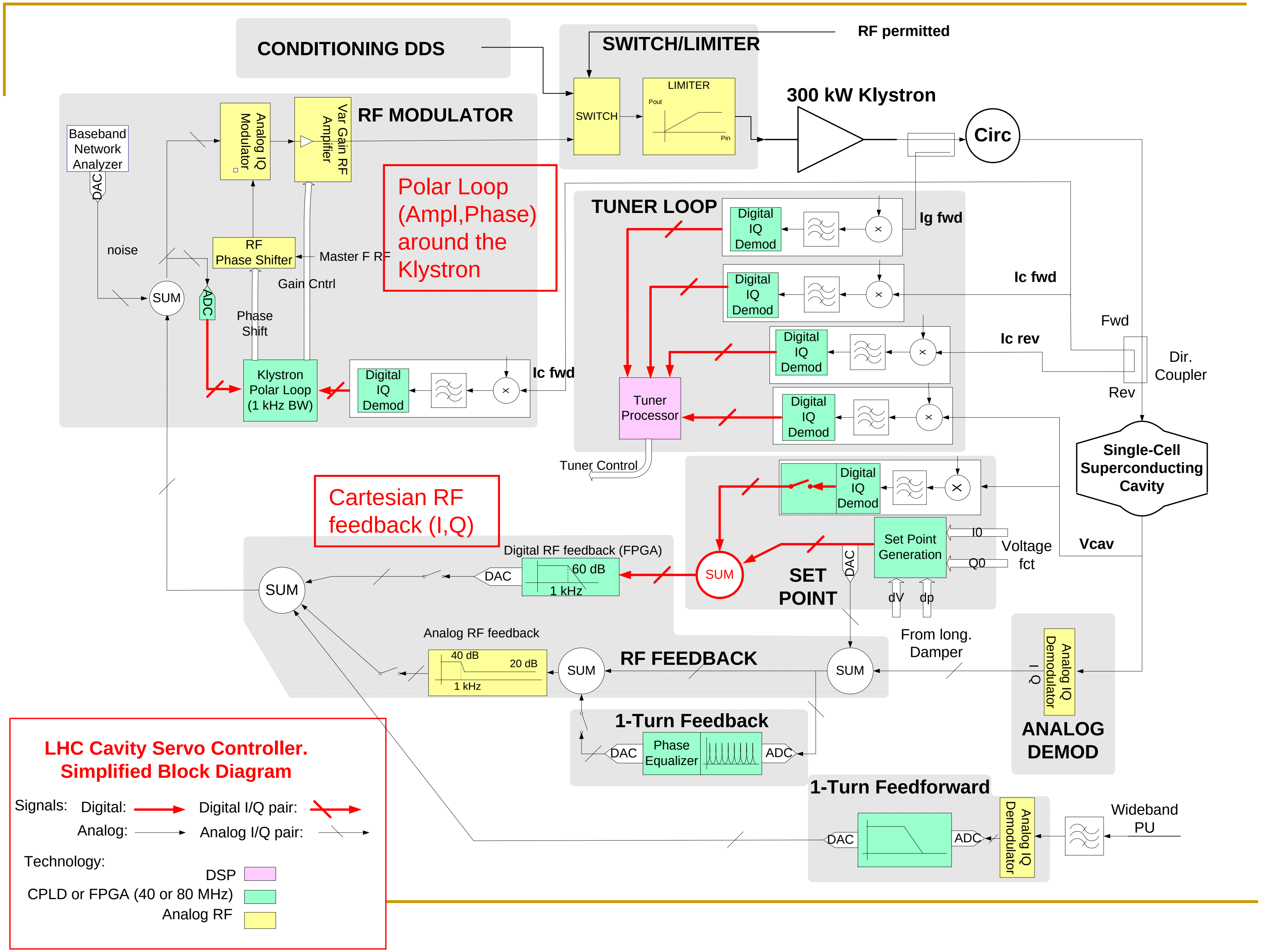


Hadron collider with very high beam current.

Challenges: Impedance reduction (stability) and low noise (lifetime)

LHC Cavity Controller Loops

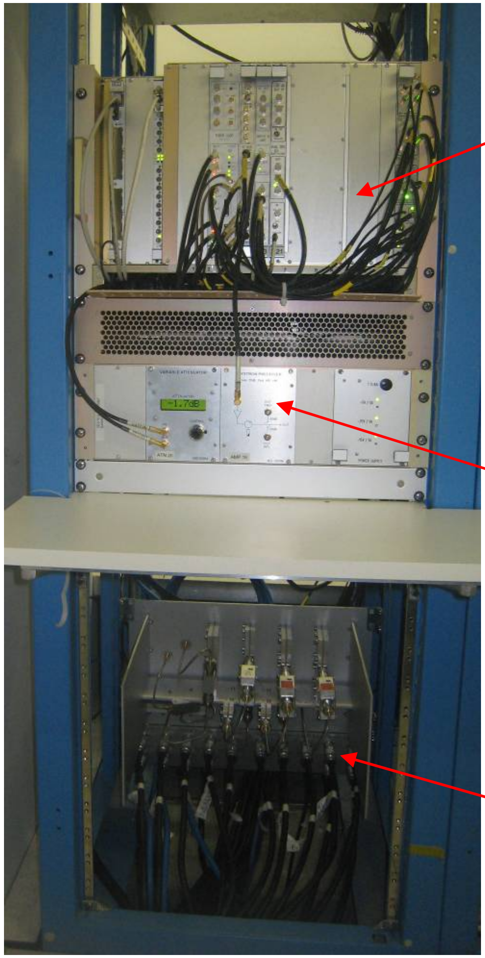
- **A Tuner Loop**: Minimizes klystron current. (Half detuning)
- **An RF Feedback Loop**: Reduces the cavity impedance at the fundamental (by 20 linear for Q=20000, by 180 at Q = 180000). Precision of RF voltage, transient beam loading and longitudinal stability
- **A Klystron Polar Loop**: Compensates for the klystron gain/phase changes. (HT drifts and ripples).
- **A 1-T Feedback**: Adds factor 10 reduction on the revolution frequency side-bands. (Transient beam loading + longitudinal stability)
- A **Conditioning System** monitoring the Main Coupler Vacuum while feeding the Line with Frequency Modulated bursts of RF power of increasing amplitude
- A **Klystron Drive Limiter** that prevents from driving the klystron over the saturation limit during loop transients.


CONDITIONING DDS
SWITCH/LIMITER
RF permitted
SWITCH
LIMITER
Pout
Pin
300 kW Klystron
Circ
RF MODULATOR
Baseband Network Analyzer
DAC
Analog IQ Modulator
Var Gain RF Amplifier
Polar Loop (Ampl,Phase) around the Klystron
noise
RF Phase Shifter
Master F RF
Gain Cntrl
Phase Shift
SUM
ADC
Klystron Polar Loop (1 kHz BW)
Digital IQ Demod
Ic fwd
TUNER LOOP
Ig fwd
Ic fwd
Ic rev
Fwd
Dir. Coupler
Rev
Tuner Processor
Tuner Control
Single-Cell Superconducting Cavity
Cartesian RF feedback (I,Q)
Digital RF feedback (FPGA)
DAC
60 dB
1 kHz
SUM
Set Point Generation
I0
Q0
Voltage fct
Vcav
SET POINT
dV
dp
From long. Damper
Analog RF feedback
40 dB
20 dB
1 kHz
RF FEEDBACK
1-Turn Feedback
Phase Equalizer
ADC
Analog IQ Demodulator
I Q
ANALOG DEMOD
1-Turn Feedforward
Wideband PU
LHC Cavity Servo Controller.
Simplified Block Diagram
Signals: Digital: Digital I/Q pair:
Analog: Analog I/Q pair:
Technology:
DSP
CPLD or FPGA (40 or 80 MHz)
Analog RF

Features

- RF feedback implemented in a low group delay I/Q Loop
- Extensive Diagnostics:
  - Important signals (~30/cavity) are stored for monitoring
  - Two sets of memory
    - Post-Mortem memory: Free-running, stopped by specific machine-wide post-mortem trigger, fixed sampling rate. Meant to correlate acquisitions after a fault.
    - Observation: Piloted by operator that sets sample rate and triggers the acquisition. Meant for monitoring during operation.
  - Built-in Network Analyzer
    - Excitation memories to inject signals (step, sine-wave, white noise,…) coupled with observation memories implement a Signal Analyzer
- Fully remote controlled

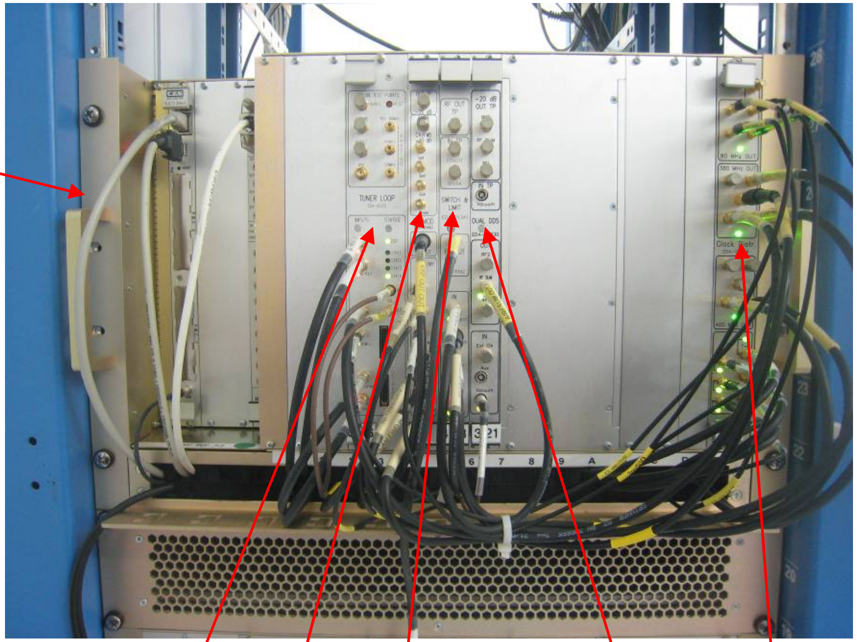
Implementation



Cavity Controller VME crate

Antenna calibration and 100 mW pre-driver

RF cable splitting



Switch&Limit

Clock Distri

Tuner Control

Conditioning DDS

RF Modulator

LHC LLRF VME Tuner Crate

LHC LLRF

LHC LLRF Faraday Cage

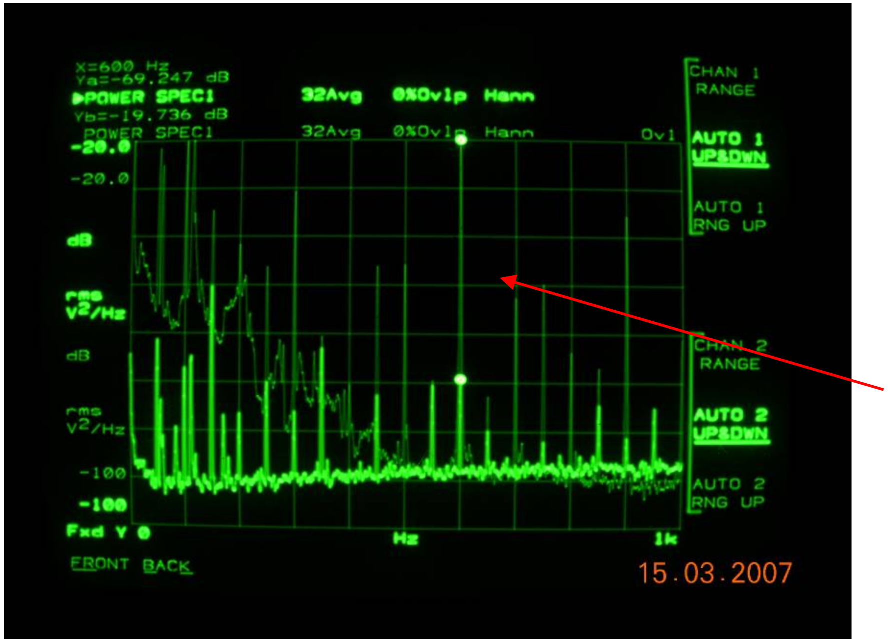
Noise reduction with RF feedback

Phase Vcav/Ref

Open Loop 10 mV/div -> **5 dg pk-pk**, 5 ms/div (File PhaseMeasOpen 14 March 2007)

Closed Loop 2 mV/div -> **0.1 dg pk-pk**, 5 ms/div (PhaseMeasAtt_0A 14 March 2007)

- Phase noise Vcav vs ref.
- SM18 test stand, March 2007
- Calibration: 10 mV/dg @ 400 MHz
- Q=60000, 1 MVacc, 35 kW



Open Loop vs Close Loop. 50 dB reduction @ 600 Hz
(File PhaseNoise3 15 March 2007)

- Power Spectral Density of cavity phase noise (Vcav vs Ref) with and without RF feedback
- ZLW1 mixer and Spectrum Analyzer
- 300 mV/dg @ 400 MHz
- 50 dB reduction of 600 Hz line

LHC LLRF Developments

- LLRF design started in 2003. Completed by 2008+.
- ~ 4 man.year per year over the seven years period
- Volume:
  - 20 racks in UX45 plus 15 racks in SR4
  - ~ 50 special LLRF VME crates plus 5 standard VME crates
  - ~ 500 NIM/VME cards of 36 different makes
- Much expertise developed
  - Signal Processing in FPGA (CIC filters, CORDIC, I/Q Demodulator)
  - Synchronization problems in multi-clocks systems
  - Mixed signals PCBs: RF front-end and digital part. Grounding, decoupling, linear/switched mode P.S.
  - Design flow/tools: Visual Elite (FPGA) then Cadence (Schematics/Layout)
  - Use of on-board diagnostic memories plus excitation buffers

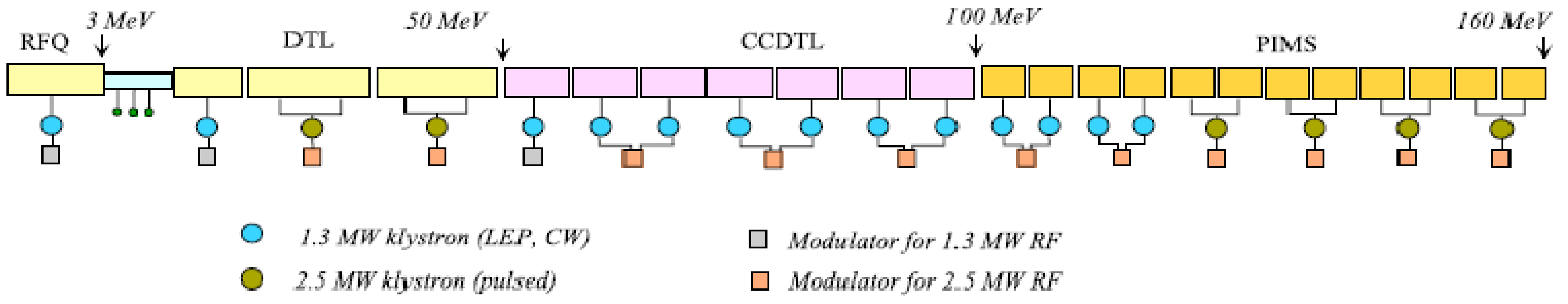
3. Linac4 LLRF

Linac4 LLRF

- H- Linac injecting 160 MeV beam in the PSB
- Replaces Linac 2 (designed 1975)
- Commissioning in 2013. From start-up 2014 source of all proton beams
- ~80 m long
- Normal Conducting structures (Q_L from 6k to 40k) at 352.2 MHz
- 2 Hz rep rate
- 40 mA Linac current
- Beam Pulse length: 80 - 400 μs nominal, 1 ms max
- Wide variety of structures: re-entrant cavities (buncher), RFQ, DTL, CCDTL, PIM
- LLRF design started in 2009.
- **Target: Field stabilization within 1 deg and 1 %**

Moderate intensity pulsed NC Linac.
Challenge: Transient Beam Loading (chopping)

Lay-out



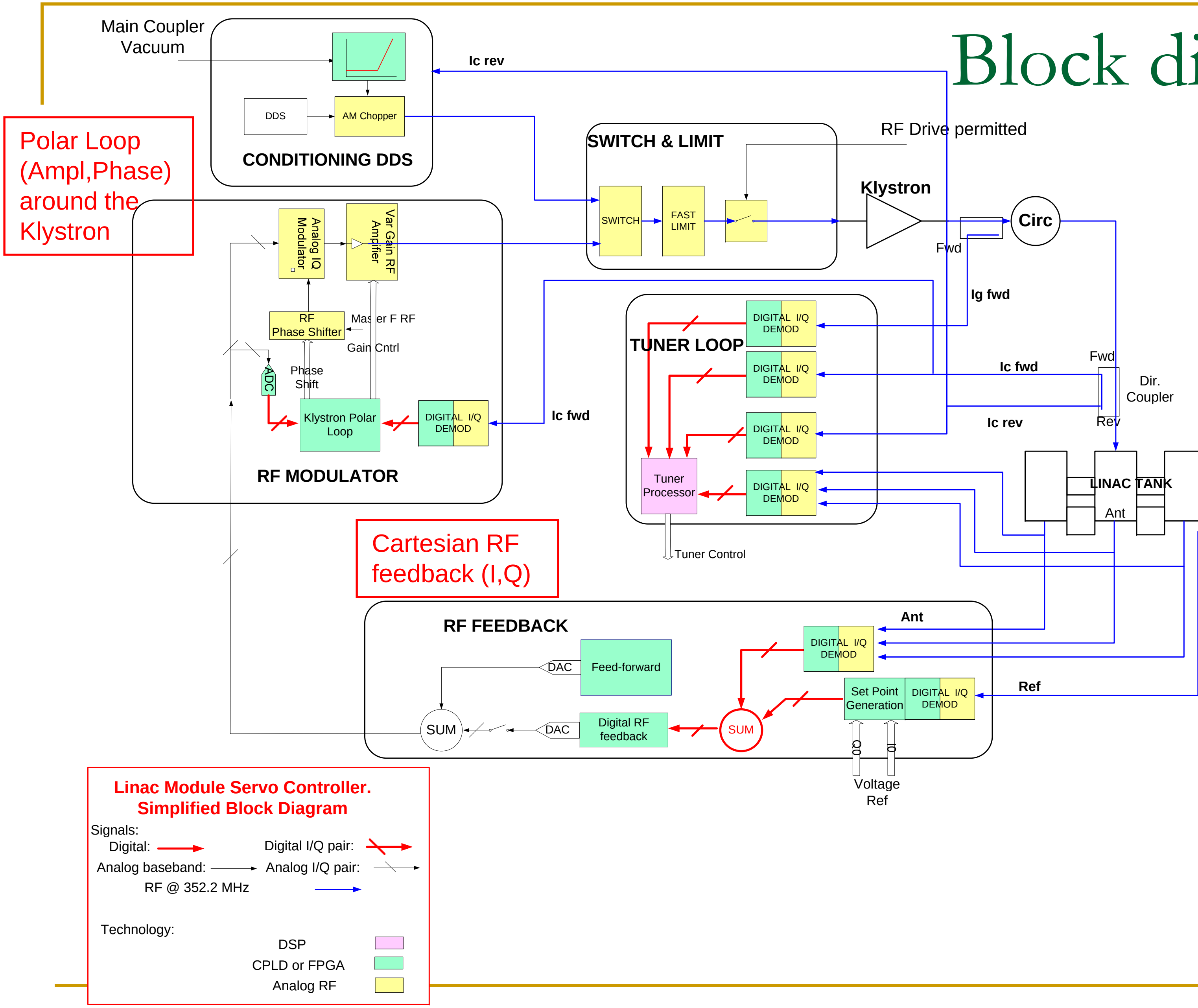
Linac 4 lay-out.

Functionalities. For each tank

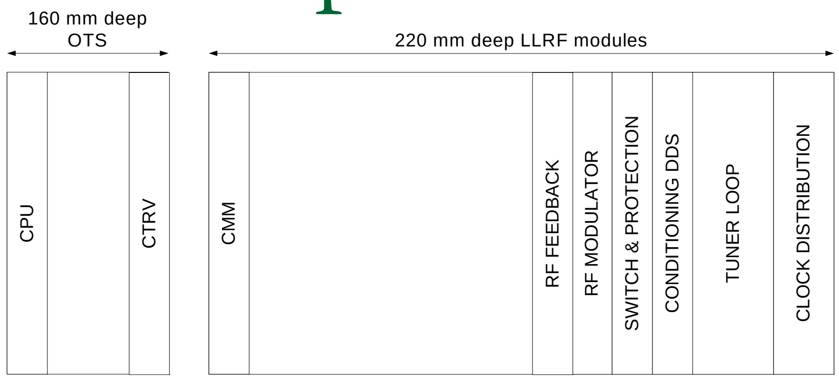
- A **Tuner Loop** to keep the structure on resonance
- An **RF Feedback**, and a **Feedforward** (Iterative Learning) to keep the accelerating voltage at the desired value in the presence of beam transient
- A **Klystron Polar Loop** to compensate the variation of klystron gain and phase shift caused by High Voltage (HV) supply fluctuations and droop
- A **Conditioning System** monitoring the Cavity Vacuum/Reflected Power while feeding the Line with Frequency Modulated bursts of RF power of increasing amplitude
- A **Klystron Drive Limiter** that prevents from driving the klystron over the saturation limit during loop transients.

Similar – but somewhat simpler – than the LHC LLRF (slide 7)

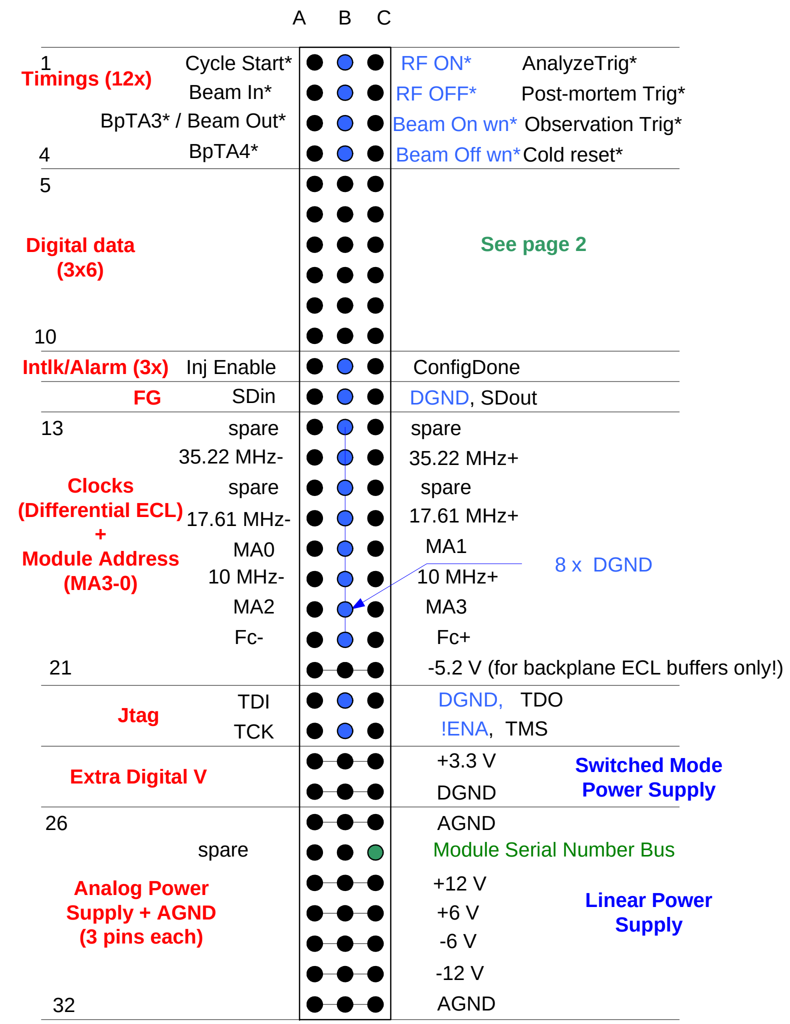
Block diagram



Developments



- Same crate as LHC LLRF but re-assigned lines on J2 backplane
- Same design flow: Visual Elite for FPGAs, Cadence
- Re-use FPGA blocks: I/Q demod, CIC, Cordic
- But… **re-do all VME modules** (simplifications, obsolete components,…)



LINAC LLRF backplane
Lower connector: 3 x 32 pins
version 11/30/2008

SPL LLRF studies

- H- Linac at Linac4 output (from 160 MeV to 4 GeV)
- Multi-cell Super-Conducting structures (Q_L ~10^6) at 704.4 MHz
- 2 Hz rep rate
- 20 mA Linac current
- Only study so far (fast tuner to compensate the Lorentz Force detuning)

4. HIE-Isolde LLRF *proposal*

HIE-Isolde LLRF

- CW operation
- Super Conducting QWR structures
- $Q_L \sim 10^7$ around 100 MHz
- Solid state amplifier Peak Power < 1 kW . One amplifier per cavity. 250W needed on tune.
- 1 pA Linac current
- **Target: Field stabilization within 0.5 deg and 0.5 %**

Very low intensity CW SC Linac.

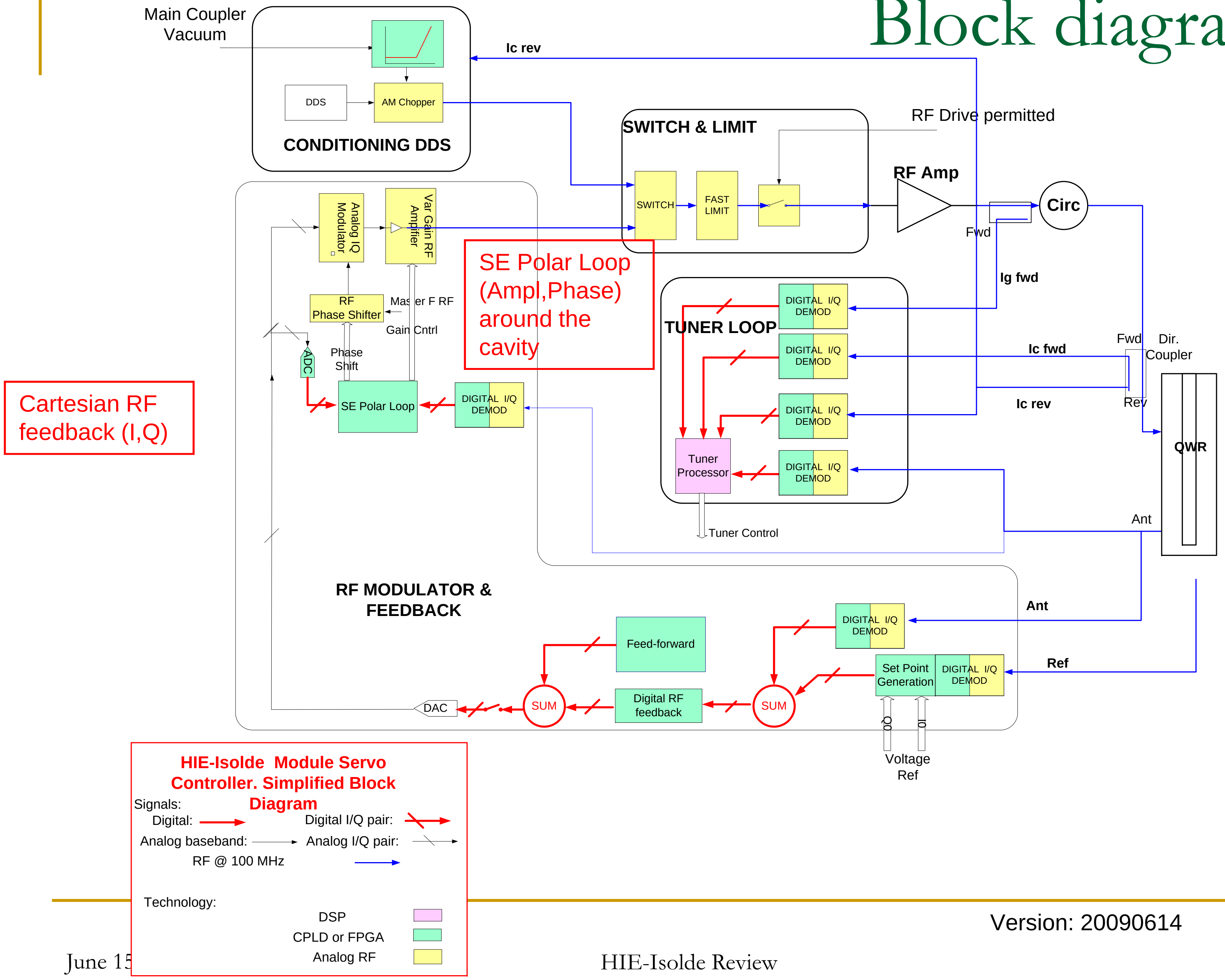
Challenge: **Very high Q_L**

Functionalities. For each cavity

- A **Tuner Loop** to keep the structure on resonance
- An **RF Feedback** to keep the accelerating voltage at the desired value in the presence of perturbations (vibrations, Helium pressure fluctuations, ..). Normal operation in **Driven Mode**.
- A **Self-Excited Polar Loop** to enable **SEL Operation** at start-up when the tune is way off or without tuner
- A **Conditioning System** monitoring the Window Vacuum while feeding the cavity with Frequency Modulated bursts of RF power of increasing amplitude
- A **Klystron Drive Limiter** to limit the drive in Self-Excited Loop mode

Similar to Linac4 – but klystron loop replaced by SEL loop around the cavity

Block diagram



Version: 20090614

Normal operation. Driven feedback system.

- Cavity Controller close to Cavity.
  - Max 30 m round-trip (~ 100 ns cable delay)
  - Allowing 100 ns for RF Amplifier

  RF feedback BW (2-sided) in excess of 2 MHz …if sufficient Amplifier power.
- For each cavity, the Set point is individually provided as an (I,Q) set vector
- The Phase and amplitude controls in the RF Modulator are set at fixed values (SE Polar Loop OFF)

Tuner

- $Q=10^7$ -> only 10 Hz 2-sided BW
- Stability of the structure
  - Mechanical resonances (64 Hz?)
  - Microphonics (2 Hz rms?)
  - Sensitivity to He pressure fluctuations 0.01 Hz/mbar (0.3 Hz for expected 30 mbar ripple)
  - Precision of the tuning mechanics: **1 μm** -> ~10 Hz = **1 BW !**

  To be measured ASAP

  Then study/simulation with the LLRF
- Resolution of the Tuner RF front-end
  - 200 kHz tuning range = 20000 BW
  - At 5 kHz offset, V_{cav} is reduced by 60 dB

Startup

- With cavity way out of tune, Tuner loop may not lock…
- Two possibilities
  - Open Loop using the Conditioning DDS
    - Sweep frequency of Conditioning DDS to find the resonance.
    - Then move the tuner to get in the Locking Range of the tuner loop
  - **Self-Excited Mode**
    - With the RF Feedback
      - Reduce RF feedback gain so that resonance can only take place in the Cavity BW
      - Intentionally add 180 degrees to the Modulator Phase to make the RF feedback unstable
    - With the SE Polar Loop
      - Open the RF feedback. Set a fixed (I,Q) at the modulator input.
      - Adjust phase of SE Polar Loop to initiate resonance
- Advantage: The Self-Excited Loop can be used without tuner (Lab tests)
- To be studied
  - SEL implemented in I/Q coordinates (using the RF feedback) vs. implementation using the SE Polar loop
  - Control of Cavity voltage when in SEL mode

Thank you…

Additional material if questions arise

RF feedback Theory

- RF Feedback theory [6],[7]
  - Minimal cavity impedance (with feedback) scales linearly with T

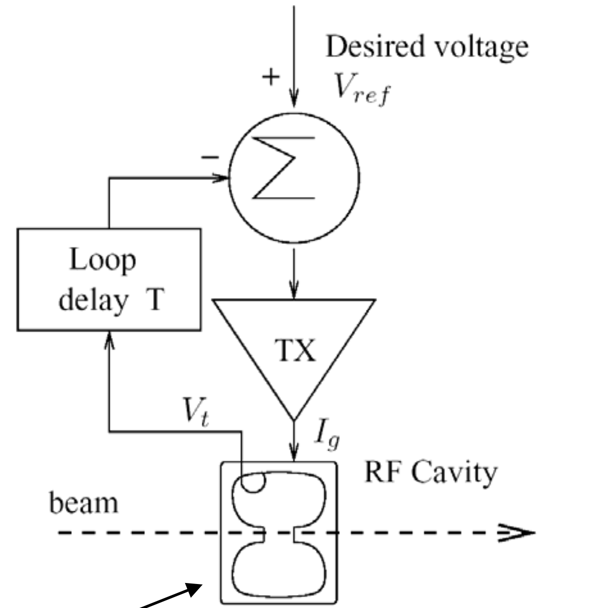
$$R_{\min} = \frac{2}{\pi}\frac{R}{Q}\omega_0 T$$

  - Achieved for a gain value proportional to Q

$$G_{opt} \approx \frac{Q}{\omega_o T}$$

  - Achievable fdbk BW inversely proportional to T

$$\Delta\omega = \frac{1.3}{T}$$



assumed single-cell