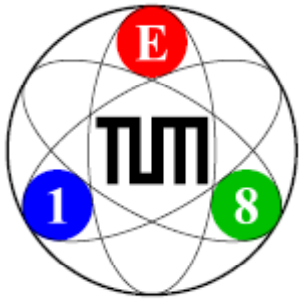


COMPASS APV readout

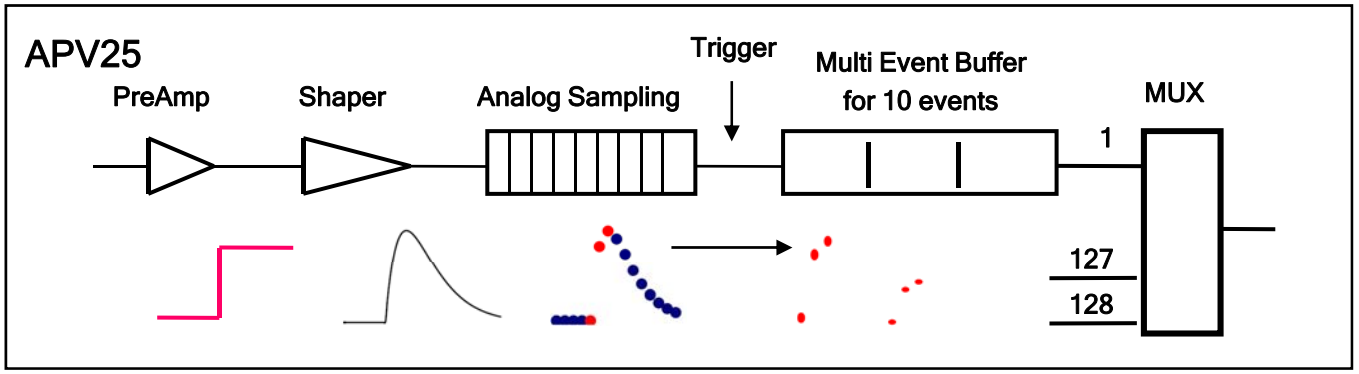
I.Konorov

APV25-S1

APV25-S1 developed for CMS silicon µ-strip detectors

Features:

- 128 channels
- analog pipeline (SCA) runs with 40MHz clock
- 1 or 3 samples /event
- 50 ns peaking time
- external trigger
- no zero suppression



APV25 readout in COMPASS

- Silicon, GEM, PixelGEM, RICH(MWPC)
  Noise : GEM 1200-1400 e- @20pF capacitance

- 3 samples/event -> Pulse Shape Analysis -> Amplitude & Time
- Readout without zero suppression (LatchALL), trigger rate about 1kHz
- Readout with zero suppression(SPARSE), trigger rate up to 50kHz

APV card

Connector to detector
- 130 pins
- 2 pins for detector ground
- Detector should have solid ground

Protection circuit: 2 diodes to GND + 220pF

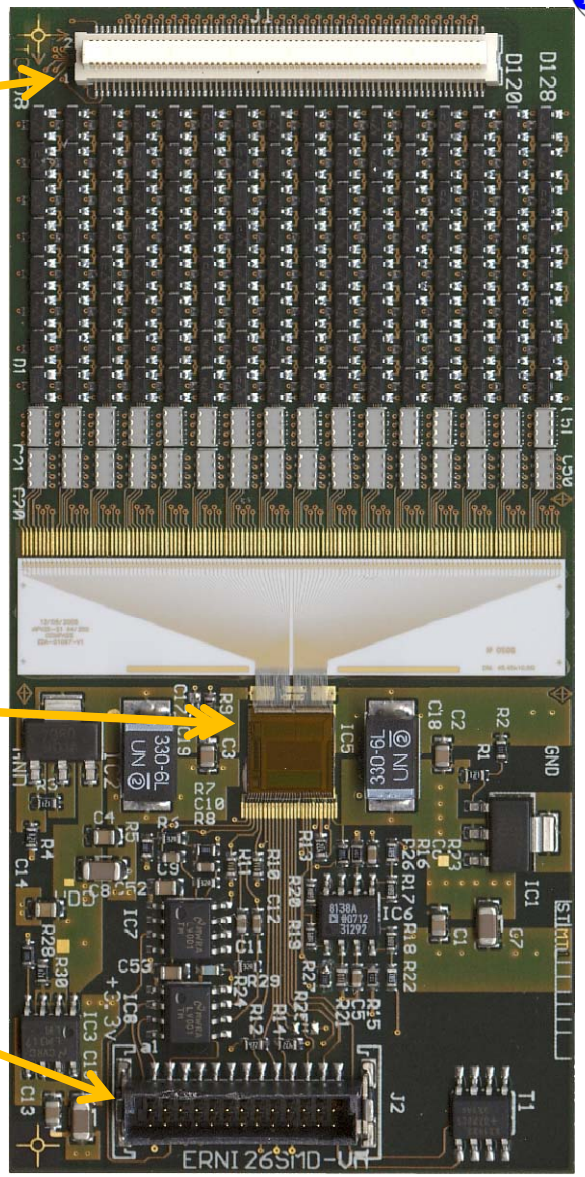
Pitch adapter

APV: 128 channels

Back end connector
- Power
- CLK, Trigger – differential signals
- I2C

Power : +5V, -3.3V

APV voltages: +2.5V, +1.25V



ADC module and transition card

- 4 connectors for 4 APV chips each
- 16x12bit 40MHz ADC
- FPGA XC4VLX25
  - Interface support
  - Data processing
- USB interface
  - Only for configuration
- Power

  +5V , 3 A

  -5V , < 1A
- APV power, independent

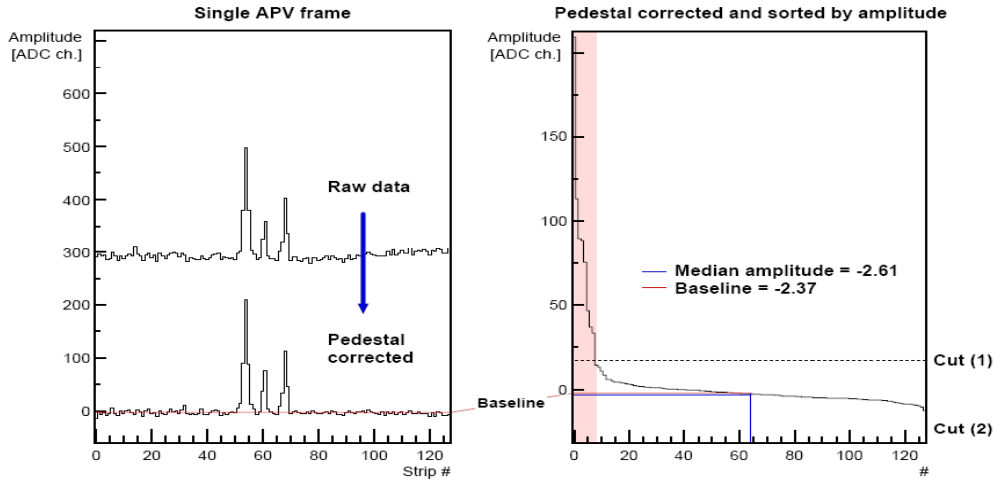
  +5V, 0.3A/chip

  -5V, 0.1 A/chip

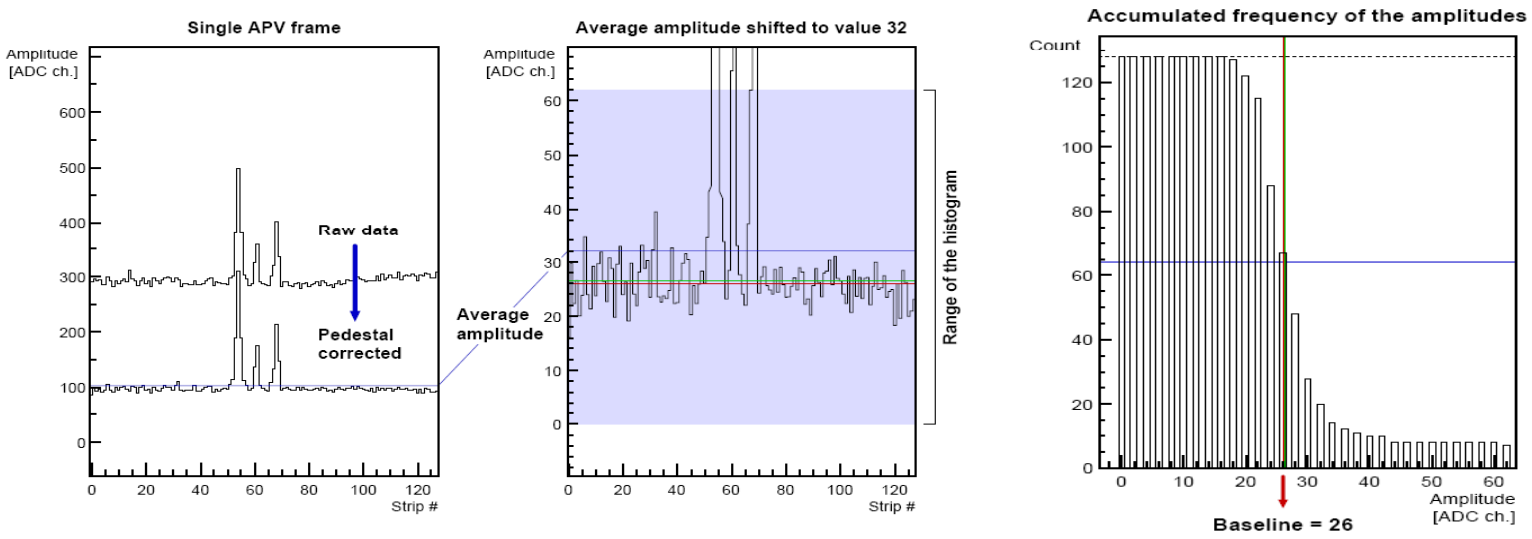
http://www.e18.physik.tu-muenchen.de/~ikonorov/COMPASS/COMPASS%20Electronics.html

FPGA Data processing: pedestal and common mode noise correction

Median algorithm



Implementation of median algorithm in FPGA



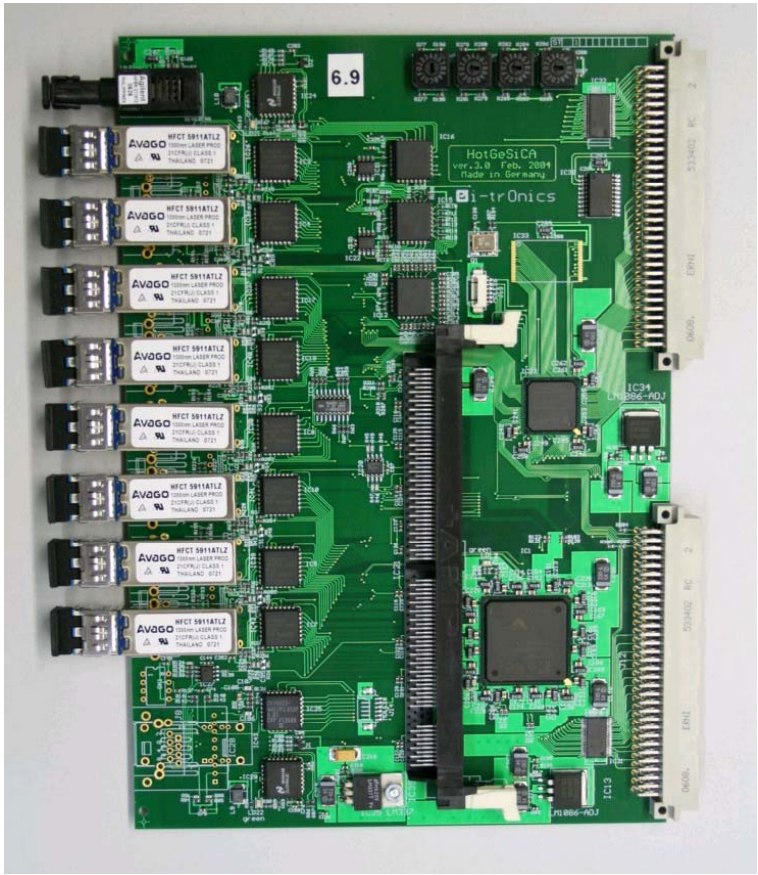
HGeSiCA module

6U VME module

- VME interface
  - configuration
- 8 front-end cards
- TCS interface
- Data concentrator
- Slink interface via P2

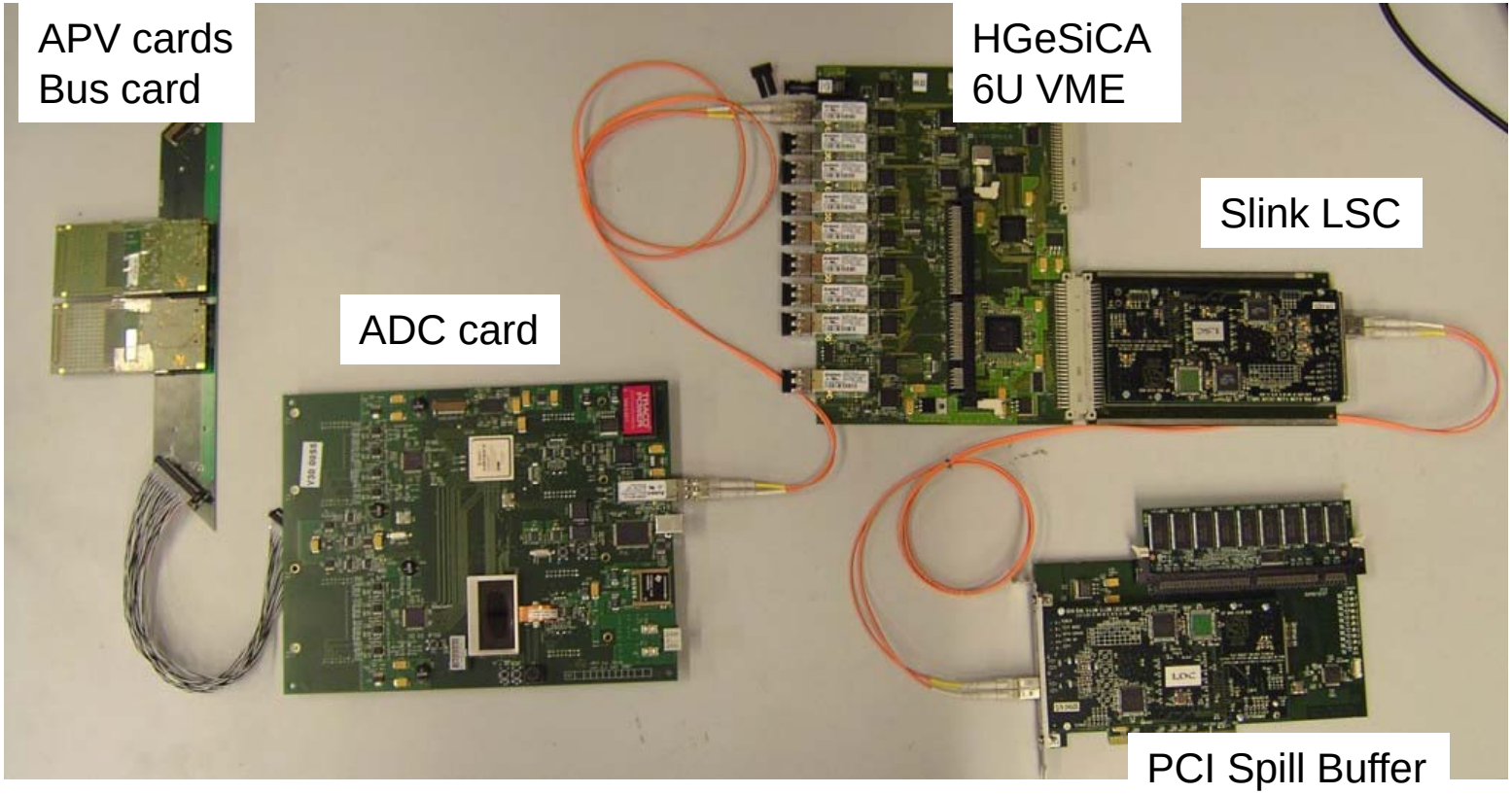
Extra functions

- standalone woTCS data taking
- very slow VME interface
- Trigger injection via P2



http://www.e18.physik.tu-muenchen.de/~ikonorov/COMPASS/COMPASS%20Electronics.html

APV Read Out Chain



- 16 APV chips can be attached to one ADC
- 8 ADCs can be attached to one HGeSiCA
- Configuration via VME backplane
- Trigger/Clock distributed by Trigger Control System
- Pipeline readout: maximum 10 triggers/125usec

Configuration and Software

- Front-end configuration via VME backplane
  - Loading FPGA firmware
  - Configuration
    - HGeSiCA registers
    - APV registers
    - ADC registers
    - Loading pedestals and thresholds
- ConfigServer : COMPASS software for distributed computers
  - All parameters , except pedestals and thresholds stored in MySQL
  - DIM client protocol

- Monitoring software – GEM Monitor:
  - measuring pedestals & thresholds
  - Checking data consistancy
  - Debugging readout problems features

Possible readout configurations

- COMPASS like
  - TCS + ADC + HGeSiCA + Slink + SpillBuffer
  - Unlimited number of ADCs and Front-ends
- VME
  - ADC + HGeSiCA
  - Extra effort to inject triggers and Spill signal via P2
  - Maximum 8 ADC cards
  - Question of time synchronization for measuring hit time better than 25 ns
- USB
  - Requires additional software development
  - Providing trigger signal
  - No common 40MHz clock if more than one ADC card used

RD51

- If RD51 decides to use COMPASS APV readout electronics few questions to be addressed:
  - System configuration and what should be provided
    - APV cards ?
    - ADC+HGeSiCA ?
    - Spill Buffer ?
  - When to be provided ?
  - Electronics production will be outsourced !
  - Due to system complexity it is required that there is at least one system expert within RD51