cta cherenkov telescope array

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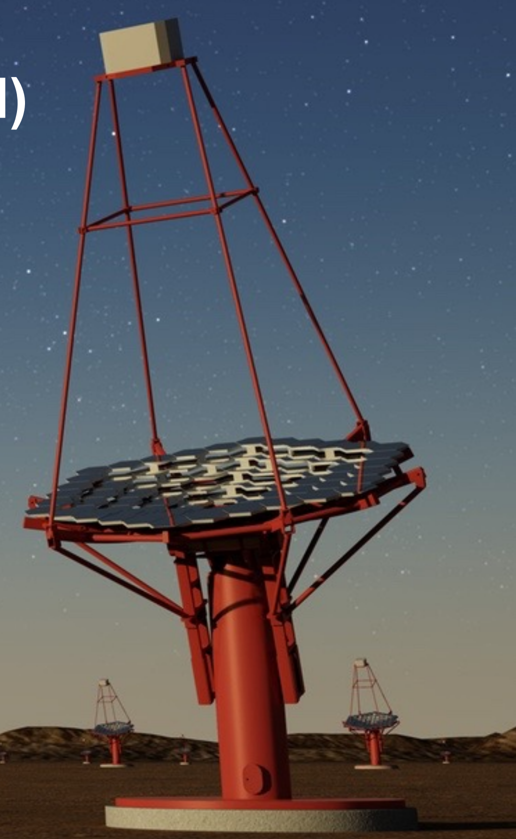
High performance prototype SiPM camera

for the single mirror small-sized telescope (SST-1M) for the Cherenkov Telescope Array (CTA) project

Matthieu Heller

(DPNC, Université de Genève)

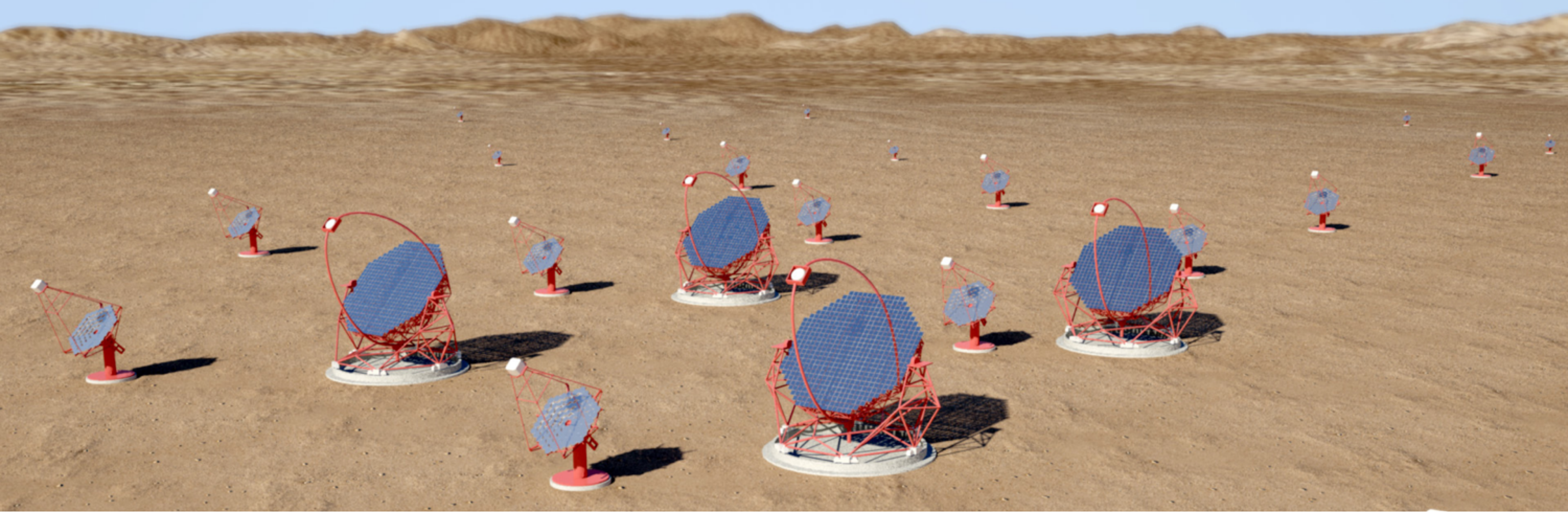
on behalf of the SST-1M sub-consortium and the CTA consortium



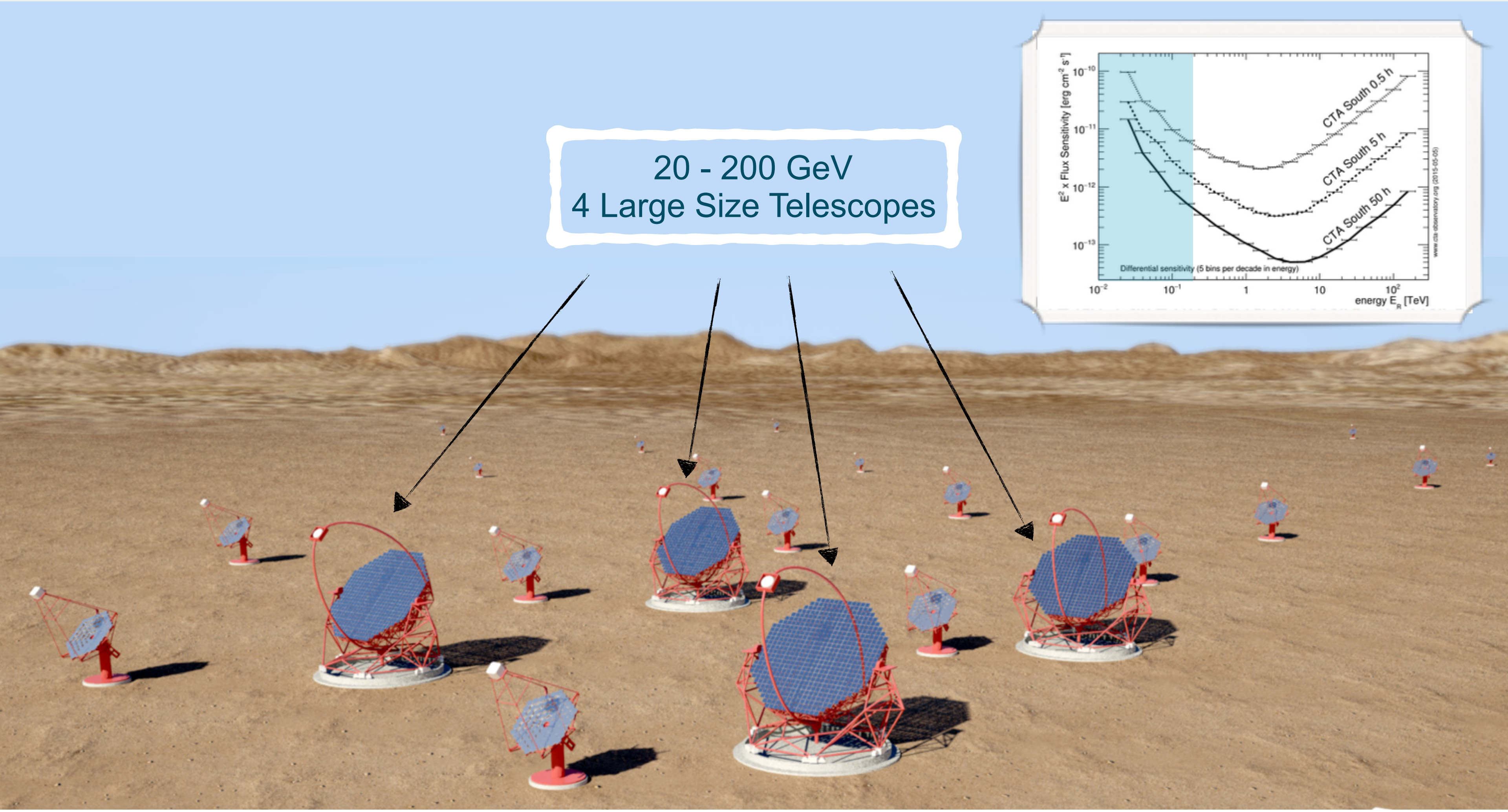
SPS meeting, Lugano, 23-25 August 2016

The Cherenkov Telescope Array

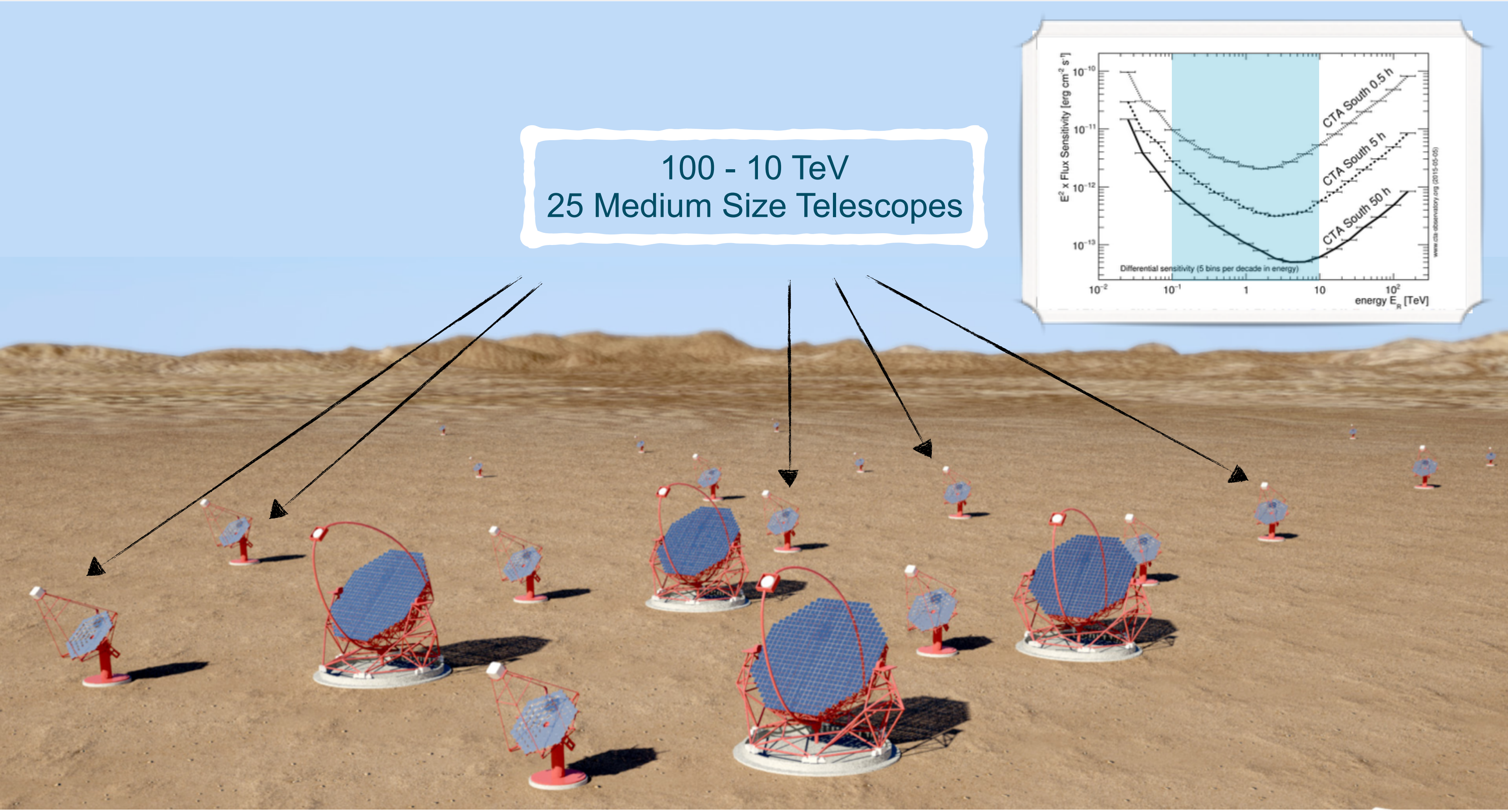
- **A user facility / proposal-driven observatory**
  - With two sites with a total of >100 telescopes
- **Project with 32 nations**
- **More than 200 institutions**
- **More than 1300 members**



The Cherenkov Telescope Array



The Cherenkov Telescope Array



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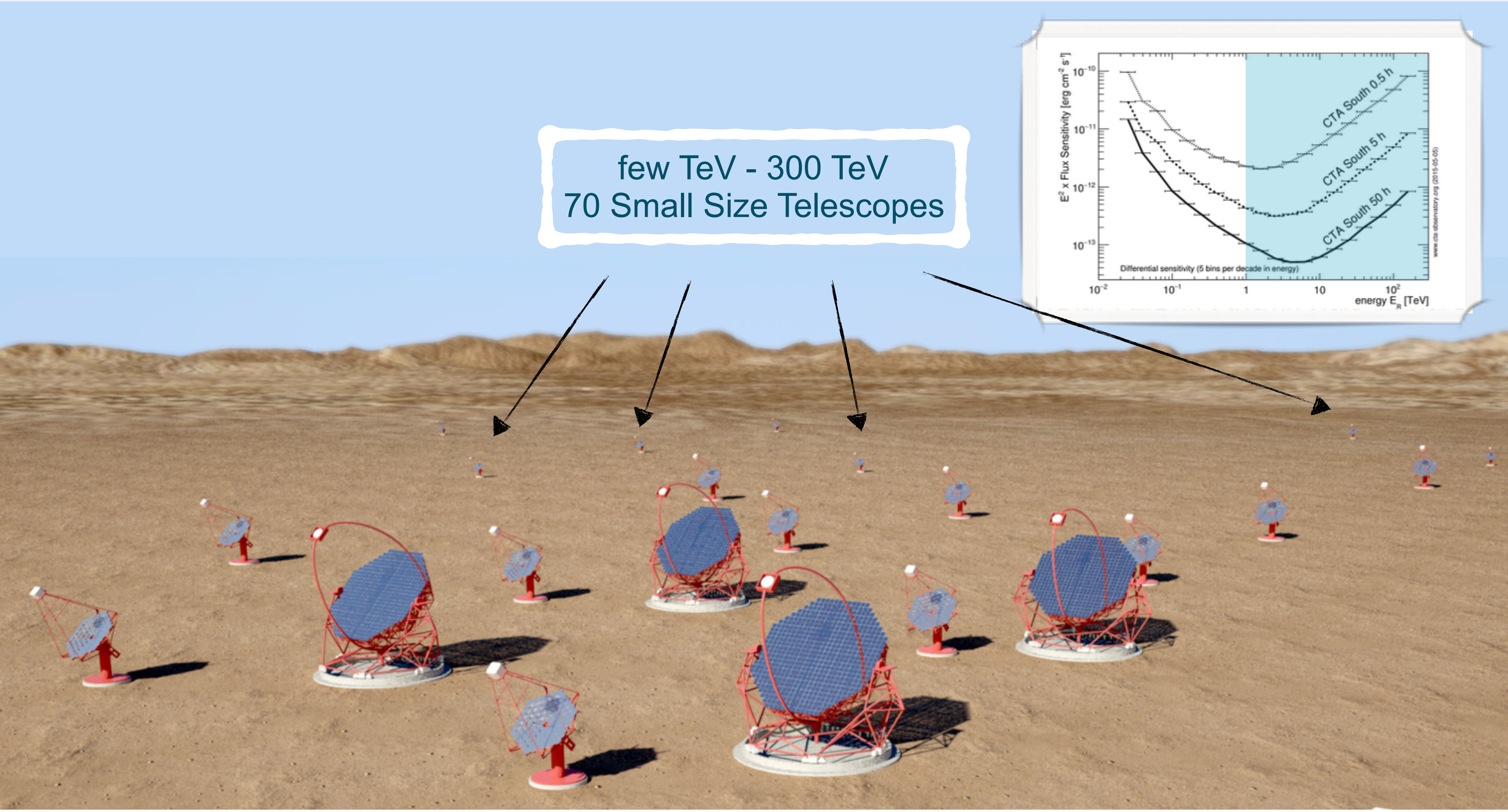
The Cherenkov Telescope Array

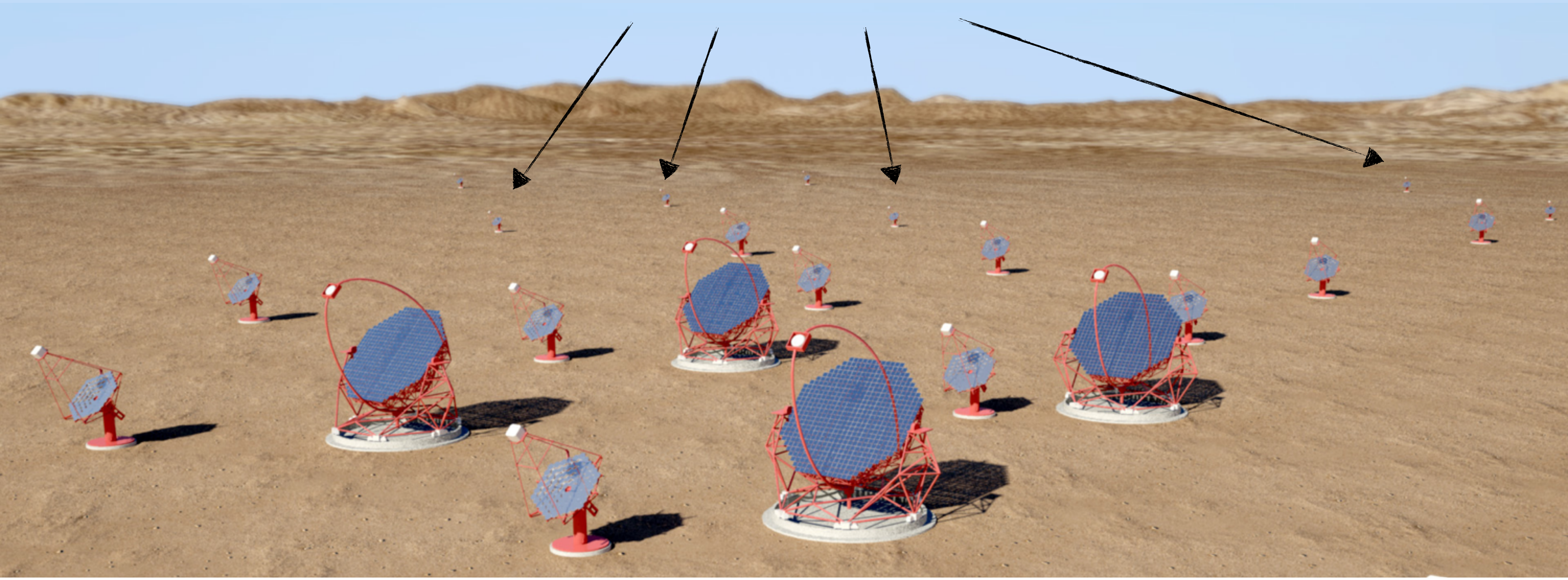


The Cherenkov Telescope Array

For SSTs, 3 designs proposed:
- 2 dual mirrors (ASTRI, GCT)
- 1 single mirror (SST-1M)

few TeV - 300 TeV
70 Small Size Telescopes

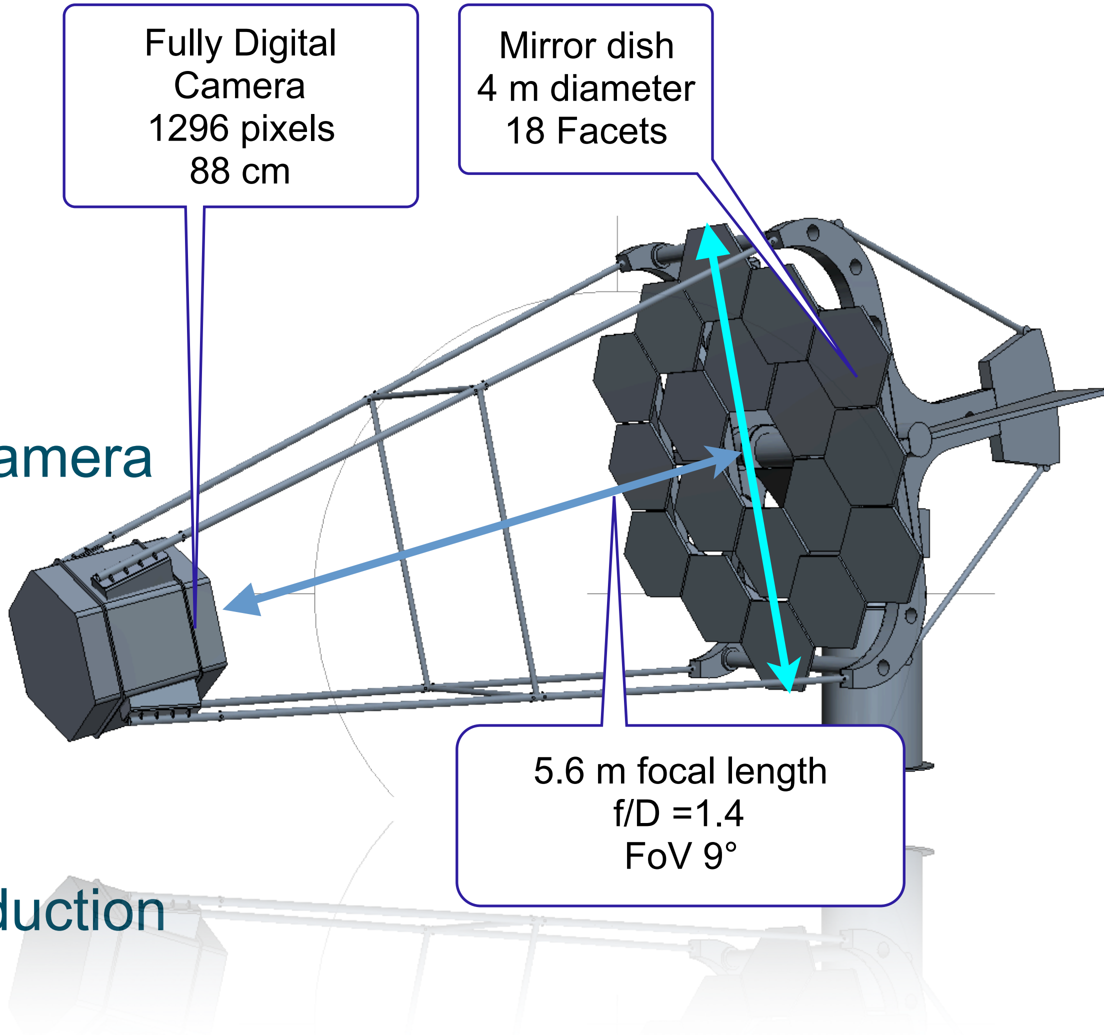
SST-1M in numbers:
- ~ 20 telescopes
- 5 countries
- 12 institutes
- 22 FTE (60 people)



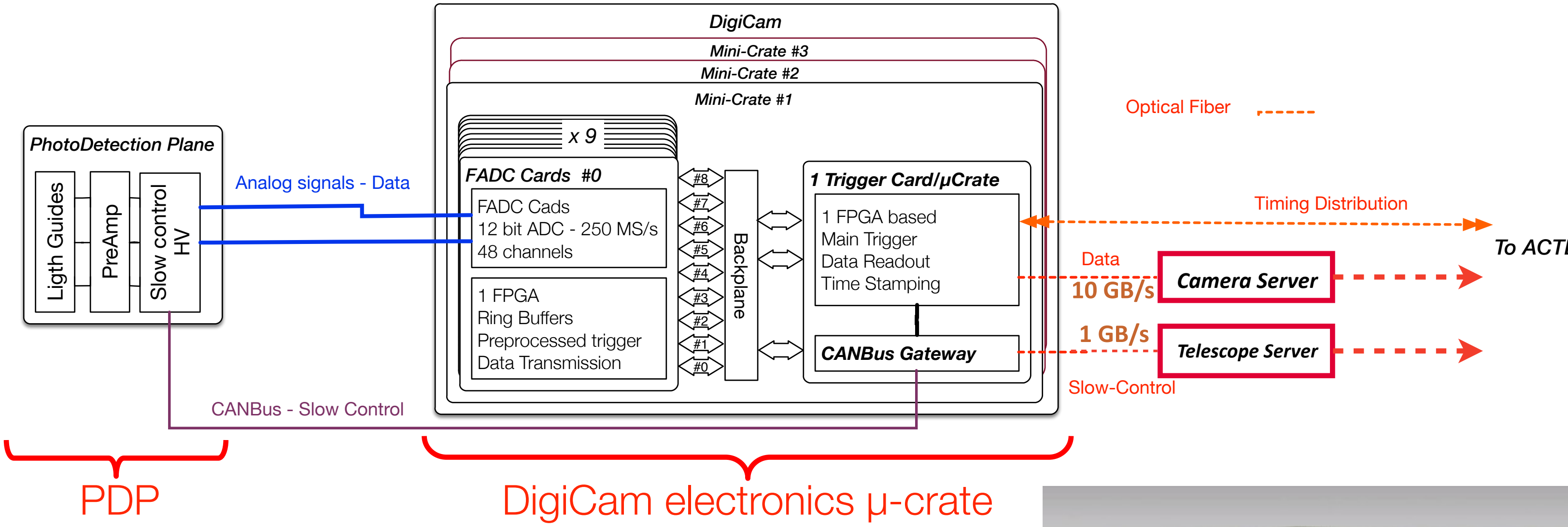
The single mirror small-sized telescope

The telescope concept

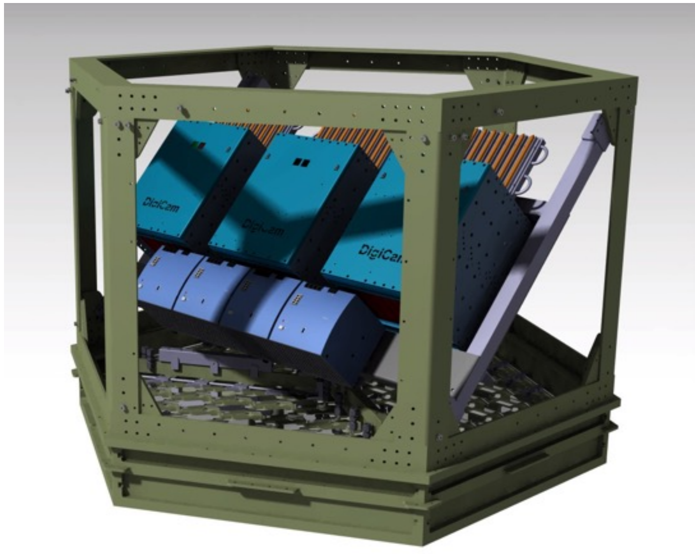
- Davies-Cotton Design
  - Proven optical design
  - Lightweight ~ 8.6 t
  - Low Cost
- Innovative G-APD-based camera
- Fully digital readout
- Easy Installation
- Easy maintenance
- Straightforward logistics
- Industrial approach for production



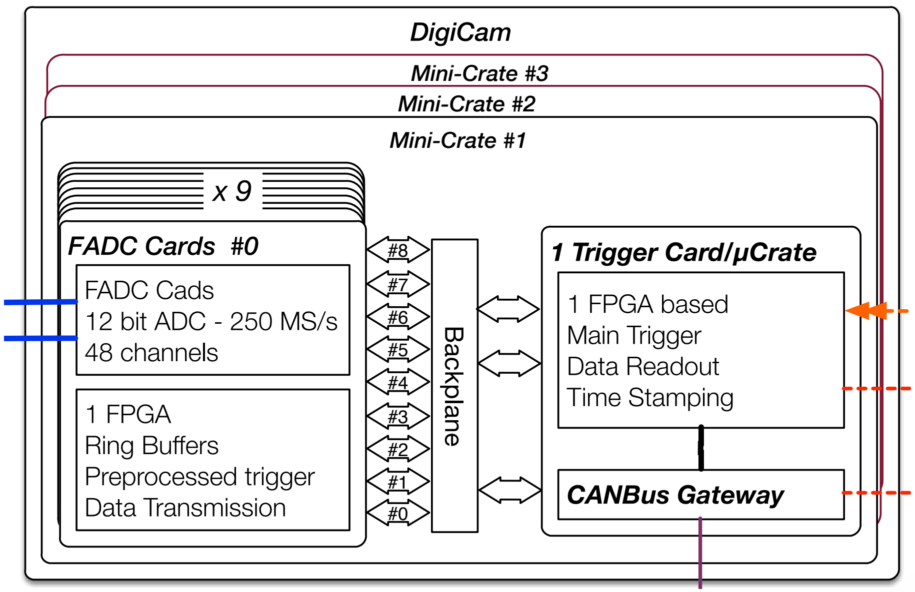
The camera concept

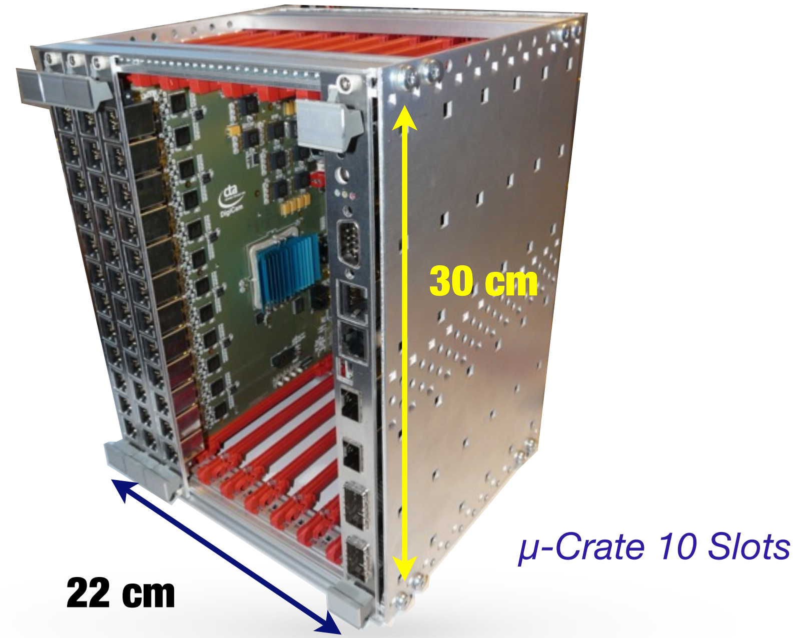


- Separation of Analog PDP and Digital Readout
  - Analogue signals over CAT6/RJ45
  - DC coupling for NSB monitoring
- IP65: Window and chassis sealed
- Water cooled
- Compact, robust, lightweight and self-contained



Digital readout - DigiCam

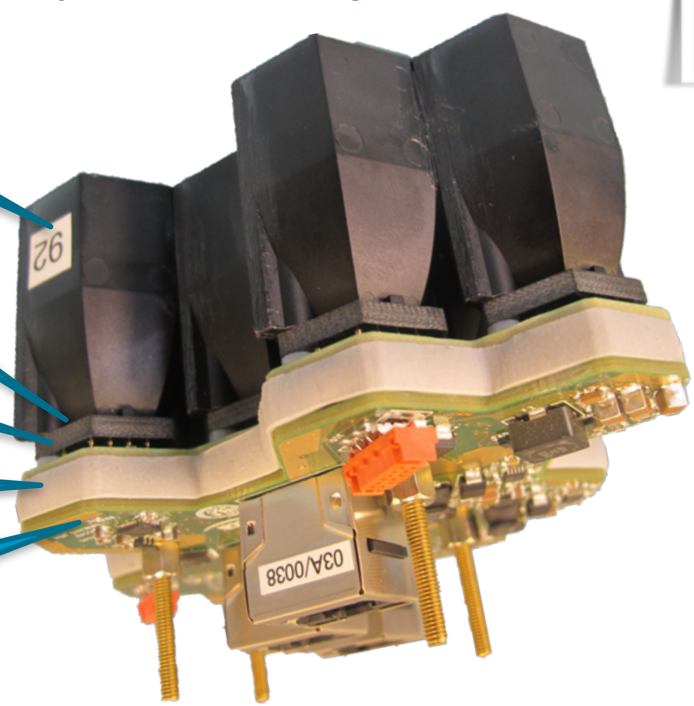


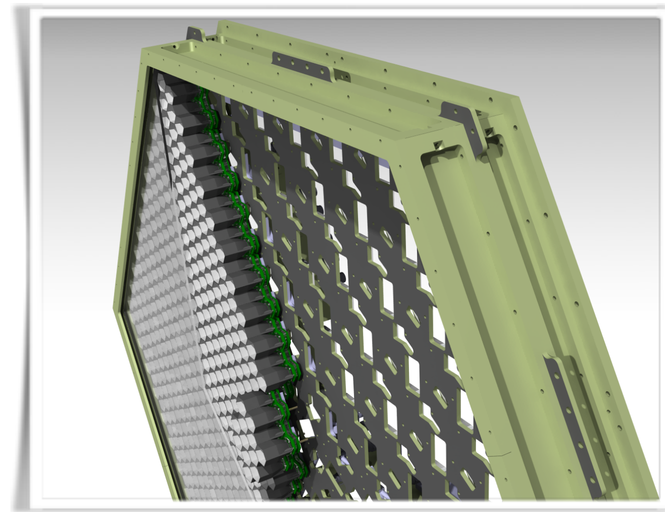


- Sampling rate 250 MHz
- Readout rate: 32 kHz @ 80 ns readout window, no dead-time
- Fully digital trigger and readout (High-speed/High-throughput)
- Serial architecture based on multi-Gigabit links (trigger and ADC readout)
- Trigger path with reconfigurable algorithms and signal preprocessing

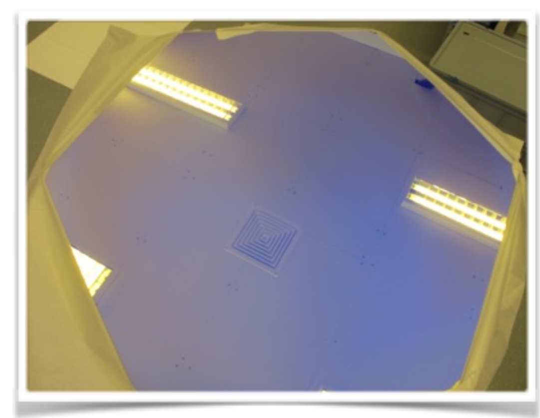
Photo Detection Plane - Overview

- 1296 pixels, 108 modules (12 pixels each)
- Power consumption ~ 500 W
- Total weight 35 kg
- Borofloat entrance window 3.3 mm
  coated with AR filter (Cut-off at 540 nm)
- Aluminum backplate (6 mm) as backbone
  and cold plate for Cooling
- Sensor bias automatically adjusted according
  to temperature





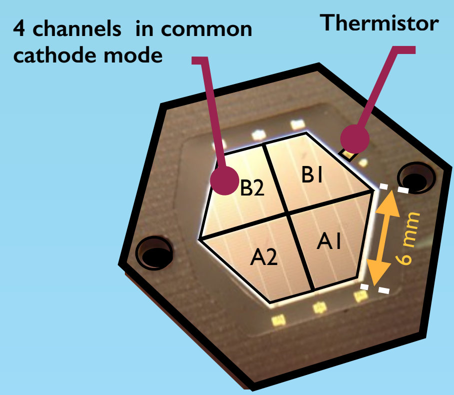
Section of the PDP



Borofloat window

Photo Detection Plane - The Pixels

The sensors



Channels: 4

Area: 23.8 mm²/ch

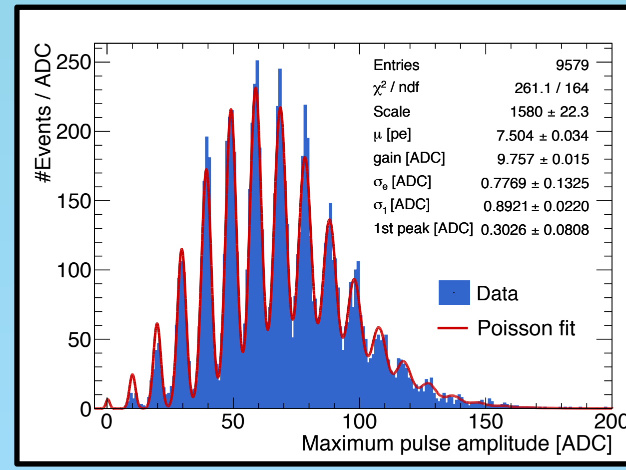
Cell size: 50 µm x 50 µm

Fill factor: 68 %

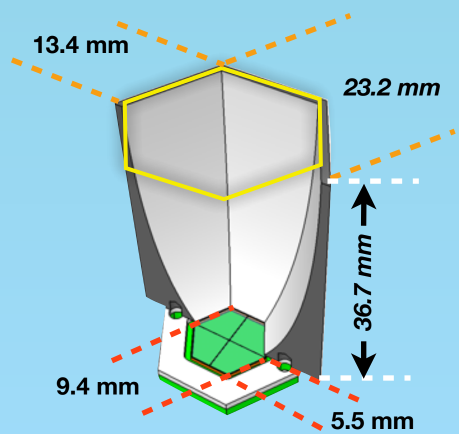
N. pixels: 9210 pixels/ch

Capacitance: 840 pF/ch

DC rate: 1 MHz/ch



The Light Guides

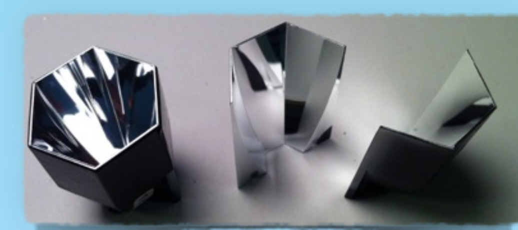


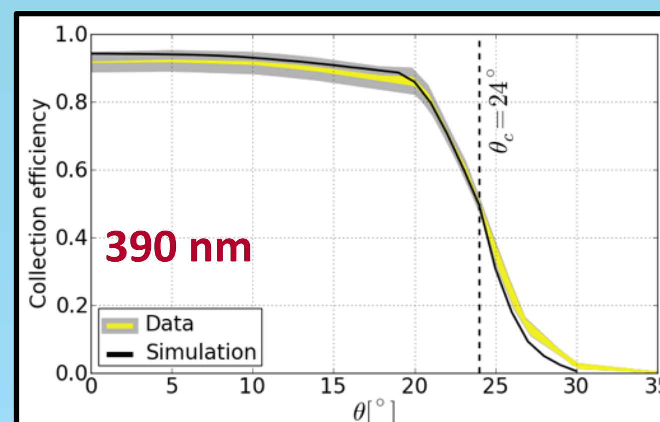
Point Spread Function

- ➡ *Angular pixel size (0.25°)*
- ➡ *Top Physical size = 23.2 mm*

f/D & Camera Diameter

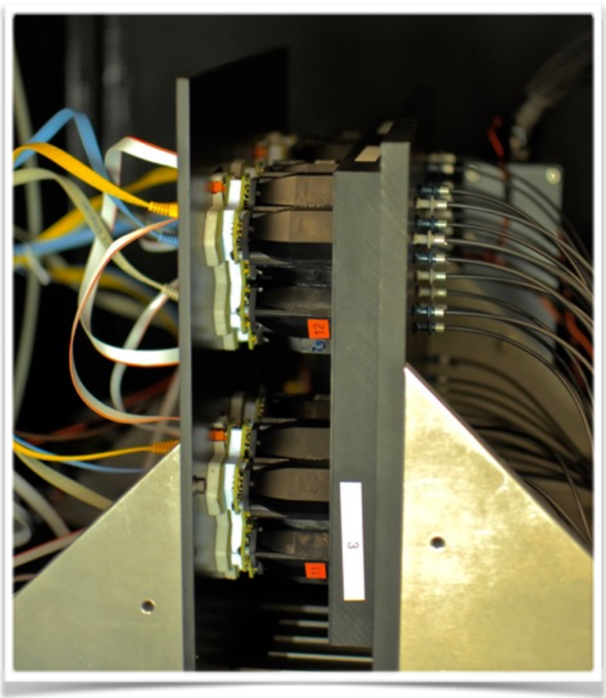
- ➡ *Cut-off Angle (24°)*
- ➡ *Cone Height = 36.7 mm*



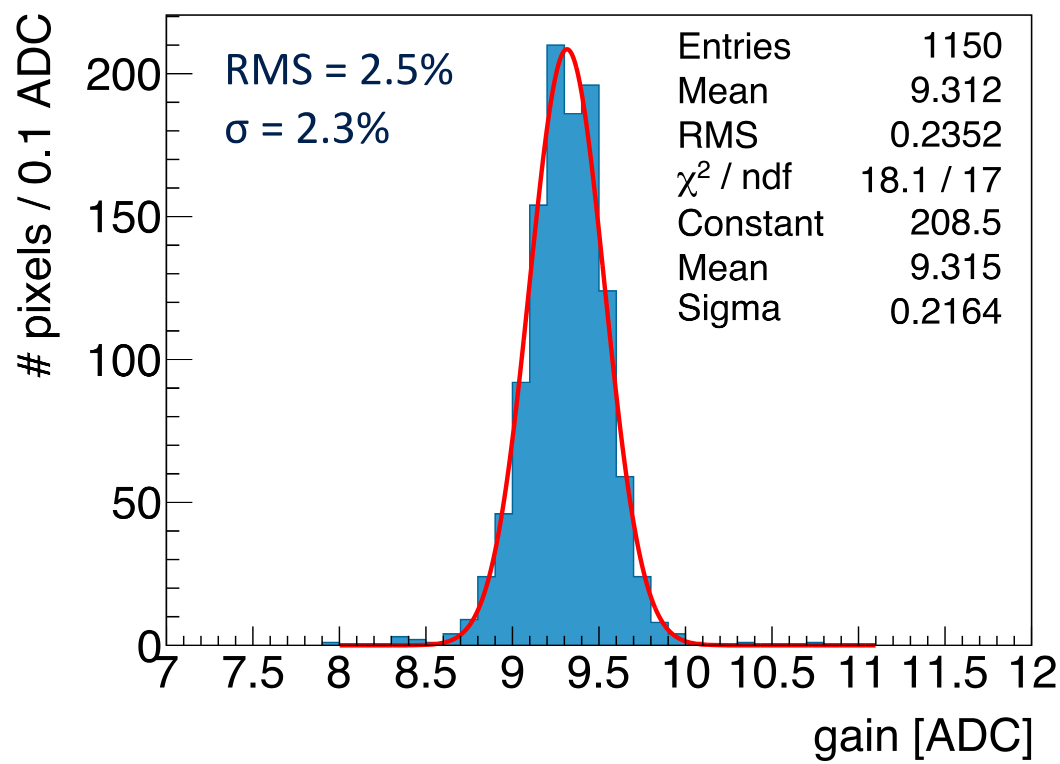


Performance - Module testing and calibration

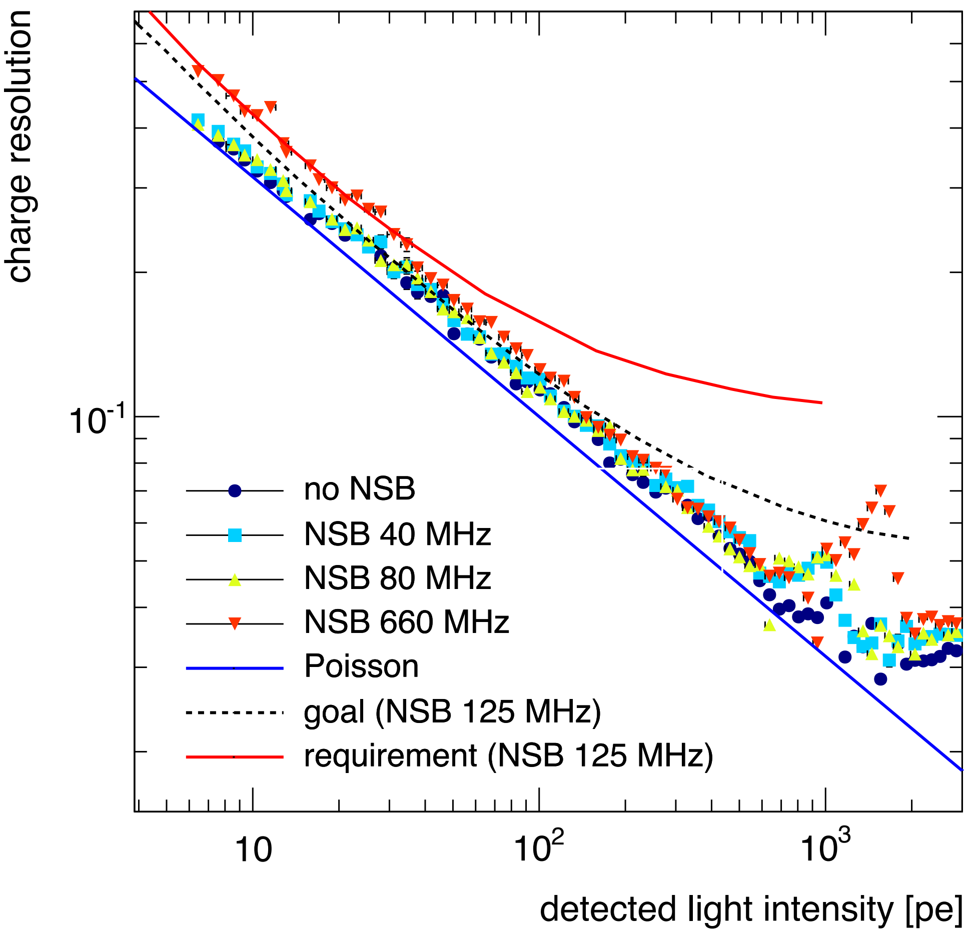
- Systematic characterization of all modules
- Measurement of critical parameters for calibration
- All data stored in reports and later in data base
- Mean optical cross talk 7.7 %
- Mean dark count rate 2.8 MHz



Gain



Performance - Charge resolution measurement

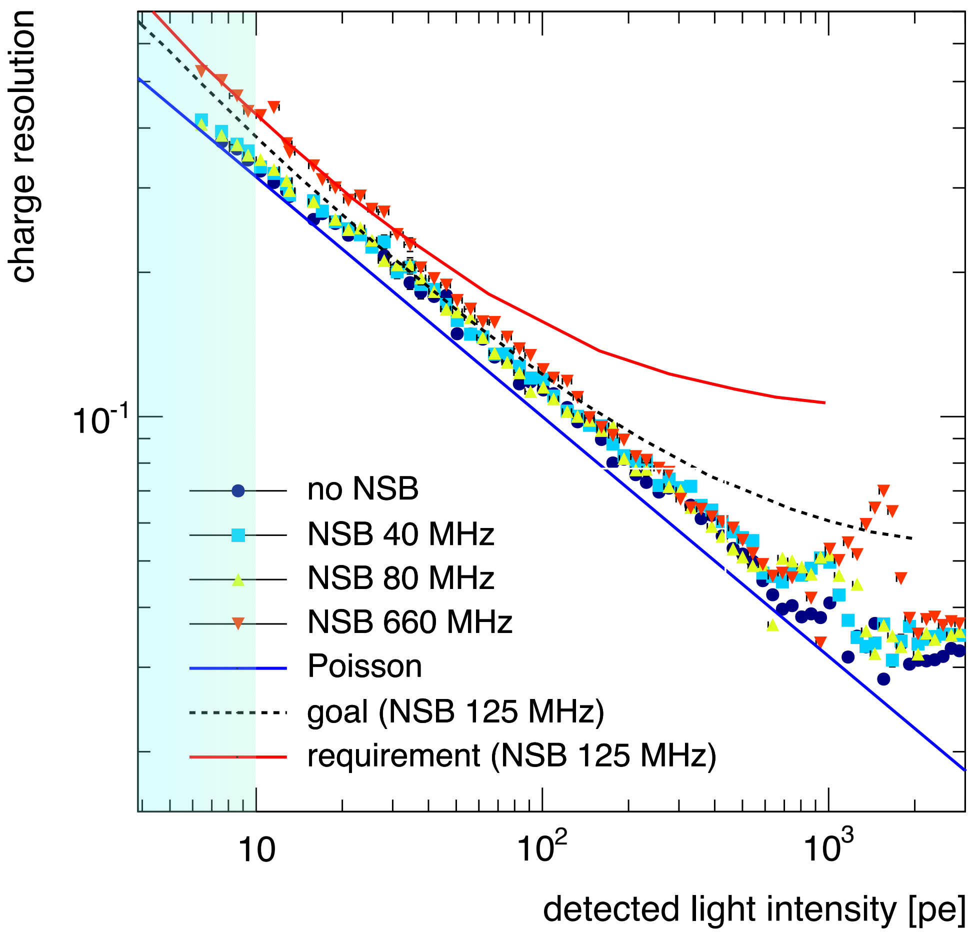


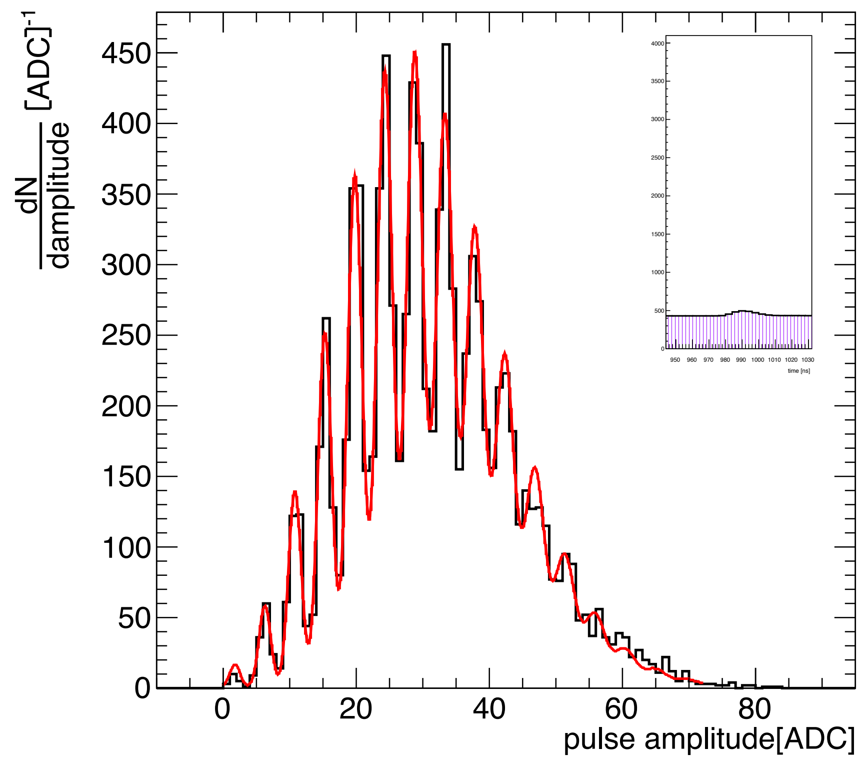
- The charge resolution is the key parameter to assess quality of image reconstruction
- Measurement performed injecting both pulsed and continuous light

➡ **Below CTA goals for dark night and below requirements for half moon conditions (660 MHz/pixel)**

Performance - Charge resolution measurement

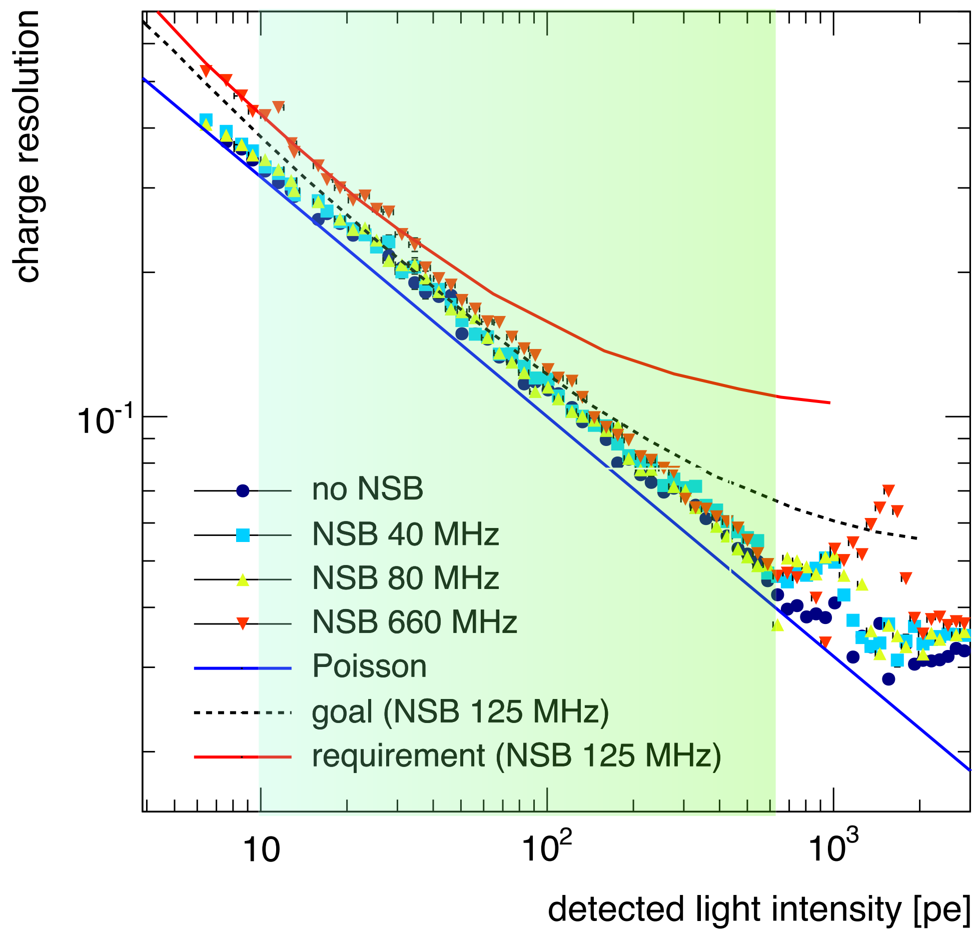
Linear
low light

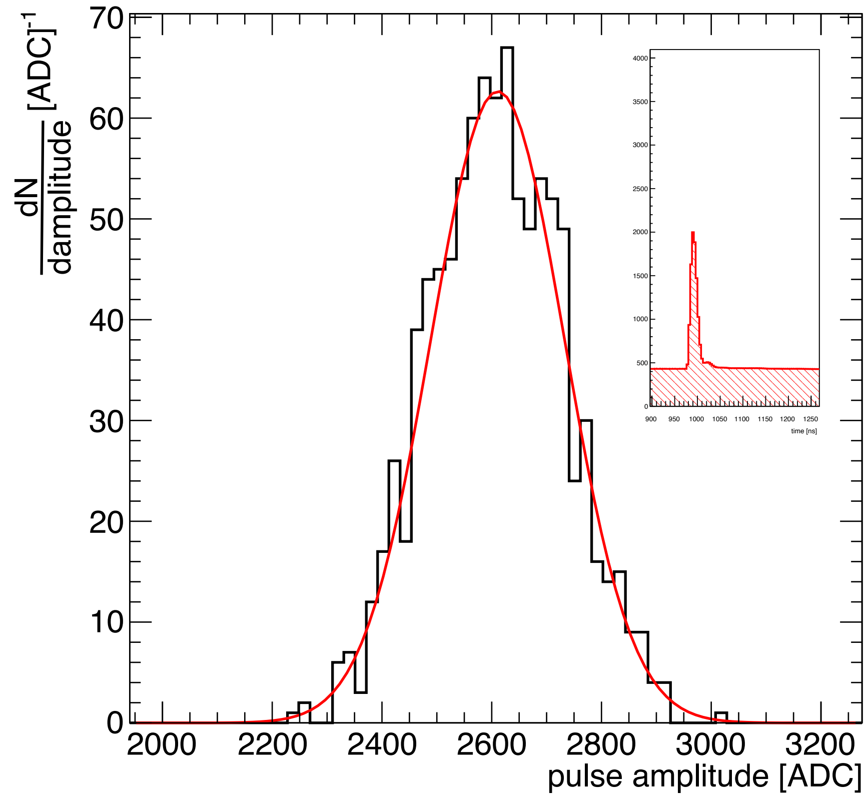




Performance - Charge resolution measurement

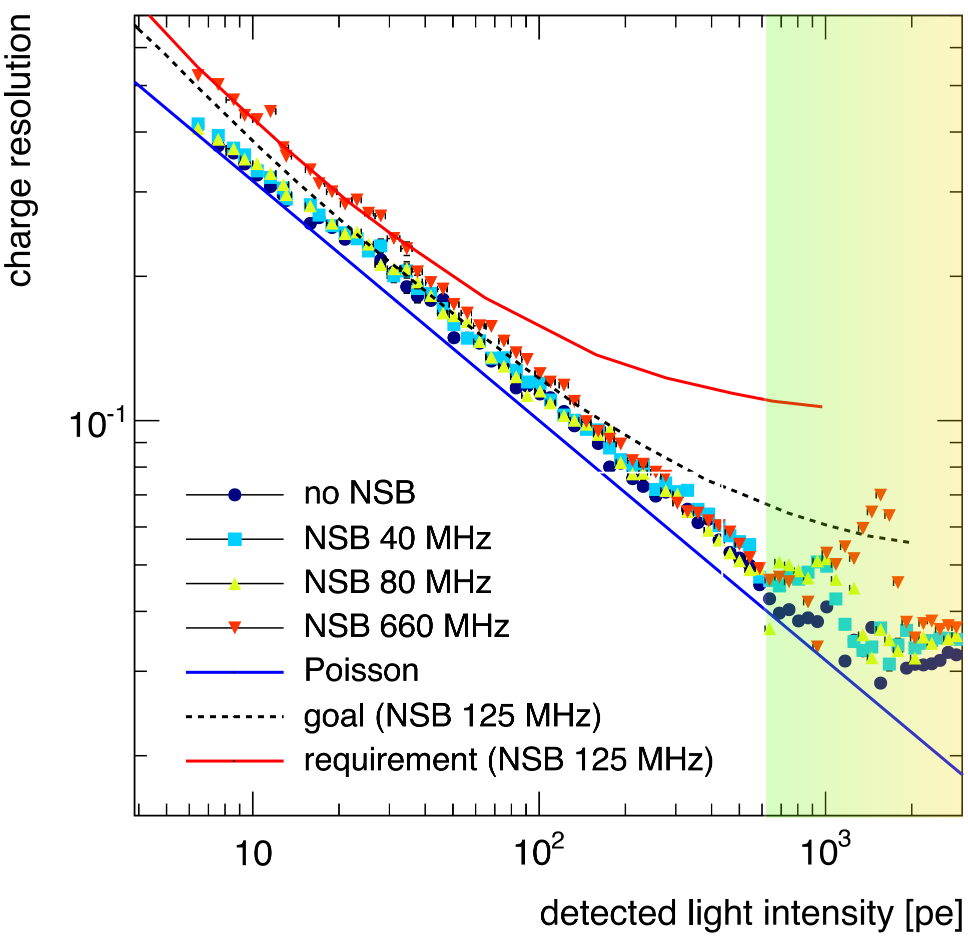
Linear
medium light

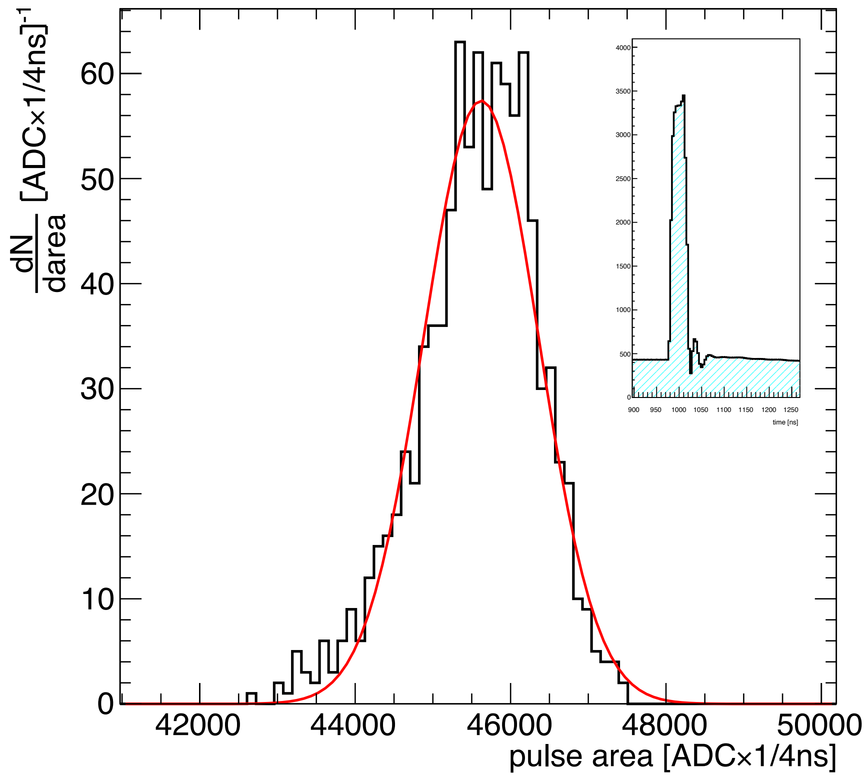




Performance - Charge resolution measurement

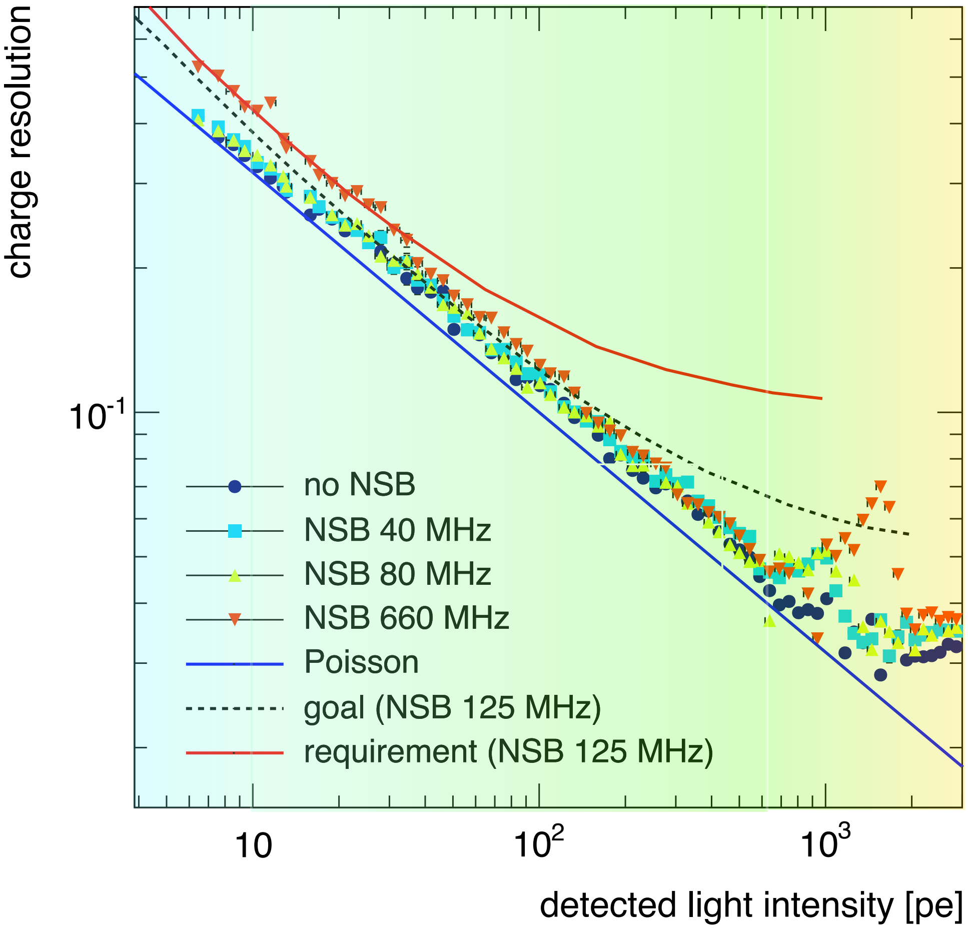
Saturation
high light



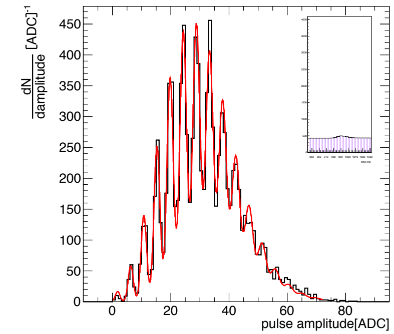


Performance - Charge resolution measurement

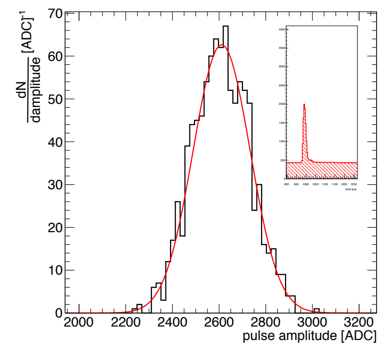
Linear low light	Linear medium light	Saturation high light



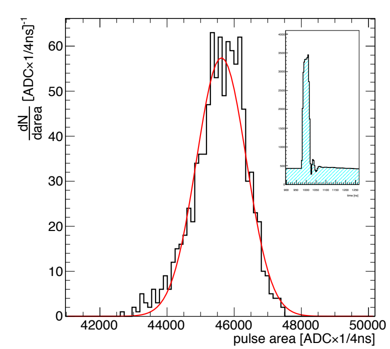
Linear low light

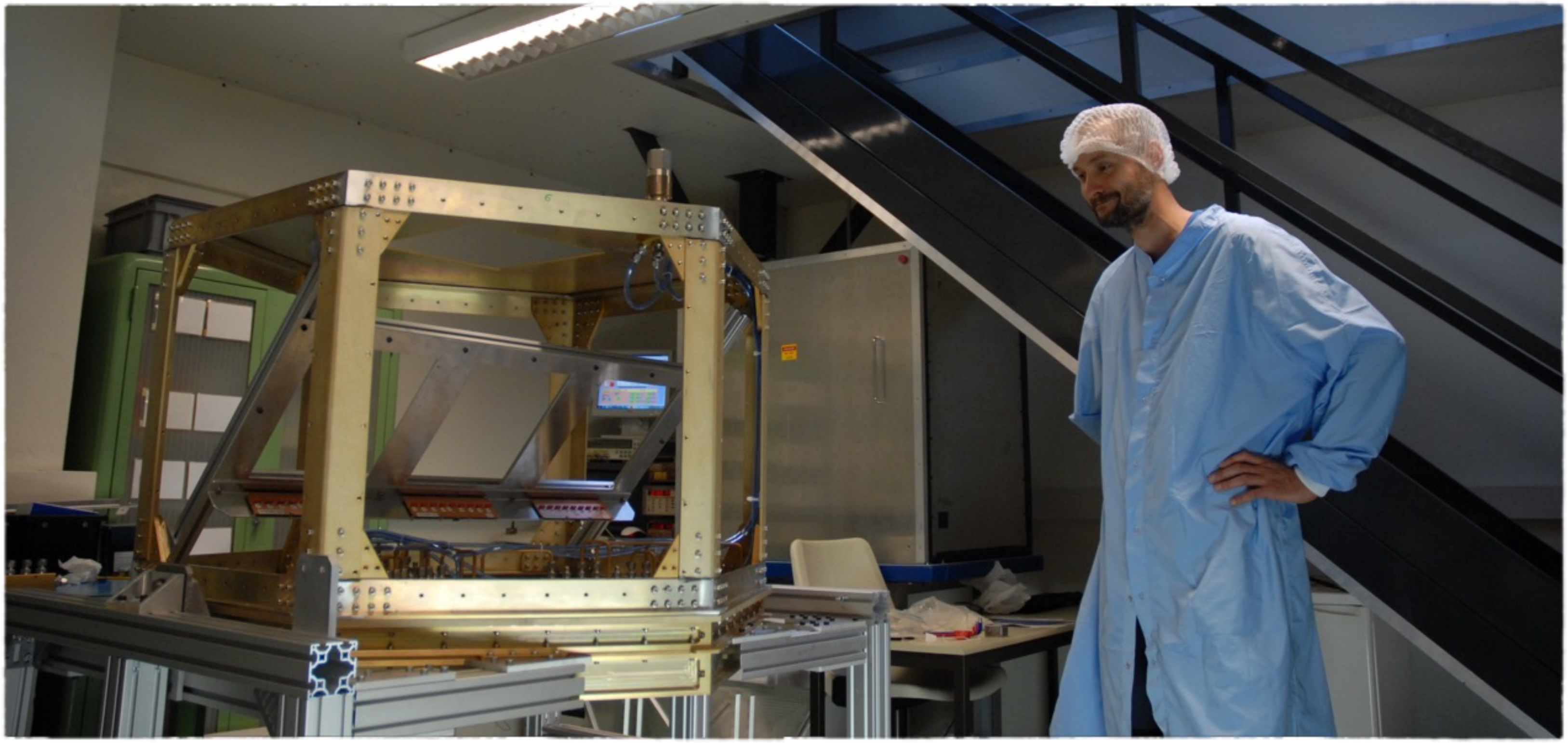


Linear medium light



Saturation high light





The commissioning phase

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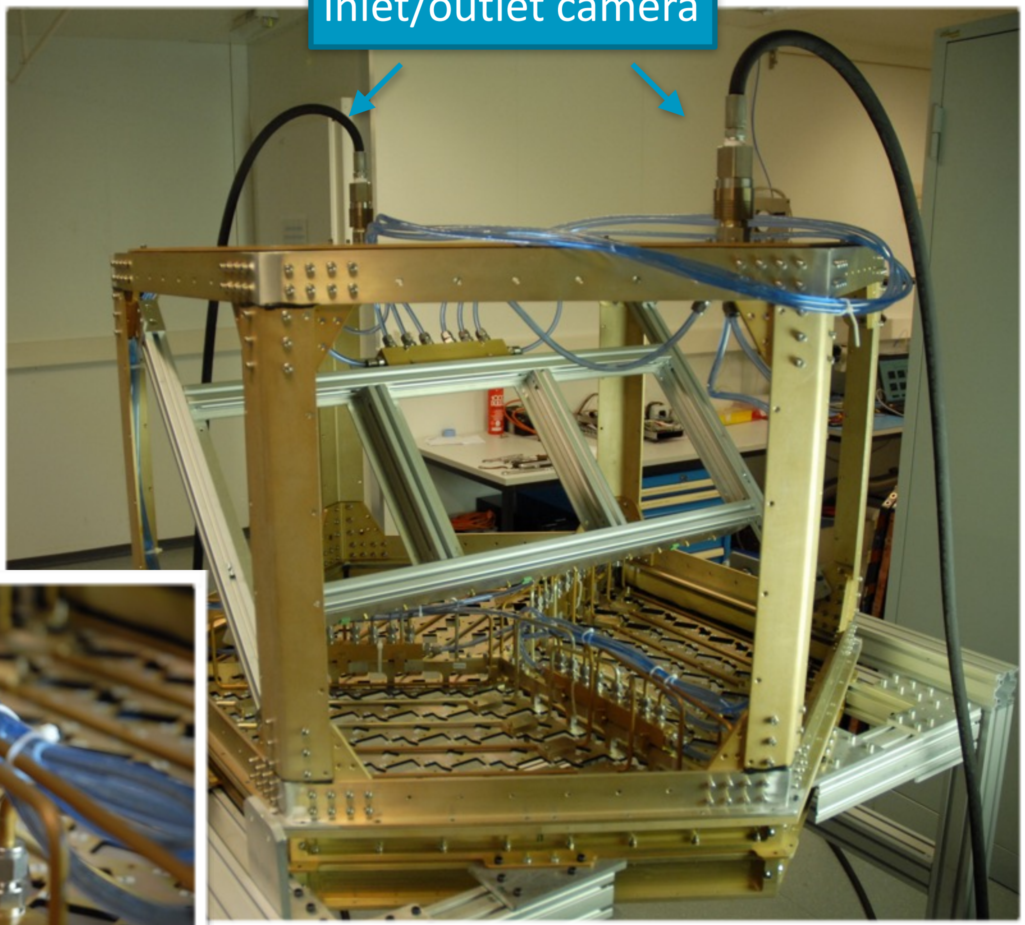
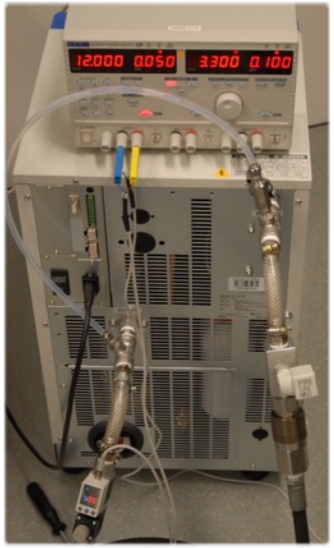
Assembly - Cooling system

inlet/outlet camera

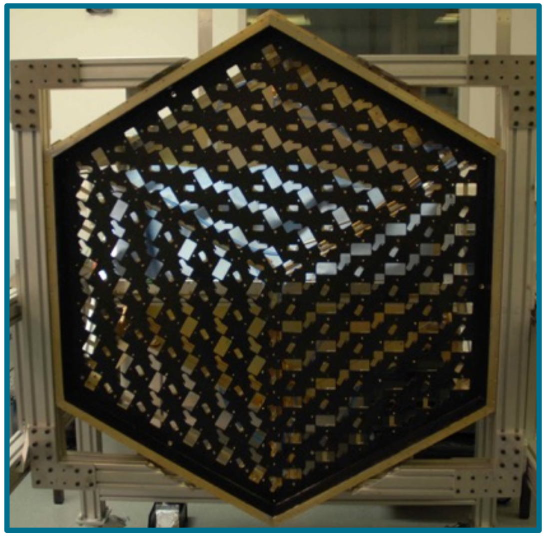


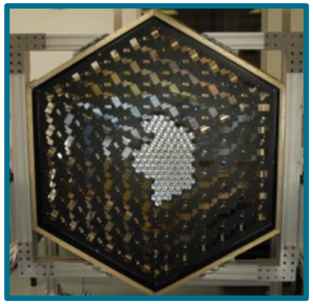
Sector manifold

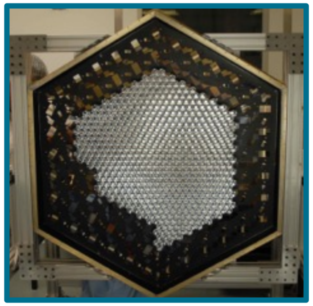


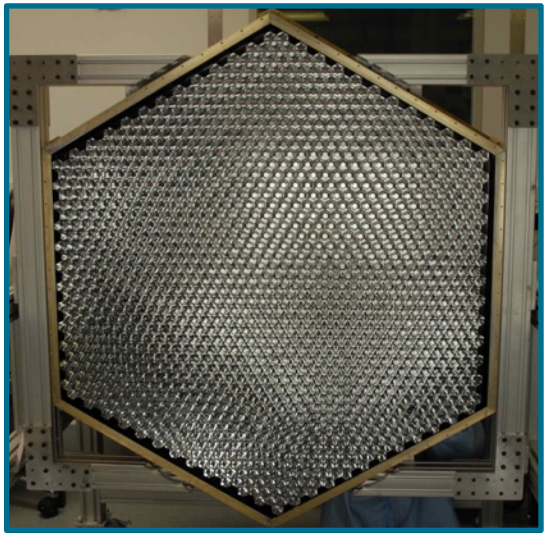
Chiller

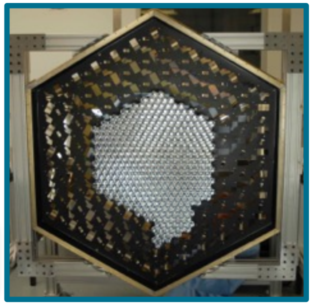
Assembly - Photo Detection Plane

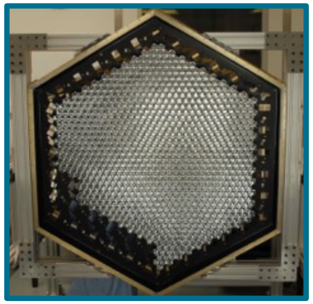






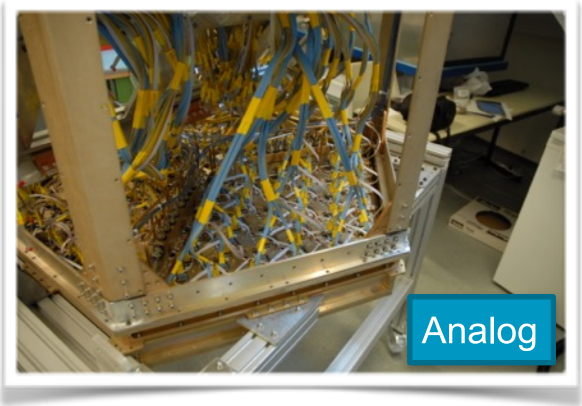






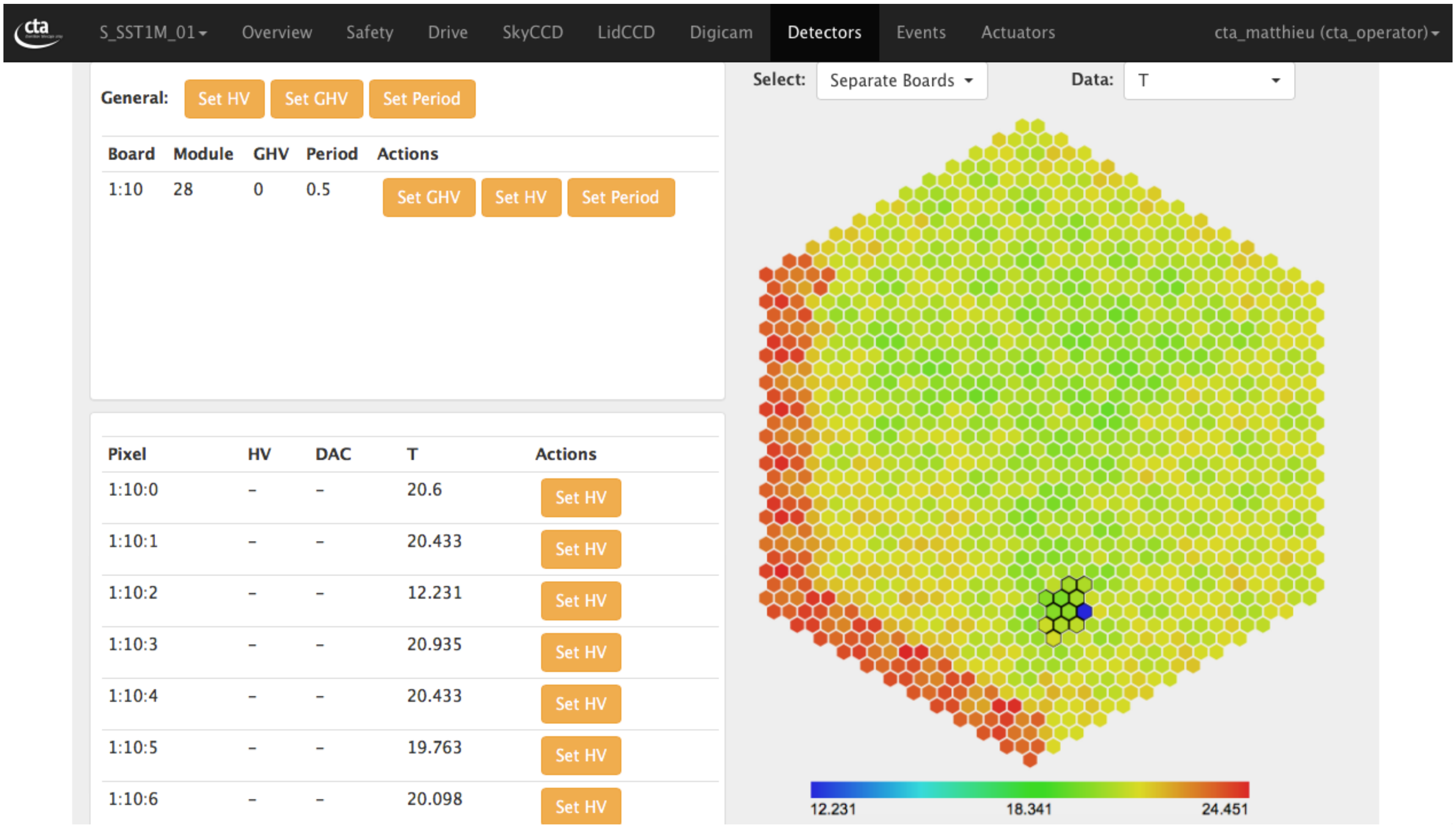
1 day of work to assemble full PDP

1 day for cabling

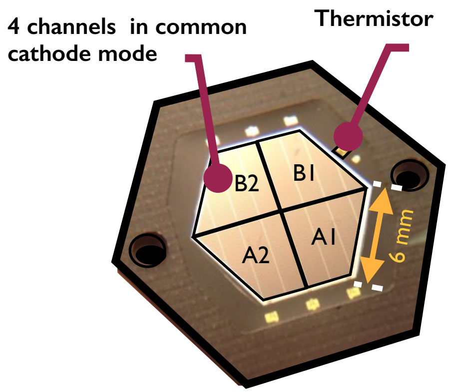


Commissioning - Web GUI

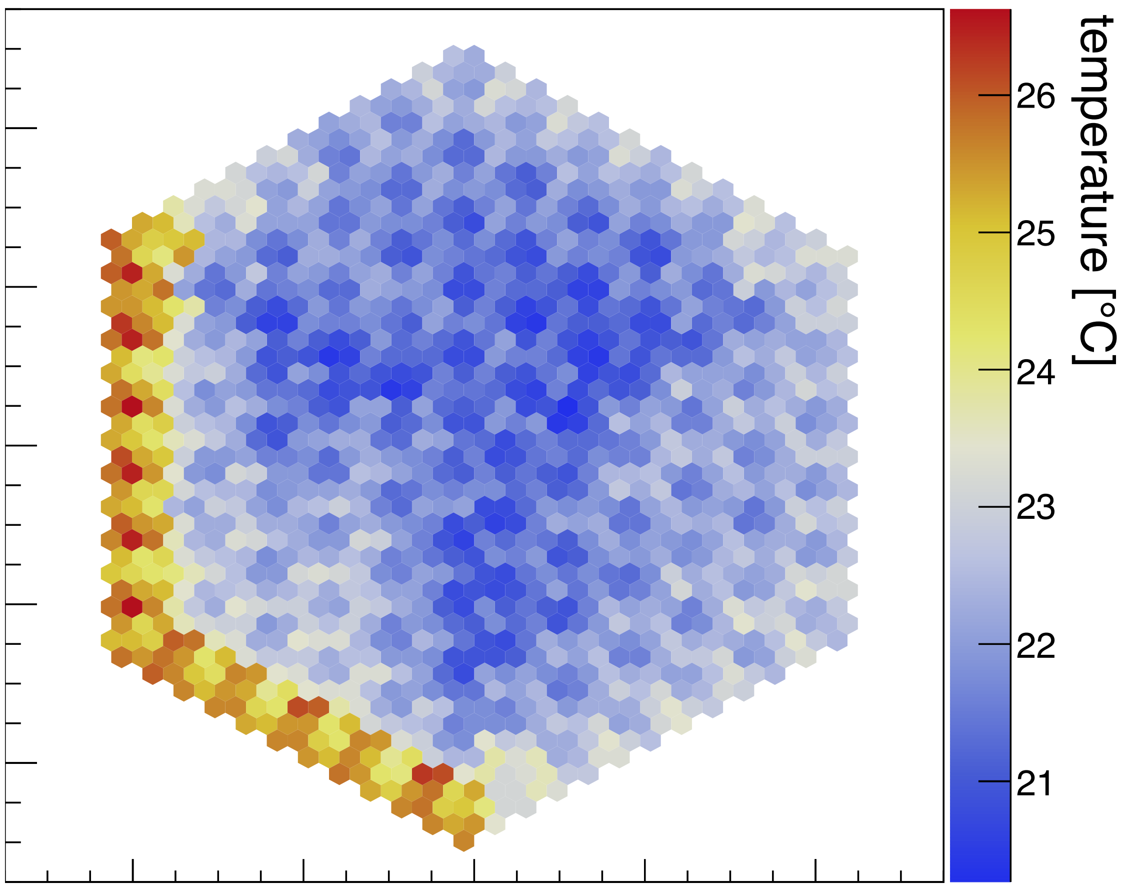
Monitor and control slow control parameters (T, HV, …)



Commissioning - Design validation

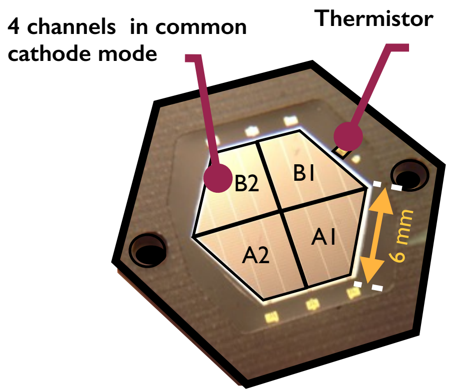


Temperature map



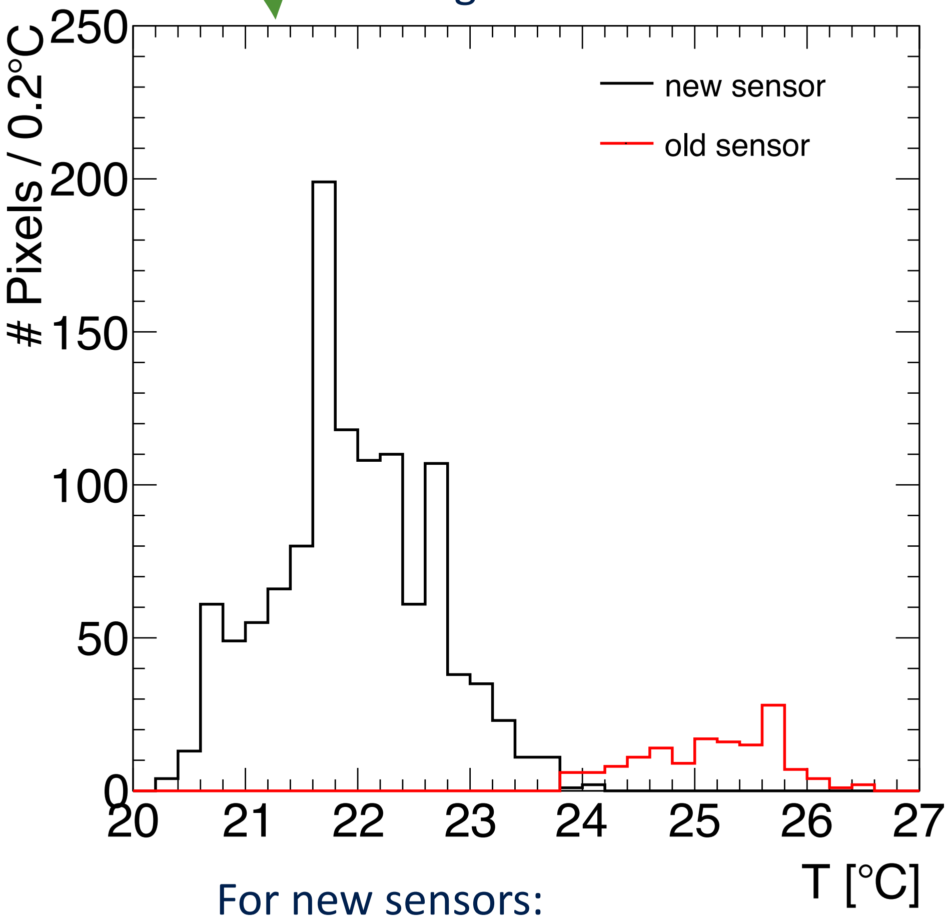
- Using the thermistor embedded in the sensor package, the temperature map of the camera is produced
- The warmer region is composed of modules using different sensors and different electronics which is more power consuming

Commissioning - Design validation



- Using the thermistor embedded in the sensor package, the temperature map of the camera is produced
- The warmer region is composed of modules using different sensors and different electronics which is more power consuming

✓ Cooling validated



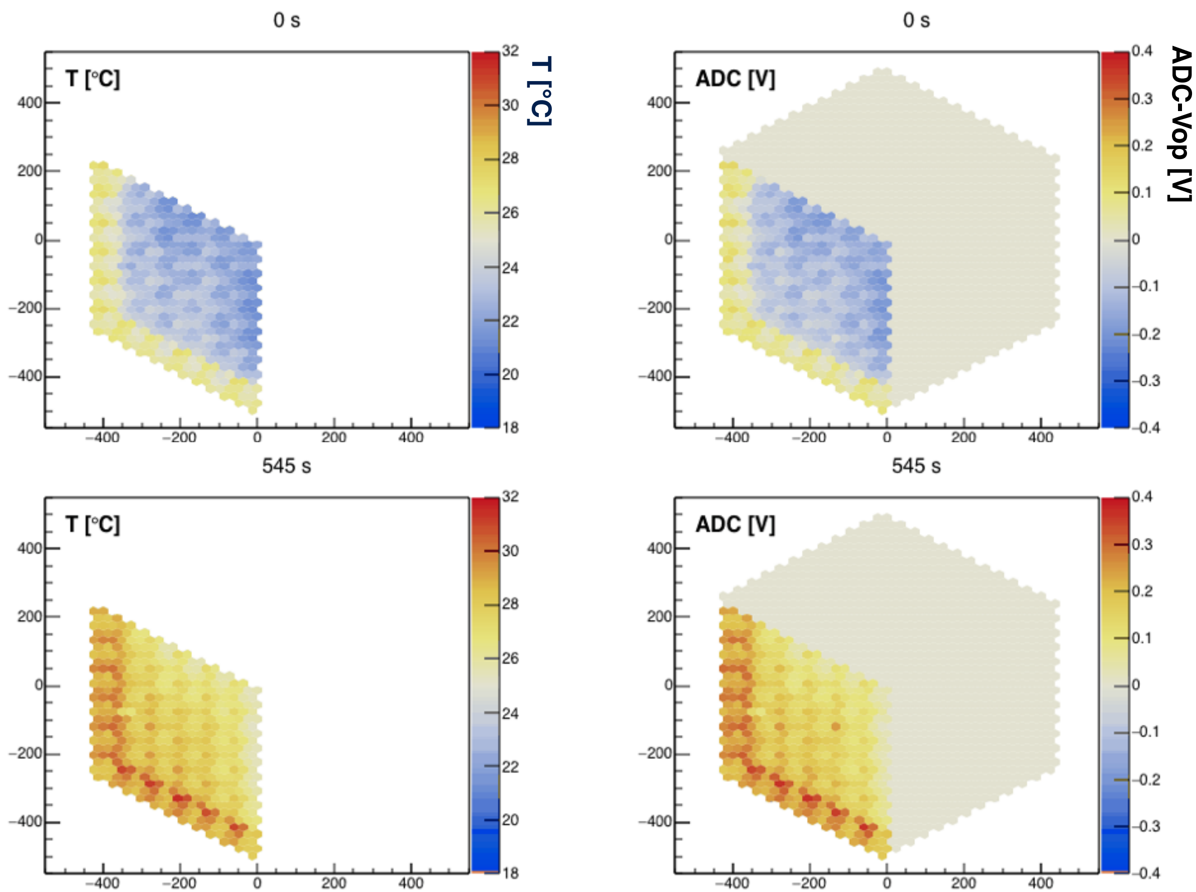
For new sensors:

- Temperature < 25 ℃
- Non uniformity < 4 ℃

Commissioning - Design validation

Cooling ON

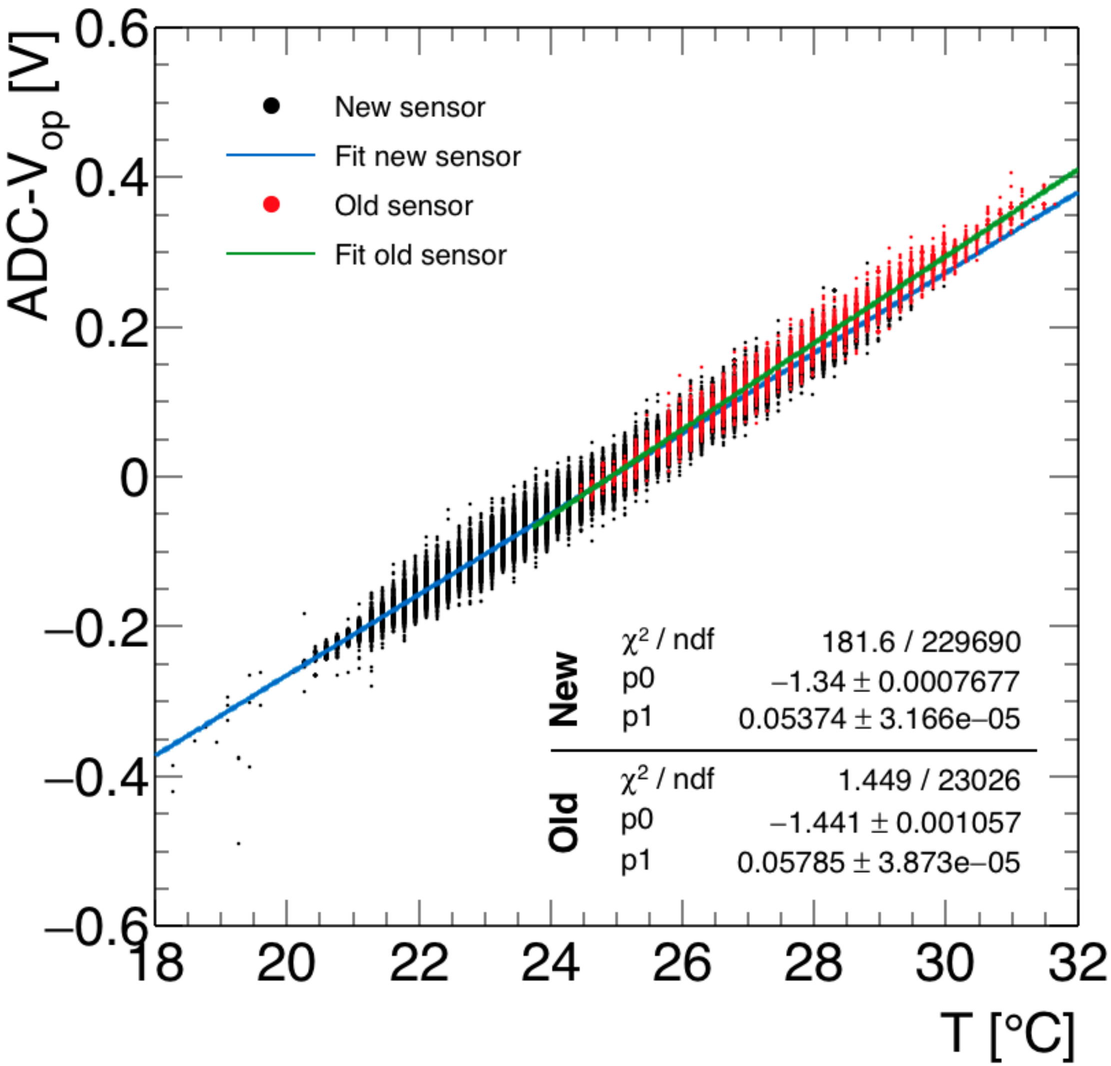
Cooling OFF
after 9 min



Sectors monitored one by one for these tests:

- Chiller turned off to force temperature variation
- The bias voltage measured follows the temperature variation as expected

Commissioning - Design validation



✓ Slow control and communication validated

Control:
- ✓ Enable boost for bias
- ✓ Activate bias voltage
- ✓ Reference voltage and temperature setting
- ✓ Temperature variation factor

Monitoring of:
- ✓ Temperature and bias voltage
- ✓ Compensation loop

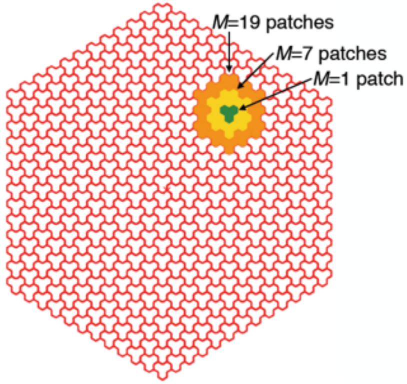
Simulation

Lot of effort to have a simulation (CARE) which better reproduces the real camera architecture:

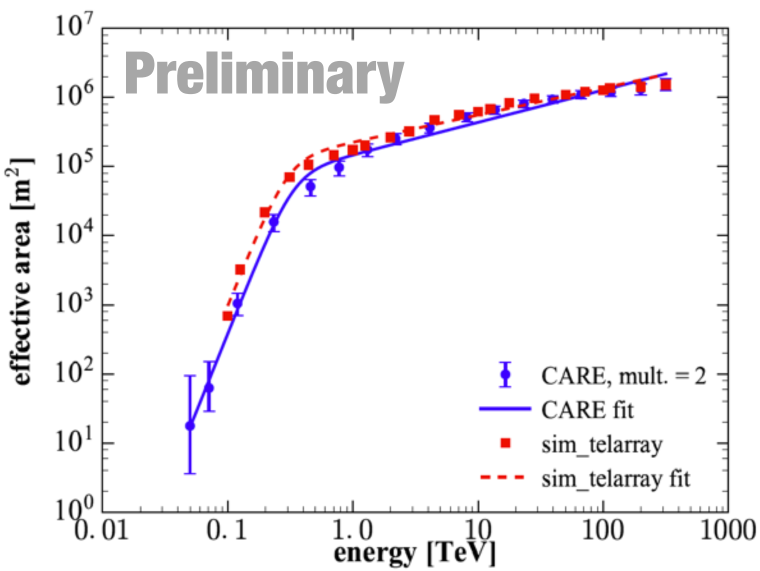
➡ Validated against standard simulation tools

➡ Now working on trigger optimization & readout scheme:

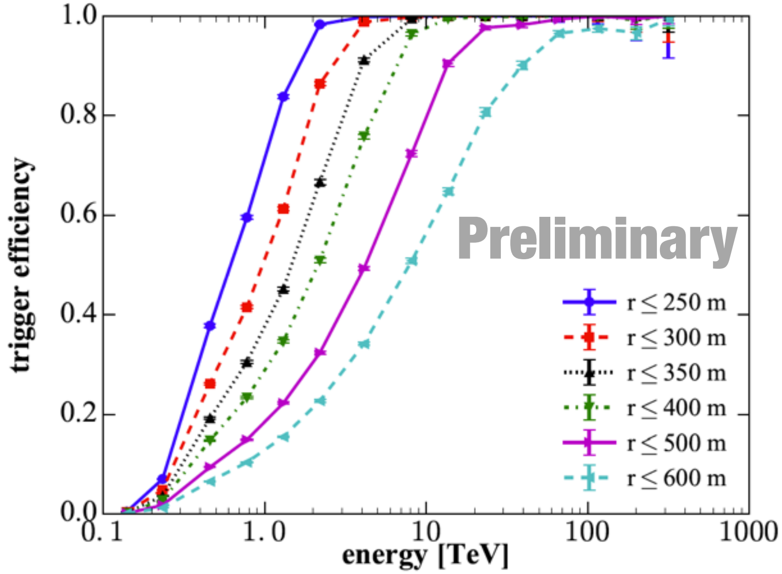
- varying number of patches
- trigger threshold
- pattern geometry



Validation of CARE against sim_telarray



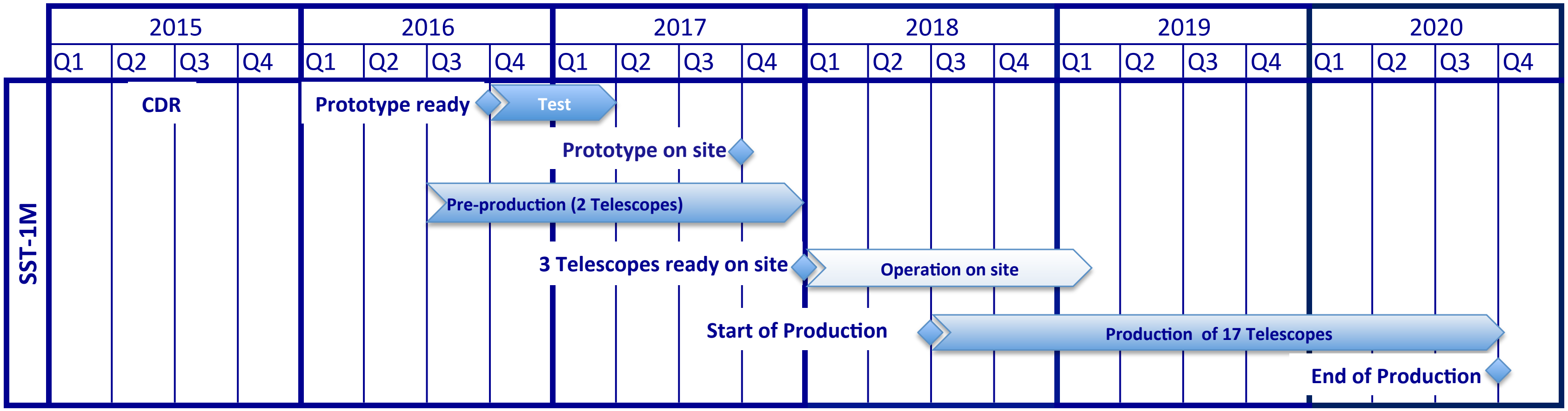
Trigger efficiency with custom topology



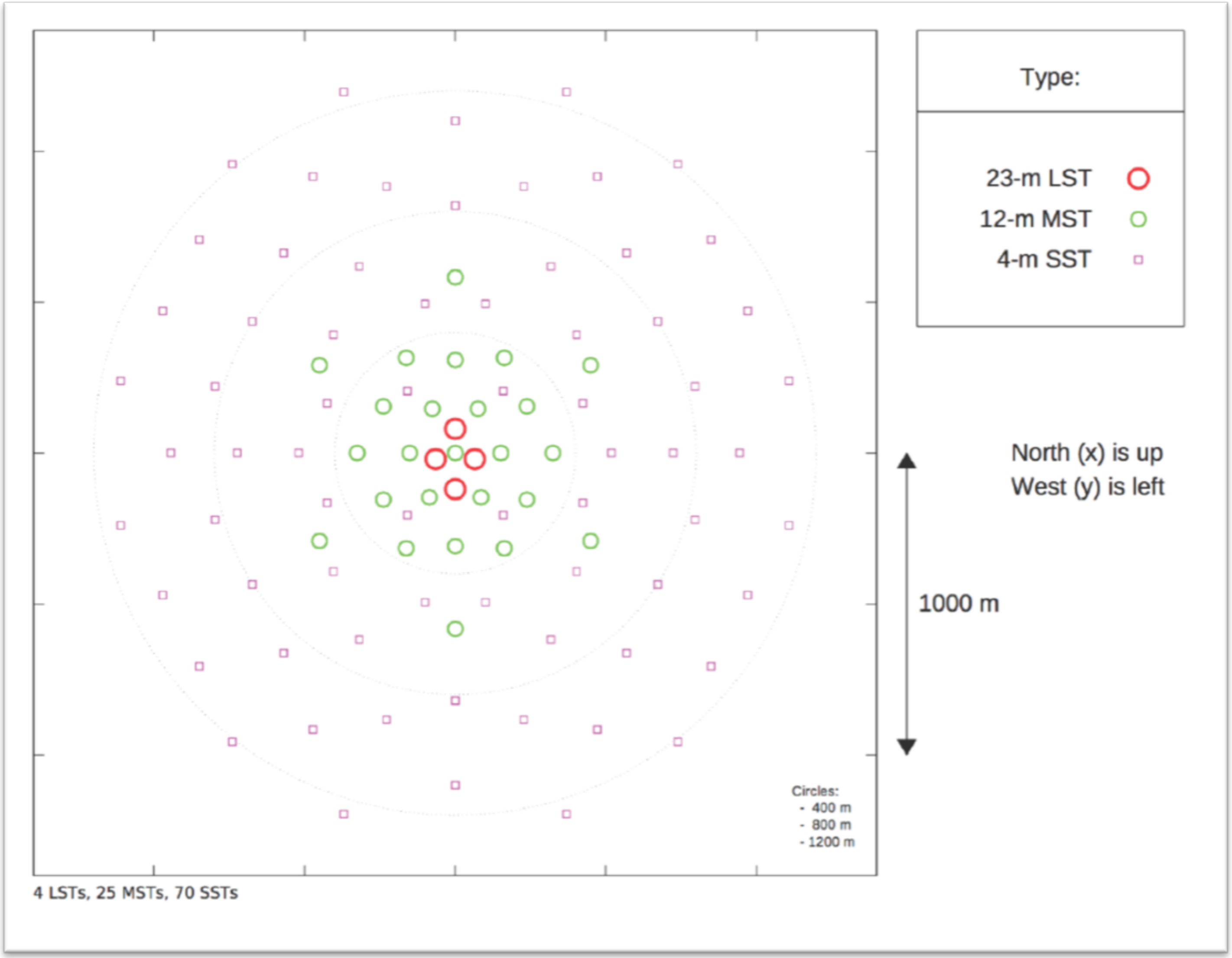
Summary

- Commissioning of the camera is ongoing
- Full readout chain to be tested during the two coming weeks
- Camera ready in October
- Telescope prototype should be completed by November followed by a long and intense operation phase
- Next phase will be the pre-production (2 additional telescopes)
  - Due to the targeted production scale, the detector R&D phase has followed an industrial production flow with solid work on specification documents (design, tests,…) prior to implementation

Back-up slides

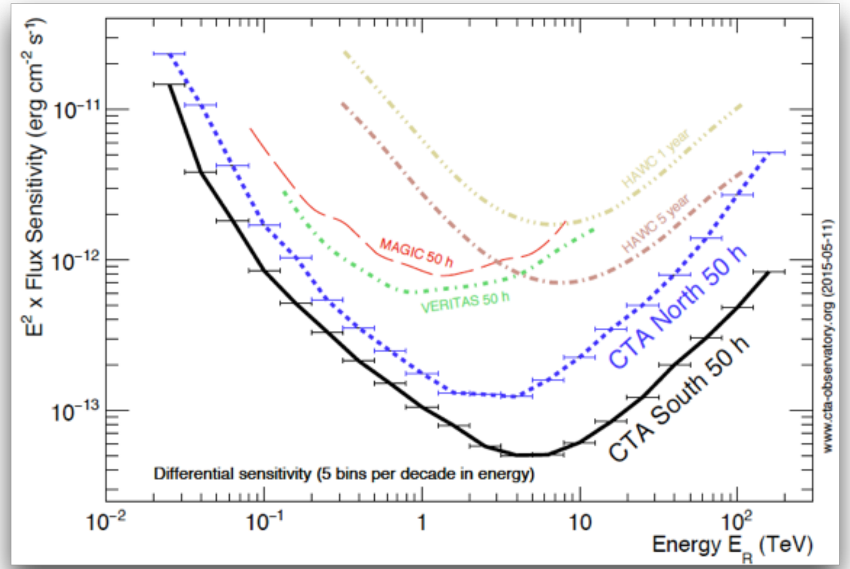


The Cherenkov Telescope Array - Layout

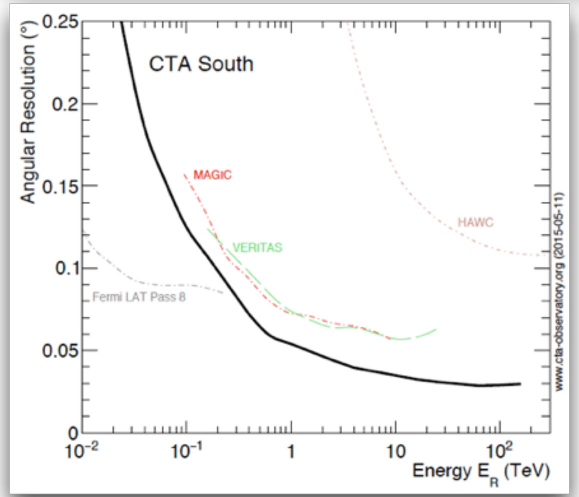


credits: CTA consortium

The Cherenkov Telescope Array - Performance

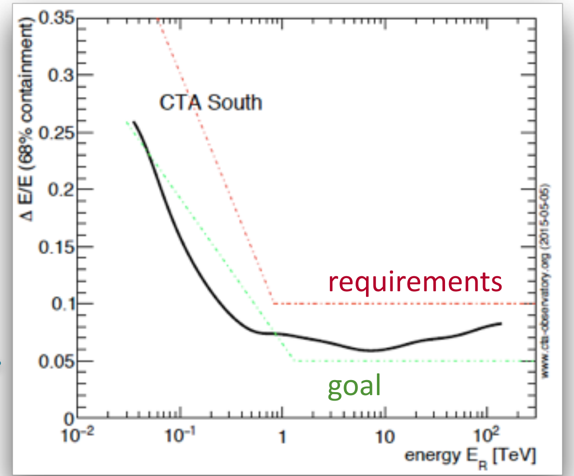


- A factor of 5-10 improvement in sensitivity in the domain of about 100 GeV to some 10 TeV
- Extension of the accessible energy range from well below 100 GeV to above 100 TeV.



Angular resolution

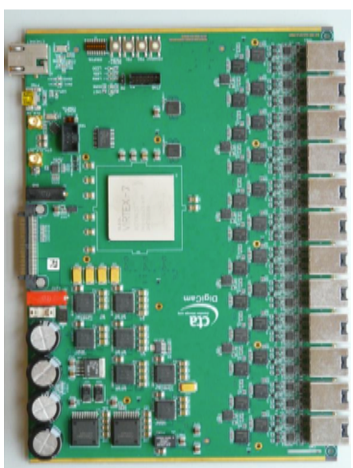
Energy resolution



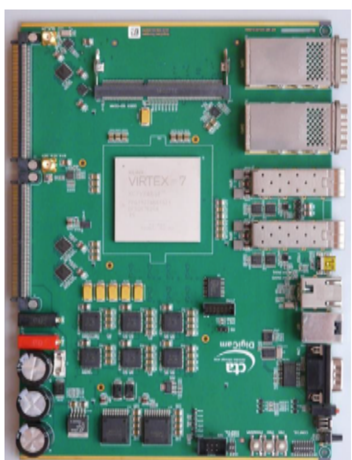
credits: CTA consortium

Latest activities - DigiCam testing

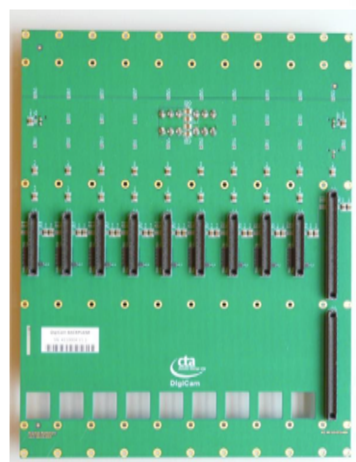
- All boards produced, tested and calibrated
- Final developments of the FPGA firmware (FADC and trigger boards) and hardware cross check
- Integration and connection to PDP end of August



FADC board (x27)

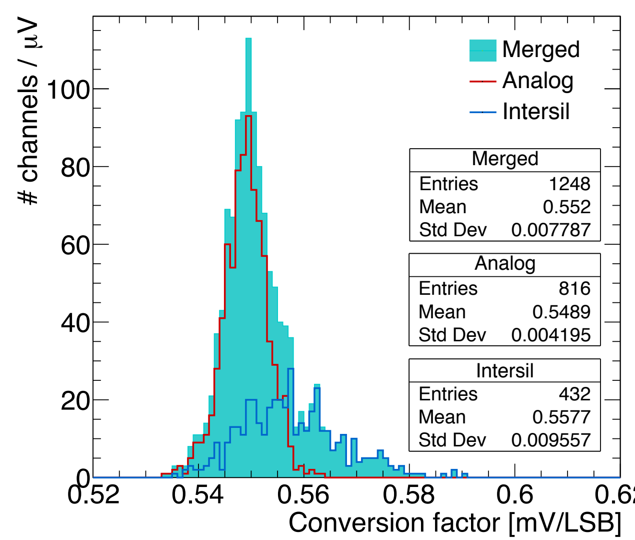


Trigger board (x3)



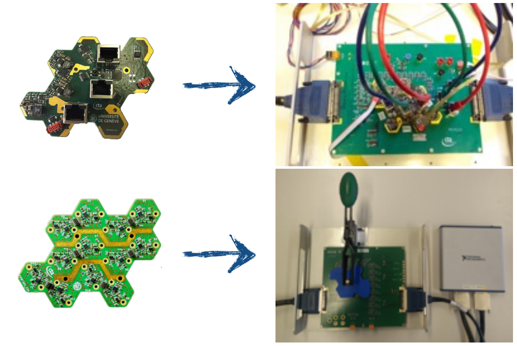
Backplane (x3)

FADC gains before equalization



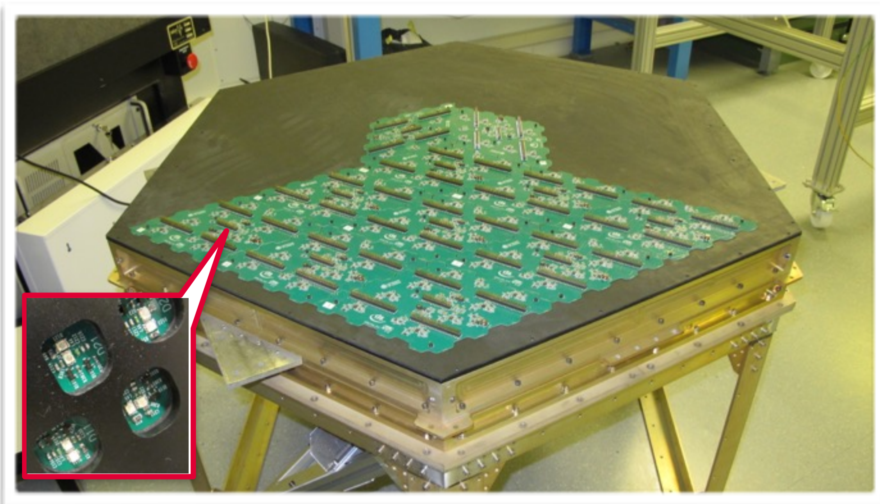
From Prototype to Series production

- Already at the prototype phase, solutions to allow for industrial scale production, testing, and calibrations have been developed:
  - Every step of the assembly phase is documented in order to be repeated
  - All fabrication processes can be performed at industrial scale (e.g. injection molding for light guides)
  - Test, calibration of front-end boards and digital boards done at the manufacturer site
  - Full camera calibration strategy using dedicated setup (e.g. camera test setup)



Production assembly

Functional tests in situ



Camera test setup (1AC+1DC led / pixel)