New CSC Readout: NRC Firmware

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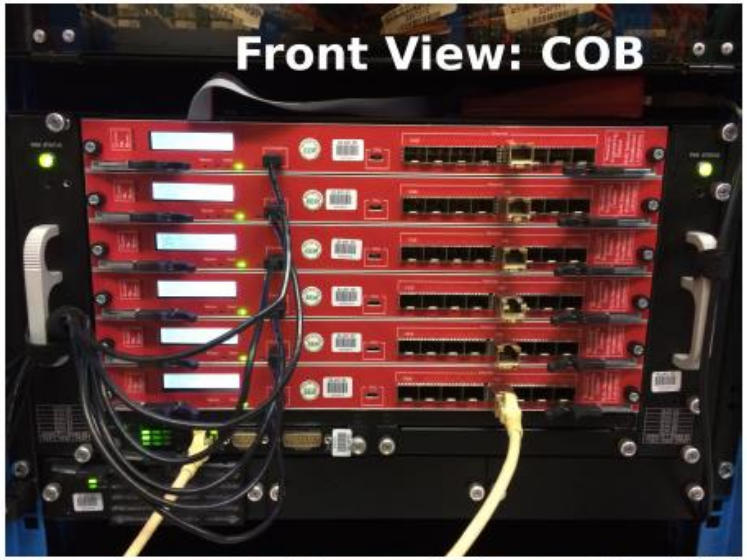
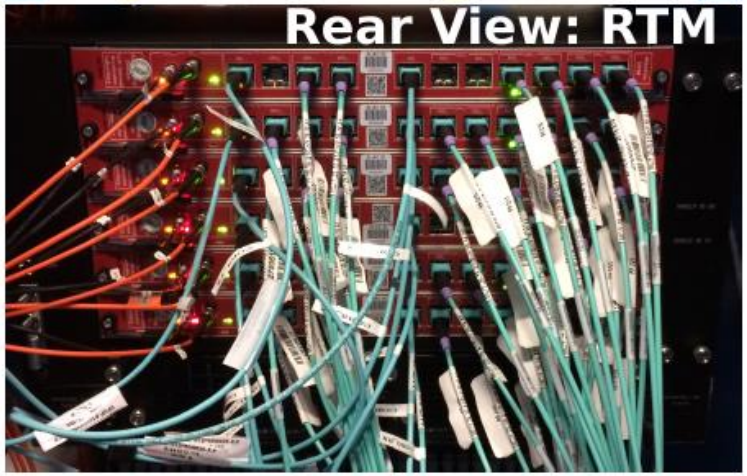
Office of Science

SLAC NATIONAL ACCELERATOR LABORATORY

Outline

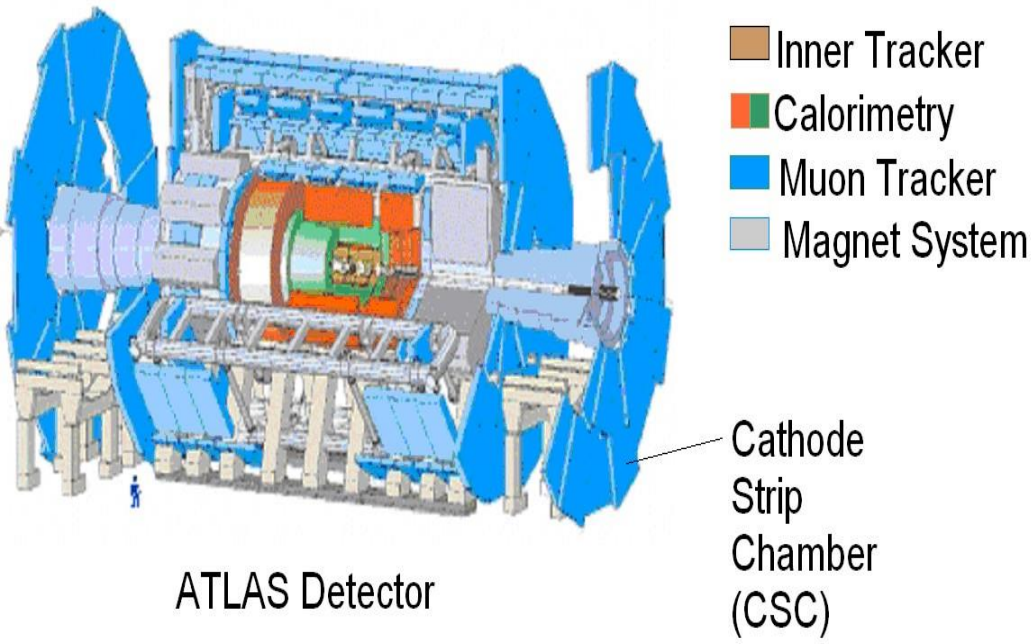
- Discuss the timing and clock distribution
- BUSY generation
- Firmware data flow and back pressure flow control
- Feature Extraction (FEX)

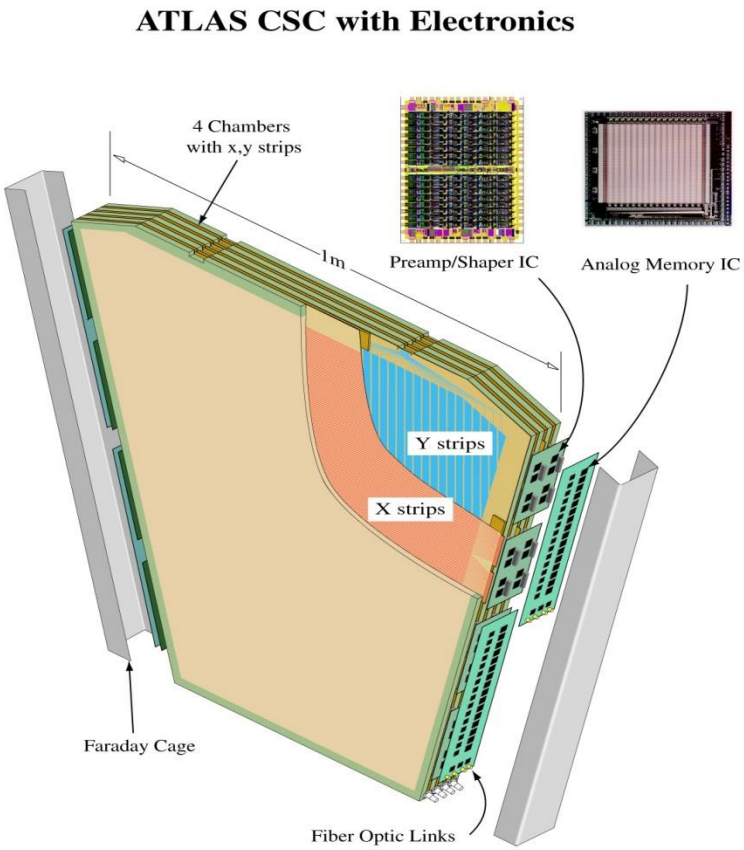




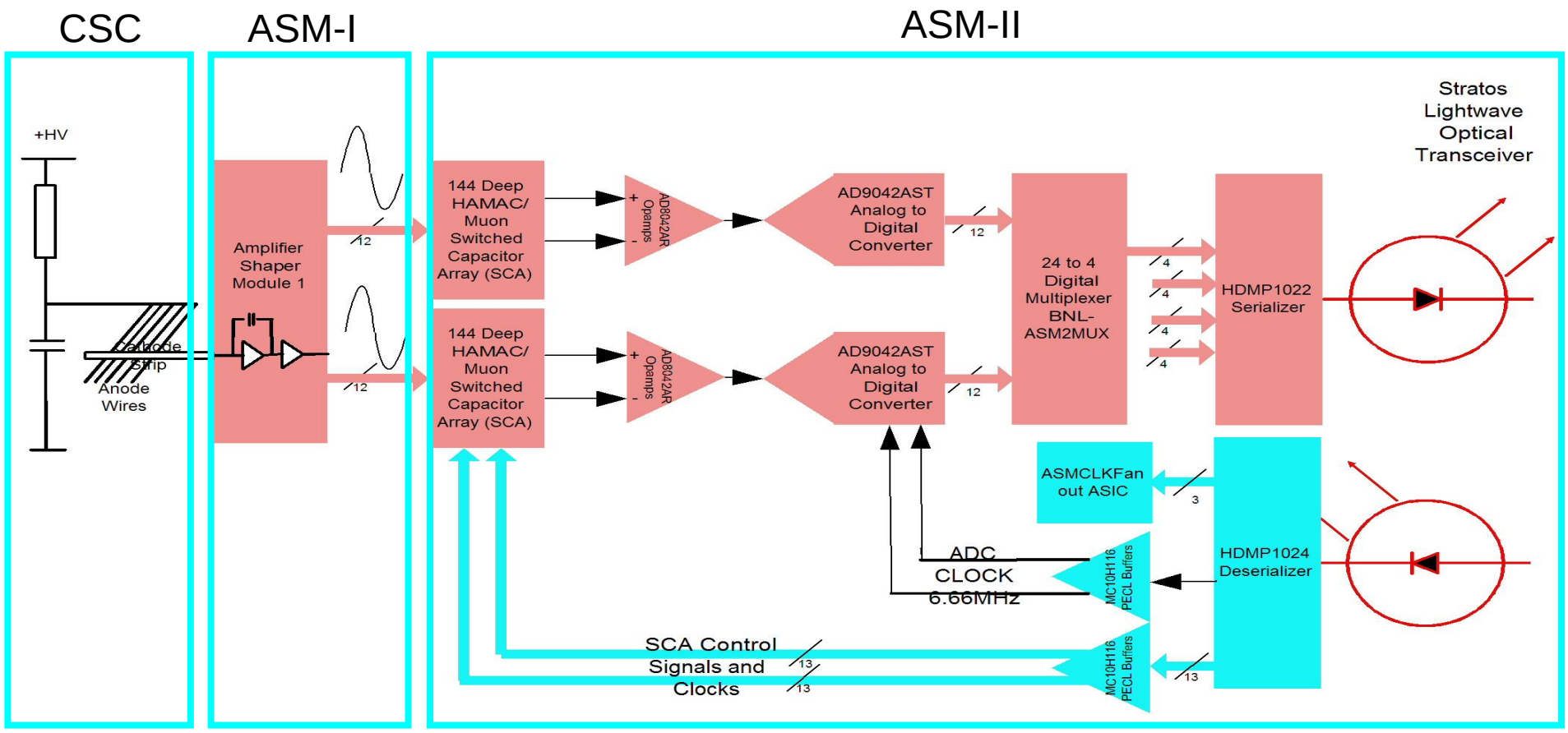
Introduction to Cathode Strip Chamber (CSC)

- Detector for measuring high momentum muons in the extreme forward region of ATLAS





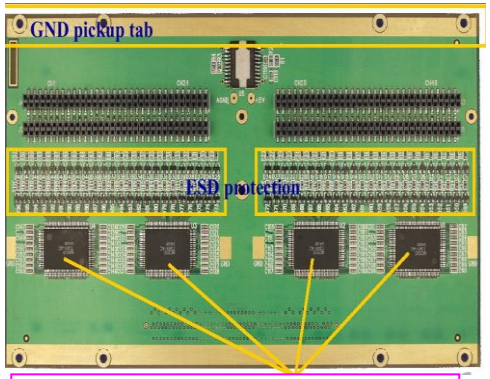
CSC: Front End Electronics

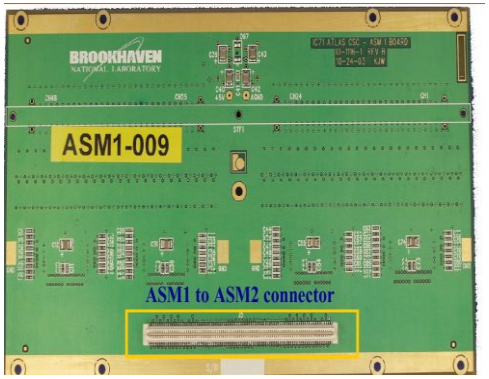


CSC: Front End Electronics

- 2 ASM-I and 1 ASM-II make one pack (ASMPack)
- 5 ASM packs per chamber
  - 4 x-strip (2 per side)
  - 1 y-strip
- 160 packs for the system (128 x-strip, 32 y-strip)
- 192 Channels per pack (30,720 total channels)

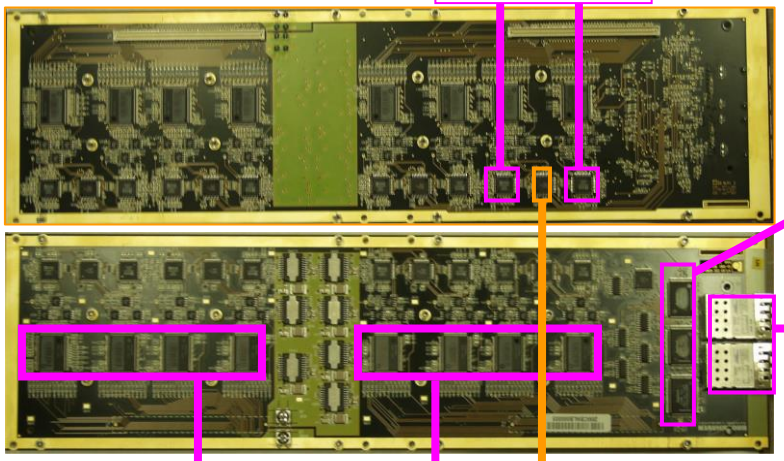
ASM-I





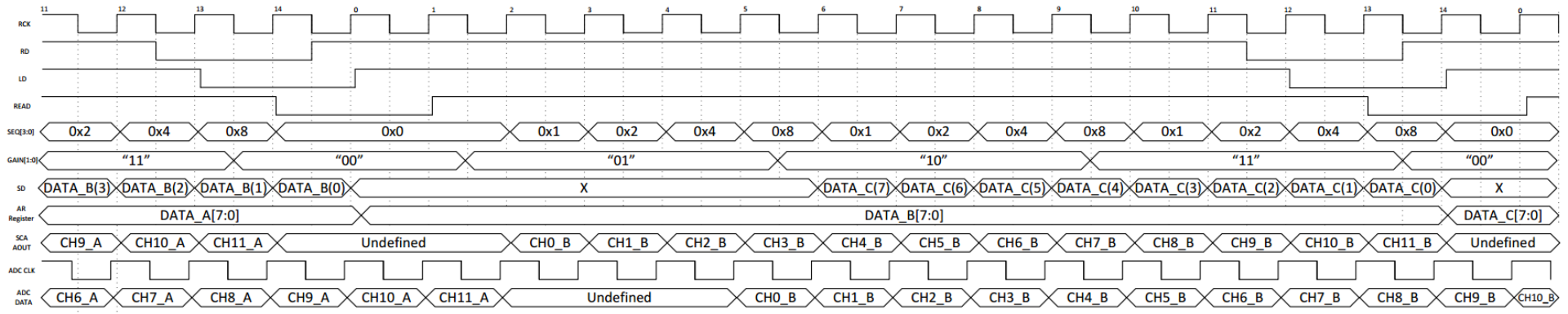
Preamp/Shaper ASIC

ASM-II



FEB Limitation

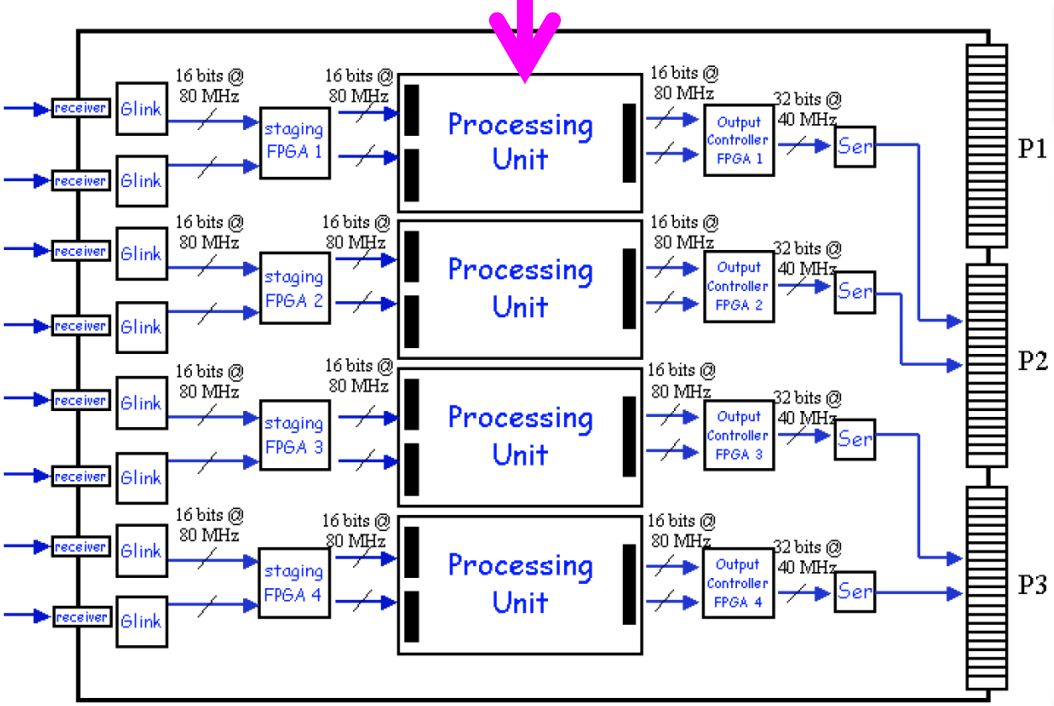
- Readout Clock (RCK) set to 6.667 MHz
  - 6.667 MHz = (ATLAS clock)/6 = 40 MHz/6
  - BNL's ASM2MUX ASIC requires a min. of 6 clock cycles to combine the two 12-bit ADC words into a single 4-bit word
- 15x RCK cycles to perform a single time slice readout
  - 2.25 μs = (15/6.667 MHz) = (90/40 MHz)
- Every trigger requires 4x time slices to be readout
  - **111 kHz = (4/2.25 μs)**
- For ATLAS upgrade, FEB can keep up with the 100 kHz rate

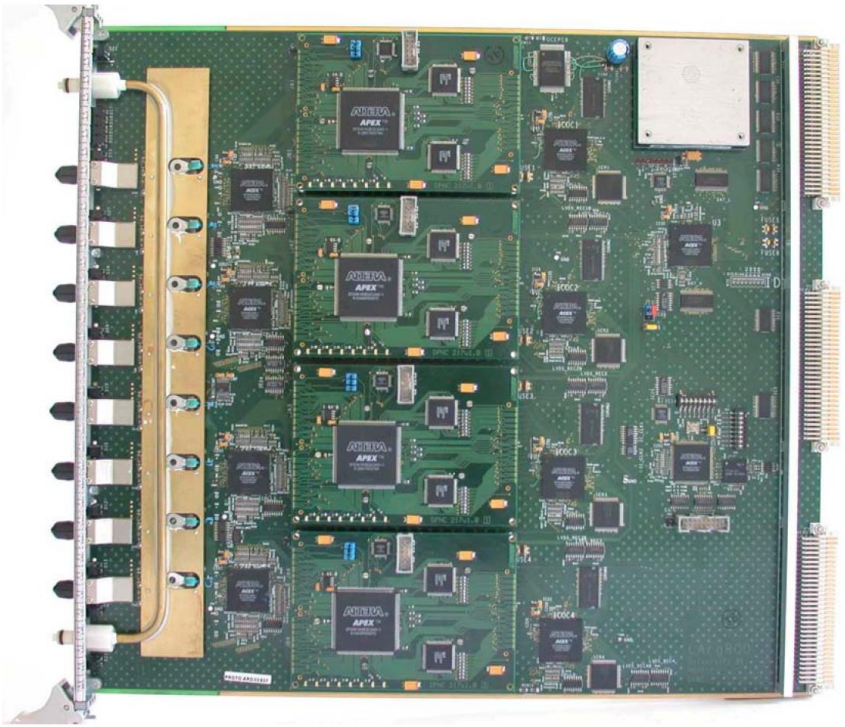


Timing Diagram for reading out the ASM-II board

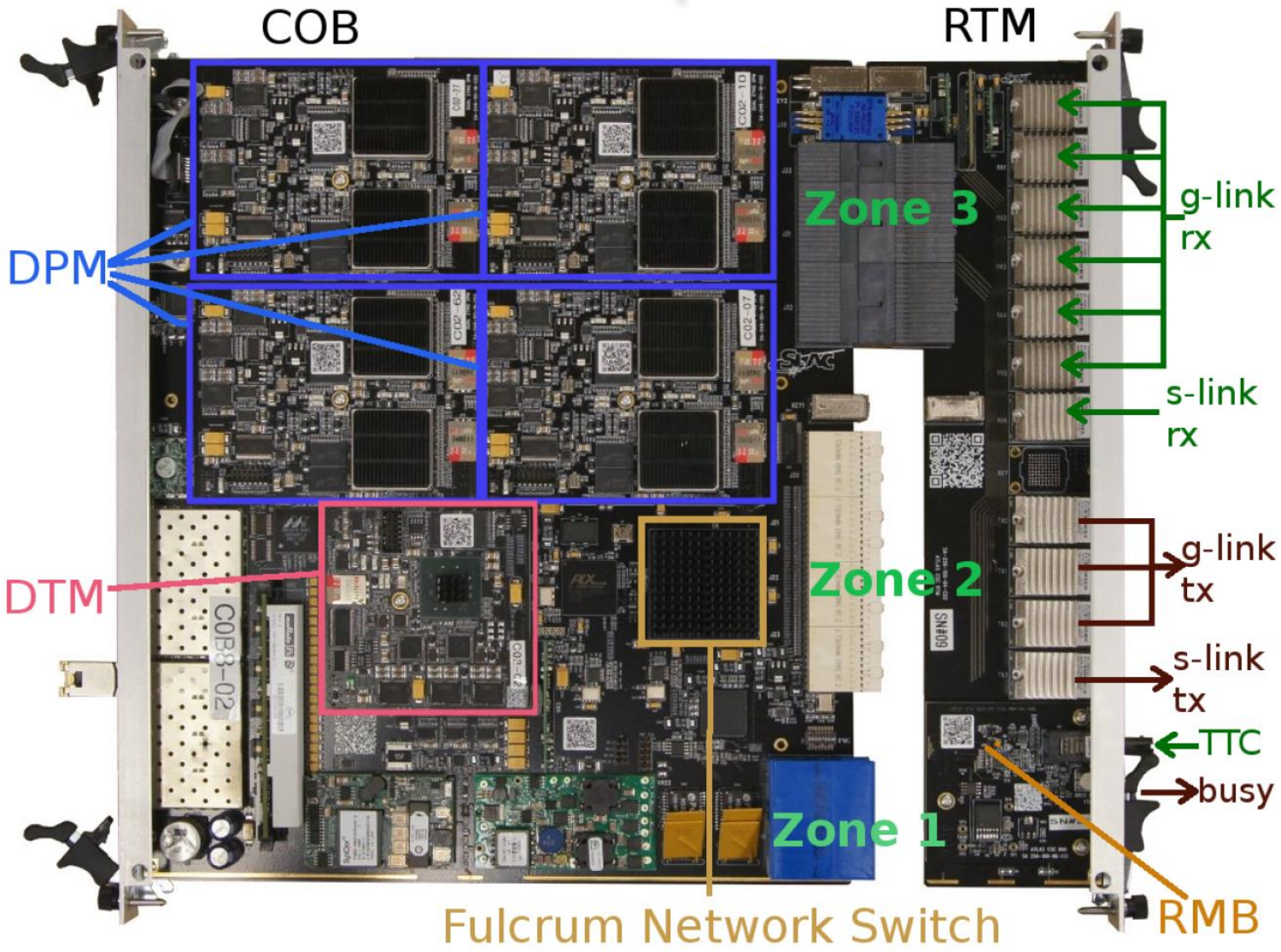
Why the backend upgrade?

DSP Module start to backpressure at 75 kHz L1A rate



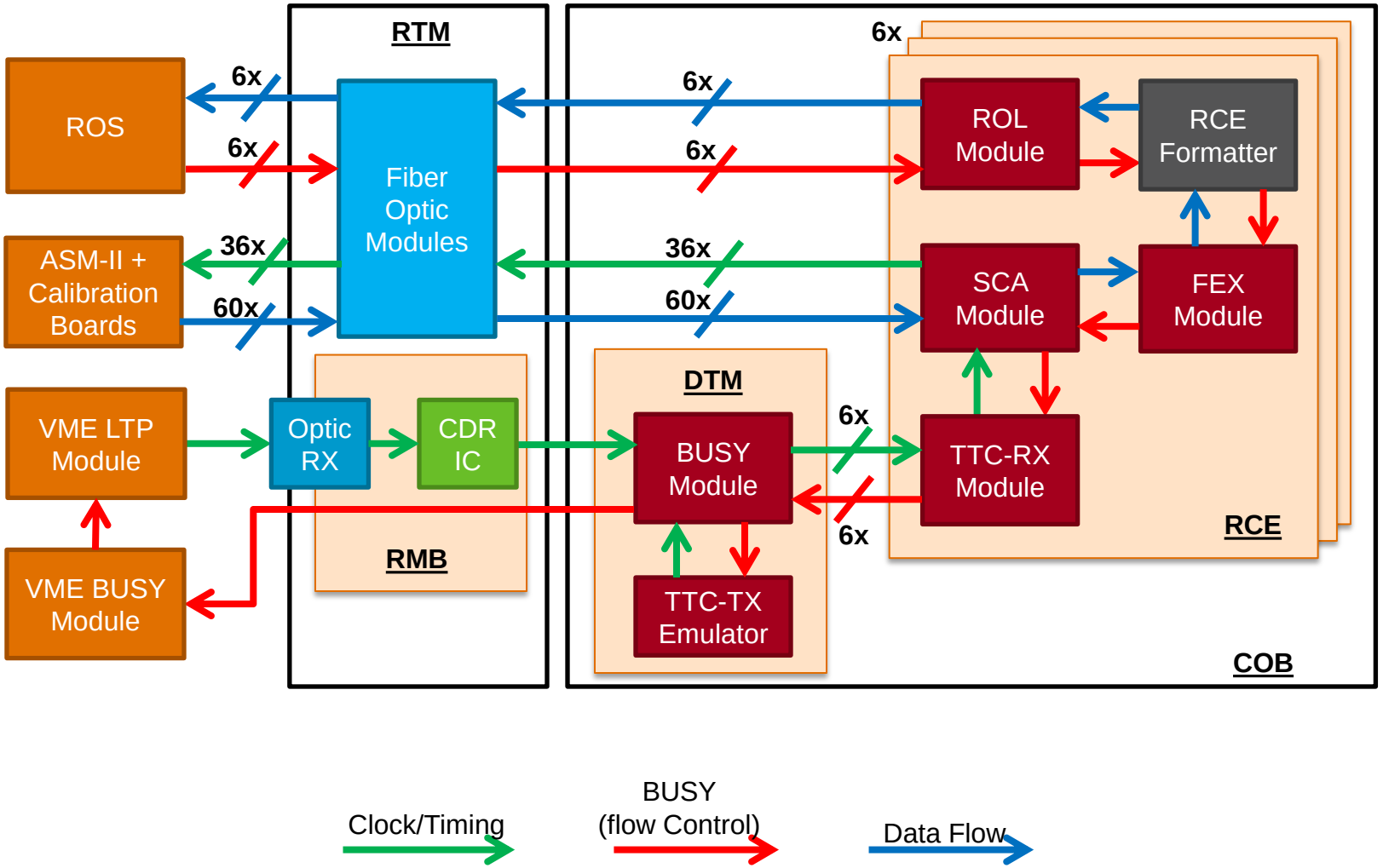


Backend Upgrade Solution: RCE Platform



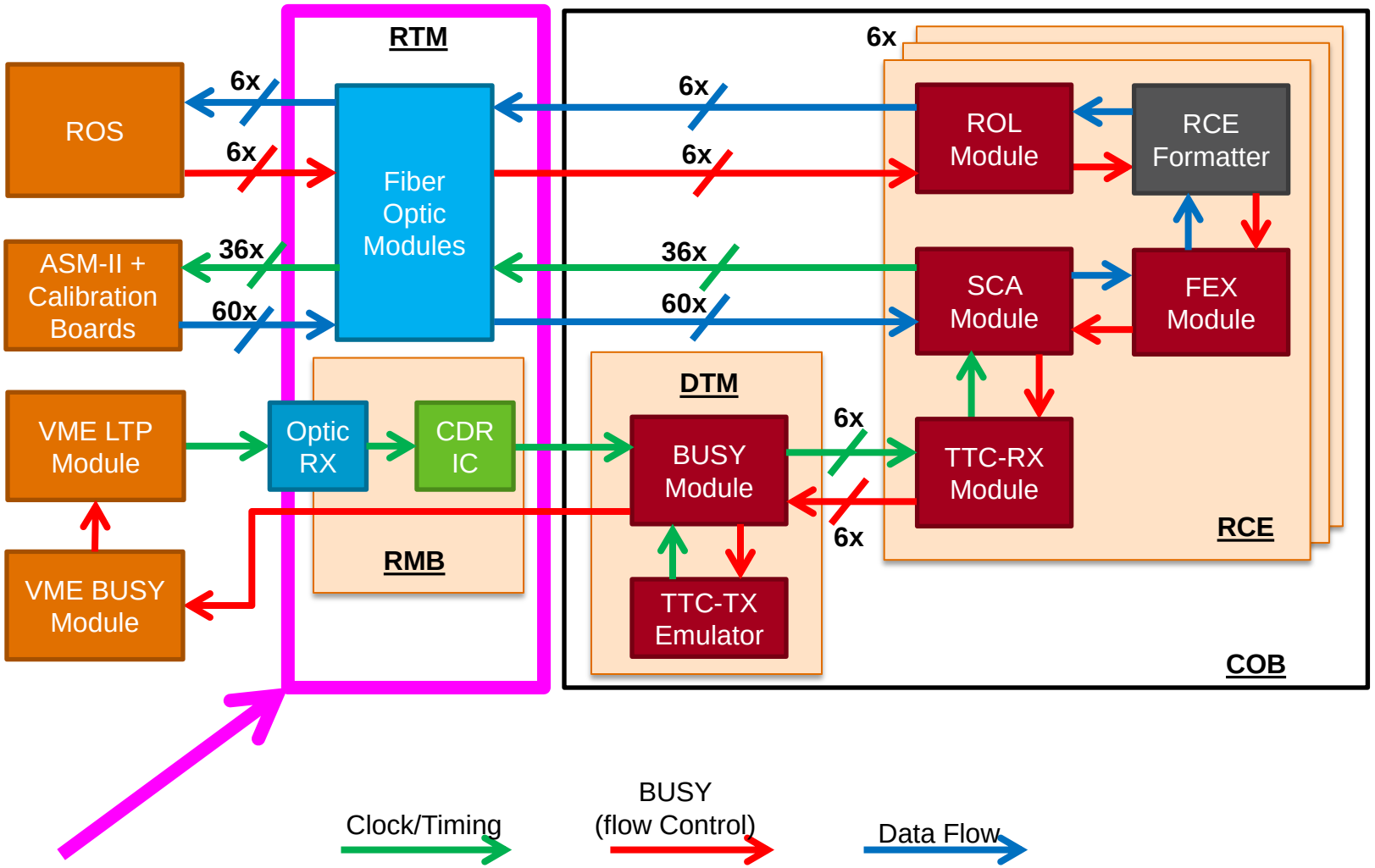
Block Diagram:
Clock/Timing + Busy Distribution + Data Flow

Note: Only showing connectivity of 1x ATCA slot



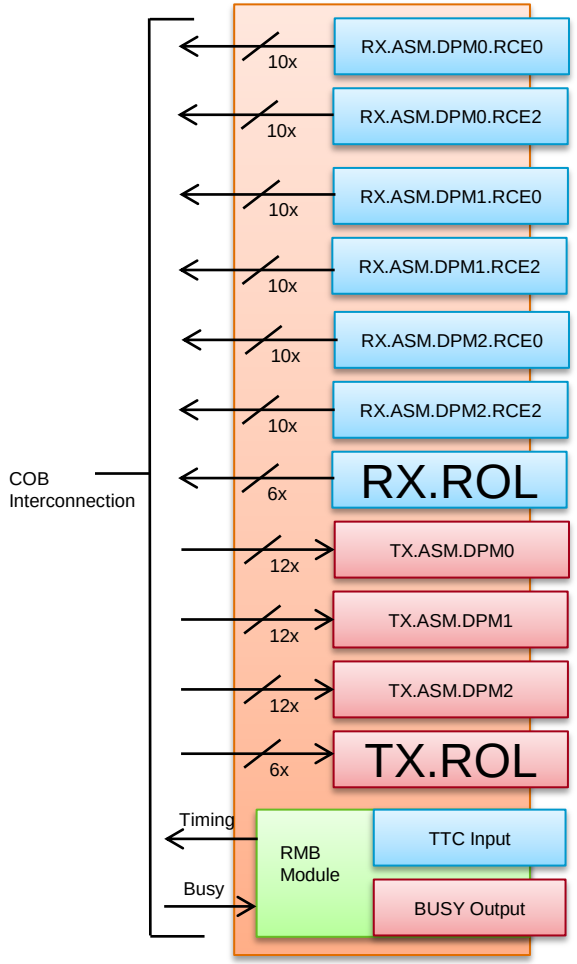
RTM Hardware

Note: Only showing connectivity of 1x ATCA slot



RTM Hardware: Overview

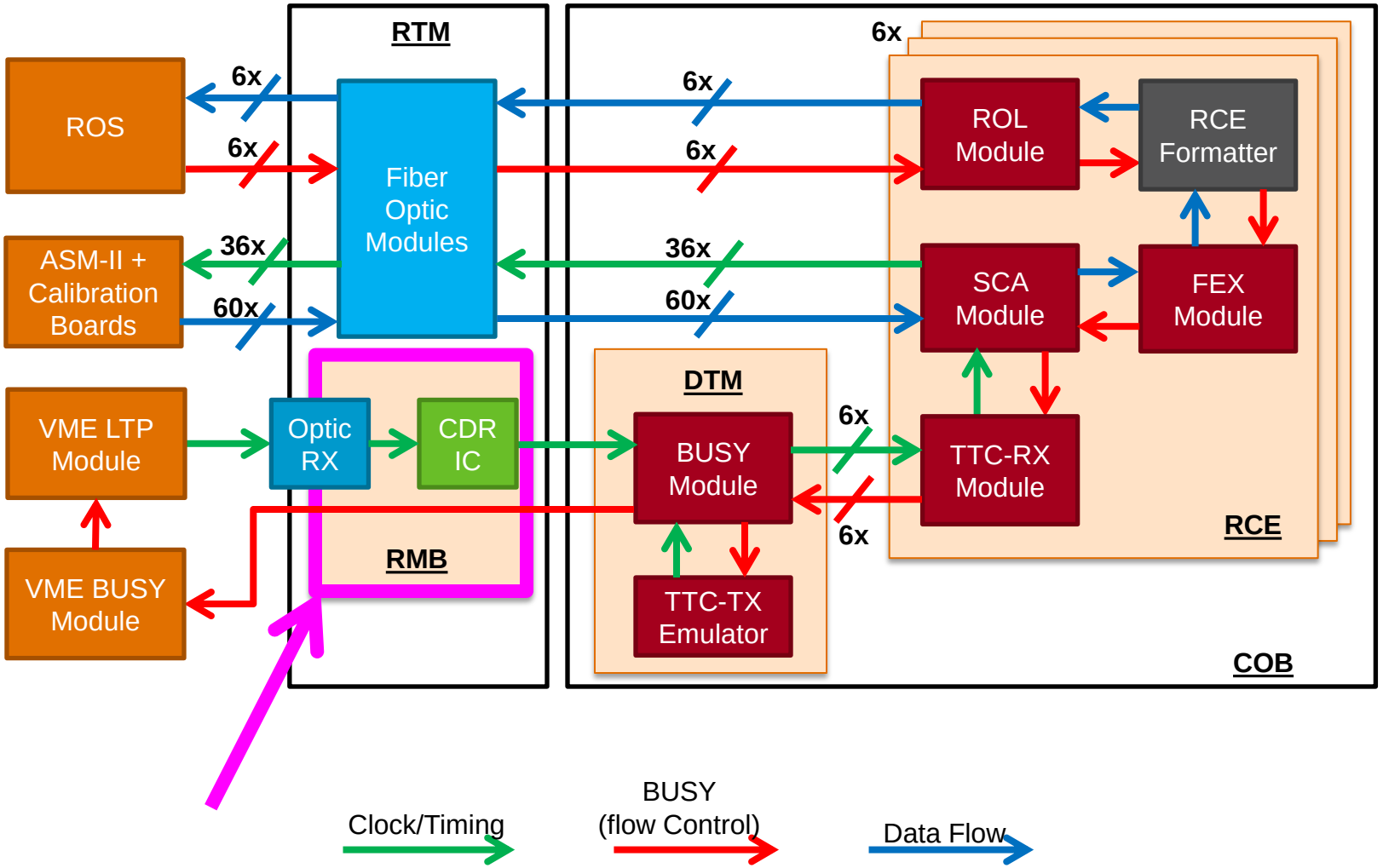
- Rear Transition Module (RTM)
- 7x RX.SNAP12 Optical module:
  - Part Number: FRXD02SL1T
- 4x TX.SNAP12 Optical module:
  - Part Number: FTXD02SL1T
- Only connecting 3 of the 4 DPMs to the SNAP12 modules
  - Total of 6x RCEs per COB
- Each RCE has a dedicated RX.SNAP12 for ASM communication
- Both RCEs of the same DPM share a TX.SNAP12 for ASM communication
- All RCEs share the common RX.ROL and TX.ROL
  - The two SNAP12 cables go through a patch panel to convert to 6x LC interfaces for the ROS
- Mezzanine Board for the TTC input and busy output
- Identification PROM and temperature sensor also on this RTM module (not shown in block diagram)



Schematics and BOM

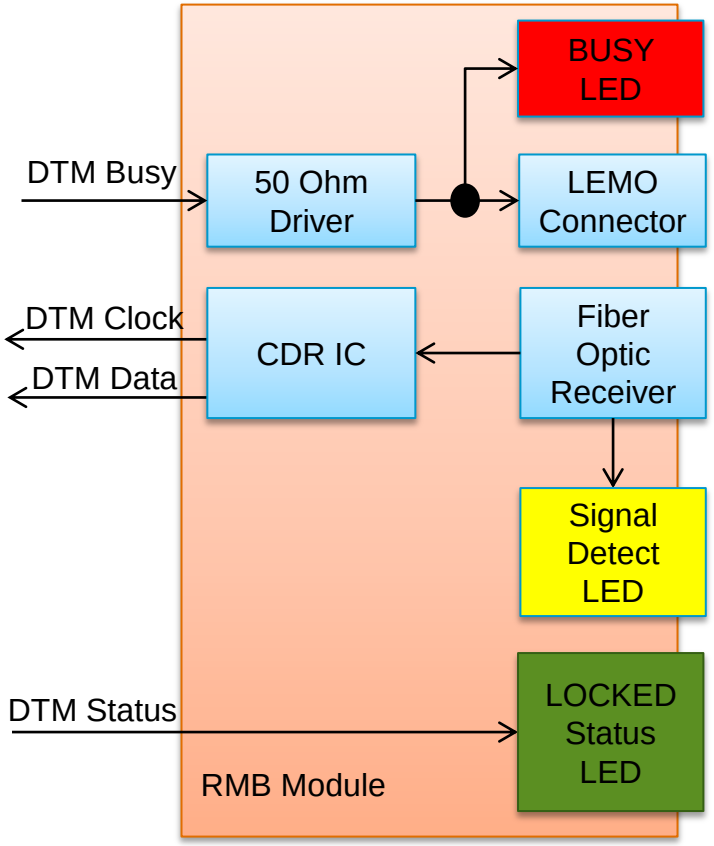
RTM Hardware: RMB

Note: Only showing connectivity of 1x ATCA slot



RMB Hardware: Overview

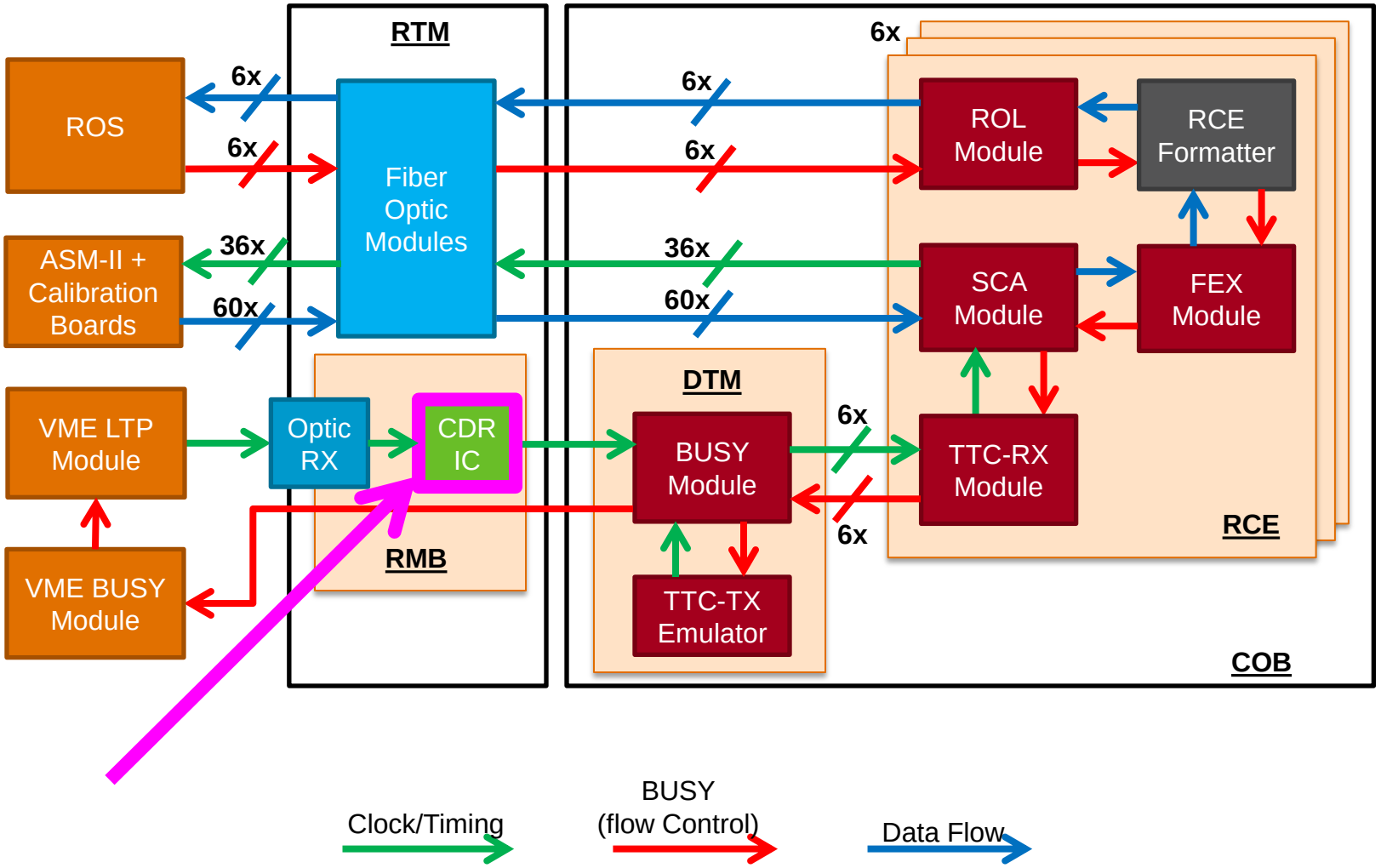
- Rear Mezzanine Board (RMB)
- 50 Ohm driver for the BUSY output:
  - Logic Level: 0~+3.3V
- Same fiber optic receiver as the old ROD
  - Part Number: HFBR-2119TZ
- Using a commercial Clock/Data Recovery (CDR) IC instead of the TTC-RX ASIC
  - Part Number: ADN2816ACPZ ($20/unit)
- Three Status LEDs
  - Optical signal detected (Yellow)
  - Busy active (Red)
  - Locked to clock and data (Green)



Schematics and BOM

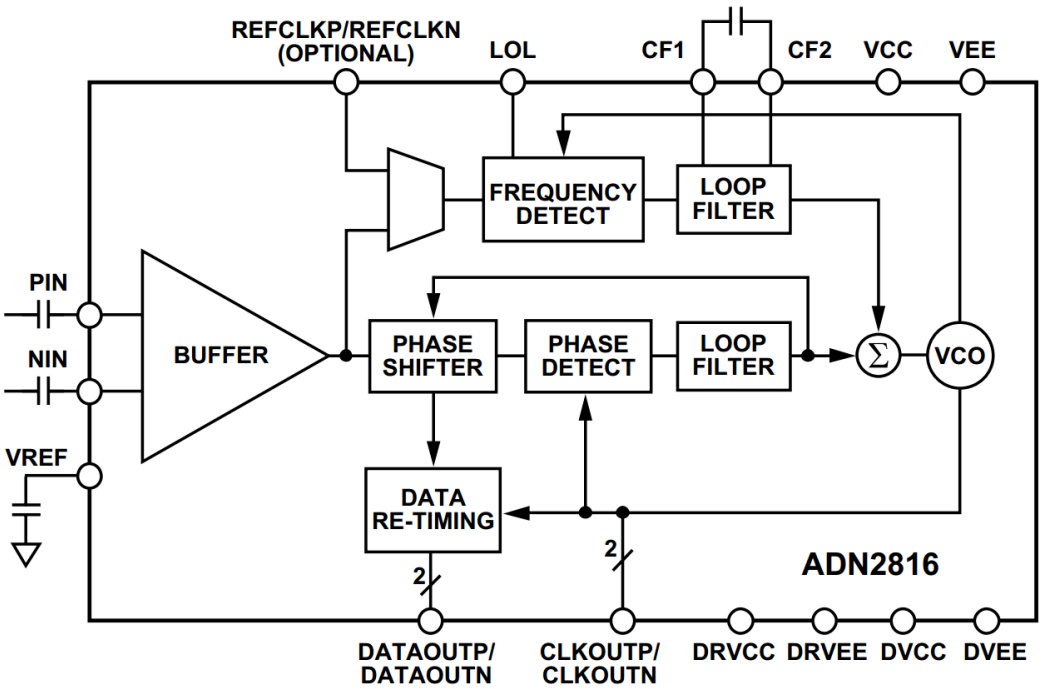
RTM Hardware: CDR IC

Note: Only showing connectivity of 1x ATCA slot



RMB Hardware: CDR IC

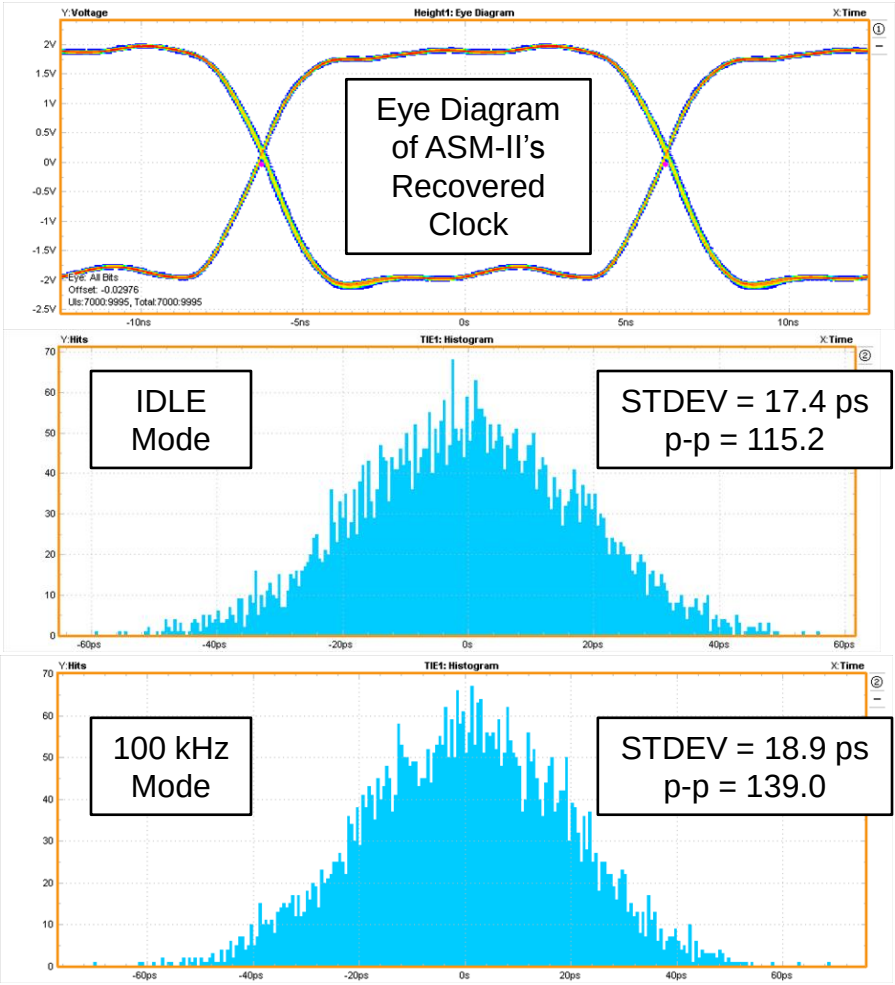
- Clock-Data Recovery (CDR)
- This IC:
  - Recovers the clock from the Bi-Phase Mark (BPM) encoded data stream
  - Outputs this recovered clock and a re-timing version of the BPM encoded data stream
- Pros:
  - Low cost ($20/IC)
  - Readily available
  - Works “right out of the box”
    - Zero programming required
- Cons:
  - Requires firmware to decode the BPM encoded data stream
- Selected this solution over the TTCrx ASIC because:
  - Uncertainty in the ASIC availability
  - Increased flexibility by pushing the BPM decoding into the firmware

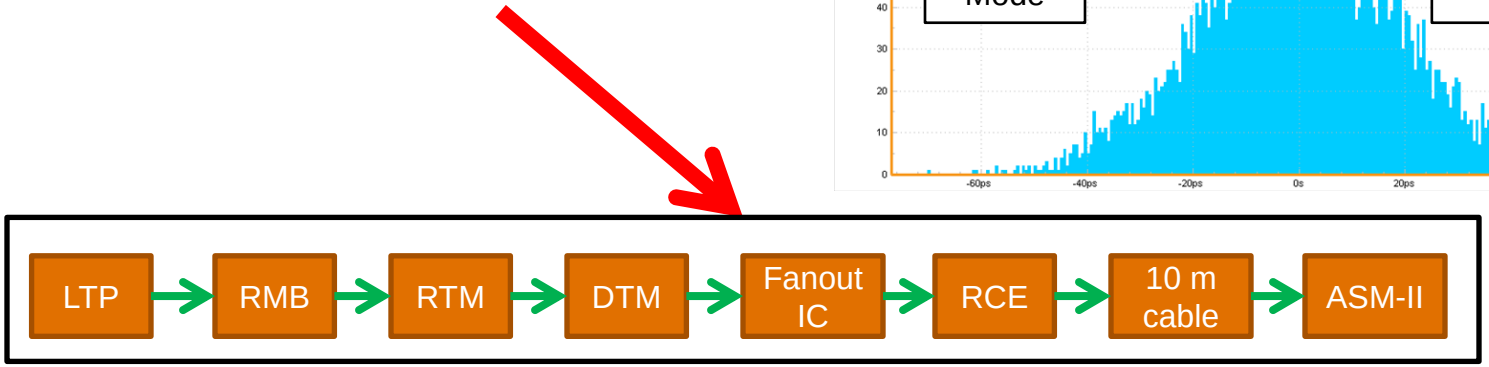


CDR IC Datasheet

RMB Hardware: Timing Performance

- Measured right at the ASM-II's recovered clock test point using a calibrated Tektronix DPO 7254 oscilloscope
- Measured for both IDLE mode (no triggering) and 100 kHz triggering
- At SLAC, measured the clock jitter through the full path:





RMB Hardware: Timing Performance Comparison

- Old ROD used a TTC-RX ASIC to recover the clock
  - No deskew of data but deskew clock
- New ROD uses a commercial CDR IC
  - No deskew of clock but deskew data
- Measured -22 dBm of optical power for this jitter testing
- Our measurements shown with the big RED circle

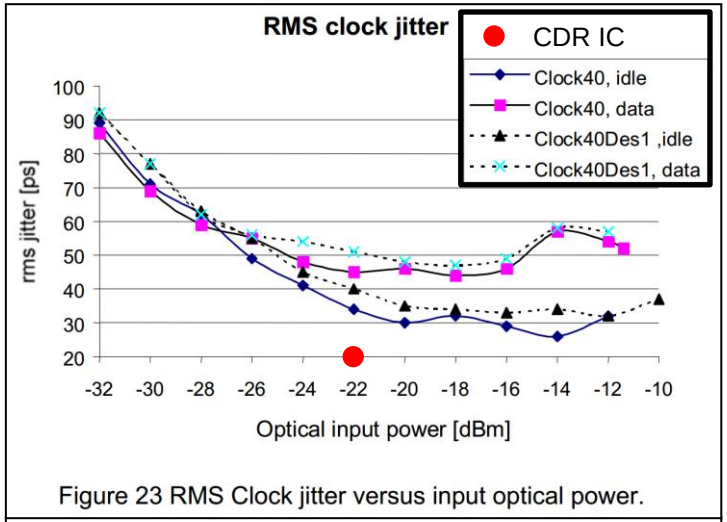


Figure 23 RMS Clock jitter versus input optical power.

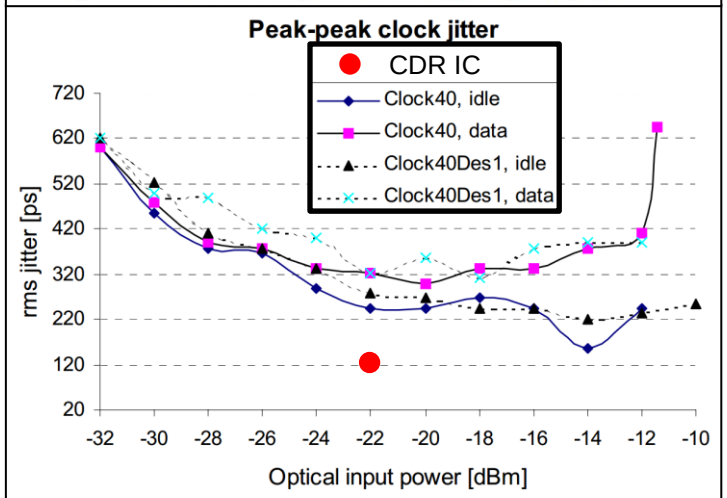
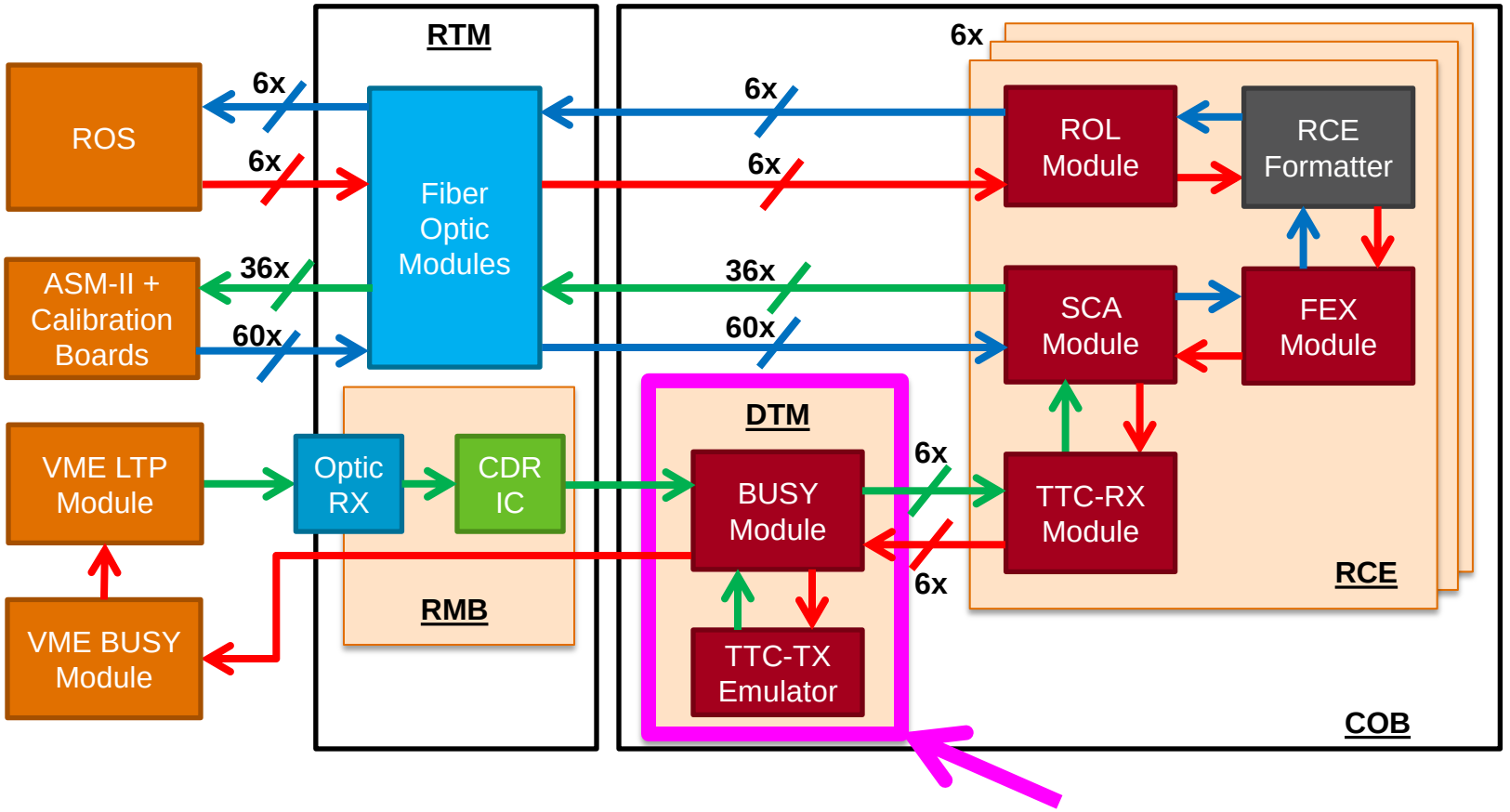


Figure 24 Peak to peak clock jitter versus input optical power.

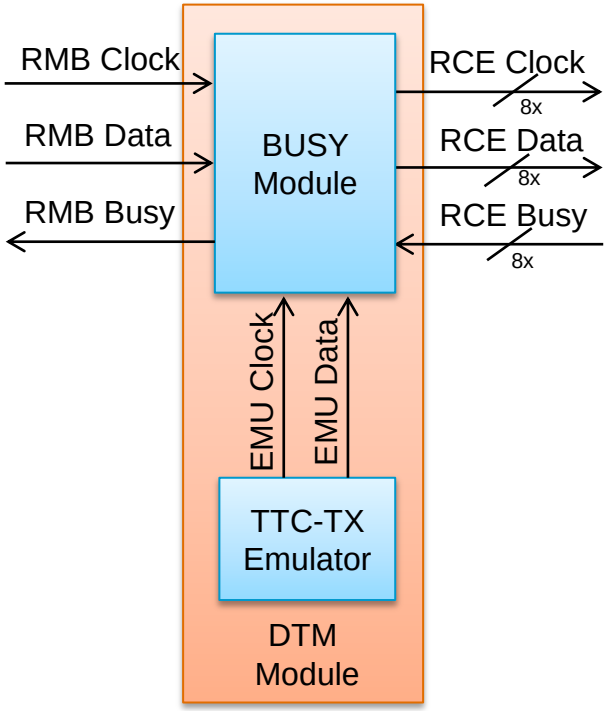
DTM RCE Firmware

Note: Only showing connectivity of 1x ATCA slot



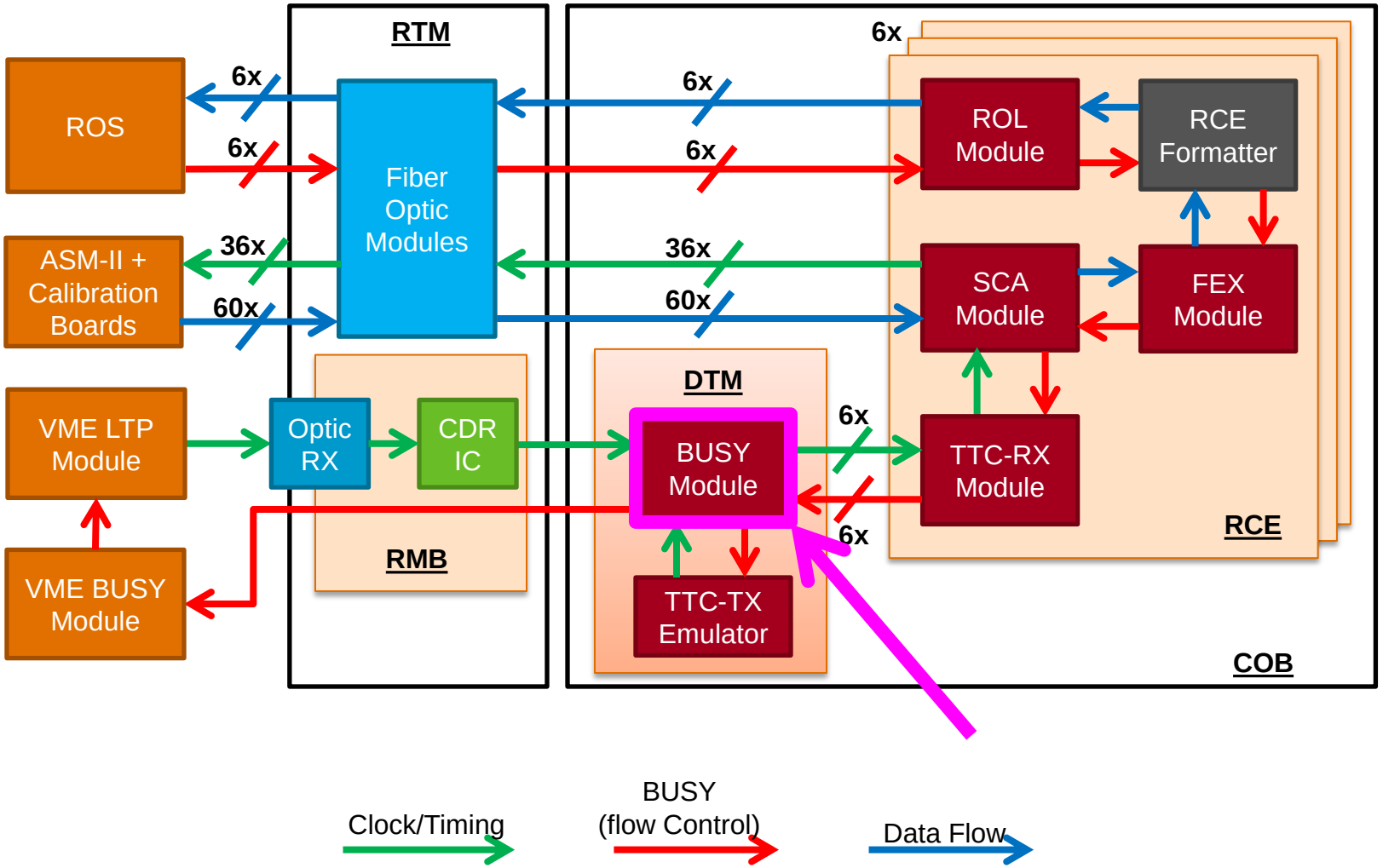
DTM RCE Firmware: Overview

- Busy Module:
  - ORs the busies from the RCEs into a single output
  - Multiplexes between an external or internal timing reference
  - Support up to 8x RCEs
    - Able to mask off unused RCE BUSY channels
- TTC-TX Emulator:
  - Emulates LTP functionality
    - Generates a local 40 MHz clock reference
    - Generates L1 triggers
    - Generates broadcast messages
    - Generates Individually-Addressed Commands



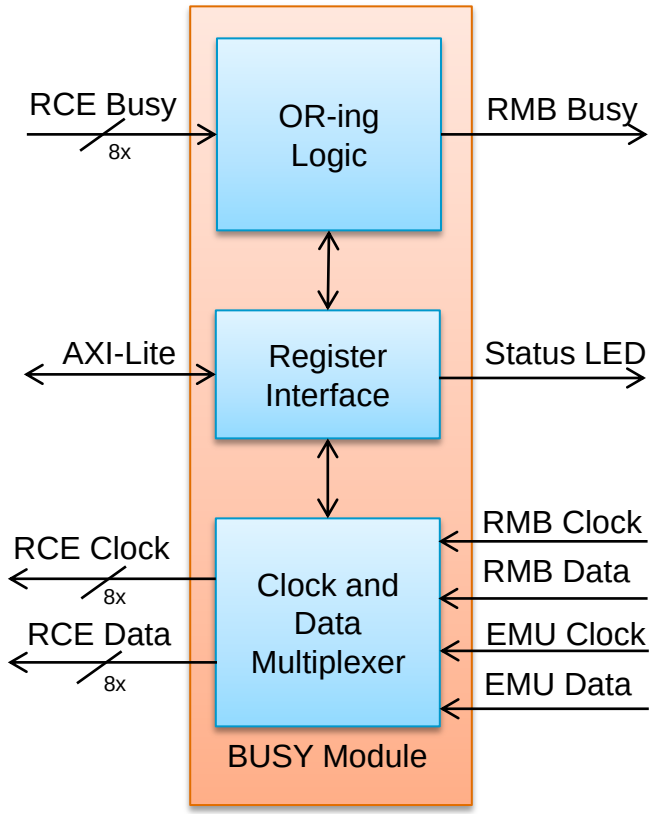
DTM RCE Firmware: Busy Module

Note: Only showing connectivity of 1x ATCA slot



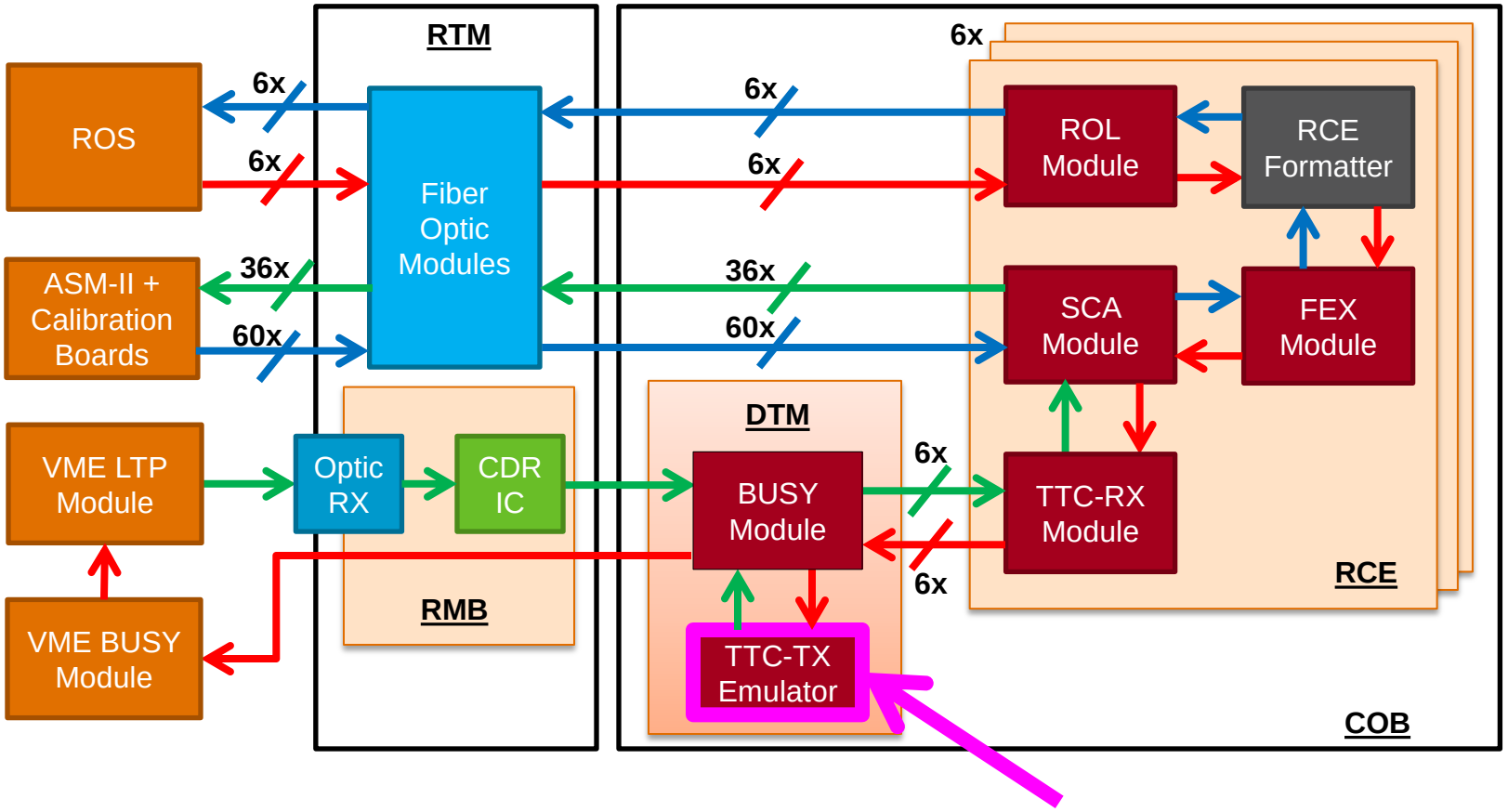
DTM RCE Firmware: BUSY Module: Overview

- OR-ing:
  - Generates a busy output based on the RCE busy bus and module's configuration
  - Able to mask off individual RCEs
  - Able to force busy no matter then RCE busy bus logic state
  - Able to invert the BUSY output sent to the RMB
- Clock and Data Multiplexer:
  - Selects the timing clock/data to be transmitted to all RCEs
  - RMB clock/data from ATLAS timing system (default)
  - EMU clock/data from local emulation module



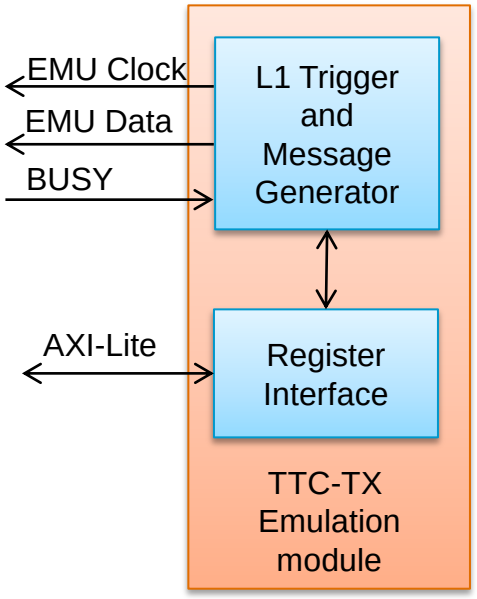
DTM RCE Firmware: TTC-TX Emulator

Note: Only showing connectivity of 1x ATCA slot



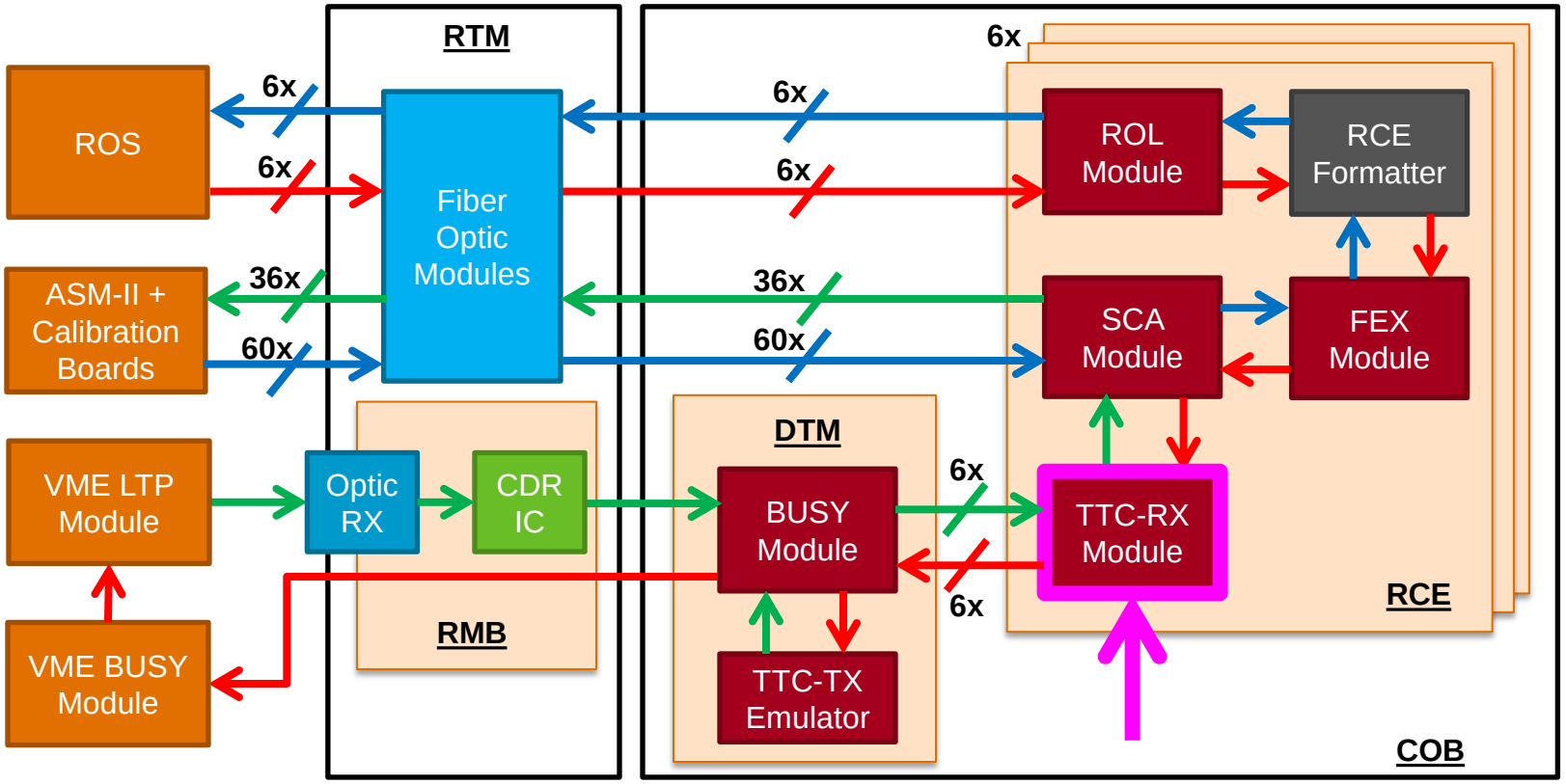
DTM RCE Firmware: TTC-TX Emulator: Overview

- This module lets us test without having a local LTP
- Synchronous timing within the same ATCA slot
  - Using a locally generated 40 MHz clock on the DTM
- Configurable:
  - Trigger Rate
  - Event Reset Rate
  - Bunch Reset Rate
- Supports a periodic continuous and periodic burst trigger/message mode
- Unsupported features:
  - Pseudo-random triggering
  - Unique trigger pattern loading
  - Trigger ID messaging
  - Multiple ATCA slot Synchronization



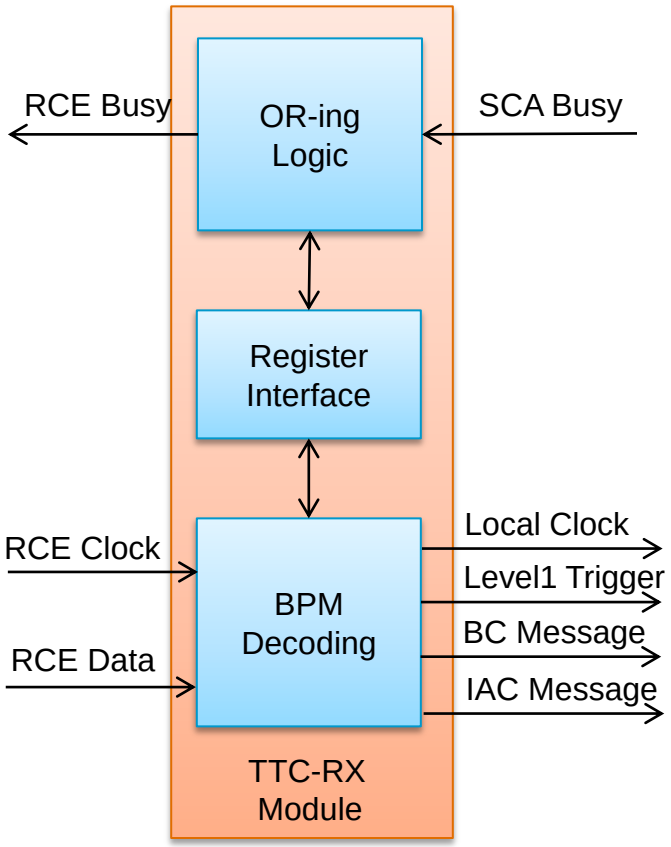
DPM RCE Firmware: TTC-RX

Note: Only showing connectivity of 1x ATCA slot



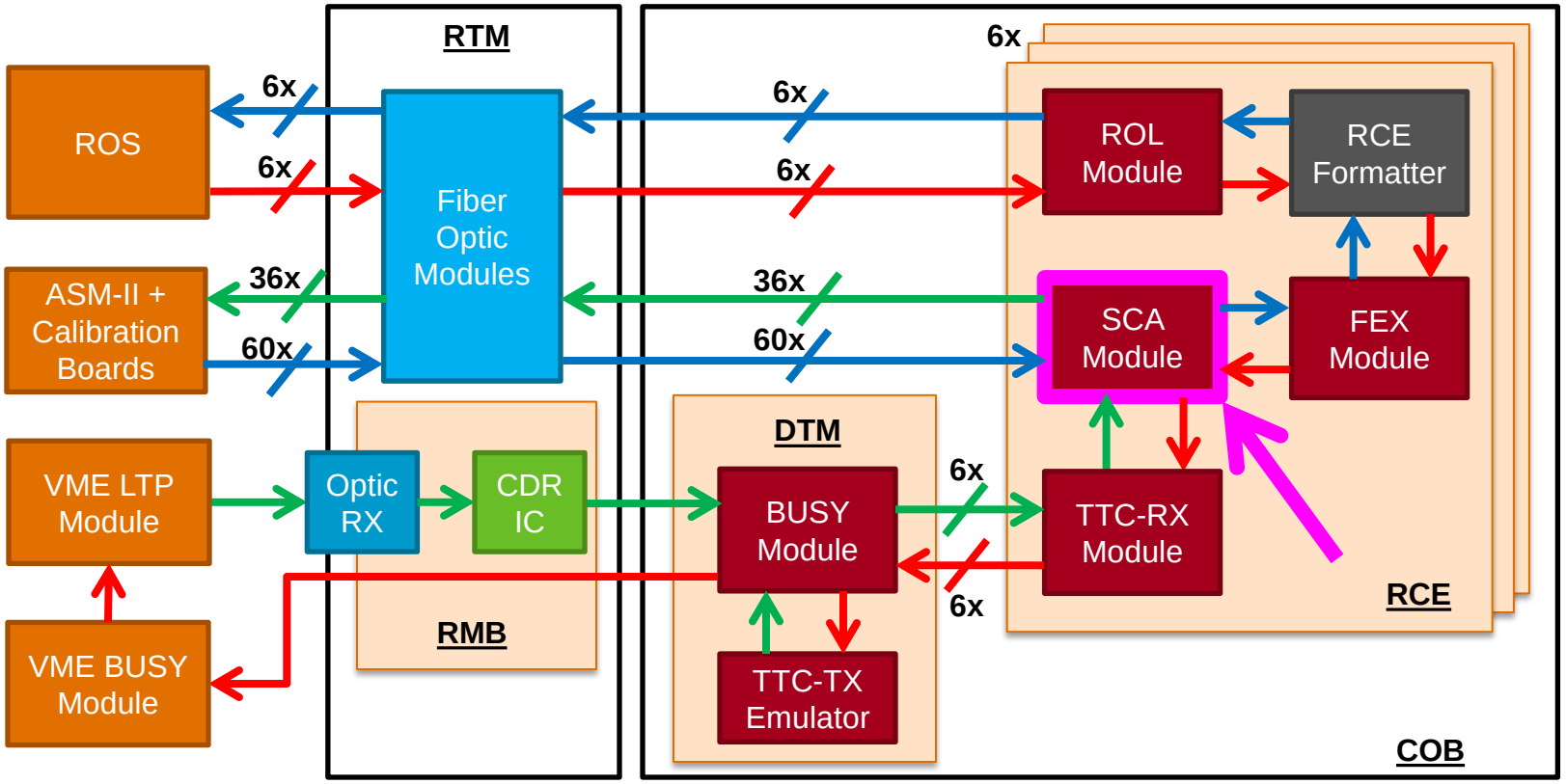
DPM RCE Firmware: TTC-RX: Overview

- Receives the BUSY from the SCA module
  - Forces BUSY at power up or hard reset
- Decodes the TTC's Level1 Triggers
- Decodes the TTC's serialized messages



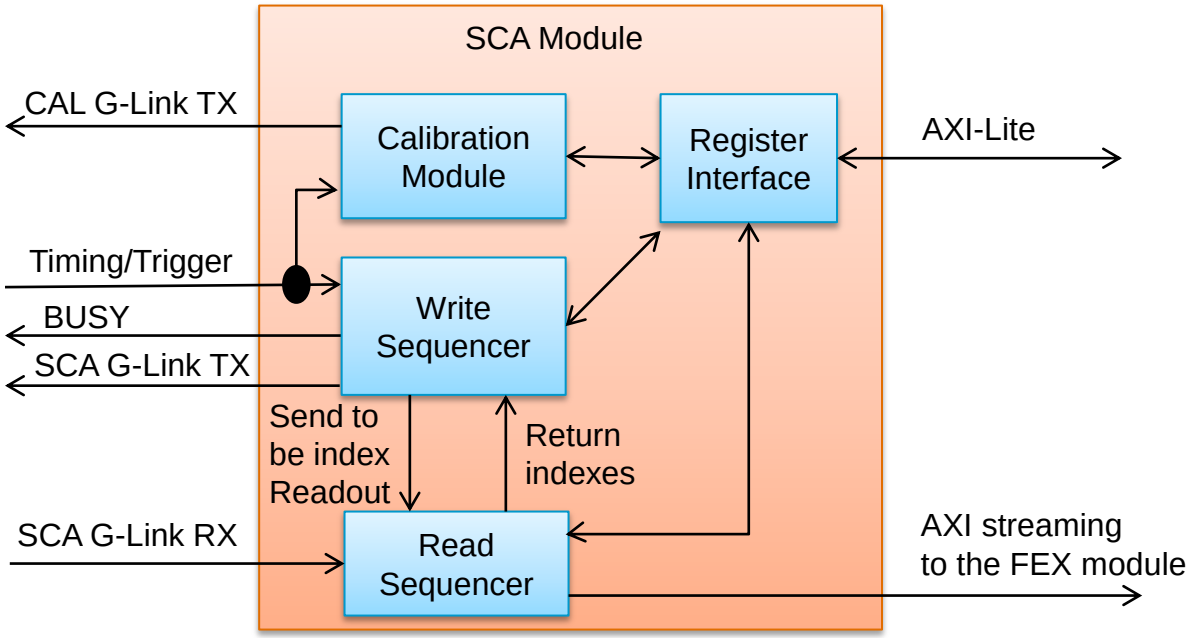
DPM RCE Firmware: SCA

Note: Only showing connectivity of 1x ATCA slot



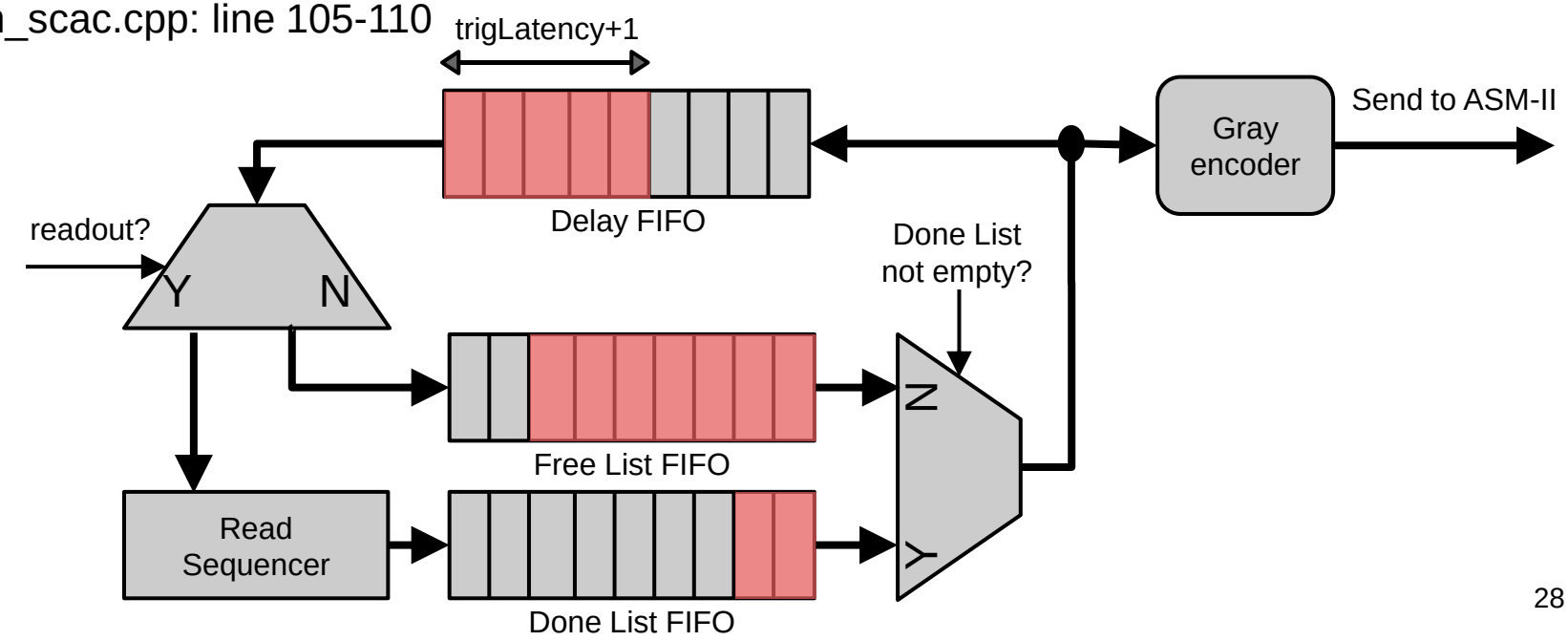
DPM RCE Firmware: SCA: Overview

- Switched Capacitor Array (SCA) module
  - Controls the front end electronics via a G-Link
- Functionality:
  - Receives the timing/trigger from the TTC-RX module
  - Generates BUSY back pressure
  - Controls the writing and reading of the SCA cells on the HAMAC ASICs
  - Generates the calibration pulses via G-Link to the Calibration board

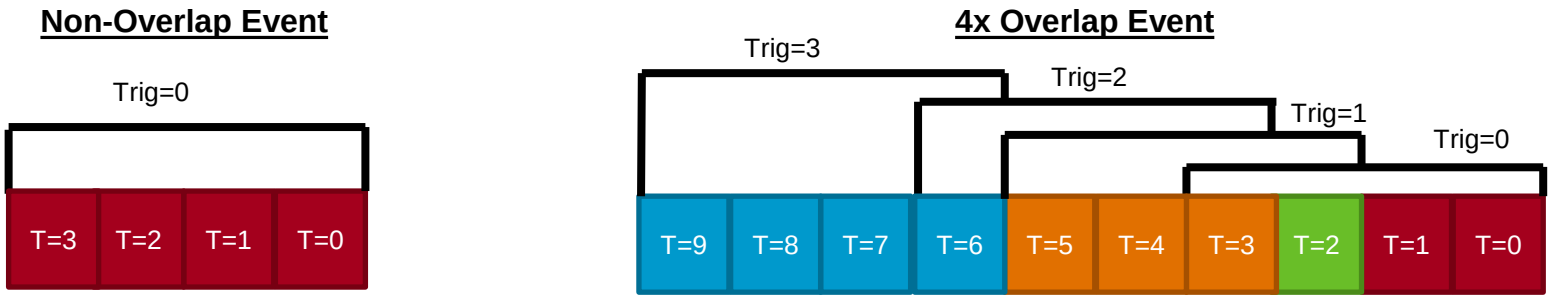


DPM RCE Firmware: SCA: Readout Sequencer

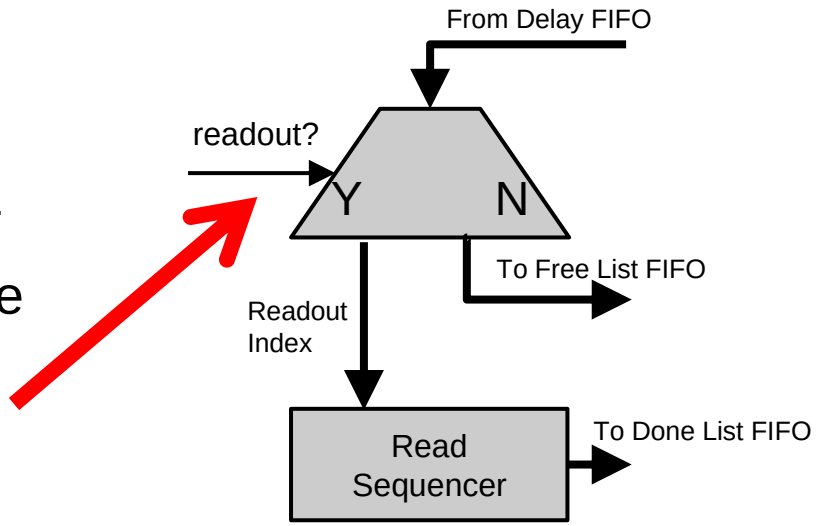
- Three Software Configuration Parameters:
  - trigLatency:
    - Number of cycles (+1) to delay the write index before making a readout decision
    - In units of the TTC clock period = 25 ns
  - scaCell:
    - Sets the number of write indexes to readout (+1) for each Level1 trigger
  - busyThreshold:
    - Threshold that's compared with the Free List FIFO's fill count to generate the BUSY output
- Writes to the ASM-II with 20 MHz clock
- Using the same "modified" Gray code scheme as the old ROD
  - ctm_scac.cpp: line 105-110



DPM RCE Firmware:
SCA: Readout Sequencer: Overlap Events

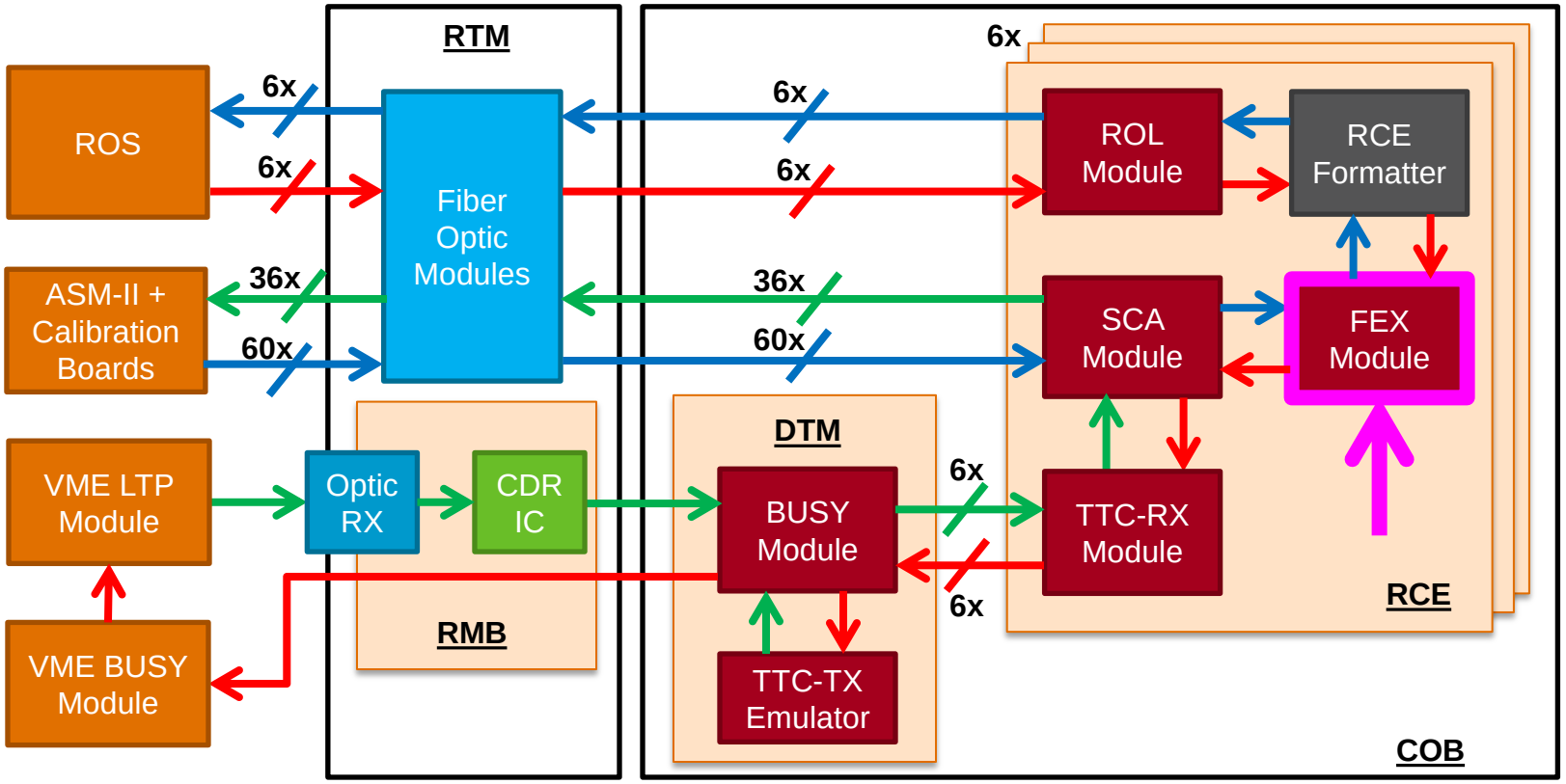


- Above shows two examples:
  - non-overlapped event (on the left)
  - 4x overlapping events (on the right)
  - Nominal four samples per Level1 Trigger
- Sends indexes from the delay FIFO to the read sequencer until the sample counter reaches the scaCell configuration value



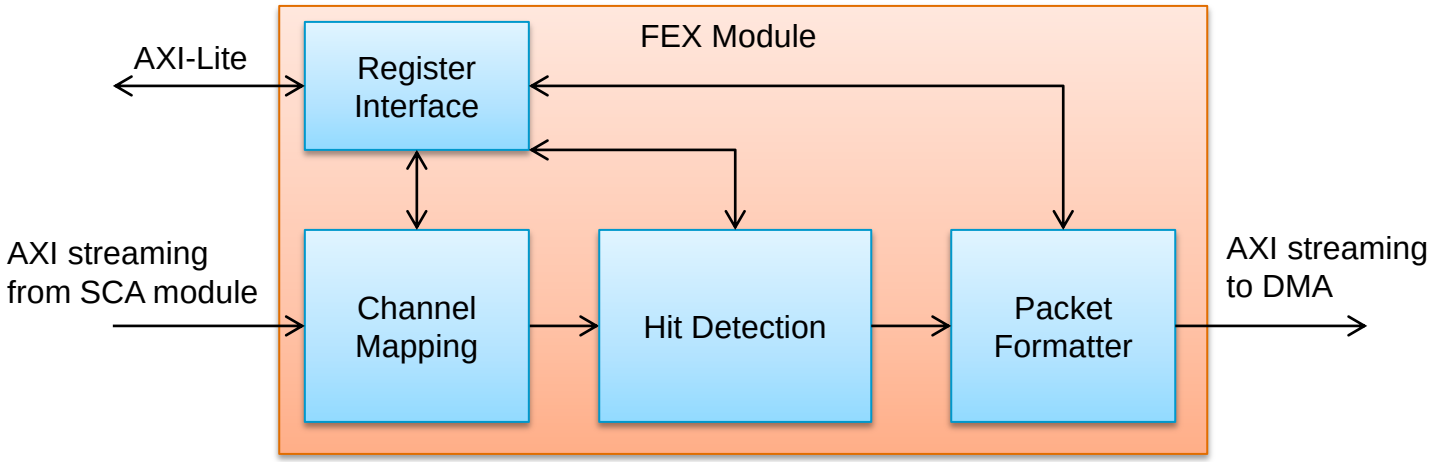
DPM RCE Firmware: FEX

Note: Only showing connectivity of 1x ATCA slot



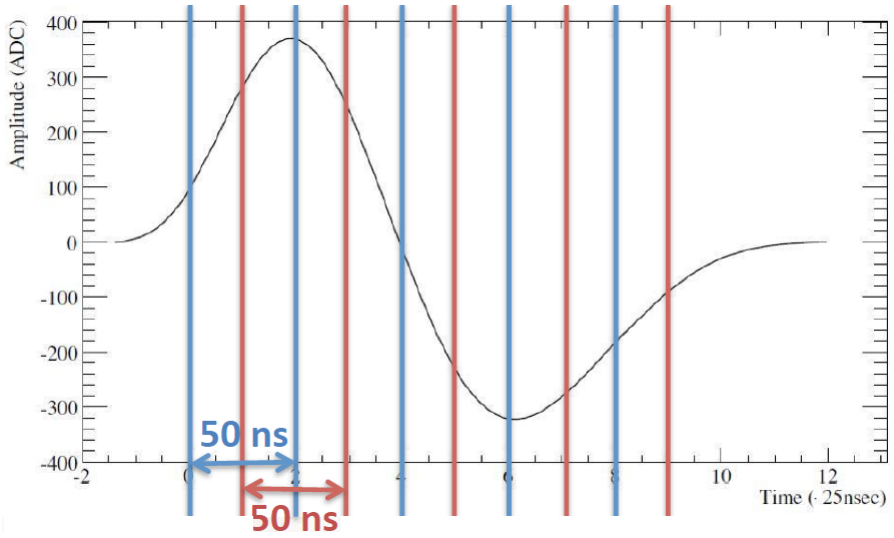
DPM RCE Firmware: FEX: Overview

- Channel Mapping:
  - Converts the data from HAMAC ASIC channel mapping to X/Y strip channels mapping
- Hit Detection:
  - Digital Signal Processing to check for data over threshold
- Packet Formatter:
  - Packets and formats the data for the event assembly
- By only sending data with “hits’, reduce the data bandwidth to the software by factor 20~40
  - 2.5~5% chamber hit occupancy



DPM RCE Firmware: FEX: Hit Detection

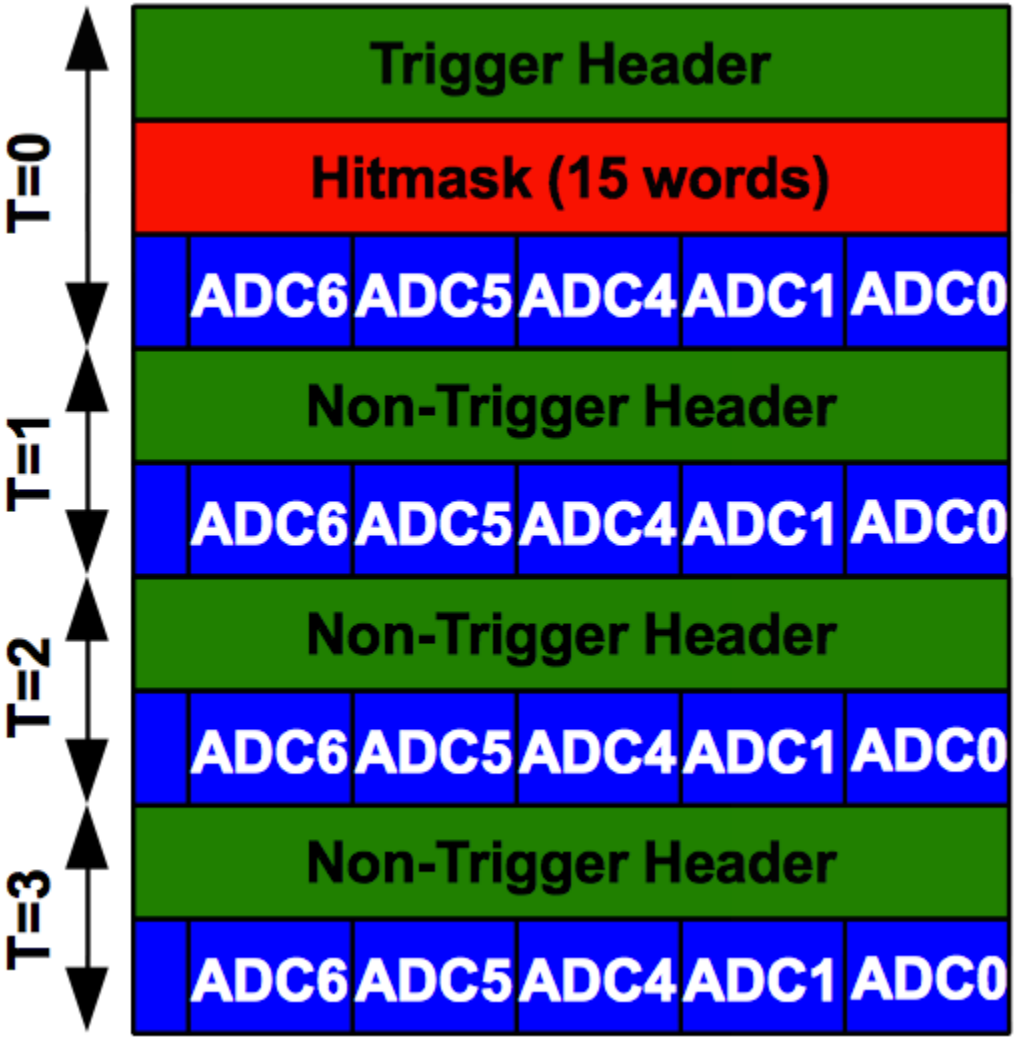
- When the write clock is HIGH, first 2nd sample used for thresholding
- When the write clock is LOW, first 3rd sample used for thresholding
- If selected sample greater than threshold, then tagged as a “HIT”
  - As well as the strip’s nearest neighbors
- Used the DSP48’s QUAD instruction mode to create 4x 12-bit comparator per DSP48
  - Used 240x DSP48 modules to reduced the FF/LUT usage



DPM RCE Firmware: FEX: Hit Detection: Data Format

SLAC

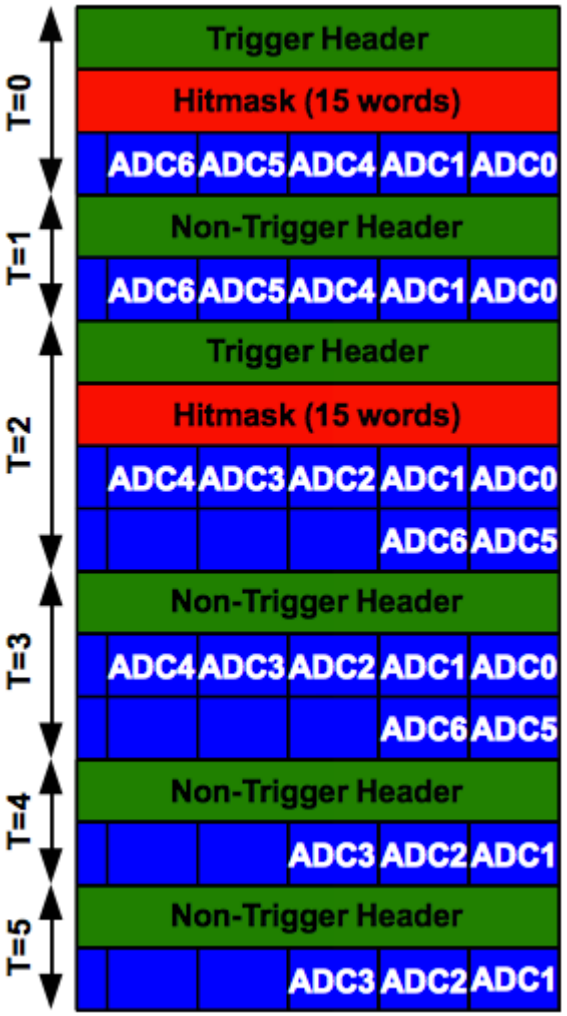
Output Format Example: Non-overlapping L1As



DPM RCE Firmware: FEX: Data Formatting

- Trigger arrived for time sample T=0 and T=2
  - T=0: ADC[5] and ADC[0] had a hit
  - T=2: Only ADC[2] had a hit
- Headers are forwarded for all the samples
- Hit masks are forwarded for each L1A
  - Hit mask contains which channels were tagged as “HIT”
  - Channels 0 and 5 are above threshold for T=0
  - Channels 2 is above threshold for T=2
- To meet performance requirement:
  - Software required firmware to count the number of hits 960-bit hitmask
    - Implemented via priority encoding

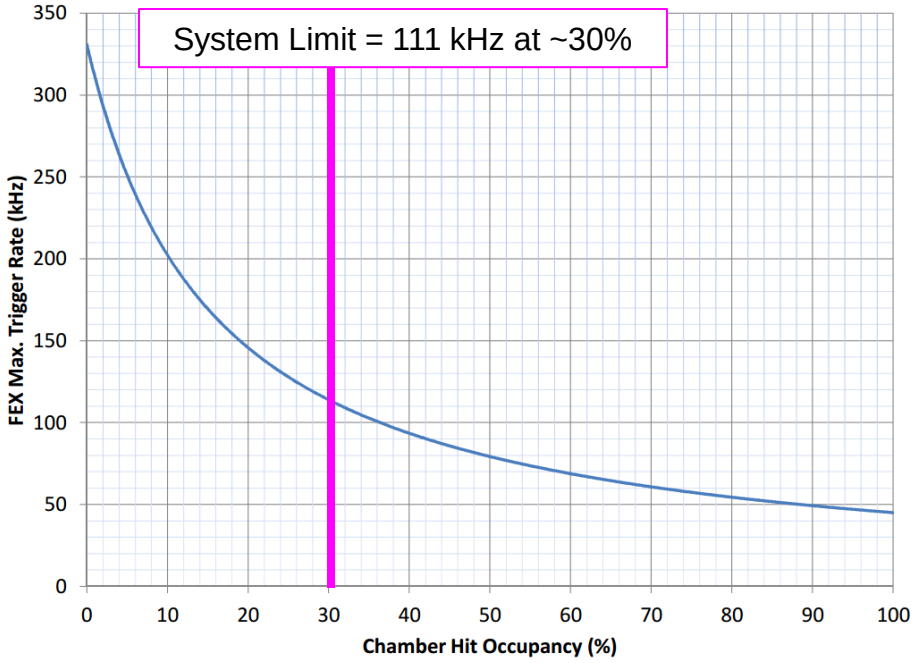
Output Format Example: Overlapping L1As



DPM RCE Firmware: FEX: Throughput

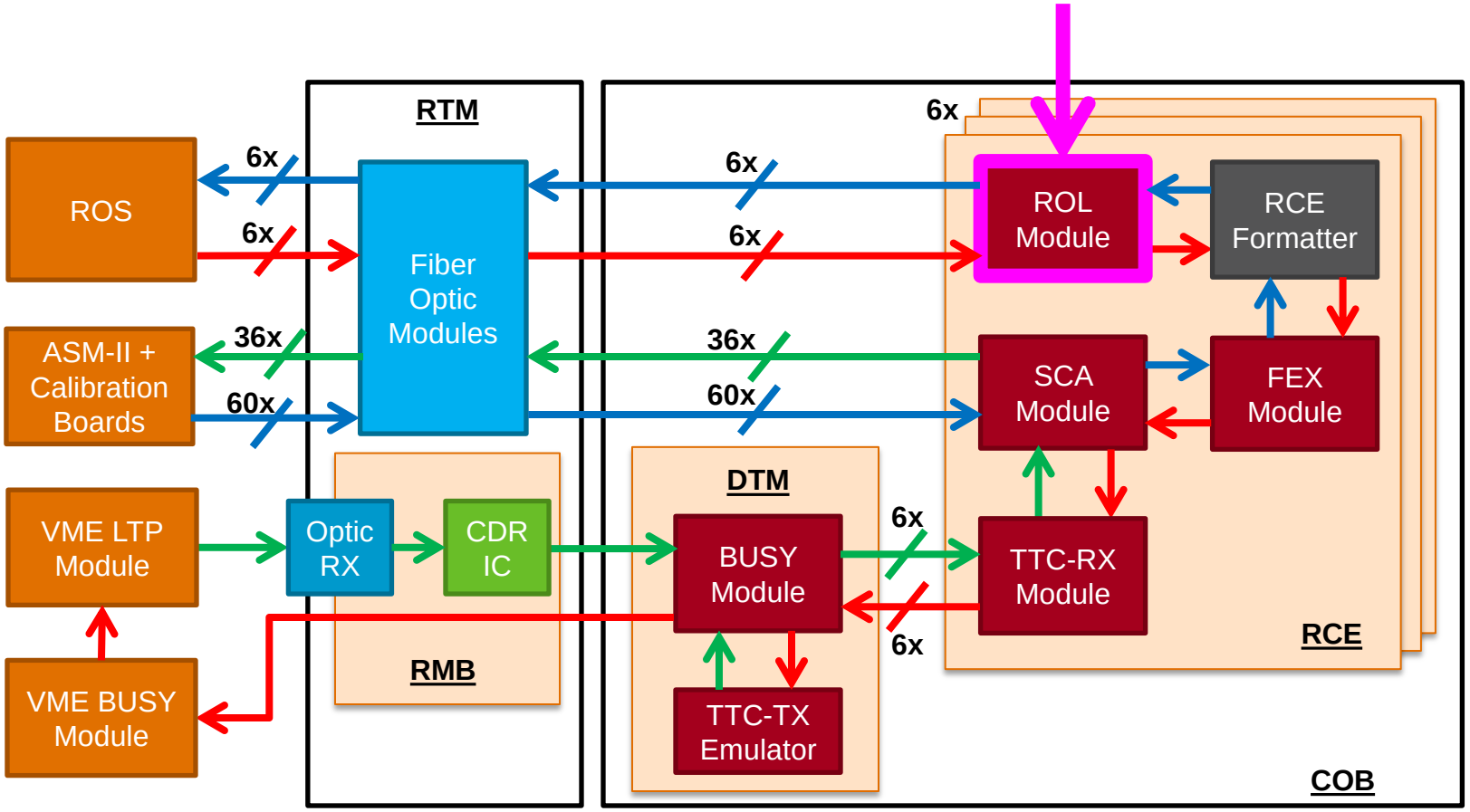
$$MaxTrigRate = \left(\frac{(FexClkFreq)(\frac{SmplPerTrig}{FmtQueue})}{Hdr + XLayerHits(\frac{192}{10}) + YLayerHits\left(\frac{48}{10}\right) + XStripHits + YStripsHits} \right)$$

- The bottleneck in the FEX module is the packet formatter
- Requires a lot of looping through the data and hit mask before calculating the headers
  - Calculate the number of ADC values to be sent
  - Determine which layers will have hit data to be transmitted
- Optimized the combinatory logic chains for the best trigger rate performance
  - Starts to back pressure the SCA max. readout rate at 30% chamber hit occupancy
- Above is an equation for max. FEX trigger rate
  - FexClkFreq = processing clock
    - 50 MHz
  - SmplPerTrig = # of samples per trigger
    - Typically configured to 4
  - FmtQueue = # of packet formatter queues
    - 4 queues in the FEX firmware
  - Hdr = # of clock cycle to calculate and transmit the headers
    - 55 clock cycles
  - XLayerHits = # of X layers with hits
    - Range from 0 to 4)
  - YLayerHits = # of Y layers with this hits
    - Range from 0 t0 4
  - 192/10 = X-Axis strip's priority encoder
  - 48/10 = Y-Axis strip's priority encoder
  - XStripsHits = # of X strips with hits
    - Range from 0 to 768 (= 4 x 192)
  - YStripsHits = # of Y strips with hits
    - Range from 0 to 192 (= 4 x 48)



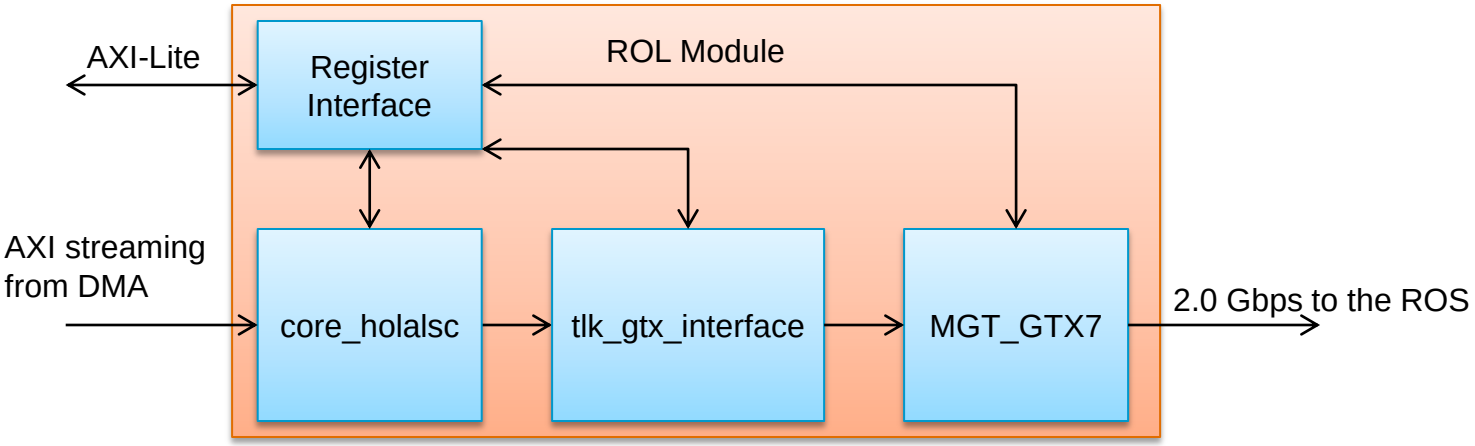
DPM RCE Firmware: ROL

Note: Only showing connectivity of 1x ATCA slot



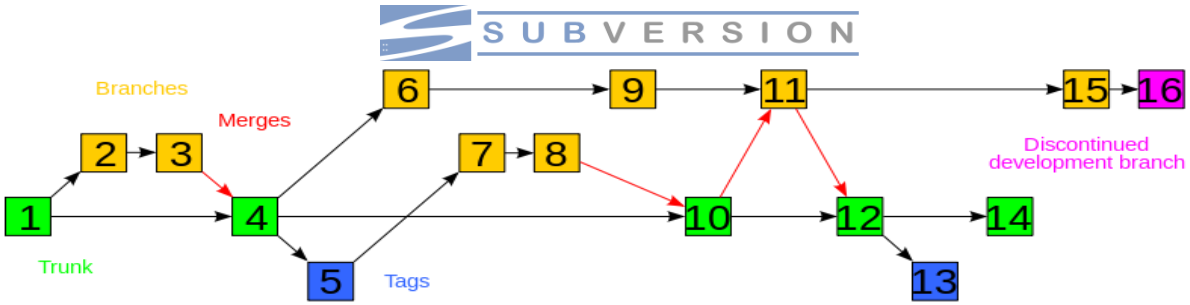
DPM RCE Firmware: ROL: Overview

- ReadOut Link (ROL) module
- core_holalsc:
  - S-Link Link Source Card (LSC) firmware core
  - Provided by Stefan Haas
    - Using Version 1.5 of “core_holalsc.vhd”
    - Latest released version as of November 2014
  - Slightly modified
    - Changed the input FIFO from Virtex-6 FIFO to Kintex-7 FIFO (RCE FPGA FIFO type)
- tlk_gtx_interface:
  - Translates the core_holalsc interface (TI TLK2501) into the GTX format
  - Provided by Stefan Haas

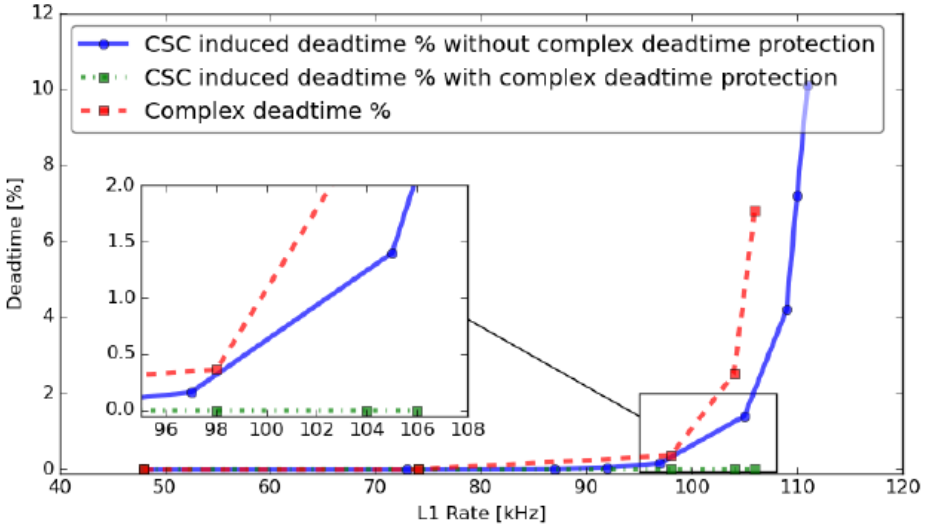


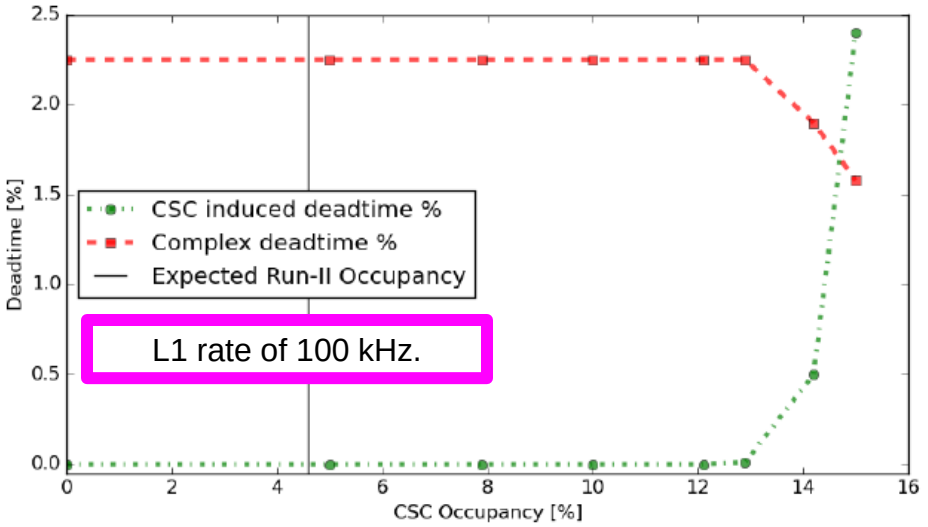
Firmware Revision Control Process

- All firmware is revision controlled using Apache Subversion (SVN)
  - Source Code: SVN repository is located at SLAC
    - **file:///afs/slac/g/reseng/svn/repos/Atlas/trunk/AtlasCsc/truck/firmware**
  - Binary Output: SVN repository is located at CERN
    - https://svnweb.cern.ch/trac/muondaq/browser/CSCFirmware
- Each firmware release includes:
  - A unique version number that's accessible via RCE's IO register space:
    - Example: 0xDA00030D
    - Version number manually generated by user
  - A unique file name:
    - Example: AtlasCscDpmAsmPack_DA00030D.bit
  - A build string that's accessible via RCE's IO register space:
    - Example: "AtlasCscDpmAsmPack: Built Tue Sep 30 08:22:12 PDT 2014 by ruckman"
    - This string is automatically updated at the start of each firmware build via our Makefile system
- Locked all SVN external modules required to compile the firmware at the end of M6
- See below for a visualization of a simple SVN project
  - Image from http://en.wikipedia.org/wiki/Apache_Subversion



Summary





- Demonstrated low system clock jitter
  - < 20 ps (STDEV) jitter
- Demonstrated performance requirement:
  - 100 kHz trigger rate through the firmware
- Demonstrated interface requirement:
  - 100 kHz trigger rate through the RCE

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