CLICpix2 validation status

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Current coverage

Around 90% (with respect to 82% from 31th August).

Latest issues link

- Readout Configuration Register (RCR) access when PRBS sequence is on
  - "special case" fix — simulation is constrained to not generate such sequence
- wrong PRBS sequence
  - update documentation — PRBS works only with 8 columns readout (simulation constrained)
- wrong readout values
  - update documentation — delay between RCR access and readout must by at least 300 ns (simulation constrained)
- partial double column readout
  - update documentation — delay between matrix programming and readout must by at least 16 (not 8) clock cycles (simulation constrained)
- (stray) output clock
  - RTL update (after discussion ;-)) — once configuration is issued, the output clock switches to 100MHz until configuration is completed
- charge injection in counting mode with long counter enabled
  - simulation fixed — add missing constraints, add bits in representation of the total TOA and TOT used by simulation
- simulation kernel failure
  - swapping problem — move from "middle" machines (32 GB RAM, 16 VCPUs) to "monster" machine (512 GB RAM, 32 VCPUs)

Current activity — Back-annotated netlist simulation

- Solved issues:
  - add hierarchical paths to internal CLICpix2 signals for netlist simulation
    - ⋆ so far we were simulating a register-transfer level (RTL) design
  - add to the scripts conditional compilation/optimization (RTL vs netlist)
  - back-annotate many modules
    - ⋆ optimization step in launching the simulation and need of relative paths utilization (portable implementation) prevent from a *$sdf_annotate* usage
    - ⋆ development of *tcl* scripts which back-annotate the design through command line
  - cope with instance names generated by the encounter
    - ⋆ the may contain spaces (' '), backslash (\) and array-like patterns (ex. [7])
    - ⋆ fix hierarchical paths
    - ⋆ upgrade the *tcl* scripts
- Waiting issues:
  - the SDF files generated by the encounter:
    - ⋆ path matching failure
    - ⋆ timing constrain matching failure
    - ⋆ lack of *$removal* timing check
    - ⋆ negative timing constraints

Summary

To do:

- complete the RTL verification with a satisfying coverage
- launch the verification environment for the netlist
- move the design files to a dedicated workspace
  - so far we work in "devel" workspace
  - the new *CLICpix2* workspace have been provided yesterday
- re-run the verification for a new metal-stack
- **Address and fix/resolve all the encountered bugs and issues**