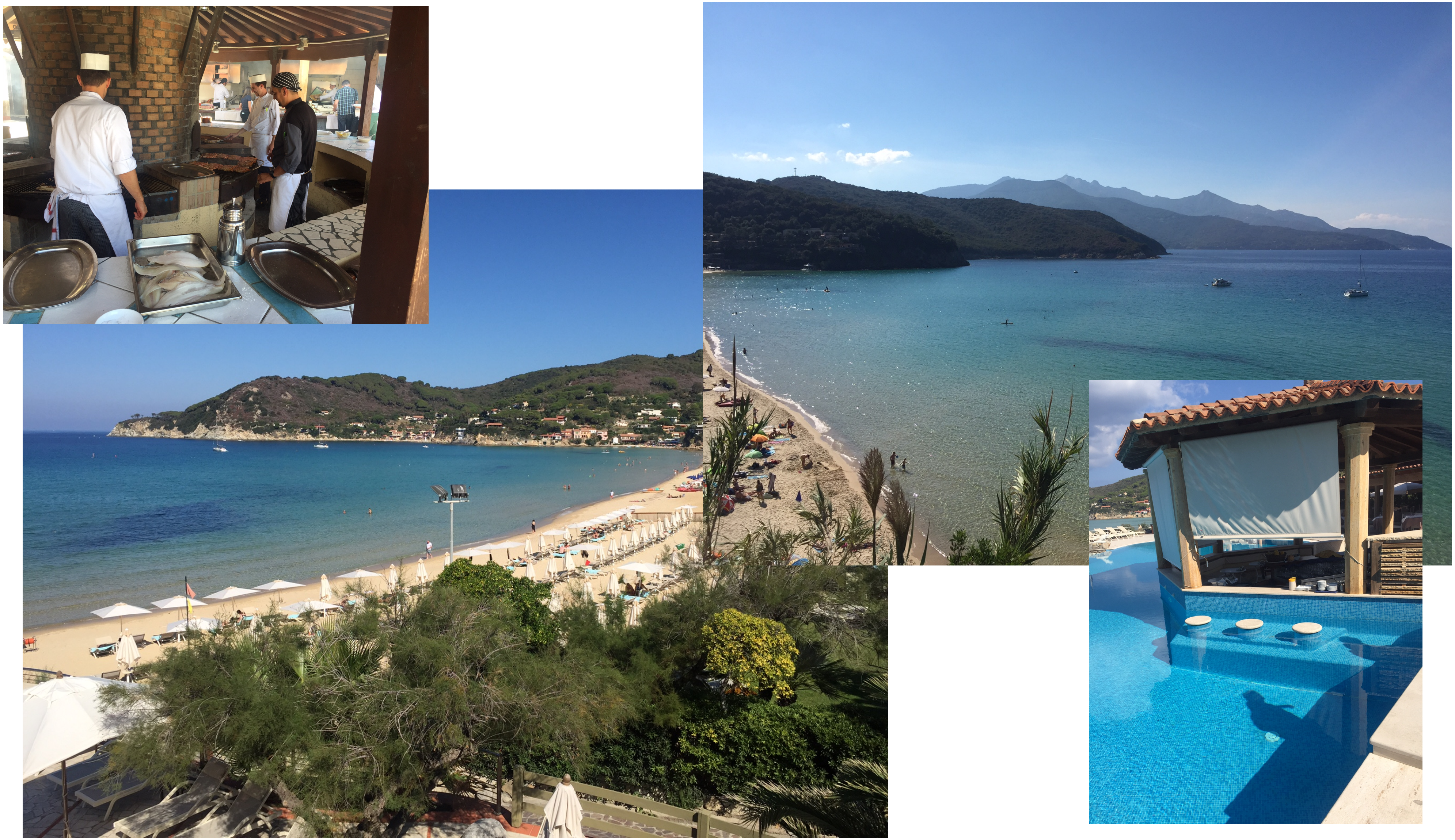
A selected summary of VERTEX2016

(CLIC-relevant highlights)

Daniel Hynds

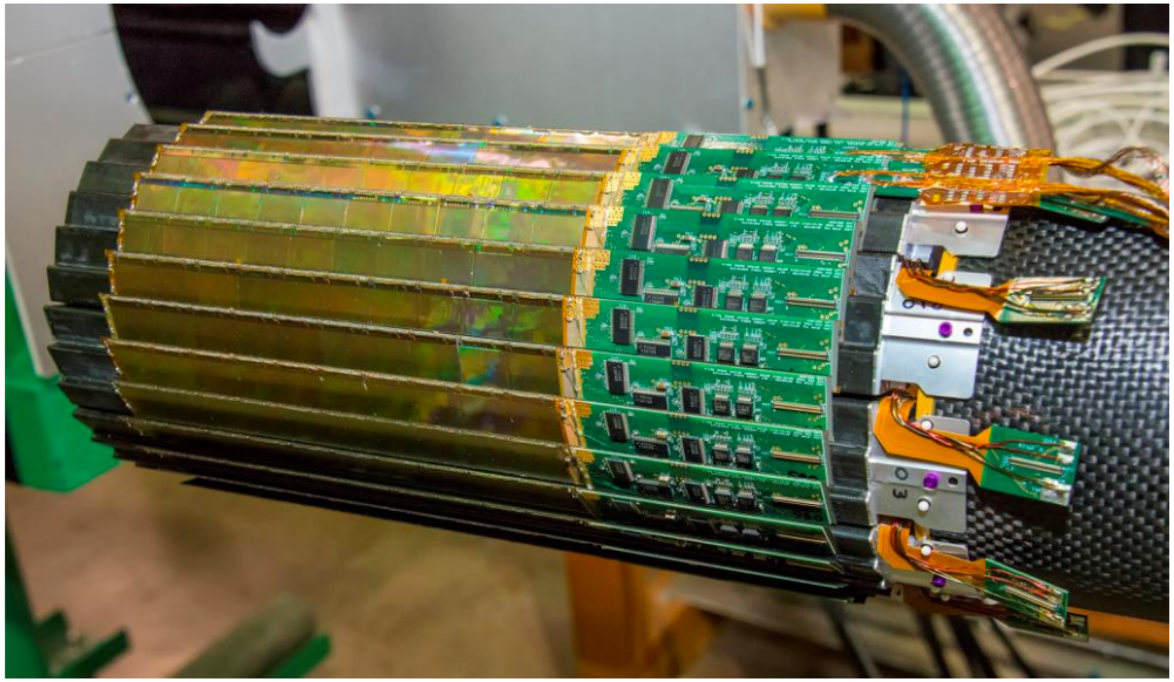
Elba…



VERTEX 2016
The 25th International Workshop on Vertex Detectors
A forum to exchange the experiences
and needs of the community,
and to review recent, ongoing,
and future activities
on silicon-based vertex detectors
La Biodola (Isola d'Elba, Italy) 25-30 September 2016

STAR

Operational Experience of the STAR MAPS Vertex Detector



Leo Greiner *for the STAR Collaboration*
Lawrence Berkeley National Laboratory
VERTEX 2016 - 25th International Workshop on Vertex Detectors
La Biodola, Isola d'Elba, Italy, 25-30 September 2016

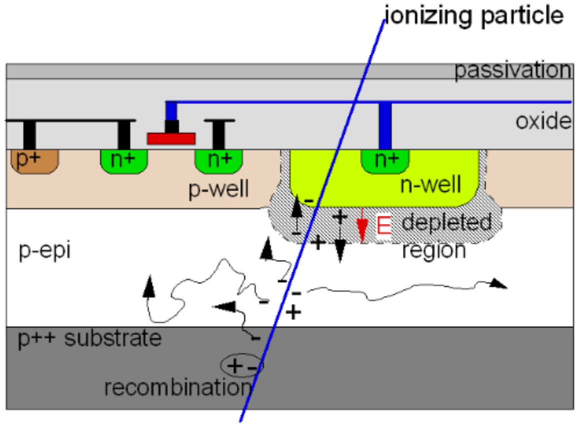
PXL Design Parameters

DCA Pointing resolution	$(10 \oplus 24\ \mathrm{GeV}/p\cdot c)\ \mu m$
Layers	Layer 1 at 2.8 cm radius Layer 2 at 8 cm radius
Pixel size	20.7 μm X 20.7 μm
Hit resolution	3.7 μm (6 μm geometric)
Position stability	5 μm rms (20 μm envelope)
Material budget first layer	X/X_0 = 0.39% (Al conductor cable)
Number of pixels	356 M
Integration time (affects pileup)	185.6 μs
Radiation environment	20 to 90 kRad / year $2*10^{11}$ to 10^{12} 1MeV n eq/cm^2
Rapid detector replacement	< 1 day

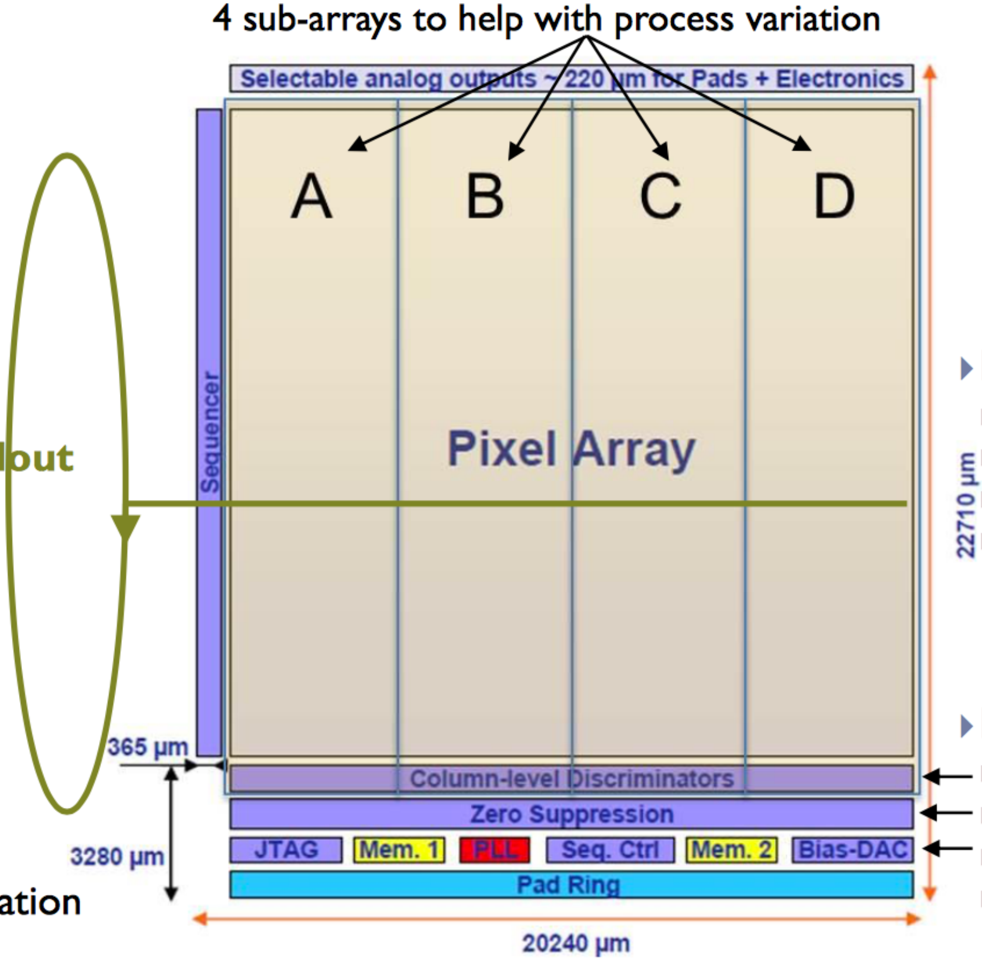
- 356 M pixels on ~0.16 m^2 of Silicon
- Air cooling
- Sensors thinned to 50 μm

PXL *MAPS* sensor

- *Ultimate-2:* third revision sensor developed for PXL by the PICSEL group of IPHC, Strasbourg
- AMS OPTO 0.35 process
- Binary readout of hit pixels



- High resistivity p-epi layer
  - Reduced charge collection time
  - Improved radiation hardness
- S/N ~ 30
- MIP Signal ~ 1000 e-
- **Rolling-shutter type readout**
  - A row is selected
  - For each column, a pixel is connected to discriminator
  - Discriminator detects possible hit
  - Move to next row
- 185.6 µs integration time
- ~170 mW/cm² power dissipation


4 sub-arrays to help with process variation

- **Pixel matrix**
  - 20.7 µm x 20.7 µm pixels
  - 928 rows x 960 columns = ~1M pixel
  - In-pixel amplifier
  - In- pixel Correlated Double Sampling (CDS)
- **Digital section**
  - End-of-column discriminators
  - Integrated zero suppression (up to 9 hits/row)
  - Ping-pong memory for frame readout (~1500 w)
  - 2 LVDS data outputs @ 160 MHz

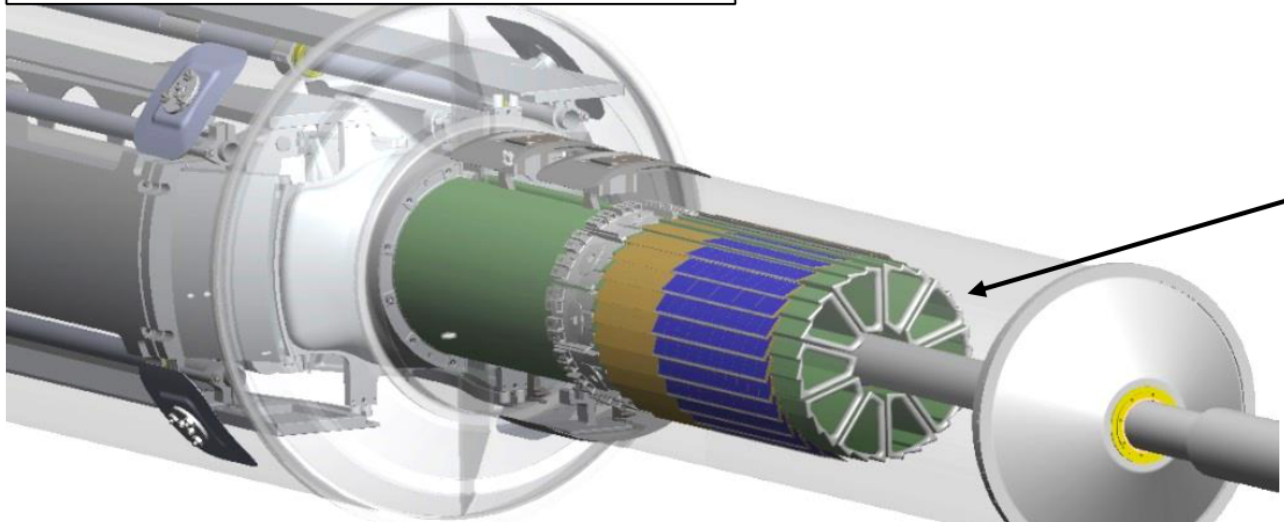
PXL System Overview

Basic Detector Element

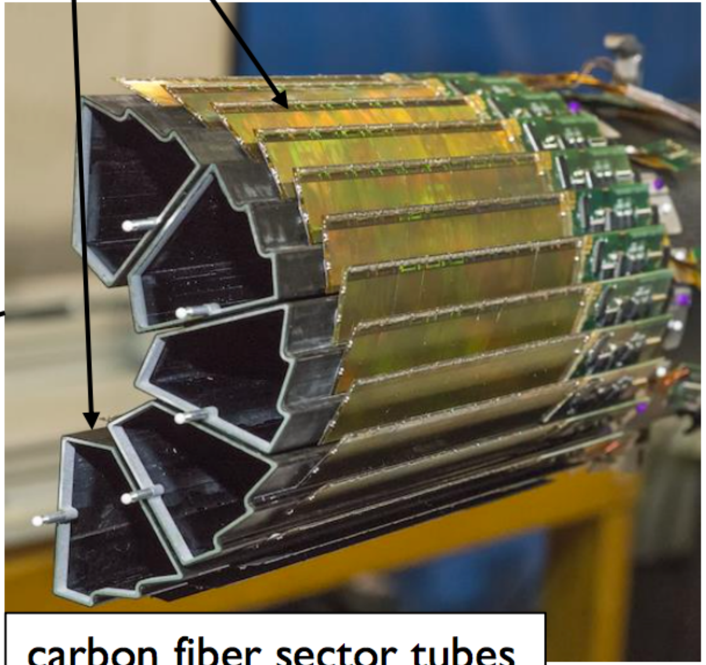
Ladder with 10 MAPS sensors (~ 2×2 cm each)

10 sensors / ladder
4 ladders / sector
5 sectors / half
10 sectors total

Mechanical support with kinematic mounts (insertion side)



Cantilevered support

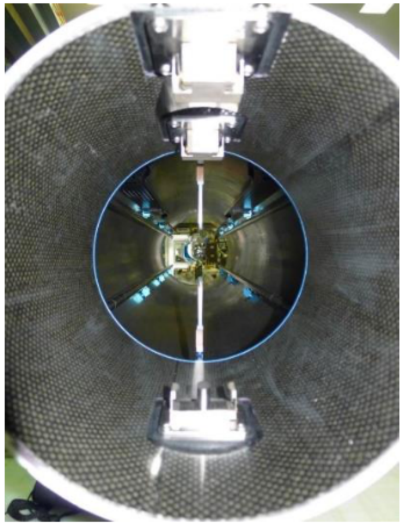


carbon fiber sector tubes (~ 200 µm thick)

Operational Aspects

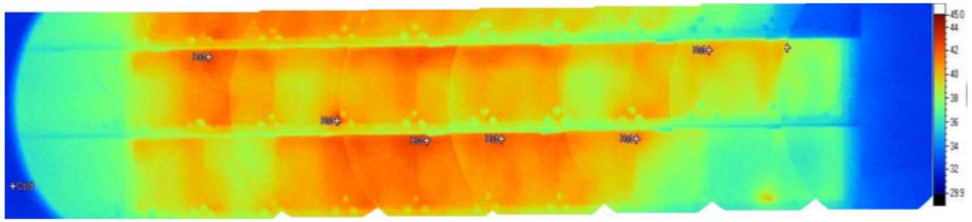
What worked **well** and what needed extra effort (after initial setup):

- Mechanics –
  - The detector halves maintained survey pixel positions after insertion and during operational heating and in the cooling airflow (10 m/s).
  - The rapid insertion and removal mechanism worked allowing removal and replacement operation of a 2nd detector in one day.
- Air cooling worked very well, typical variation in sensor temperature over the runs was within 1-2 degree C.



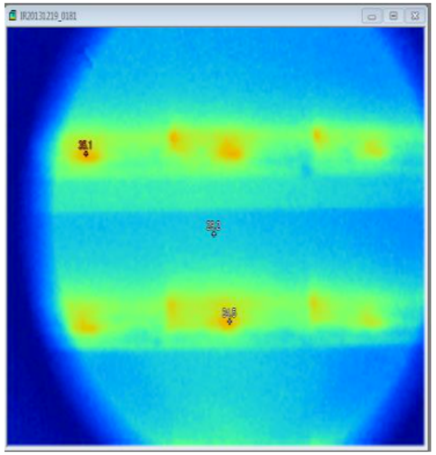
PXL Kinematic mounts

Sector vibration in the radial direction scales as:	flow^2
Sector vibration at full flow:	5 μm RMS
Sector DC displacement scales as:	flow^2
Sector moves in at full flow: **(Stable displacement)**	25 μm - 30 μm
Sector moves in when ladders powered: **(Stable displacement)**	3 μm - 8 μm



Composite IR image of PXL test ladders

IR image of production PXL ladders. Max ΔT is 12° C from ambient.



Development and construction of the Belle II DEPFET pixel vertex detector

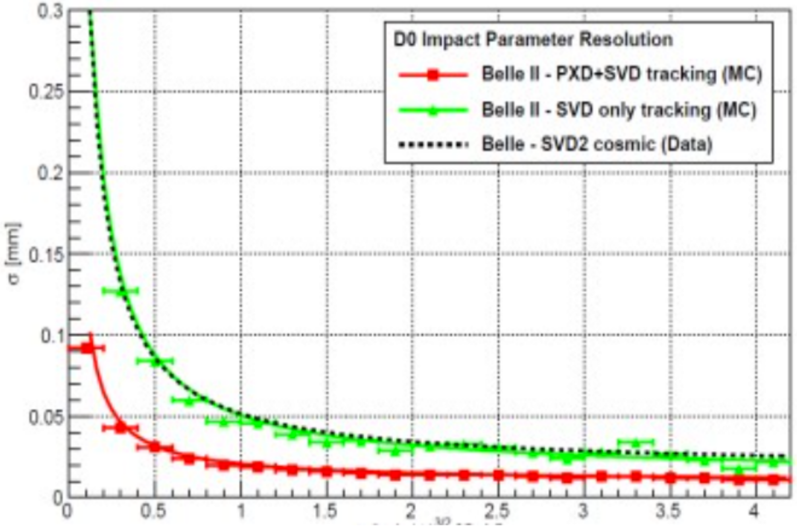
Vertex 2016, 25-30 September 2016

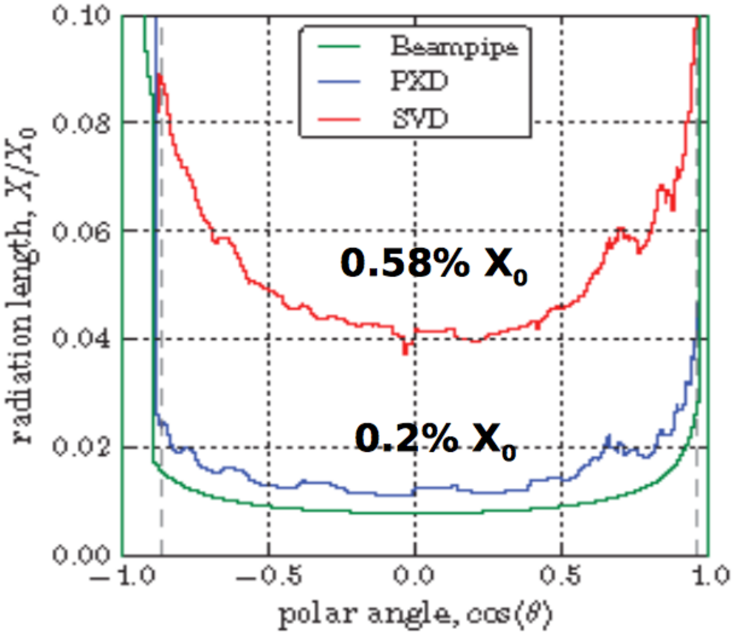
B. Schwenker for the DEPFET collaboration

GEORG-AUGUST-UNIVERSITÄT
GÖTTINGEN

Belle II vertexing requirements

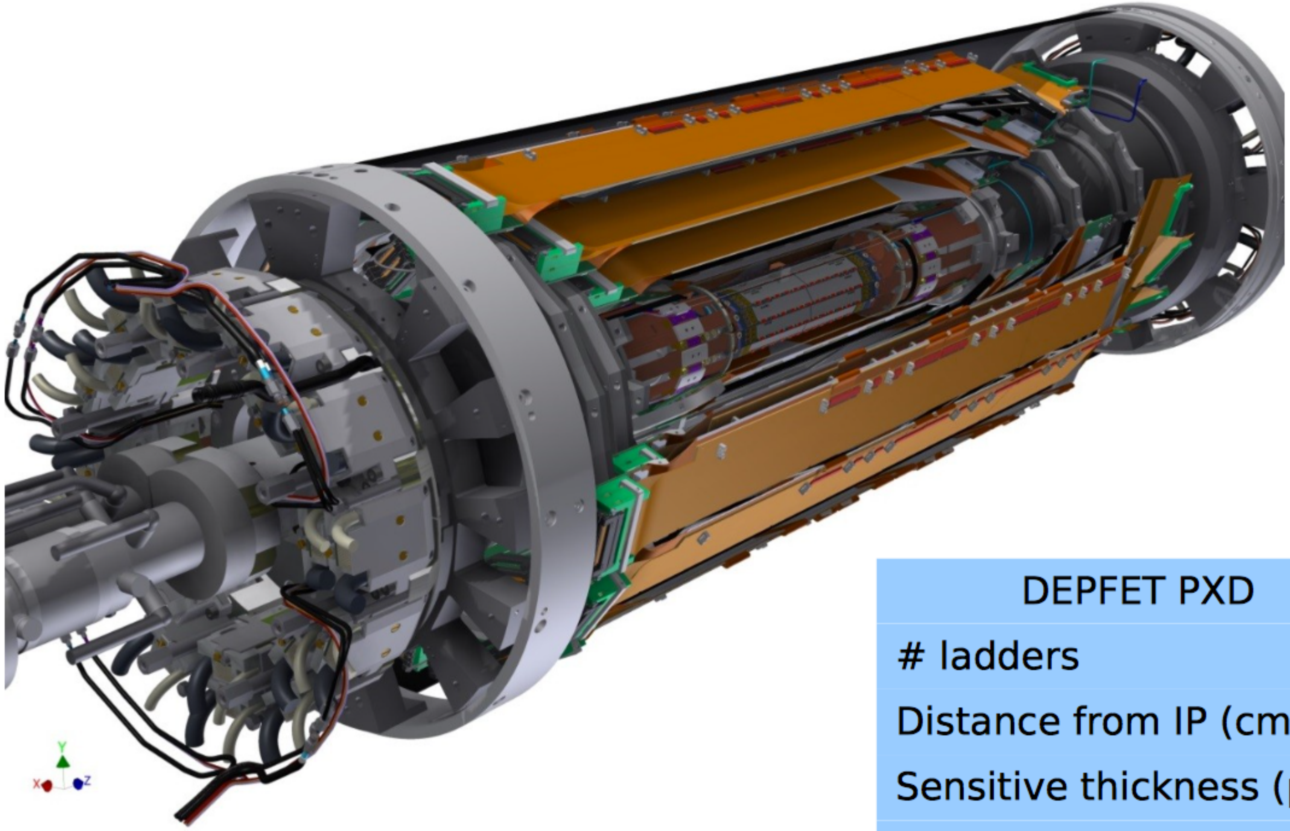
	Belle II PXD
Radiation	2 Mrad/year
	$2 \cdot 10^{12}$ 1 MeV n_{eq} per year
Duty cycle	1
Frame time	20 µs
Momentum range	50 MeV < p < multi GeV
Acceptance	17°-155°
Material budget	$0.2\%\ X_0$

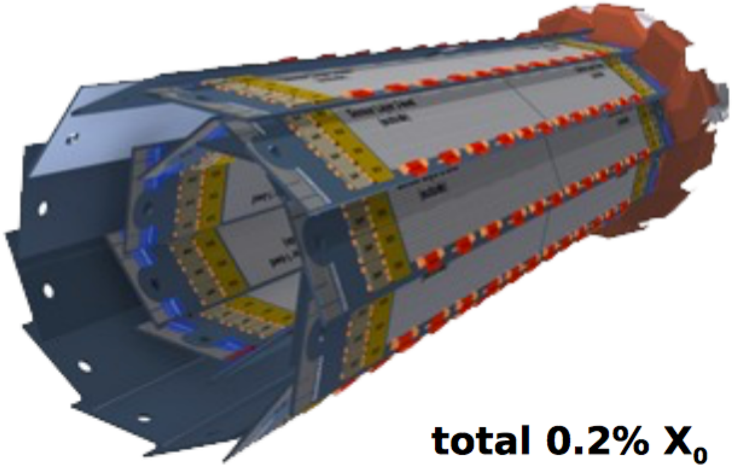




- Modest impact paramter resolution (15 µm), dominated by multiple scattering → pixel size (50 x 75 µm²)
- Lowest possible material budget (0.2% X)
  - Ultra-transparent detectors
  - Lightweight mechanics and minimal services

The Belle II vertex detector





total 0.2% X_0

- 2 DEPFET layers (PXD)
- 4 Double Sided Si-Strip Detector layers (SVD)
- **PXD + SVD integration Nov. 2017**

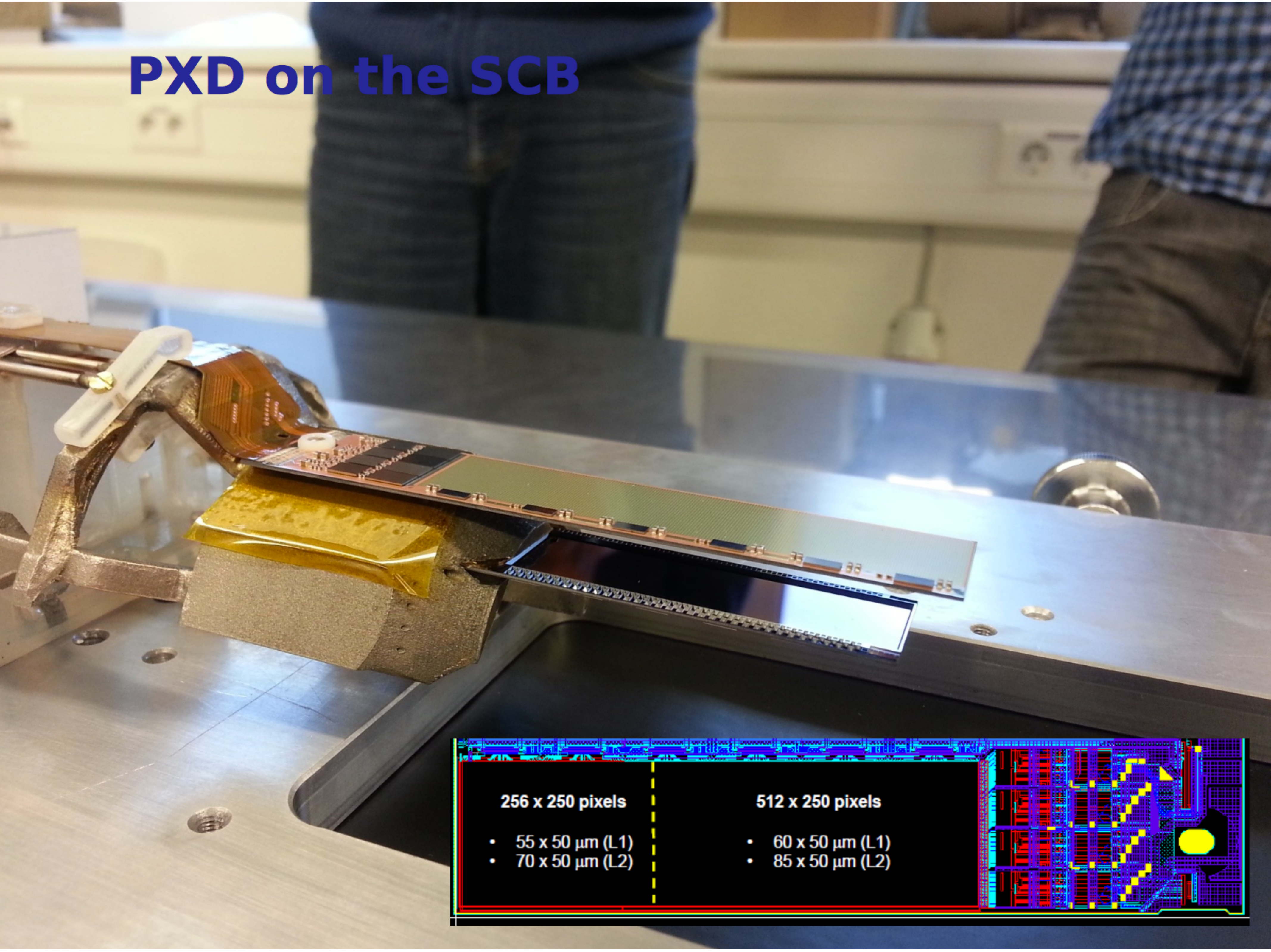
DEPFET PXD	L1	L2
# ladders	8	12
Distance from IP (cm)	1.4	2.2
Sensitive thickness (µm)	75	75
#pixels/module	768x250	768x250
Total no. of pixels	3.072×10^6	4.608×10^6
Pixel size (µm²)	55x50 60x50	70x50 85x50
Frame/row rate	50kHz/10MHz	50kHz/10MHz
Total sensitive Area (cm²)	89.6	176.9

VXD Phase 2 hardware (Beast)

- Machine commissioning
- Radiation safe environment for the VXD
- 2 PXD and 4 SVD ladders
- +X direction, highest sensitivity to backgrounds

Integration of the phase 2 hardware (incl. other radiation monitors): November 2016 @ DESY
Installation at KEK: July 2017

PXD on the SCB

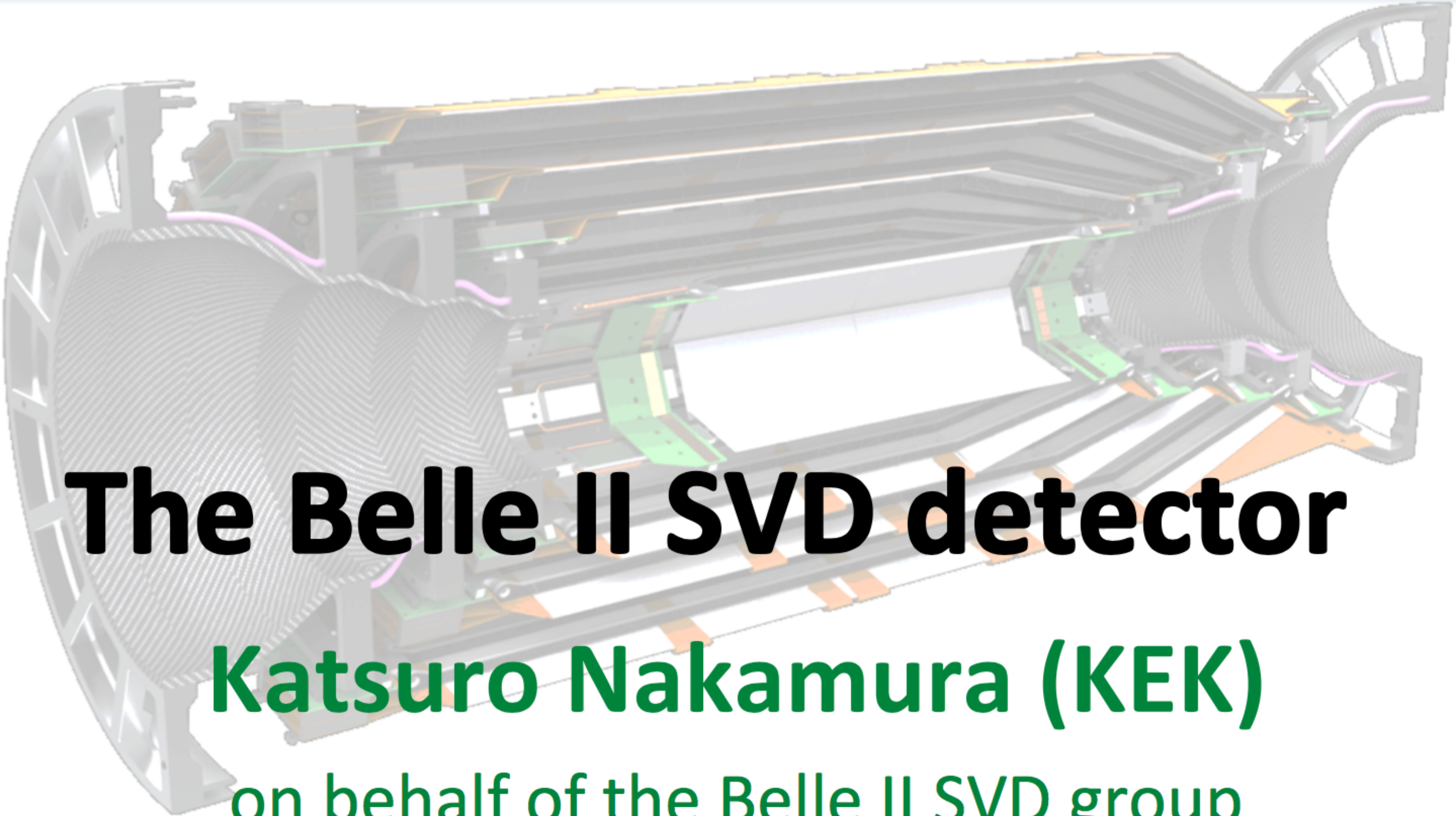


256 x 250 pixels

- 55 x 50 µm (L1)
- 70 x 50 µm (L2)

512 x 250 pixels

- 60 x 50 µm (L1)
- 85 x 50 µm (L2)



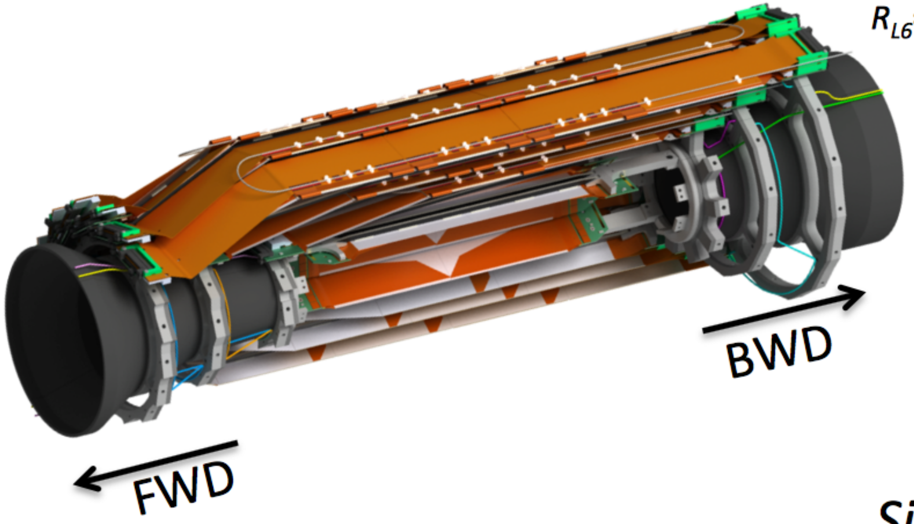
The Belle II SVD detector

Katsuro Nakamura (KEK)

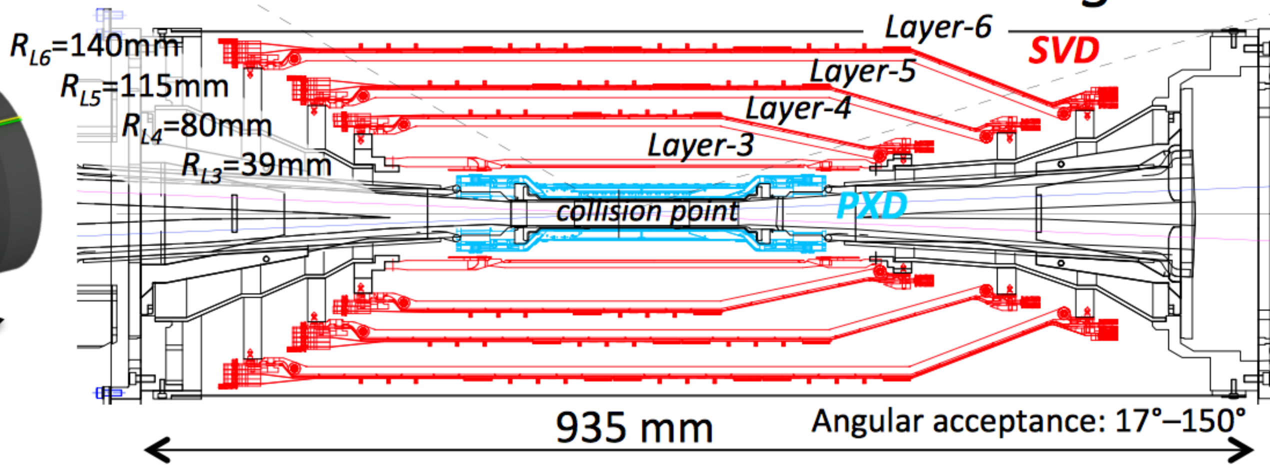
on behalf of the Belle II SVD group

VERTEX2016 Sep. 26, 2016

SVD Detector Overview



SVD model

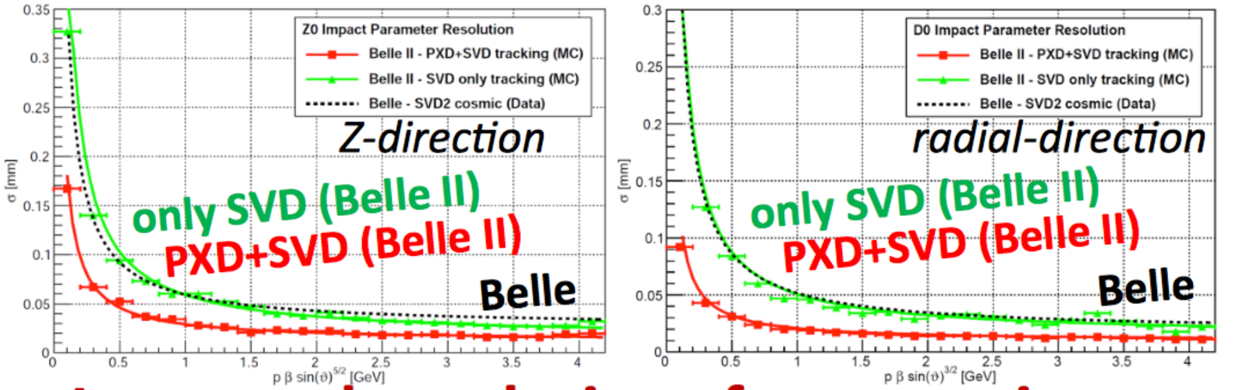


PXD+SVD cross section drawing

Angular acceptance: 17°–150°

- **4 SVD layers (Layer-3 to -6) consist of ladders.**
- **The ladders are composed of several DSSD modules.**
- **Slant shapes in FWD region for the material budget reduction.**
- **Average material budget: $0.7\%X_0$ per layer**

Simulated resolution for track impact parameter (IP)

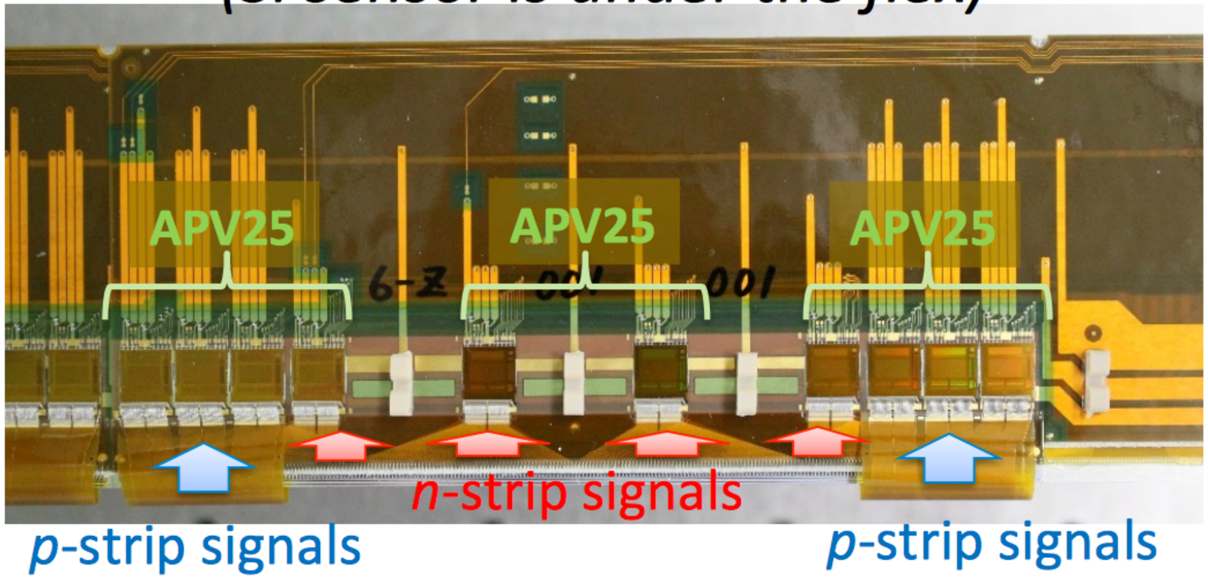


Improved resolutions from previous Belle experiment are expected.

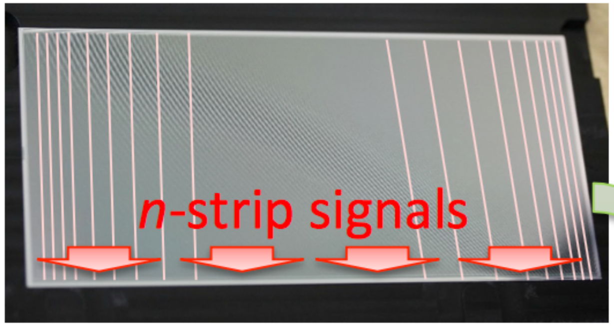
σ_{IP} ~ 20um at p_T = 2GeV/c

Chip-On-Sensor Concept

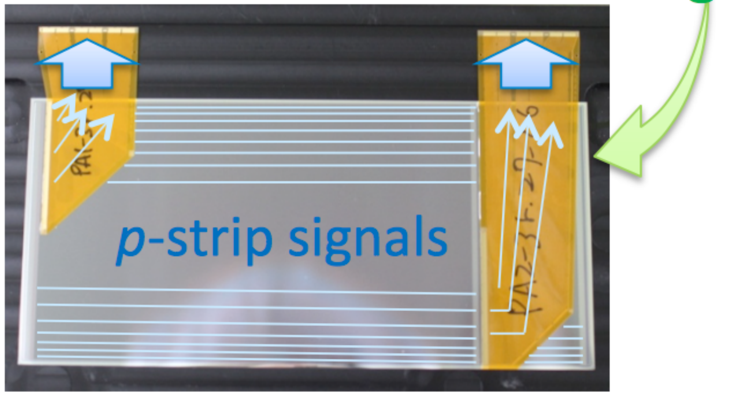
ORIGAMI flex
(Si sensor is under the flex)



Sensor under ORIGAMI (n-strips)

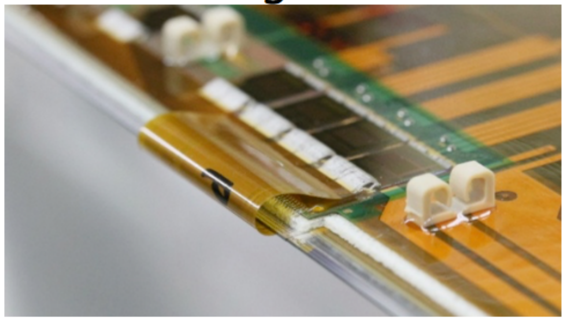


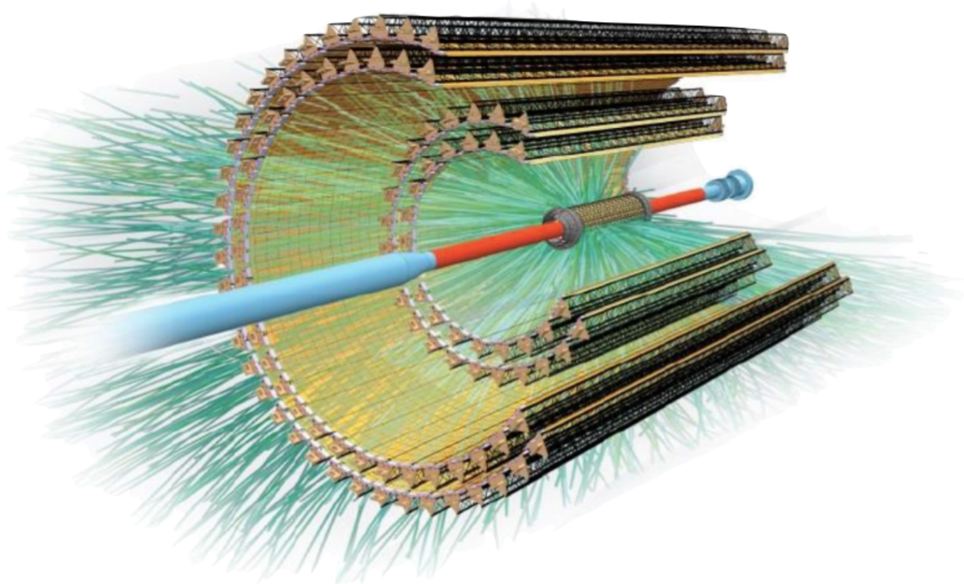
Sensor from other side (p-strips)



- **Flex circuit (ORIGAMI flex) is glued on sensor *n*-strip surface with an electrical/thermal-isolation foam.**
- **APV25 are placed on the ORIGAMI flex to minimize the analog path length (capacitive noise).**
  - Sensor strips and ORIGAMI flex are connected with Al wire-bonding (ϕ25μm).

Wire bonding with Al wires.



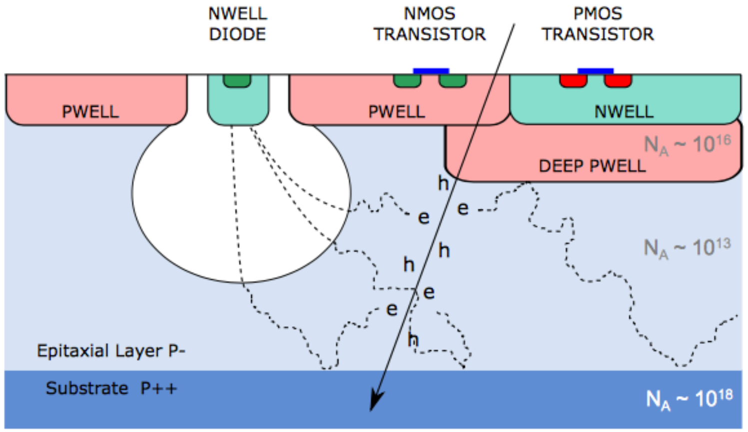


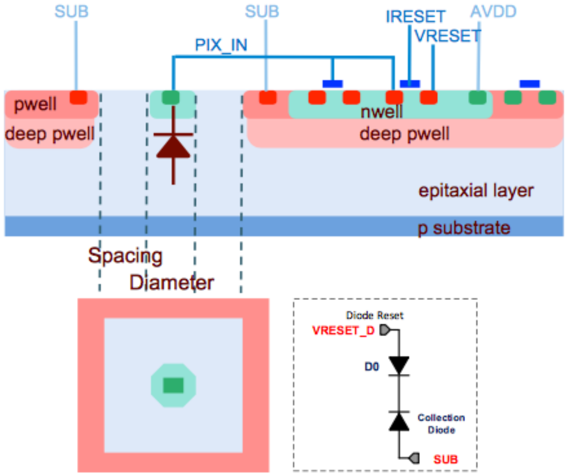
The Upgrade of the ALICE ITS

Stefania Beolè
Università degli Studi di Torino & INFN

on behalf of the ALICE collaboration

ALPIDE – Technology and Pixel Layout





CMOS Pixel Sensor - TowerJazz 0.18μm CMOS Imaging Process

- High-resistivity (> 1kΩ cm) p-type epitaxial layer (25μm) on p-type substrate
- Small n-well diode (2 μm diameter), ~100 times smaller than pixel => low capacitance (~fF)
- Reverse bias voltage (-6V < V_{BB} < 0V) to substrate (contact from the top) to increase depletion zone around NWELL collection diode
- Deep PWELL shields NWELL of PMOS transistors (full CMOS circuitry within active area)

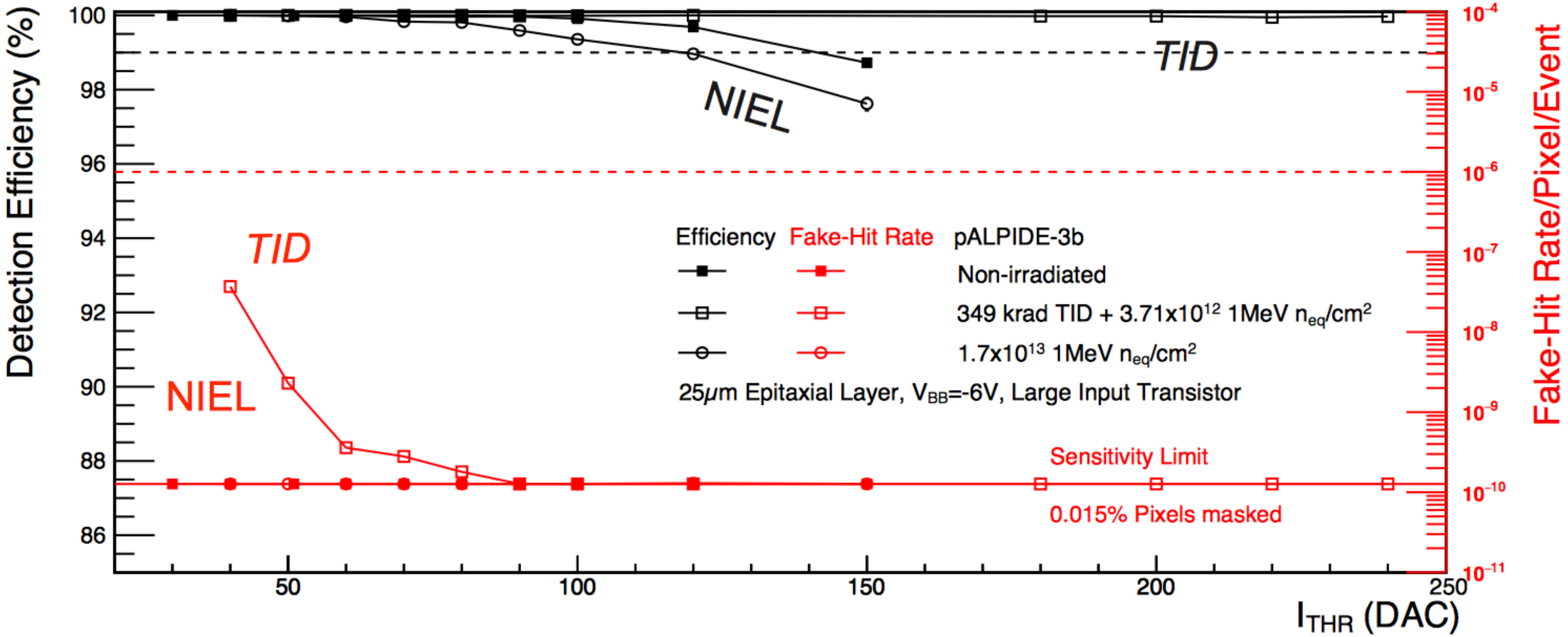
Pixel Chip Requirements

Pixel chip developed
for the ITS Upgrade

Parameter	Inner Barrel	Outer Barrel	ALPIDE
Silicon thickness	50µm	100µm	✔
Spatial resolution	5µm	10µm	~ 5µm
Chip dimension	15mm x 30mm		✔
Power density	< 300mW/cm^2	< 100mW/cm^2	**< 40mW/cm^2**
Event-time resolution	< 30µs		**~ 2µs**
Detection efficiency	> 99%		✔
Fake-hit rate *	< 10^{-6}/event/pixel		**<<< 10^{-6}/event/pixel**
NIEL radiation tolerance **	1.7x10^{13} 1MeV n$_{eq}$/cm^2	10^{12} 1MeV n$_{eq}$/cm^2	✔
TID radiation tolerance **	2.7Mrad	100krad	so far tested at 350krad

* revised numbers w.r.t. TDR
** including a safety factor of 10, revised numbers w.r.t. TDR

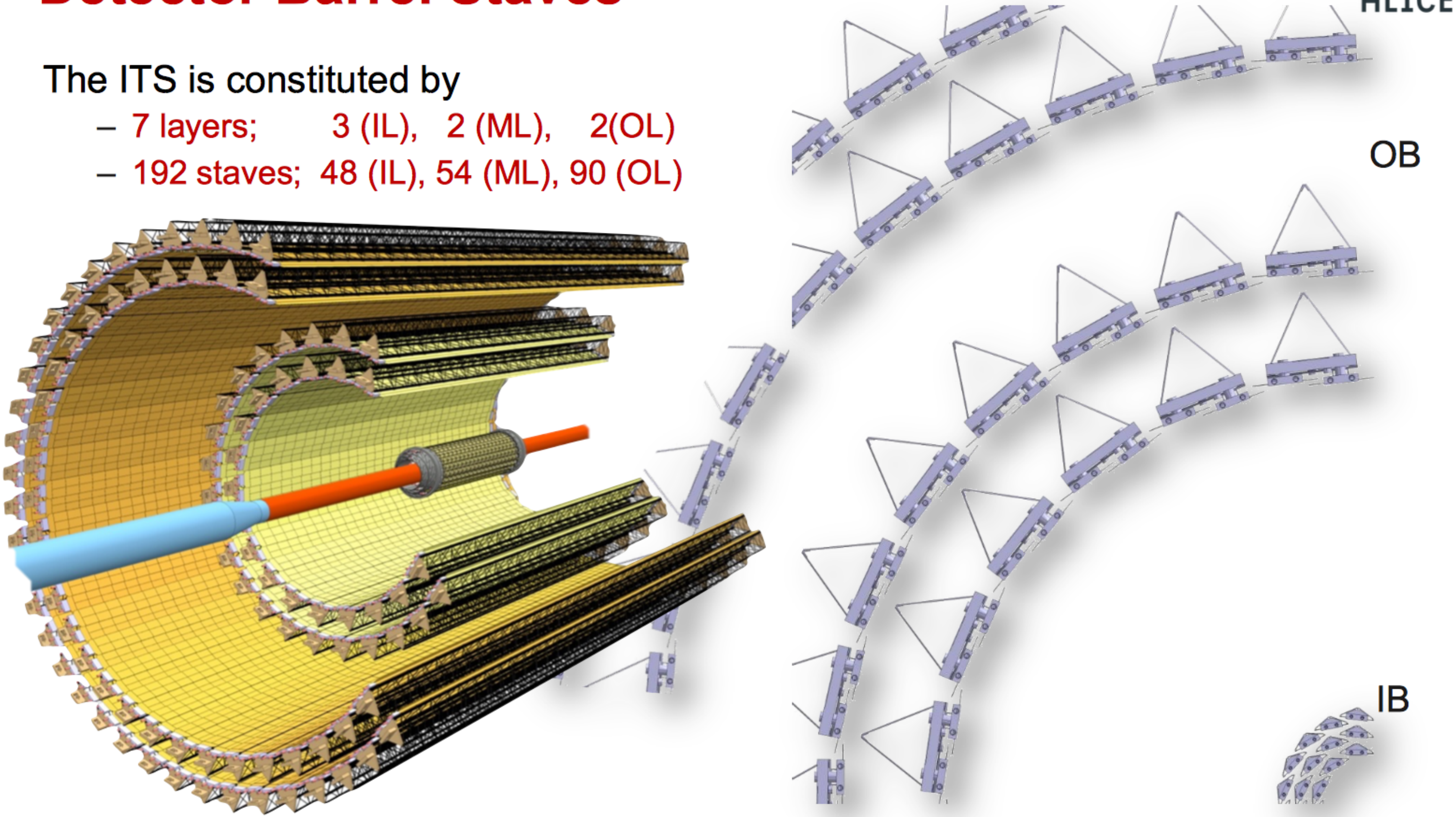
Test Beam Result of a Full-Scale ALPIDE Prototype (pALPIDE3): detection efficiency and noise occupancy



- Test beam Campaigns at PS (CERN), BTF (Frascati), DESY (Hamburg), Pohang (Korea) and SLRI (Thailand) – telescope made of pALPIDE3 sensors only
- Final pixel layout and front-end circuit selected
- Radiation effects visible
- Large operational margin maintained after NIEL and TID irradiation

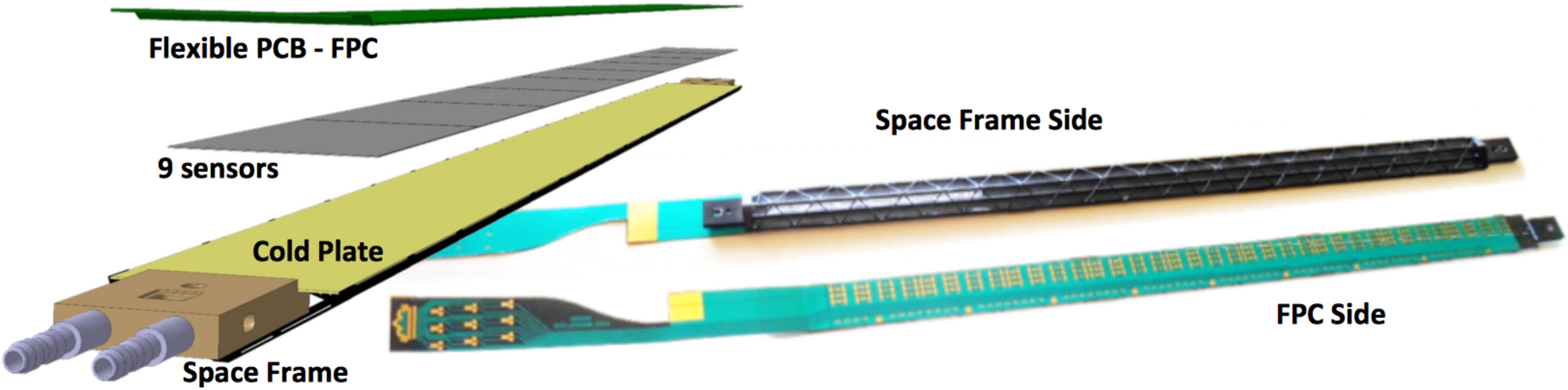
Detector Barrel Staves

The ITS is constituted by
- 7 layers; 3 (IL), 2 (ML), 2(OL)
- 192 staves; 48 (IL), 54 (ML), 90 (OL)

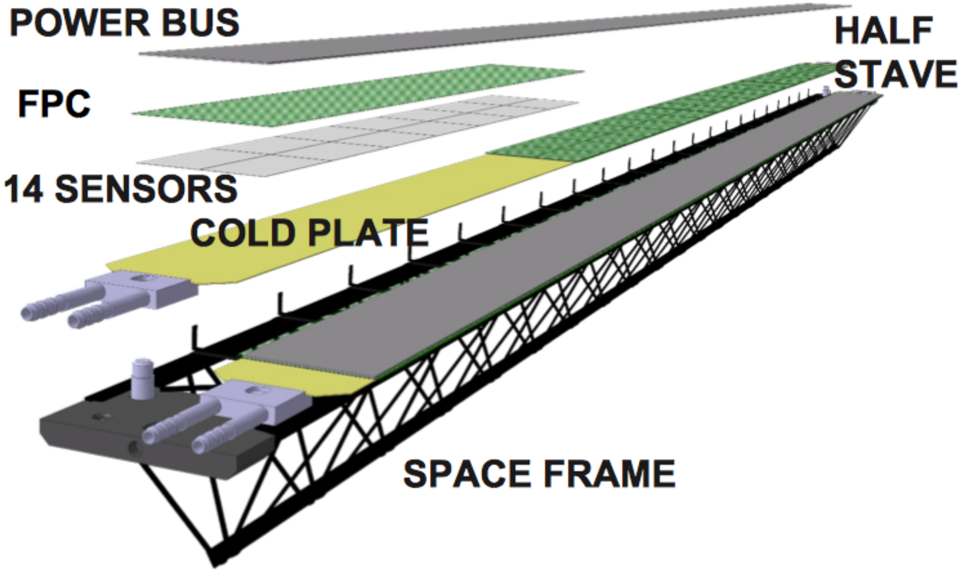


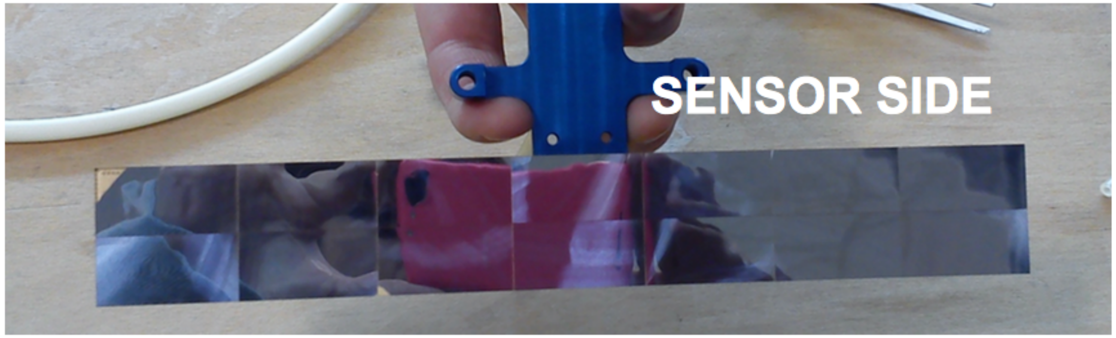
Layer #	6	5	4	3	2	1	0
n. of Staves	48	42	30	24	20	16	12

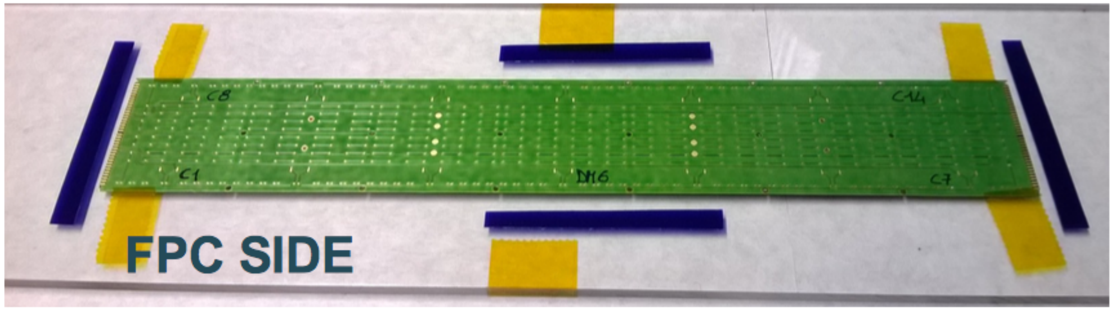
INNER BARREL STAVE



OUTER BARREL STAVE





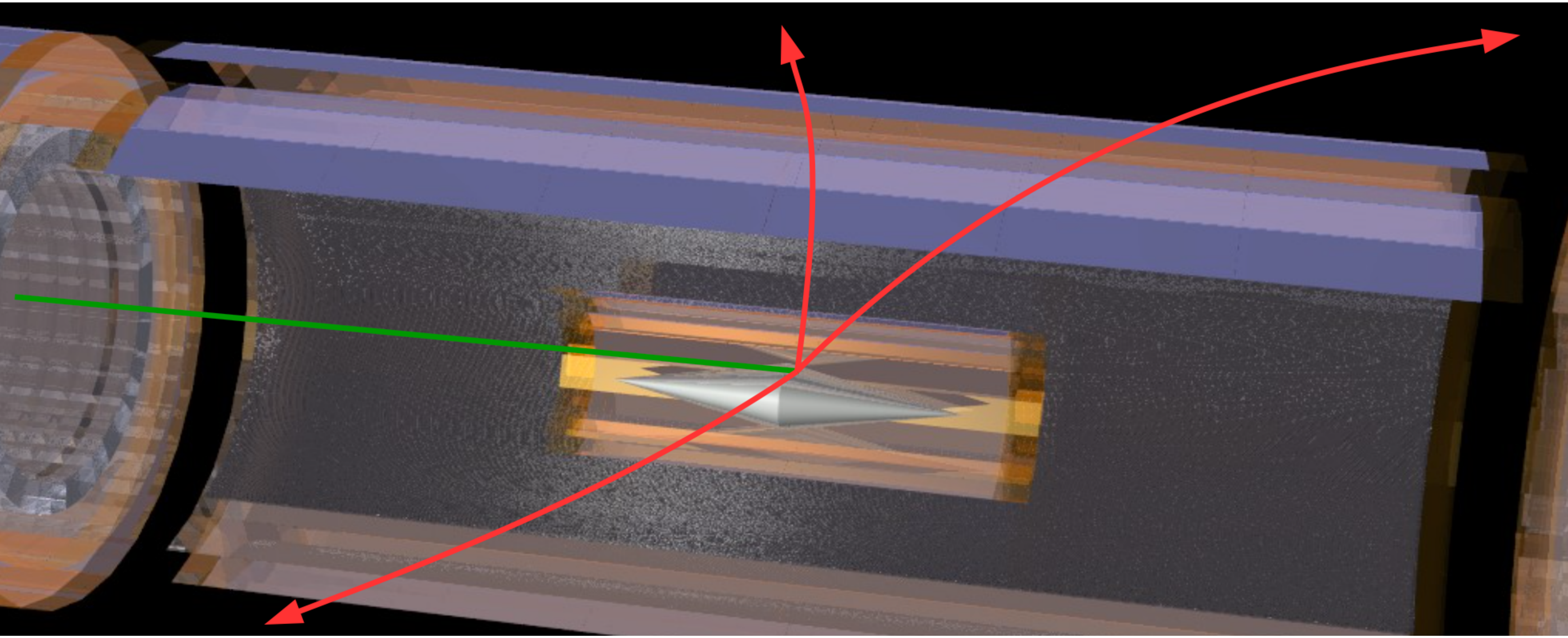


The Mu3e Pixel Detector

Vertex 2016, 26.-30. September, 2016

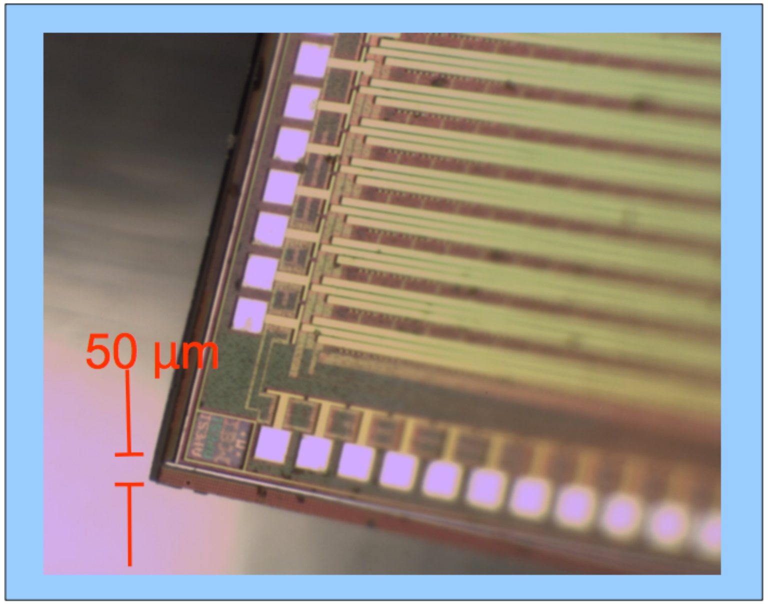
André Schöning

Physikalisches Institut, Universität Heidelberg



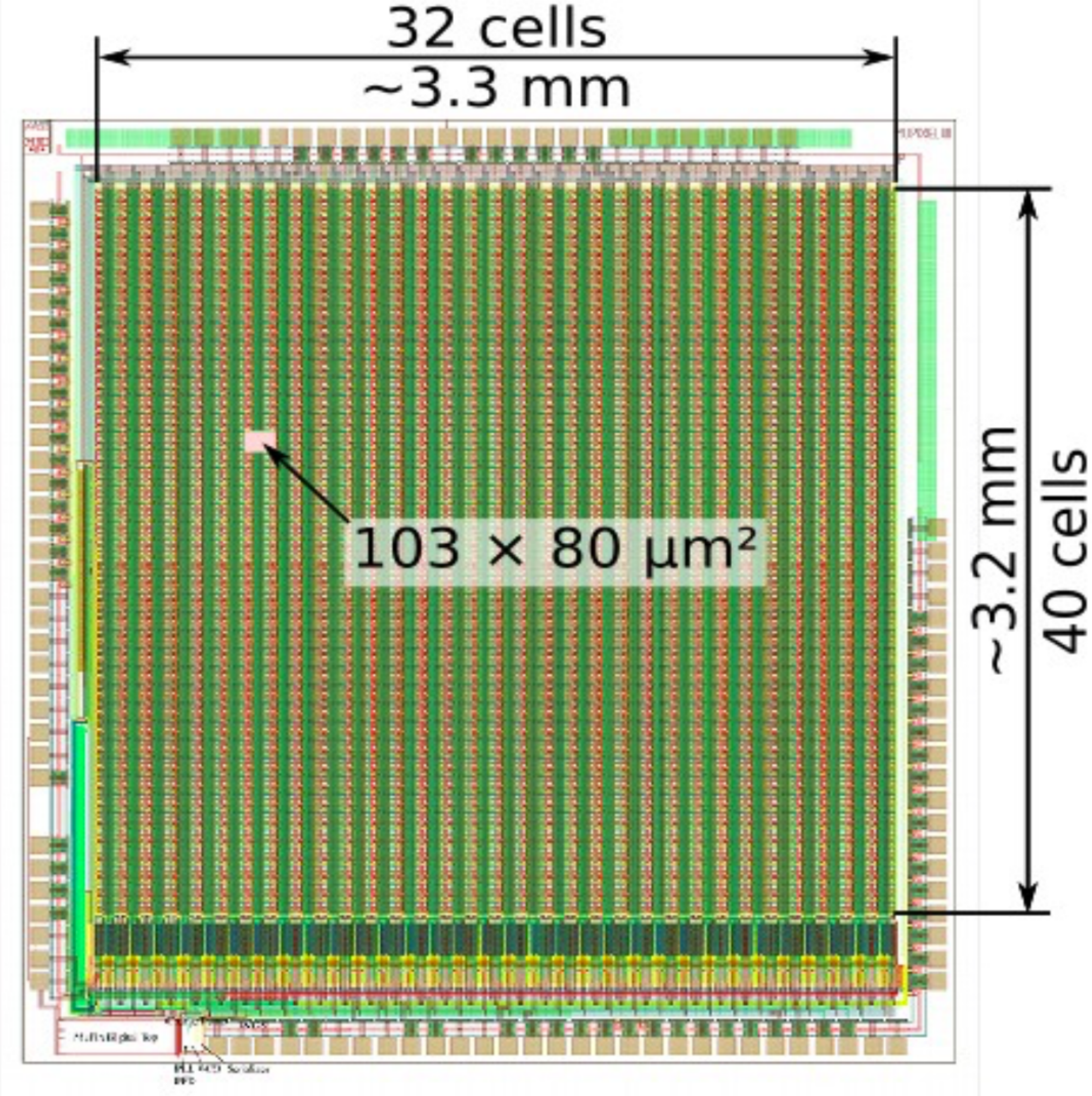
MuPix7 Prototype

Institutes: Heidelberg, Karlsruhe, Mainz



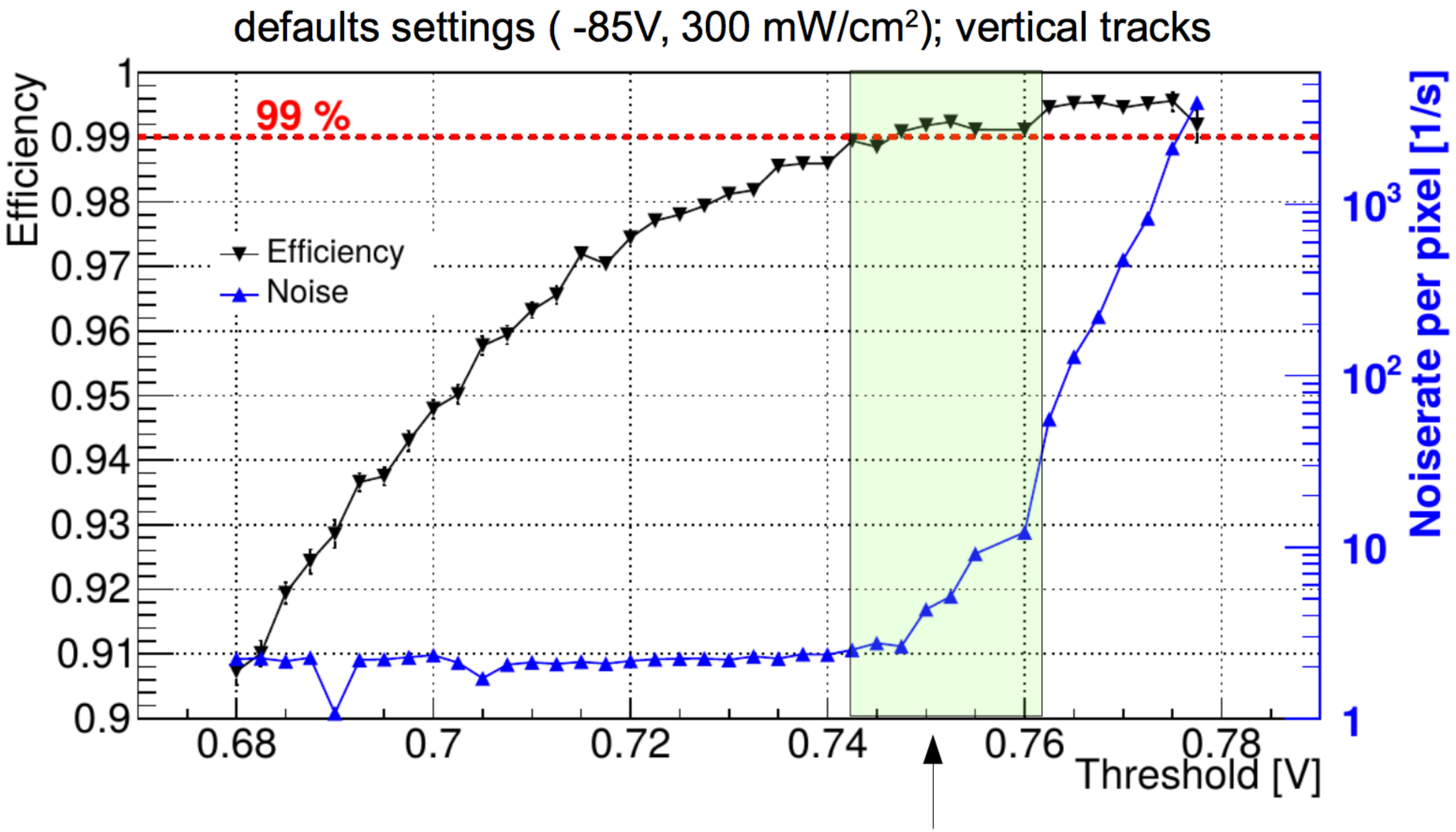
Austria Microsystems (AMS)
HV-CMOS 180 nm

20 Ωcm p-substrate



MuPix7 Efficiency and Noise

Data obtained from PSI beamtest (PiM1) using MuPix telescope

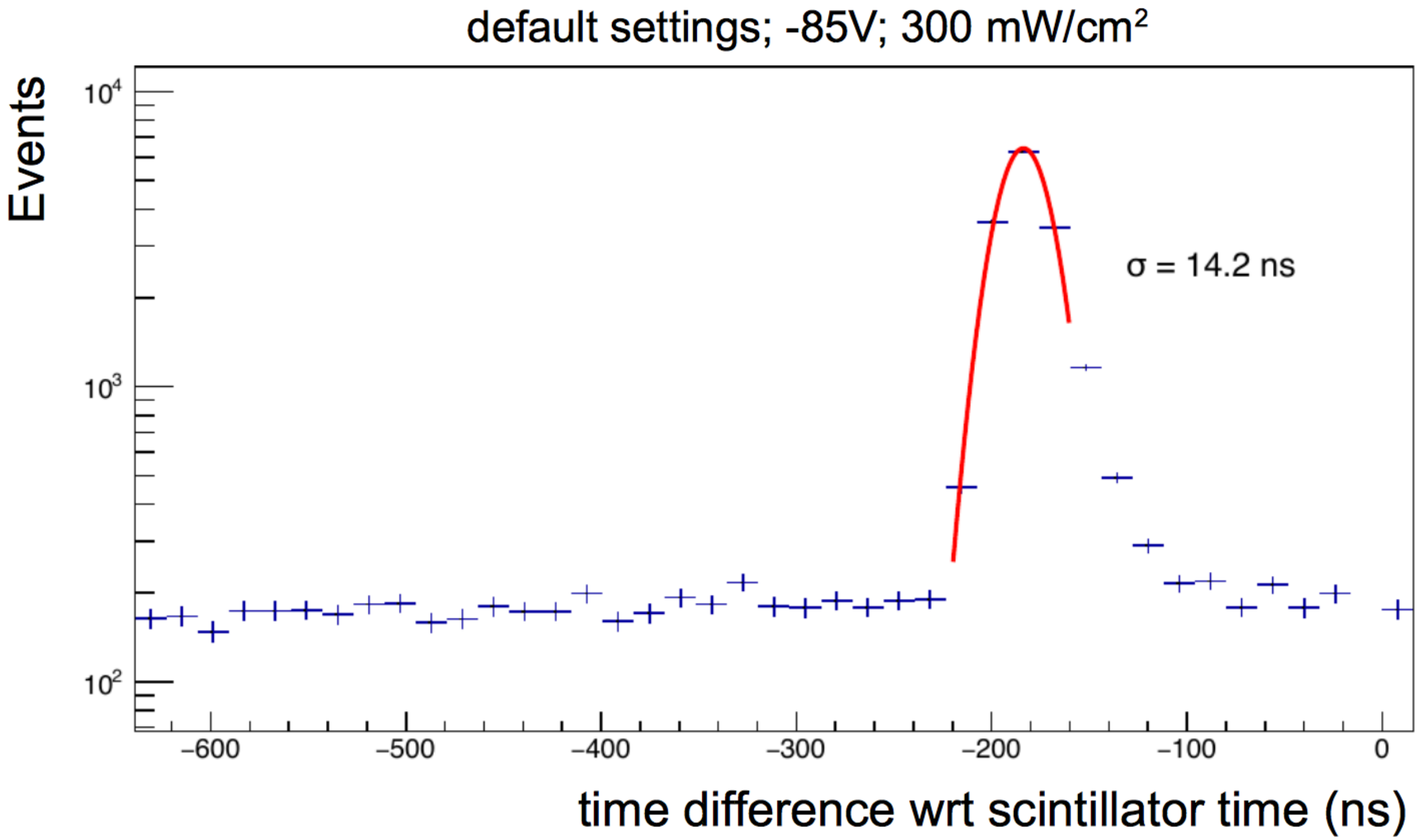


Mu3e noise limit <10^{-6}

operation region

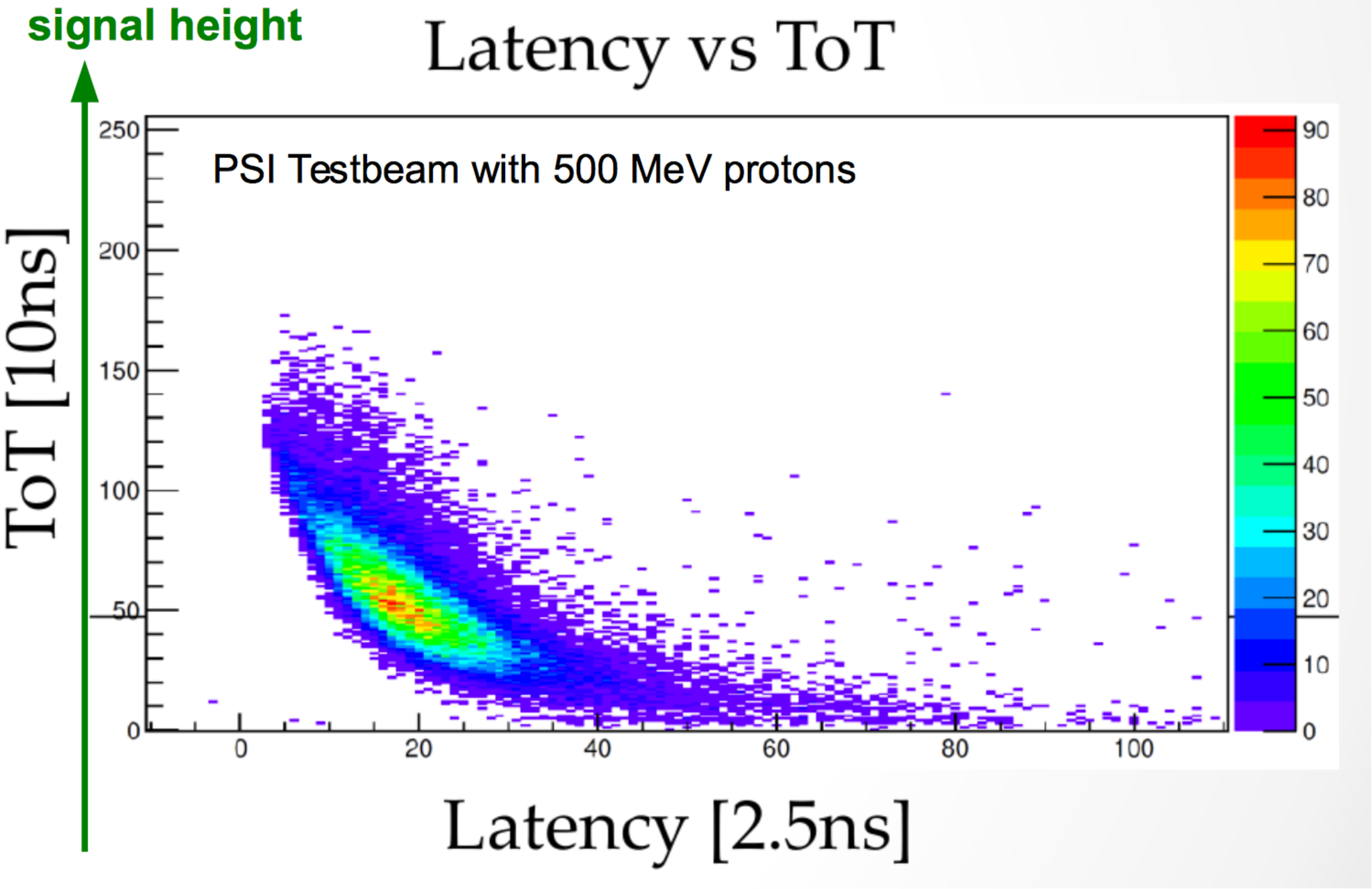
MuPix7 Time Resolution

MuPix telescope with scintillator as time reference:



Mu3e requirement sigma (t) < 20 ns fulfilled

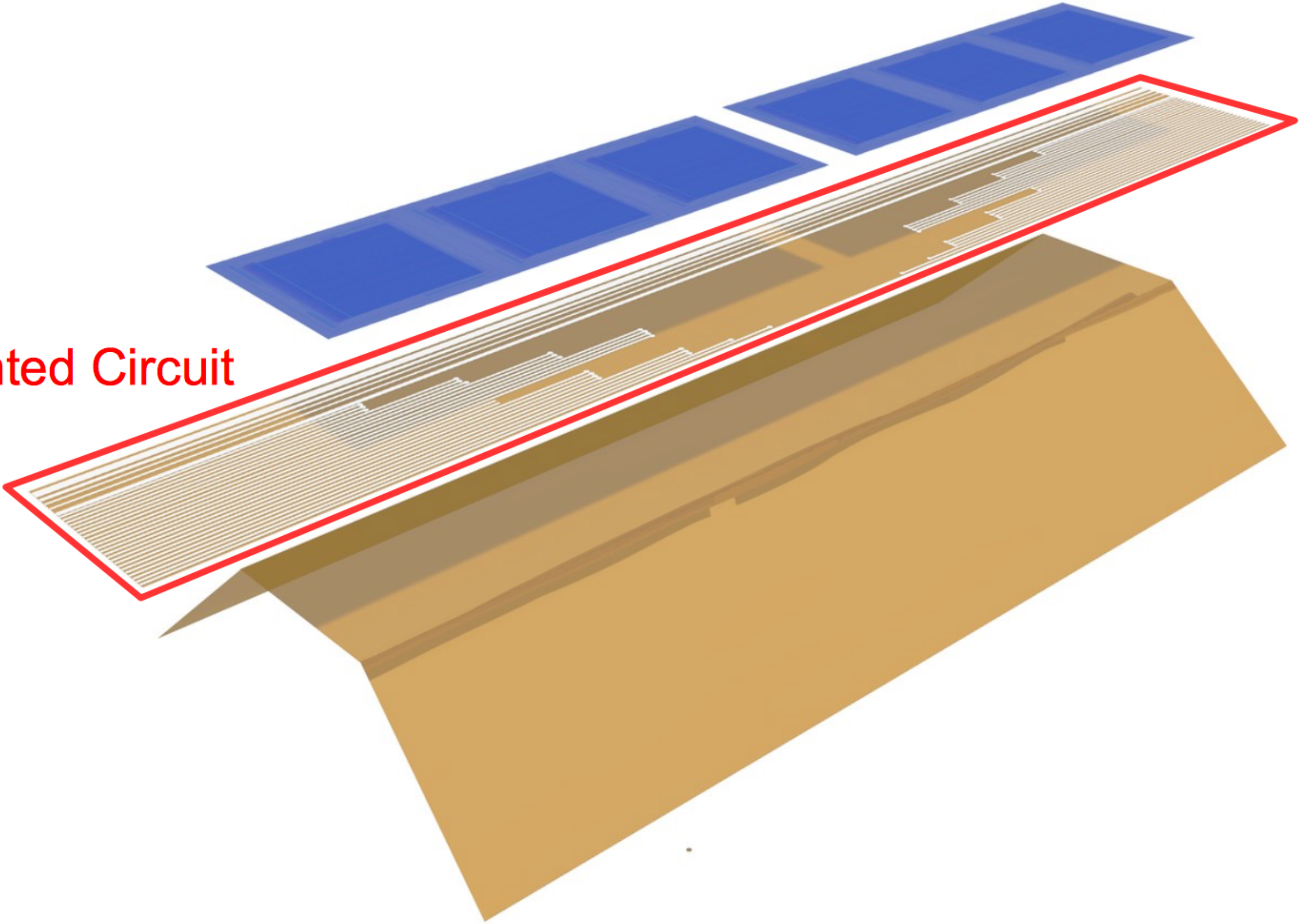
MuPix7 Time Resolution



→ timewalk correction possible

→ in test chips sigma(t) ~ 5 ns achieved (I. Peric et al. KIT)

Mu3e Flexprint



Flexible Printed Circuit Board (FPC)

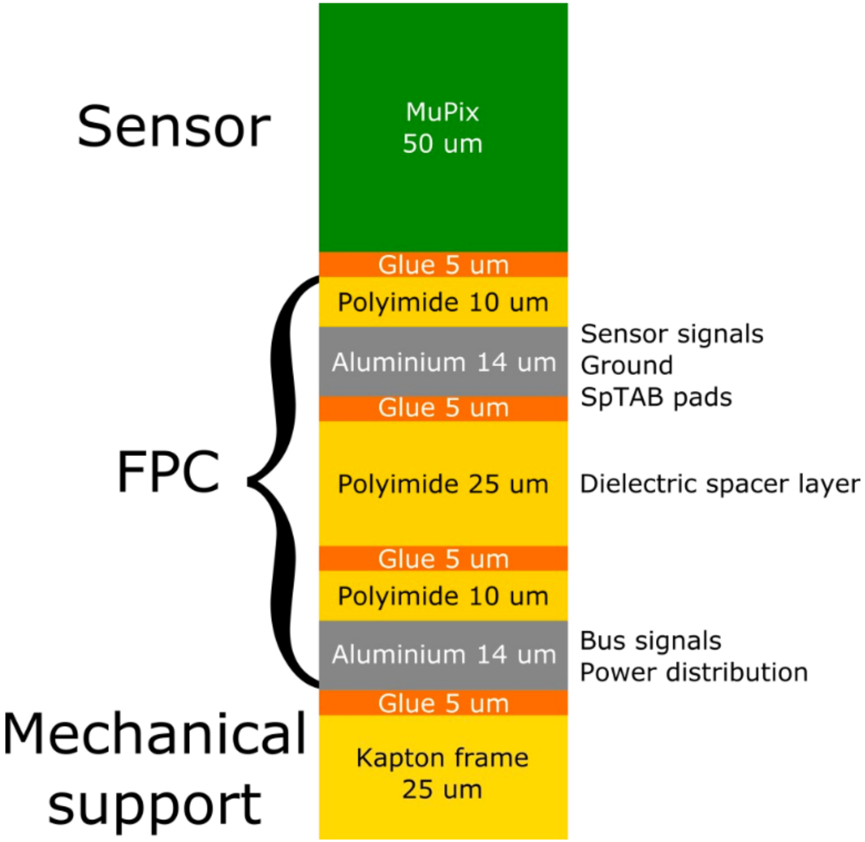
Mu3e Flexprint

Two layer aluminium (LTU Ltd.)

- 14µm Al + 10µm polyimide per layer
- Structure sizes ≥ 65µm
- Dielectric spacing 45µm

SpTAB technology

- Single point Tape Automated Bonding
- No additional (high Z) material for bonding!



Sensor

MuPix 50 um

Glue 5 um

FPC

Polyimide 10 um

Aluminium 14 um — Sensor signals, Ground, SpTAB pads

Glue 5 um

Polyimide 25 um — Dielectric spacer layer

Glue 5 um

Polyimide 10 um

Aluminium 14 um — Bus signals, Power distribution

Glue 5 um

Mechanical support

Kapton frame 25 um

universitätbonn

SI LAB
Silizium Labor Bonn

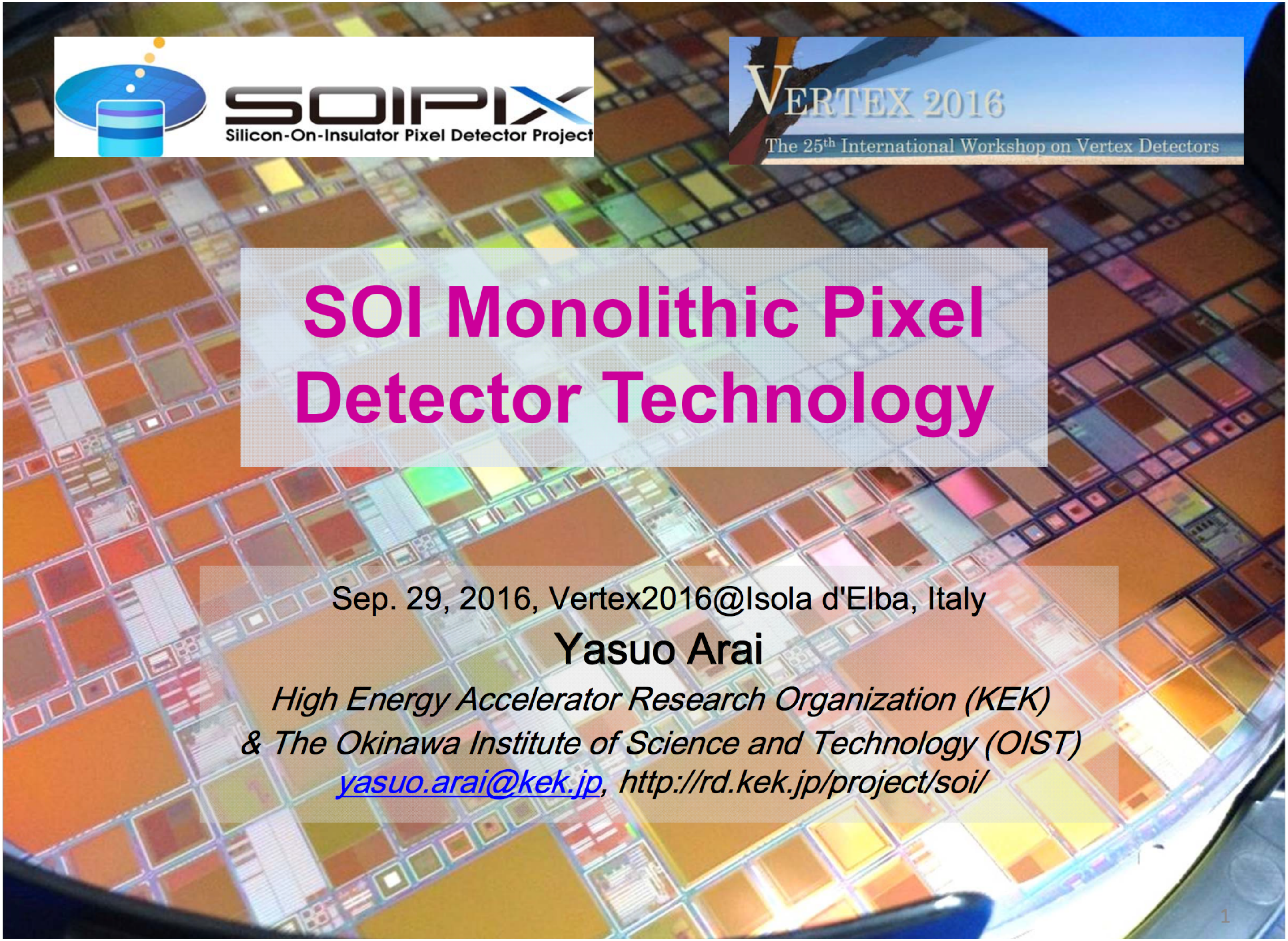
CMOS pixel development for HL-LHC

F. Hügging
University of Bonn

VERTEX 2016
ELBA, ITALY

huegging@physik.uni-bonn.de

La Biodola, Isola d'Elba, Italy - 25-30 September 2016



SOIPIX
Silicon-On-Insulator Pixel Detector Project

VERTEX 2016
The 25th International Workshop on Vertex Detectors

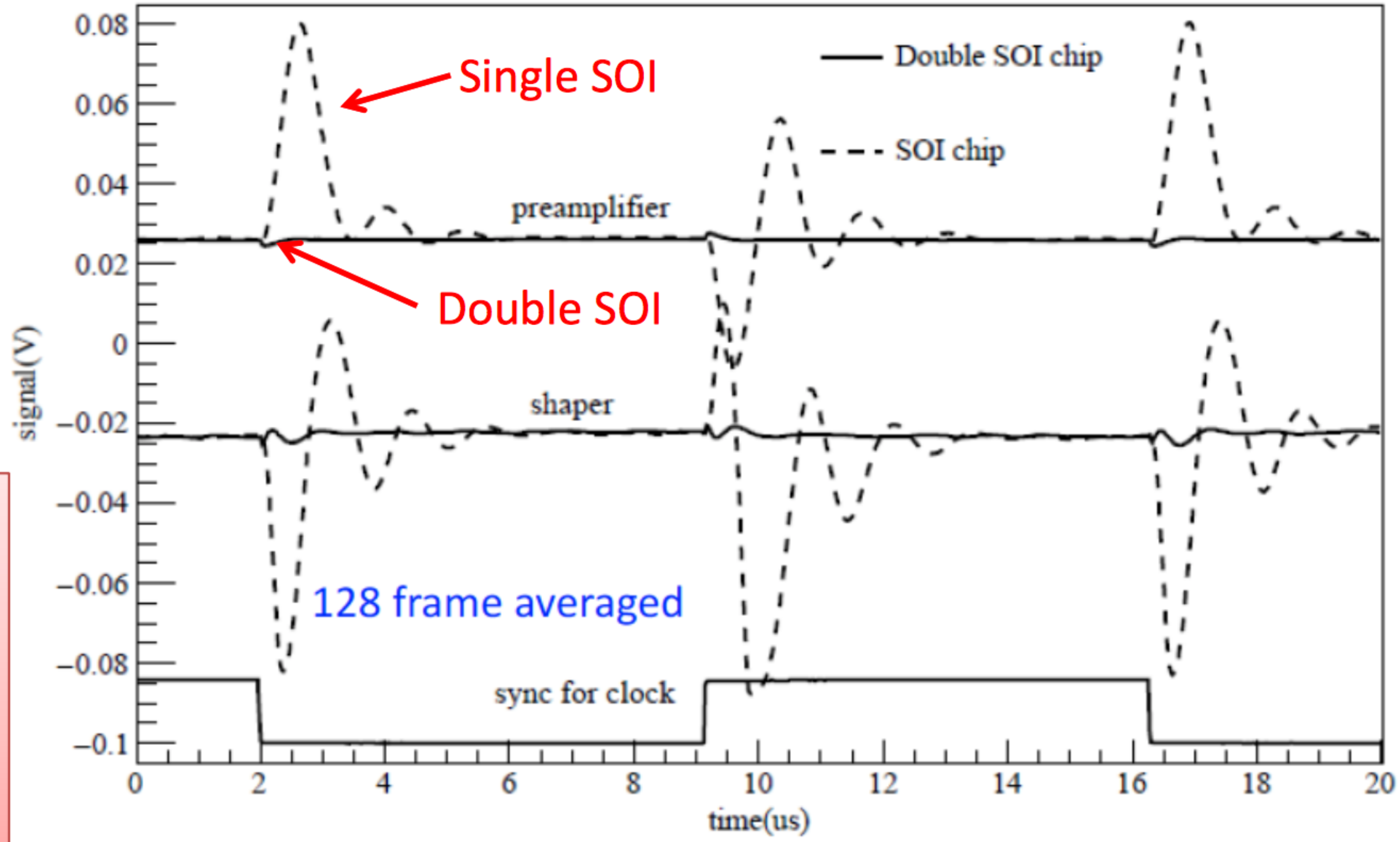
SOI Monolithic Pixel Detector Technology

Sep. 29, 2016, Vertex2016@Isola d'Elba, Italy

Yasuo Arai
High Energy Accelerator Research Organization (KEK)
& The Okinawa Institute of Science and Technology (OIST)
yasuo.arai@kek.jp, *http://rd.kek.jp/project/soi/*

Effect of Double SOI

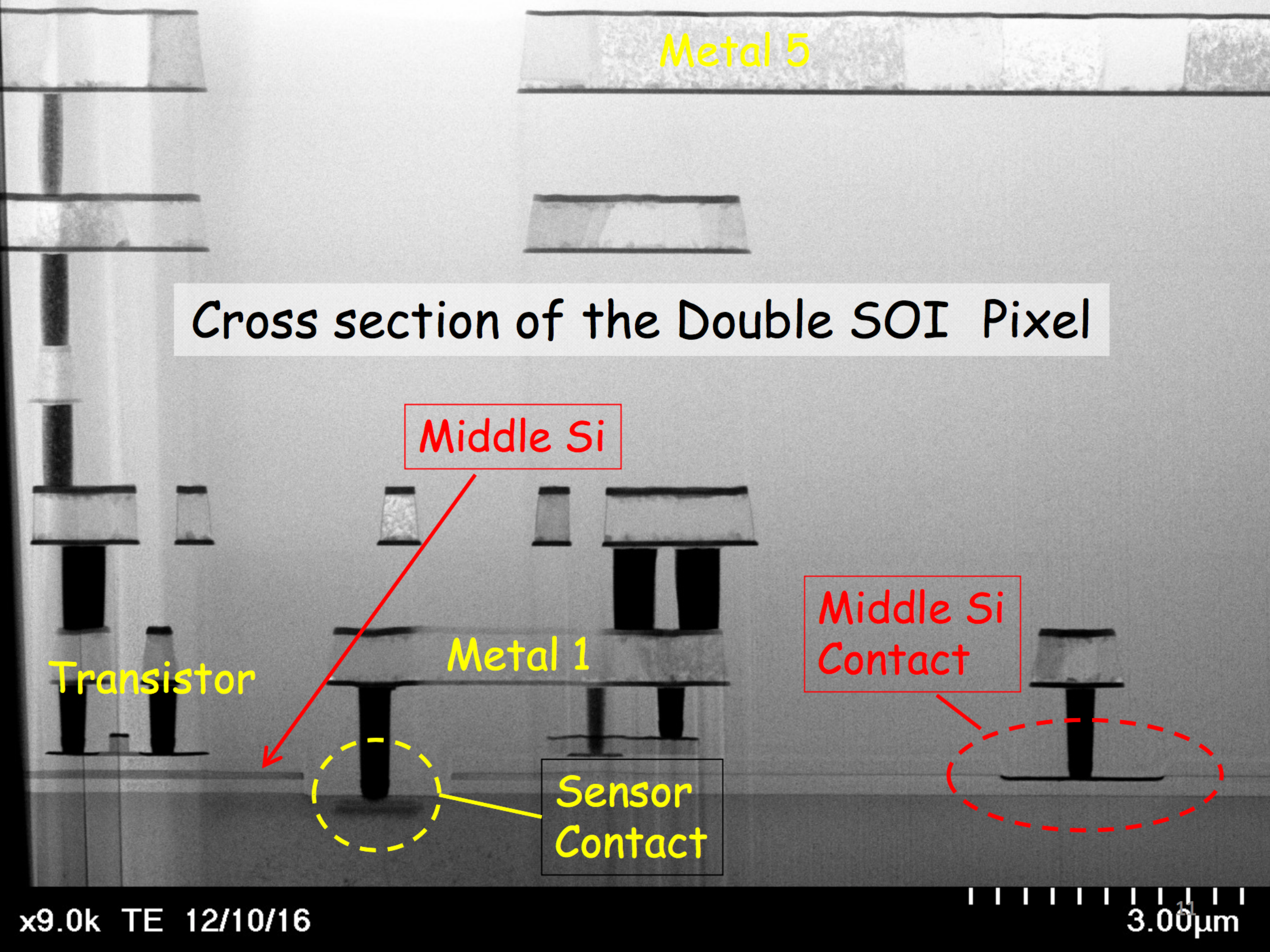
Cross Talk from Clock line



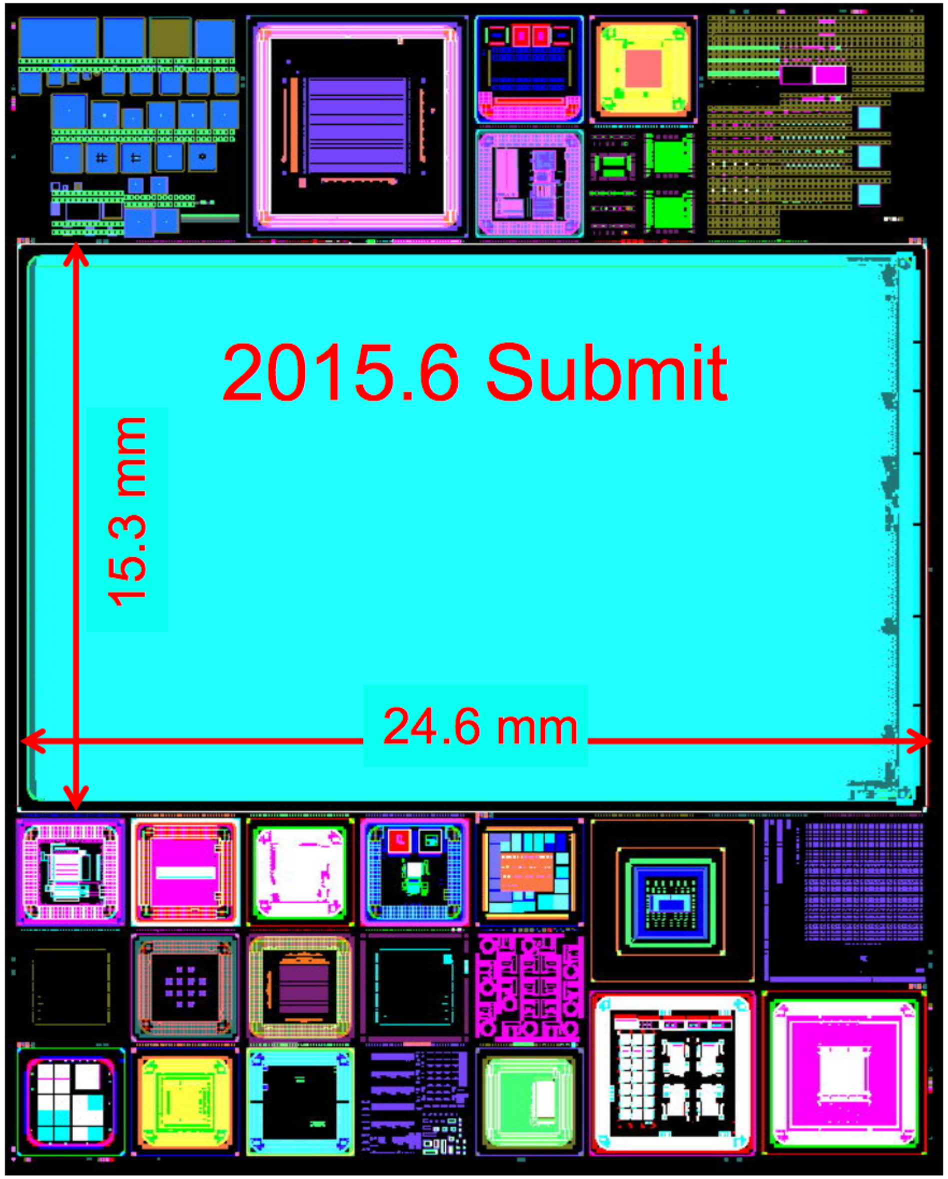
(by Lu Yunpeng (IHEP))

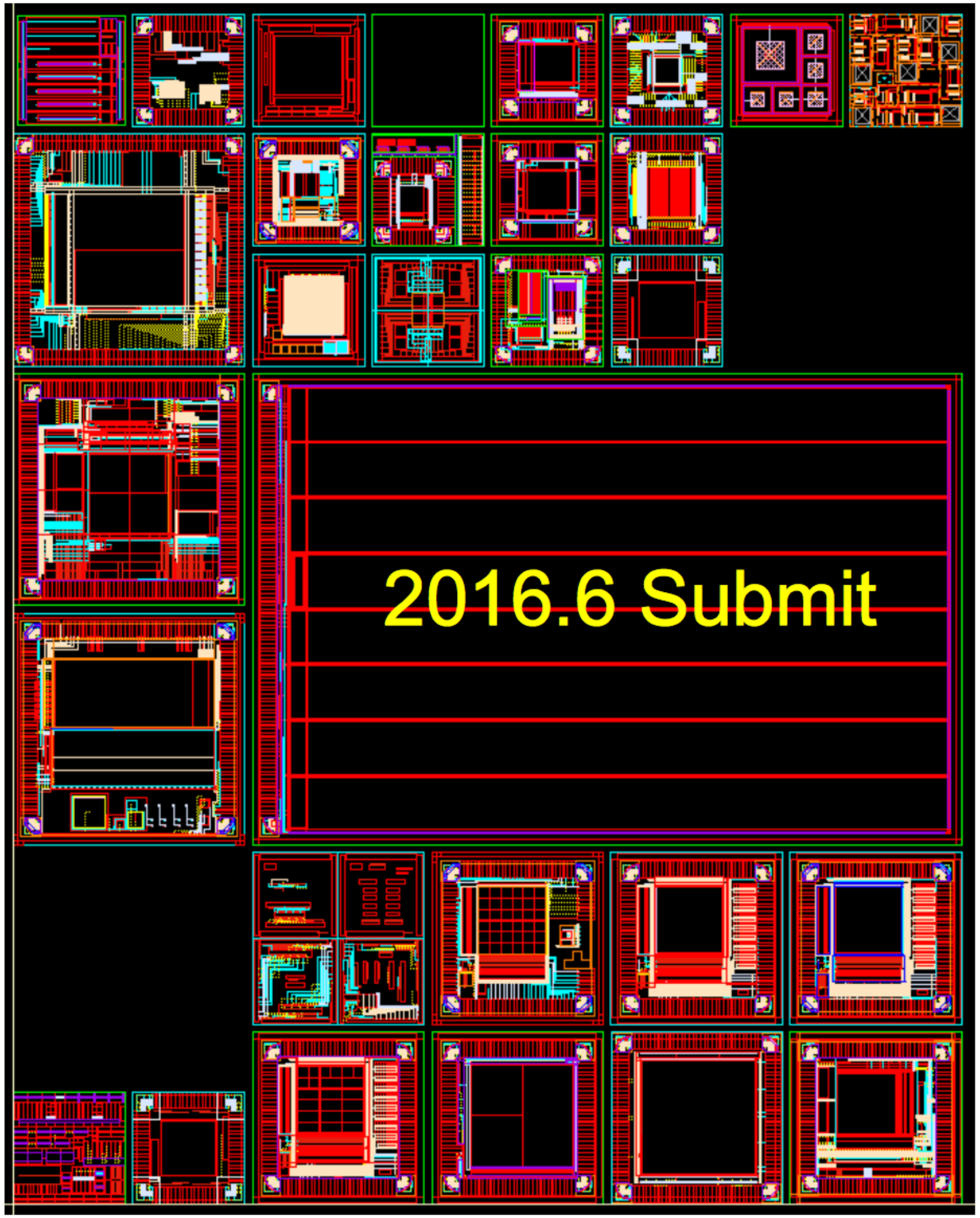
Shield:
Cross Talk
between Circuit
and Sensor is
reduced to 1/20.

Cross section of the Double SOI Pixel



KEK SOI Multi-Project Wafer run. (1~2 runs/year)

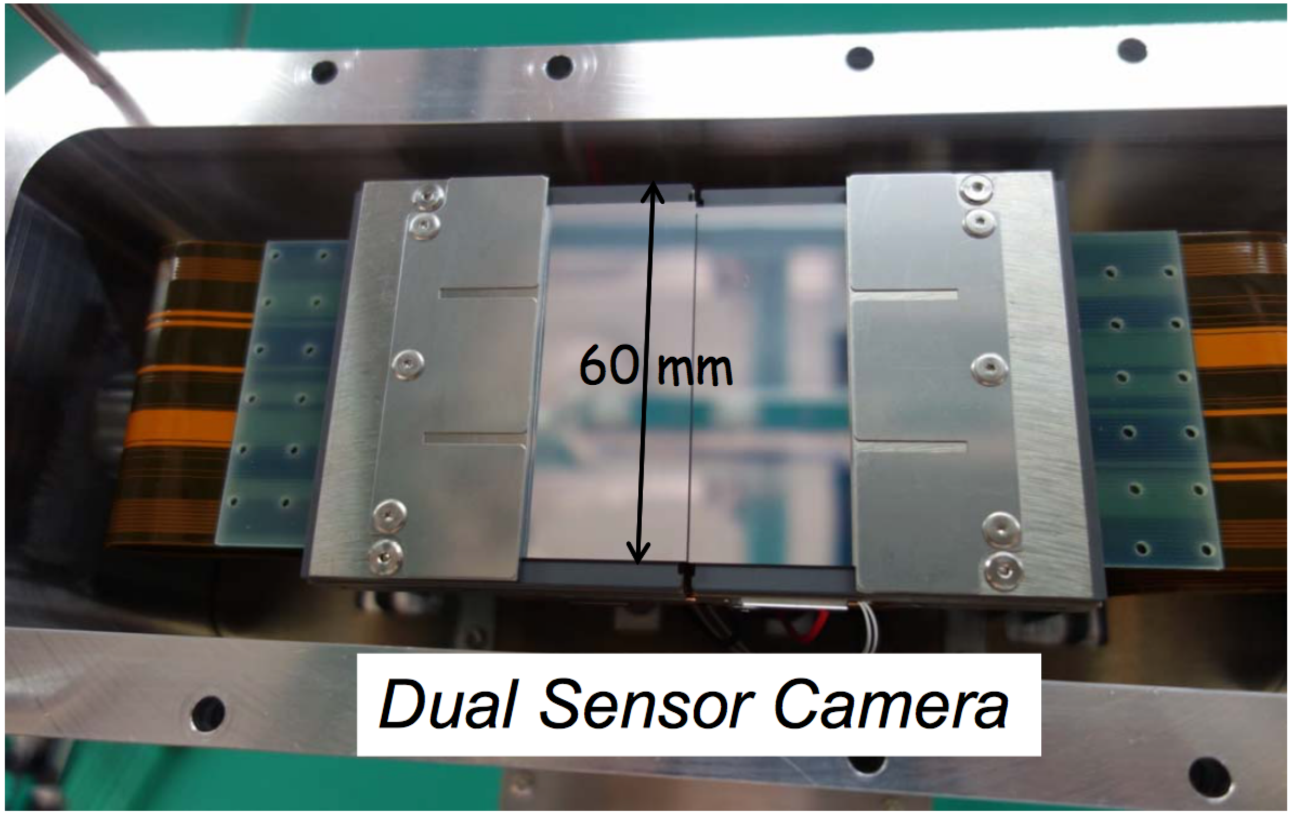




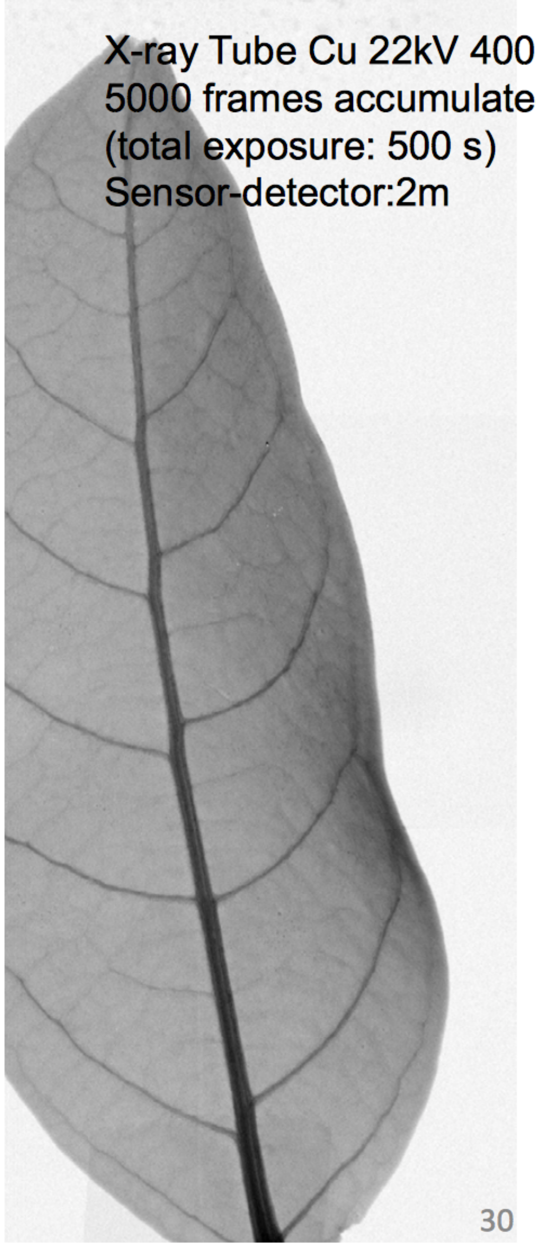
SOI Photon-Imaging Array Sensor (*SOPHIAS)* *for* X-ray Free Electron Laser (XFEL) SACLA

Utilization of SOPHIAS has been started for various experiments in SACLA@RIKEN.

- Dynamics of Atomic Structure
- Direct Observation of Chemical Reactions
- etc.



Dual Sensor Camera



X-ray Tube Cu 22kV 400uA
5000 frames accumulated
(total exposure: 500 s)
Sensor-detector:2m

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PHYSICS AT THE TERA SCALE
Helmholtz Alliance

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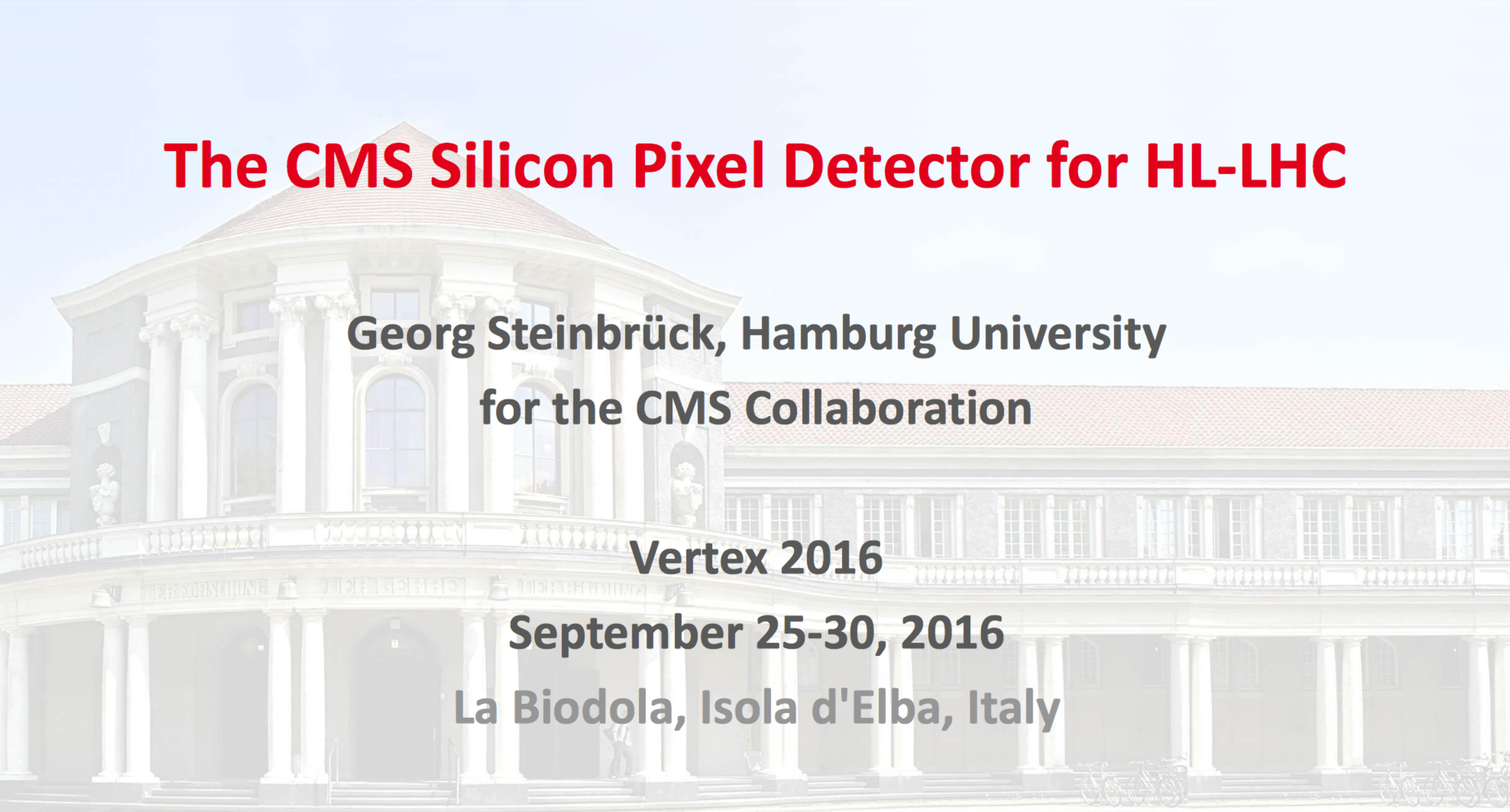
CMS

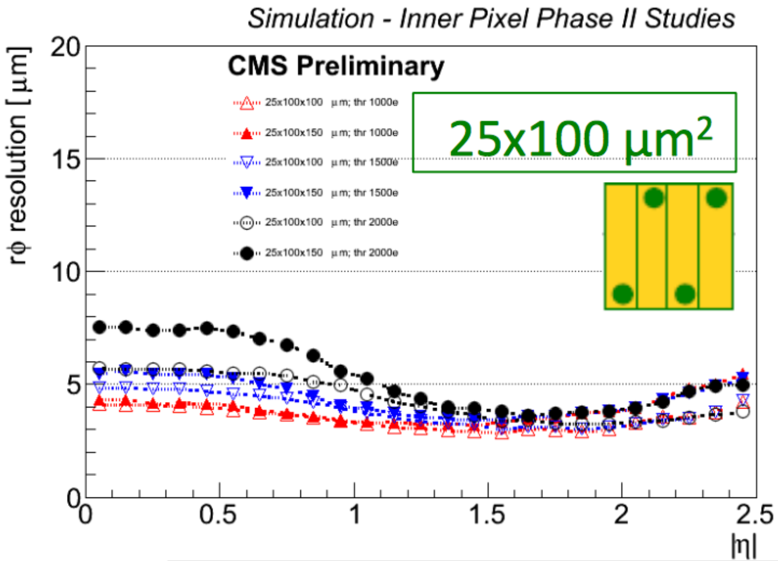


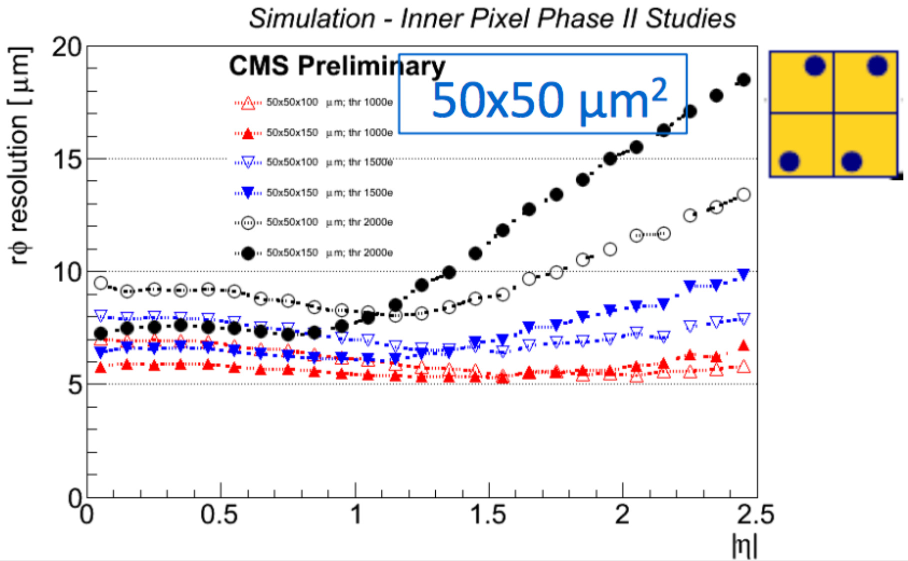
The CMS Silicon Pixel Detector for HL-LHC

Georg Steinbrück, Hamburg University
for the CMS Collaboration

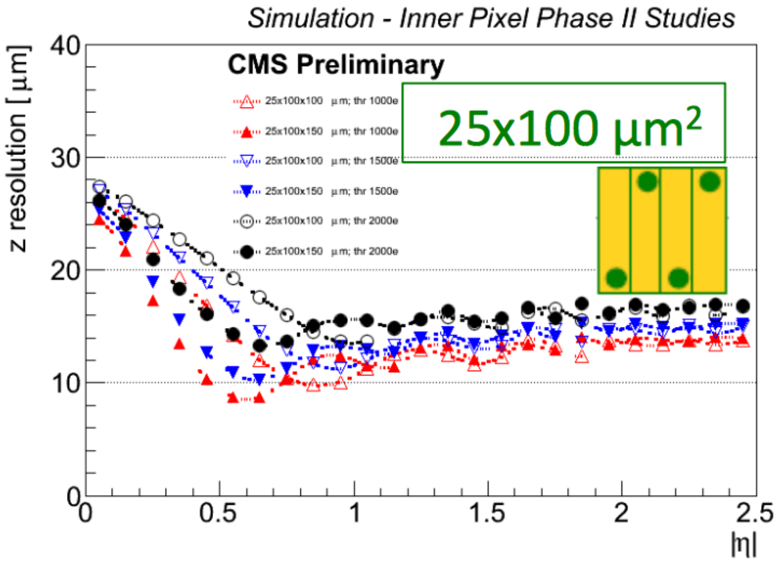
Vertex 2016
September 25-30, 2016
La Biodola, Isola d'Elba, Italy

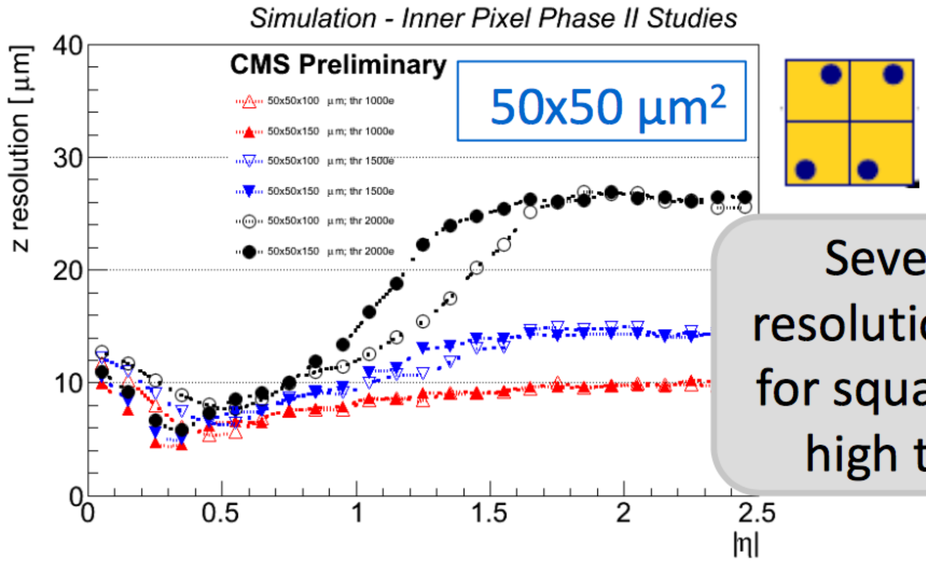
Fine Pitch Sensors





thickness open=100 µm/full=150 µm   threshold 1000e/1500e/2000e





Severe loss of resolution at large η for square pixels for high thresholds

Vertical integration technologies for tracking detectors

Valerio Re

Università di Bergamo
Dipartimento di Ingegneria e Scienze Applicate

INFN
Sezione di Pavia

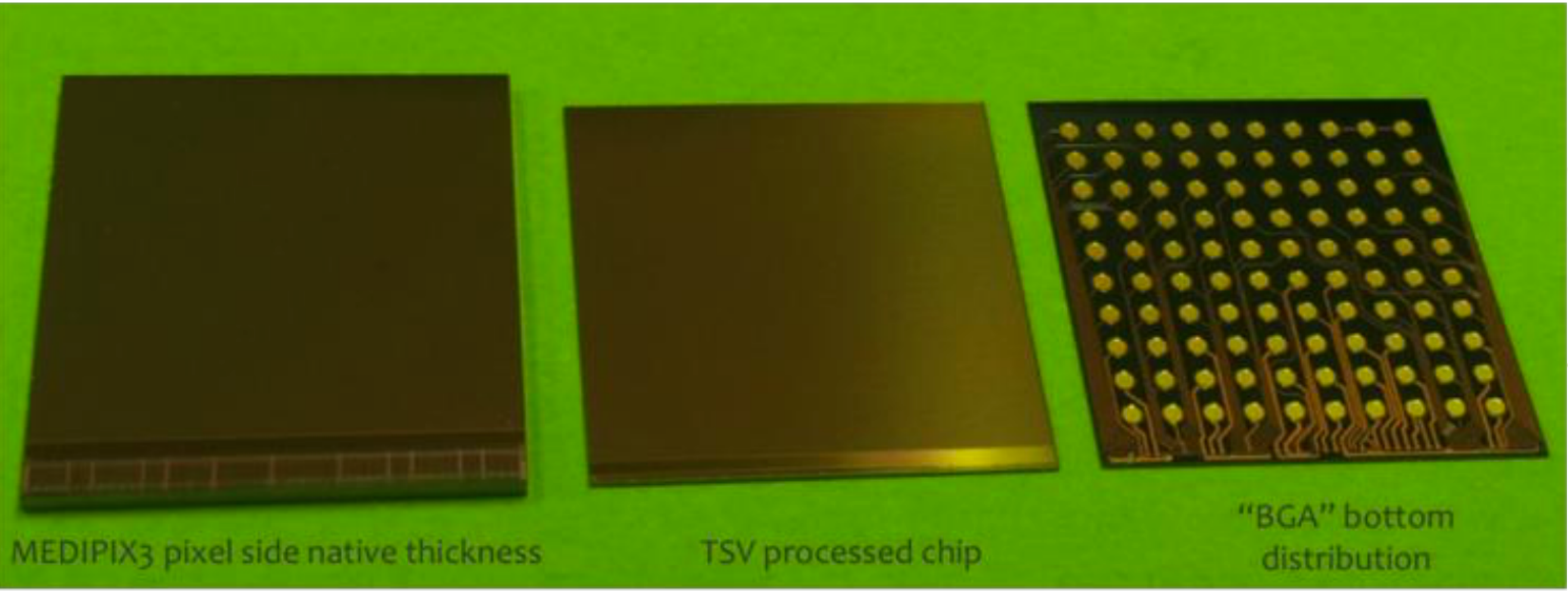
VERTEX 2016

The 25th International Workshop on Vertex Detectors

A forum to exchange the experiences
and needs of the community,
and to review recent, ongoing,
and future activities
on silicon-based vertex detectors

La Biodola (Isola d'Elba, Italy) 25-30 September 2016

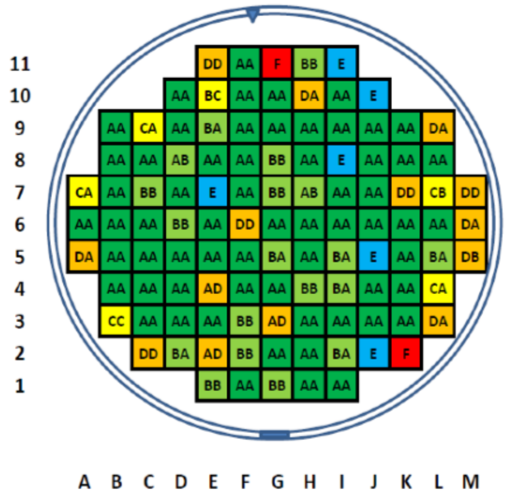
Low-density peripheral TSVs in the MEDIPIX chip



All IO logic and pads contained within one strip of 800µm width

All IO´s have TSV landing pads in place

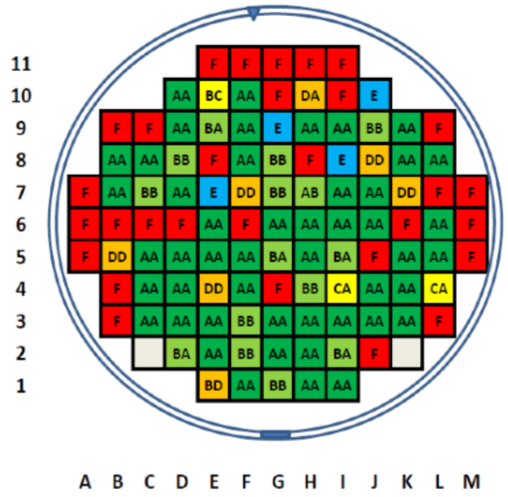
W128_AZPGBPH_before_TSV



	A	B	C	D	E	F	G	H	I	J	K	L	M
11					DD	AA	F	BB	E				
10				AA	BC	AA	AA	DA	AA	E			
9		AA	CA	AA	BA	AA	AA	AA	AA	AA	AA	DA	
8		AA	AA	AB	AA	AA	BB	AA	E	AA	AA	AA	
7	CA	AA	BB	AA	E	AA	BB	AB	AA	AA	DD	CB	DD
6	AA	AA	AA	BB	AA	DD	AA	AA	AA	AA	AA	AA	DA
5	DA	AA	AA	AA	AA	AA	BA	AA	BA	E	AA	BA	DB
4		AA	AA	AA	AD	AA	AA	BB	BA	AA	AA	CA	
3		CC	AA	AA	AA	BB	AD	AA	AA	AA	AA	DA	
2			DD	BA	AD	BB	AA	AA	BA	E	F		
1					BB	AA	BB	AA	AA				

🟩	AA	62	57%
🟩	BB, BA or AB	19	17%
🟨	CC, CA, AC, BC or CB	6	6%
🟧	D	14	13%
🟦	E	6	6%
🟥	F	2	2%
	Total	**109**	100%

W128_AZPGBPH_after TSV



	A	B	C	D	E	F	G	H	I	J	K	L	M
11					F	F	F	F	F				
10				AA	BC	AA	F	DA	F	E			
9		F	F	AA	BA	AA	E	AA	AA	BB	AA	F	
8		AA	AA	BB	F	AA	BB	F	E	DD	AA	AA	
7	F	AA	BB	AA	E	DD	BB	AB	AA	AA	DD	F	F
6	F	F	F	F	AA	F	AA	AA	AA	AA	F	AA	F
5	F	DD	AA	AA	AA	AA	BA	AA	BA	F	AA	AA	F
4		F	AA	AA	DD	AA	F	BB	CA	AA	AA	CA	
3		F	AA	AA	AA	BB	AA	AA	AA	AA	AA	F	
2				BA	AA	BB	AA	AA	BA	F			
1					BD	AA	BB	AA	AA				

🟩	AA	48	45%
🟩	BB, BA or AB	15	14%
🟨	CC, CA, AC, BC or CB	3	3%
🟧	D	7	7%
🟦	E	4	4%
🟥	F	30	28%
	Total	**107**	100%

C2 and K2 were not received

The TSV diameter was 60 µm (to match a wire bond pad pitch of roughly 100 µm) and the wafers were thinned to 120 µm for an optimised aspect ratio of 2.

TSV yield is adequate for small scale production; chip performance is preserved

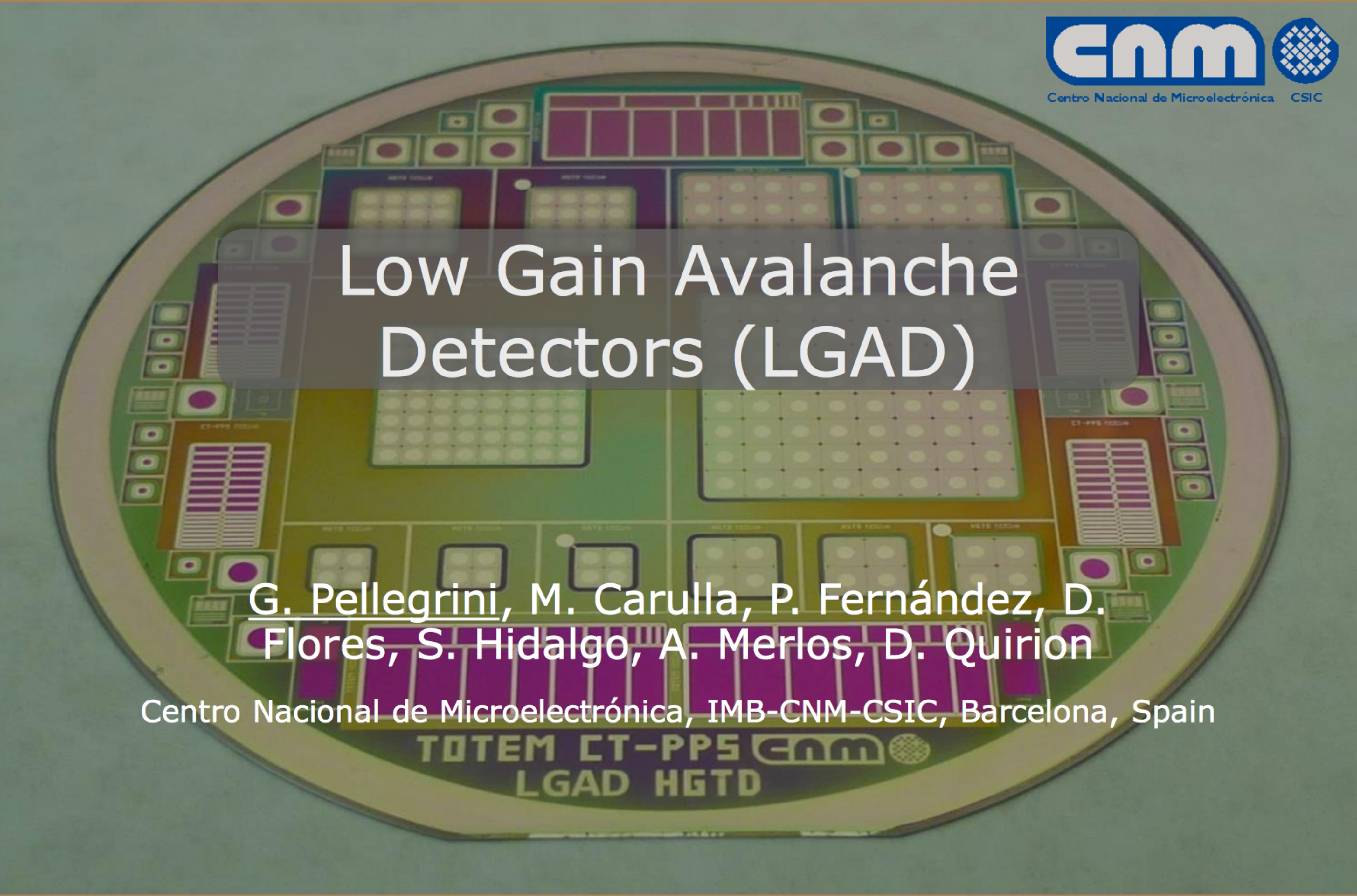
Towards a new generation of pixel detector readout chips, M Campbell et al, IWORID 2015

3D integration for the next generation of MEDIPIX and TIMEPIX chips

TSV processing on 'ultra-thin' MEDIPIX3RX chips was also performed with good yield (wafers thinned to 50 µm, TSV diameter 40 µm), as a test of extremely thin assemblies primarily for vertex detector applications in high energy physics.

Next generation of 65 nm MEDIPIX4 (spectroscopic X-ray images at rates compatible with human CT) and TIMEPIX4 readout chips (sub-ns time stamping and reduced pixel pitch):

- in both chips the **functions normally associated with the chip periphery will be located throughout the pixel matrix** taking full advantage of the opportunities provided by the TSV process.
- as the readout logic is no longer confined to one chip edge there is **more flexibility in the choice of readout architectures**. The chips should be abuttable on 4 sides.



Low Gain Avalanche Detectors (LGAD)

G. Pellegrini, M. Carulla, P. Fernández, D. Flores, S. Hidalgo, A. Merlos, D. Quirion

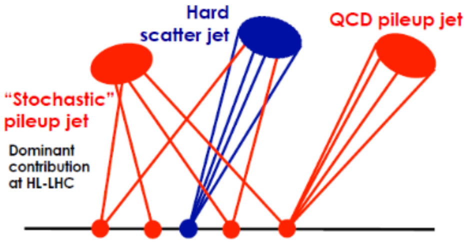
Centro Nacional de Microelectrónica, IMB-CNM-CSIC, Barcelona, Spain

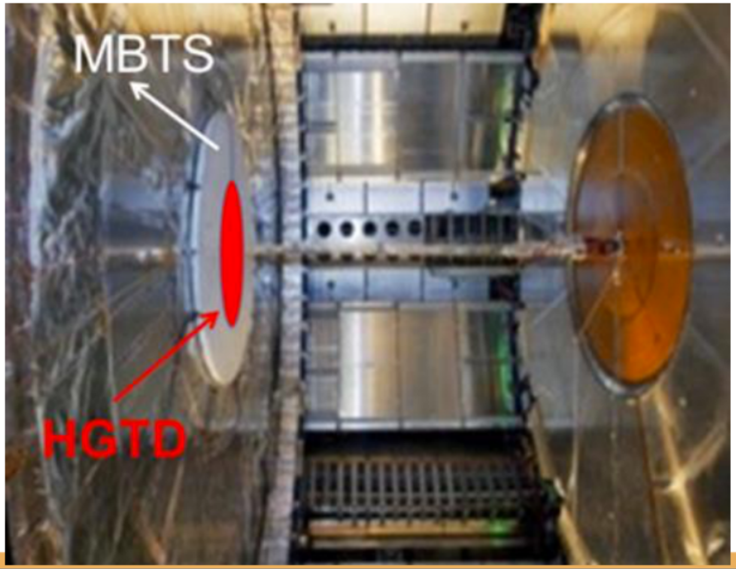
High Granularity Timing Detector

- ATLAS is proposing Ultra Fast Silicon Detector (UFSD) based on LGAD as one of the technical options for the **High Granularity Timing Detector** (HGTD)
- High granular **timing detector** can provide a new capability in ATLAS to separate pileup from hard-scatter signals, provide pileup jet rejection, and improve e/g and jet reconstruction *
- A **reduction of Substrate Thickness** from 300 μm to **50 μm** will reduce the Bulk Radiation Effects and will decrease the Collection Time.
- Integrate a **Small Gain (10-30)** in a sensor while maintaining similar Noise Levels and avoiding Readout Front-End saturation & Pile-up effects

4 active layers per side (~10 m^2 in total) in front of FCAL
HGTD baseline dimensions:
Z =[3475, 3545] mm ; **ΔZ=70mm**
Rmin ~ 90 mm (ηmax≃4.3), Rmax ~ 600 mm (ηmin≃2.4)
Possible to extend η=5.0 (Rmin ~ 50mm)
Required timing resolution: **50 – 100 ps**
Radiation hardness= $5x10^{15}n_{eq}/cm^2$

(preliminary)

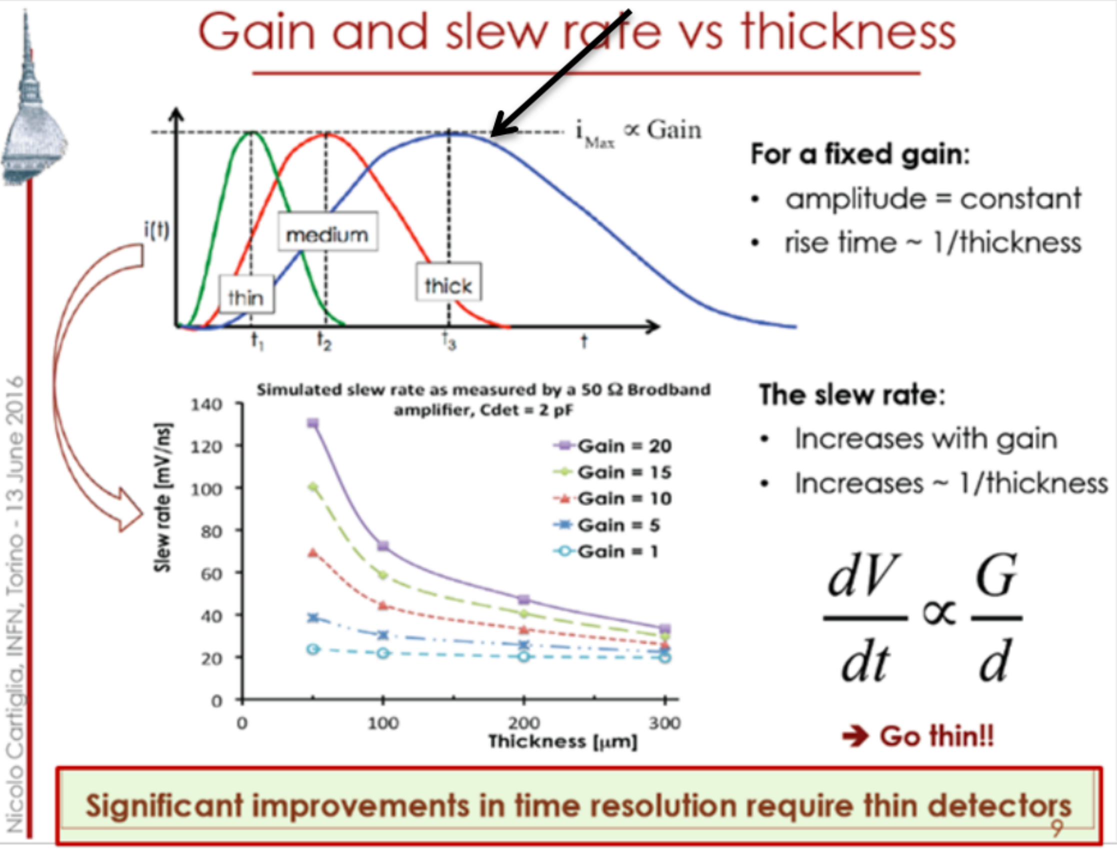




* Ariel Schwarzman, Status and Plans of the High Granularity Timing Detector Studies

Why thin LGAD for timing?

Large slew rate, good time resolutions



Gain and slew rate vs thickness

For a fixed gain:

- amplitude = constant
- rise time ~ 1/thickness

The slew rate:

- Increases with gain
- Increases ~ 1/thickness

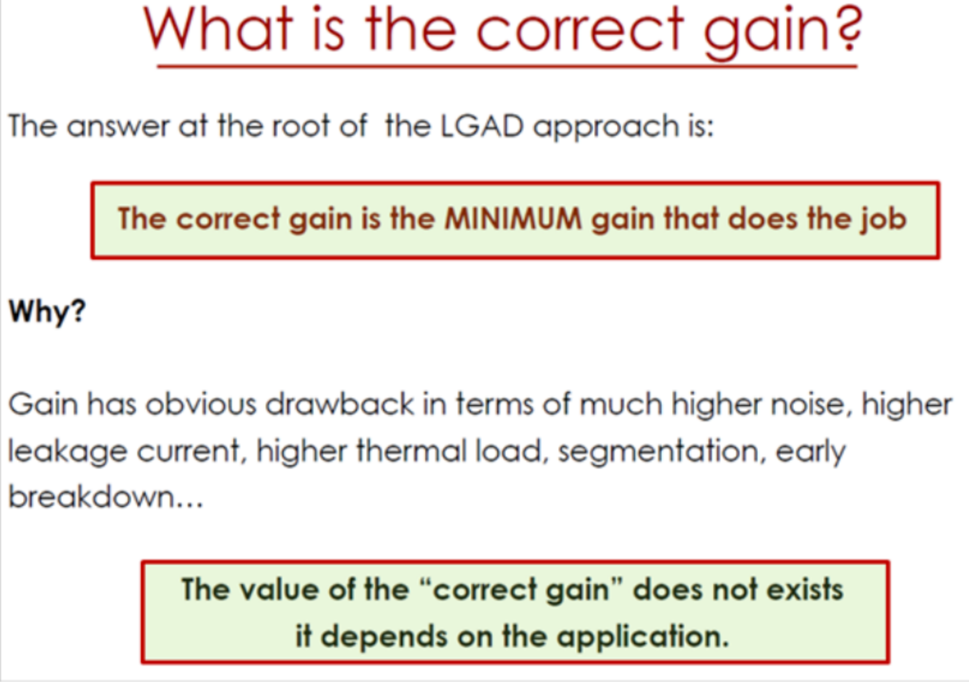
$$\frac{dV}{dt} \propto \frac{G}{d}$$

➔ Go thin!!

Significant improvements in time resolution require thin detectors

Nicolo Cartiglia, INFN, Torino - 13 June 2016

9



What is the correct gain?

The answer at the root of the LGAD approach is:

The correct gain is the MINIMUM gain that does the job

Why?

Gain has obvious drawback in terms of much higher noise, higher leakage current, higher thermal load, segmentation, early breakdown…

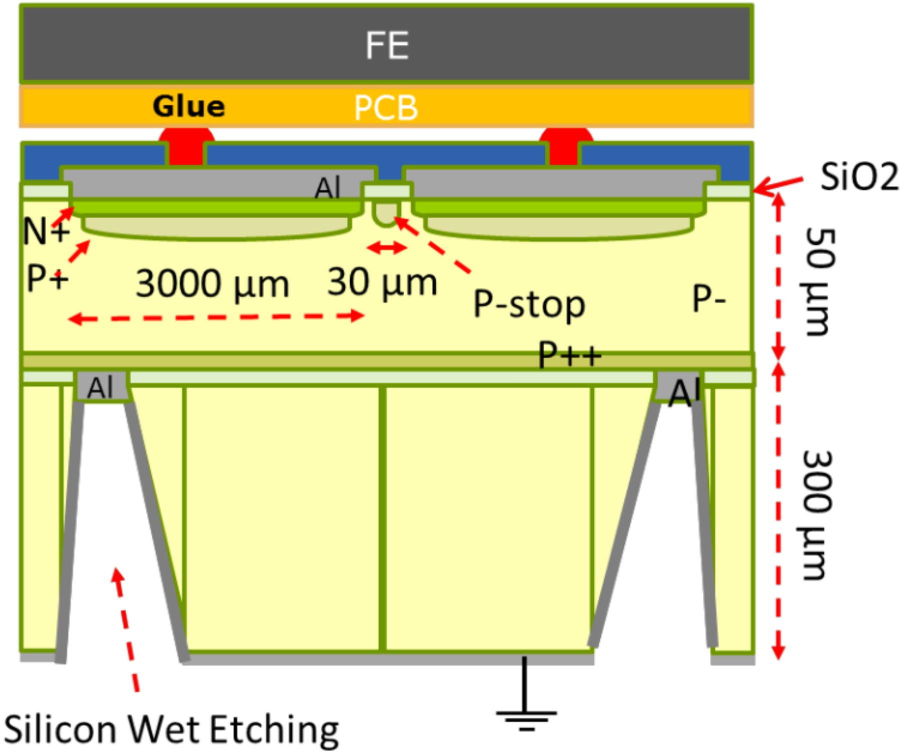
The value of the "correct gain" does not exists it depends on the application.

N. Cartiglia. Signal formation and timing in LGAD sensors. Workshop on energy and time measurement with silicon devices. AIDA 2020 Annual Meeting. DESY. Hamburg. 13 June 2016

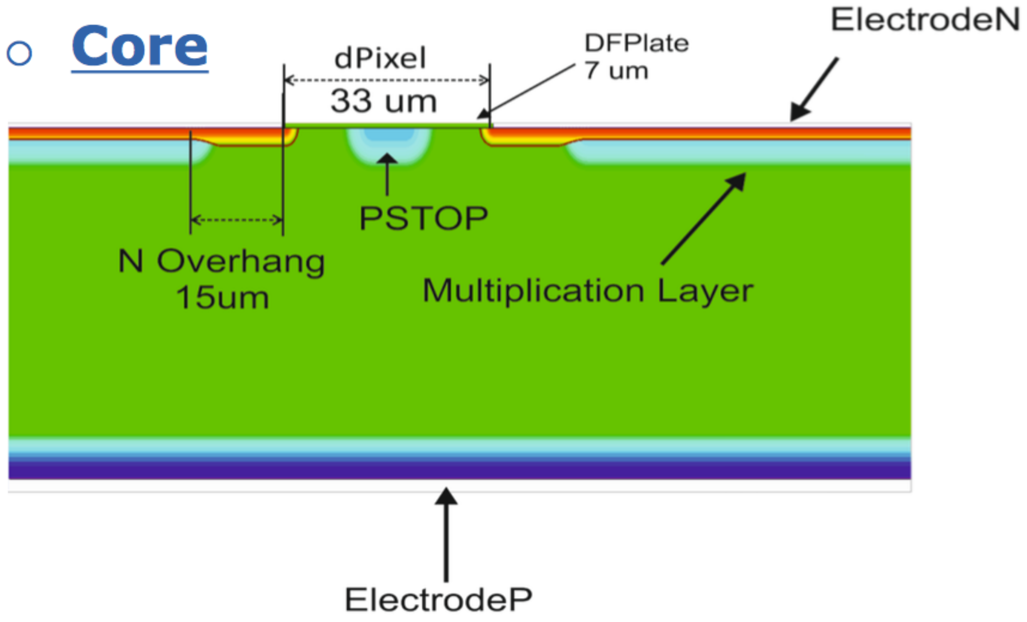
Goal is a detector that combines **excellent timing and position** measurement with very high rate capability (no dead-time after a hit). Specifically for timing, better than 40 psec measurement for a mip.

High Granularity Timing Detector (HGTD)

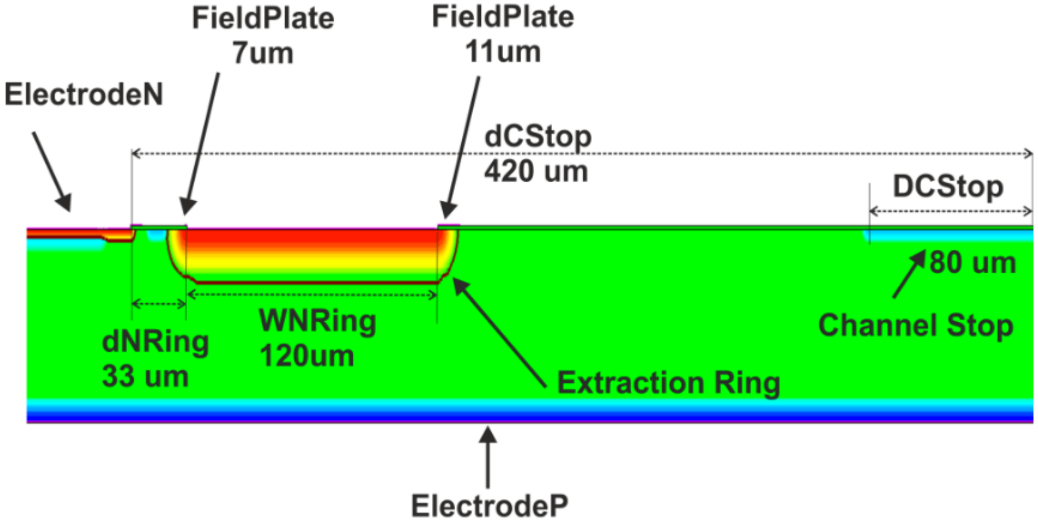
- **Two** Pixel **Size**
  - ✓ 3000 x 3000 μm^2
  - ✓ 2000 x 2000 μm^2
- **High** Resistivity **P-Type** **50 µm SOI** Wafers
- **New Run** in Progress with **75 and 50 µm Epitaxial** Wafers



- **Core**

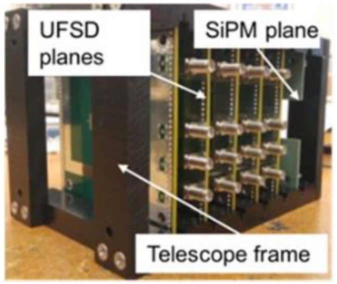


- **Termination**

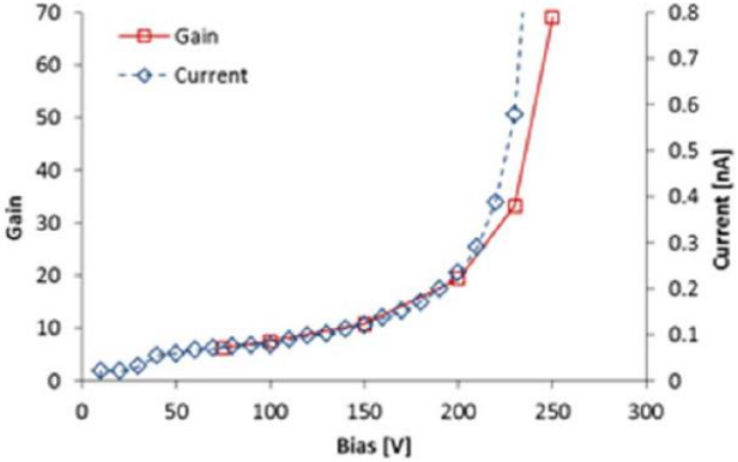


HGTD Sensor Status (last test beam results)

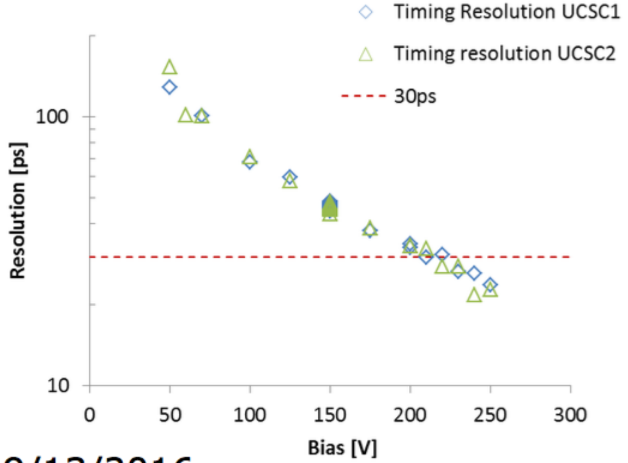
- The 45 µm sensors produced by CNM in the RD50 sponsored Run #9088 validate the principle of thin LGAD as timing detector.
- Timing resolutions of below 30ps were measured in two beam tests with 1.2mm LGAD (single pads).
- A stack of 3 UFSD reached a timing resolution of 15ps. *https://arxiv.org/ftp/arxiv/papers/1608/1608.08681.pdf*
- LGAD of 1.2mm (single pads) and 3.2mm (2x2 arrays) were produced.
- The stability of operation for small pads is good up to a gain of about 40.
- Testing was done by CNM, LPNHE, UCSC, IFAE, Ljubljana, INFN Torino

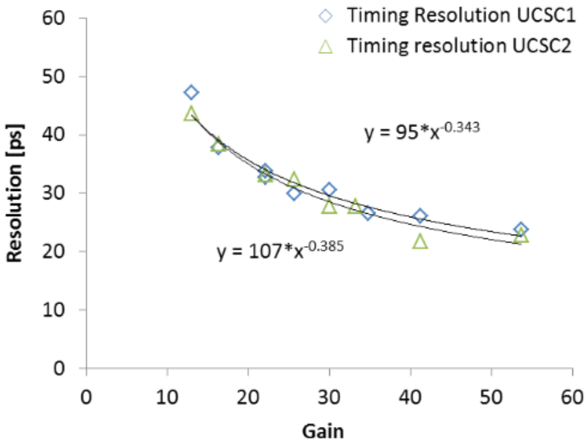


Gain M = Collected Charge/0.46fC



Good matching of 1mm LGAD
Timing resolution ~ $M^{-0.36}$





Hartmut F.-W. Sadrozinski, HGTD Sensors, 9/13/2016

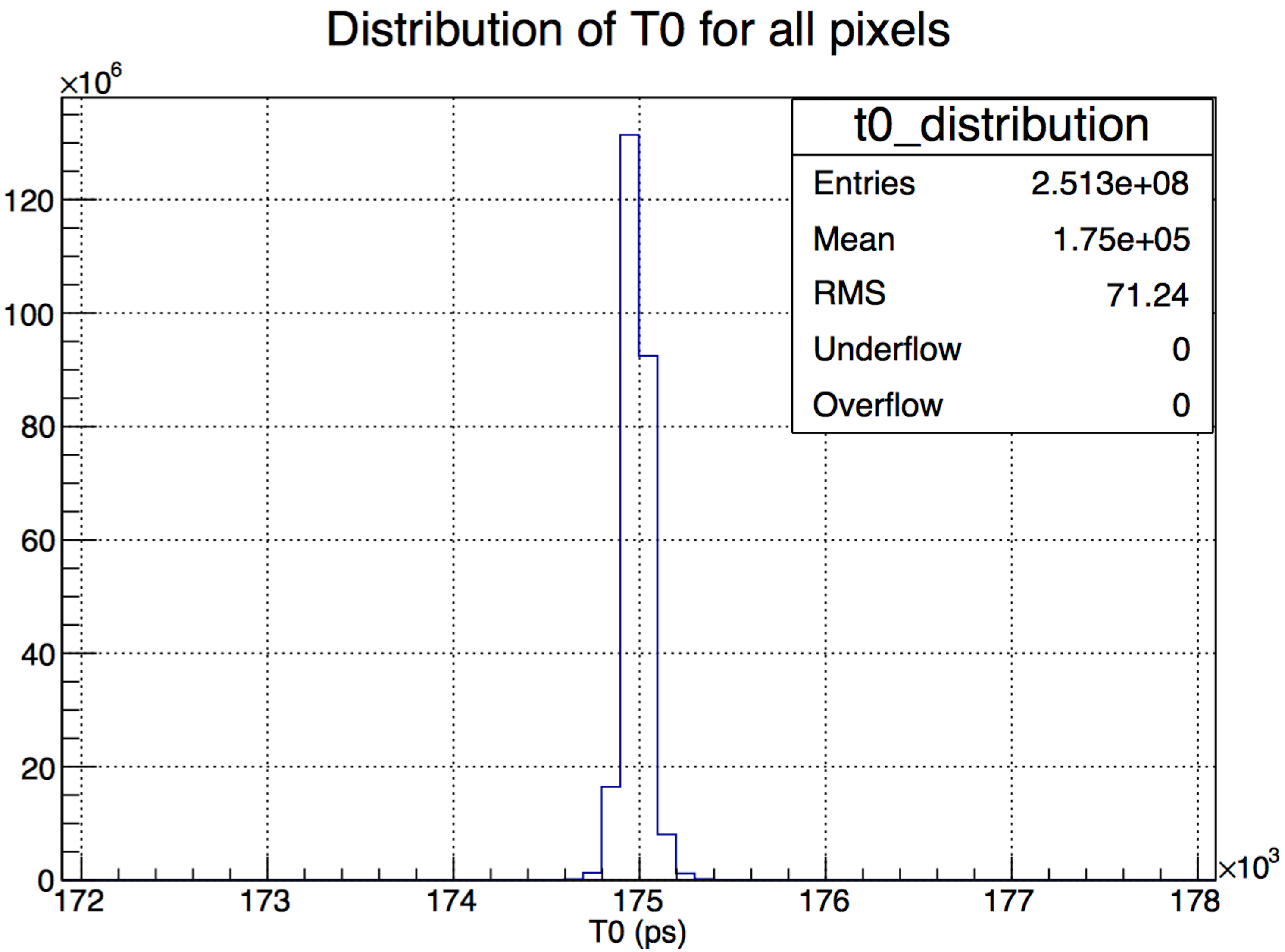
Chip Development for High Time Resolution Silicon Detectors

M. Noy

EP-ESE-FE Group, CERN

29th September 2016

TimeWalk-Corrected (T_0) Time Resolution: Bare ASIC

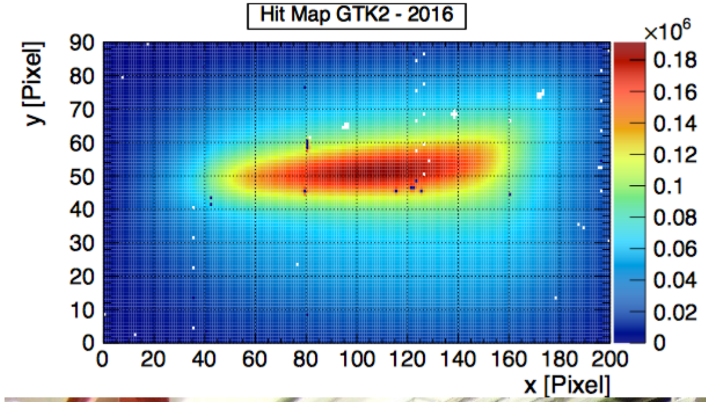


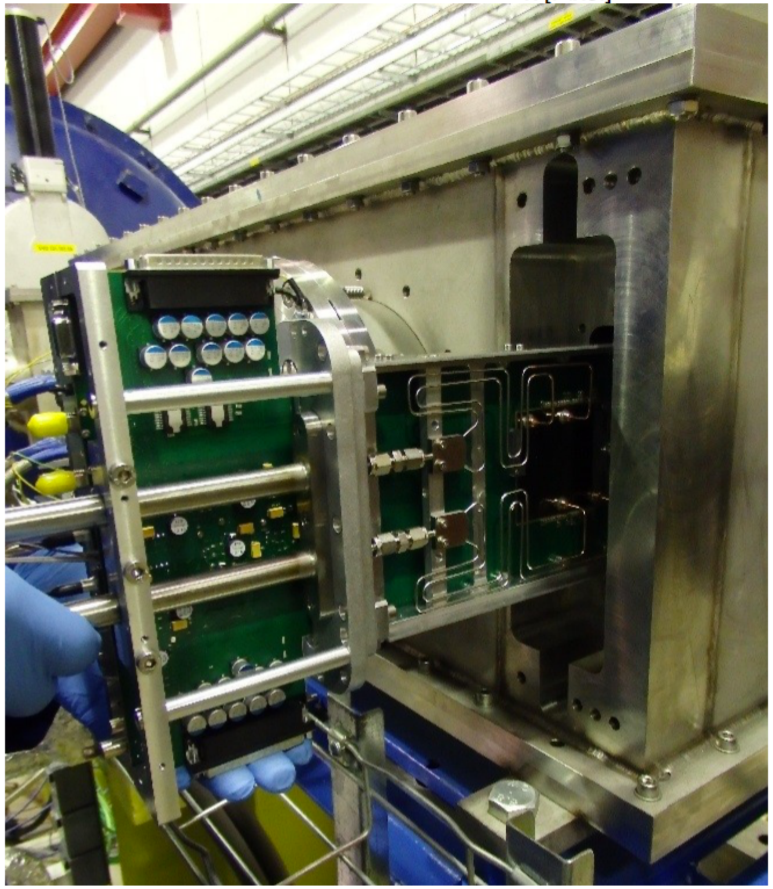
t0_distribution

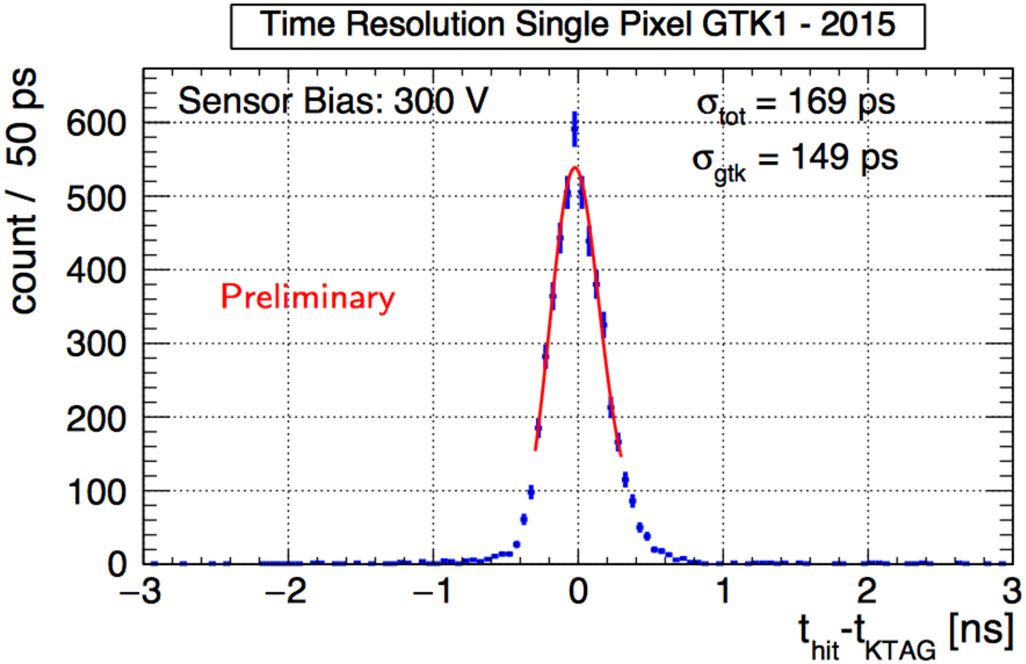
Entries	2.513e+08
Mean	1.75e+05
RMS	71.24
Underflow	0
Overflow	0

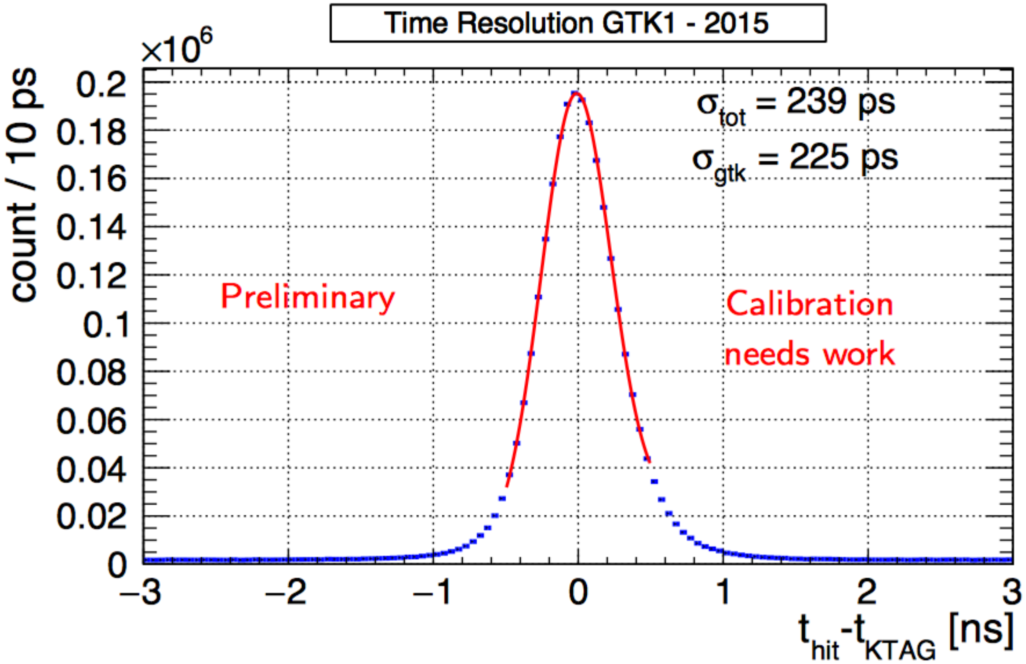
"Whole Chip" Resolution ∼ 72 ps RMS

Time Resolution in the Experiment









Time Resolution Synopsis

$$\text{Time Resolution} = \sqrt{\sigma^2_{electronics+TDC} + \sigma^2_{WeightingField} + \sigma^2_{straggling}}$$

$$= \sqrt{80^2 + 85^2 + 100^2} \sim 150\,ps$$

We will do a beam test with a high spatial resolution telescope to confirm this.

Diamond detector technology: status and perspectives

Harris Kagan
for the RD42 Collaboration

Vertex 2016
La Biodola, Isola d'Elba, Italy
Sept 28, 2016

Outline of Talk

- The RD42 Program
- Development of Material and Production Capabilities
- Diamond Devices in the LHC and Experiments
- Diamond Device Development – 3D Diamond
- Rate Studies
- Summary

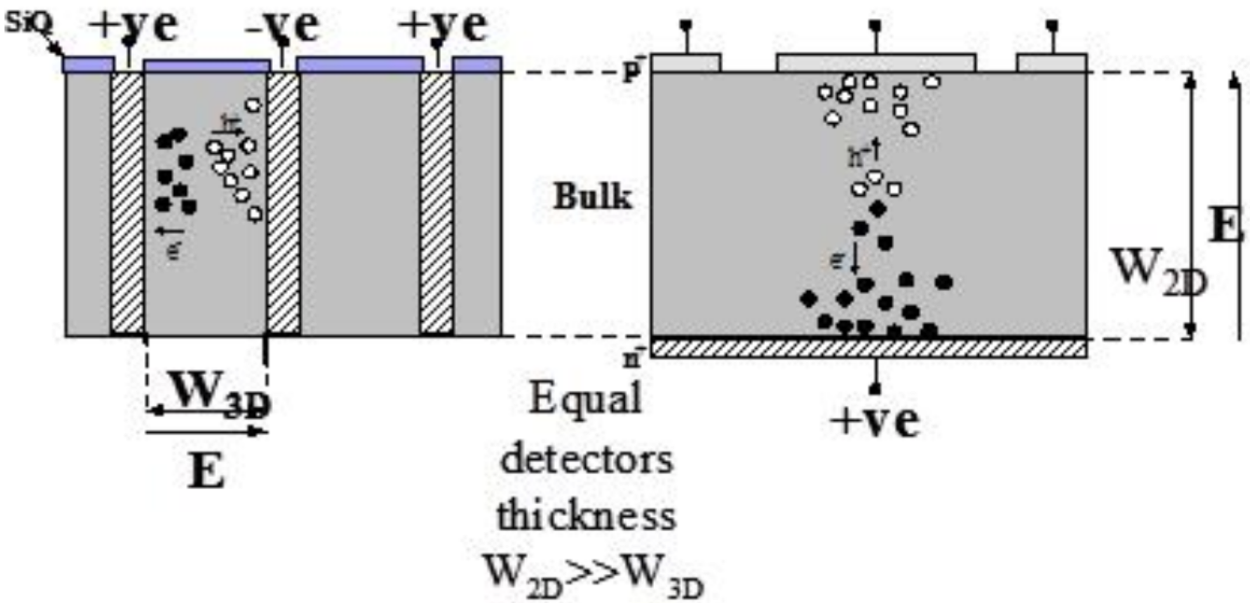
3D device in pCVD diamond

After severe radiation damage all detectors are trap limited

- Mean free paths < 75μm
- Would like to keep drift distances smaller than mfp

Comparison of 3D and planar devices

Can one do this in pCVD diamond?



Have to make resistive columns in diamond for this to work

- -columns made with 800nm femtosecond laser
- -initial cells 150μm x 150μm; columns 6μm diameter

3D device in pCVD diamond

- Measured signal (diamond thickness 500um):
  - Planar Strip ave charge
    6,900e or ccd=192um
  - 3D ave charge
    13,500e or ccd$_{eq}$=350-375um
- For the first time collect >75% of charge in pCVD