The Institution of Engineering and Technology
European Pulsed Power Conference 2009
Incorporating the CERN Klystron Modulator workshop
21 - 25 September 2009, CERN, Geneva, Switzerland

A SOLID STATE HIGH VOLTAGE KLYSTRON ANODE MODULATOR DESIGN – AN ALTERNATIVE TO TETRODE SOLUTIONS

Davide Aguglia & Carlos A. Martins

Presenter: D. Aguglia

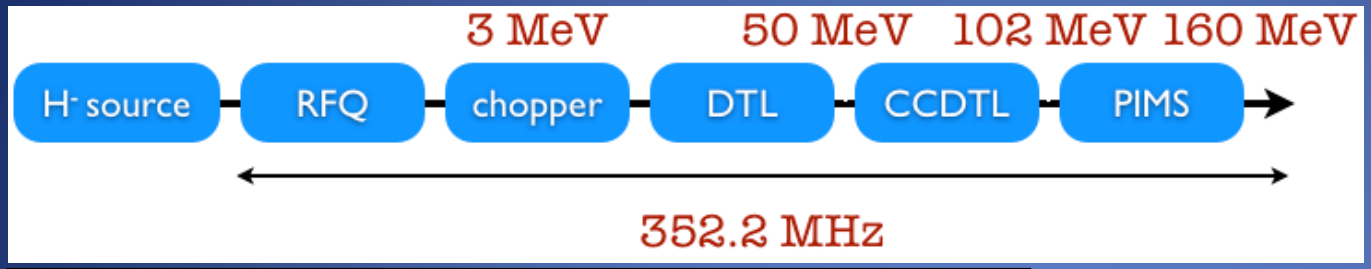
CERN – European Organization for Nuclear Research, Geneva, Switzerland.
Technology Department, Electric Power Converter Group (TE/EPC).

Outline

- Introduction & motivations
- Old & new power stage topology
- Driver topology choice
- System design challenges
- Numerical simulations
- Experimental results
- Conclusion

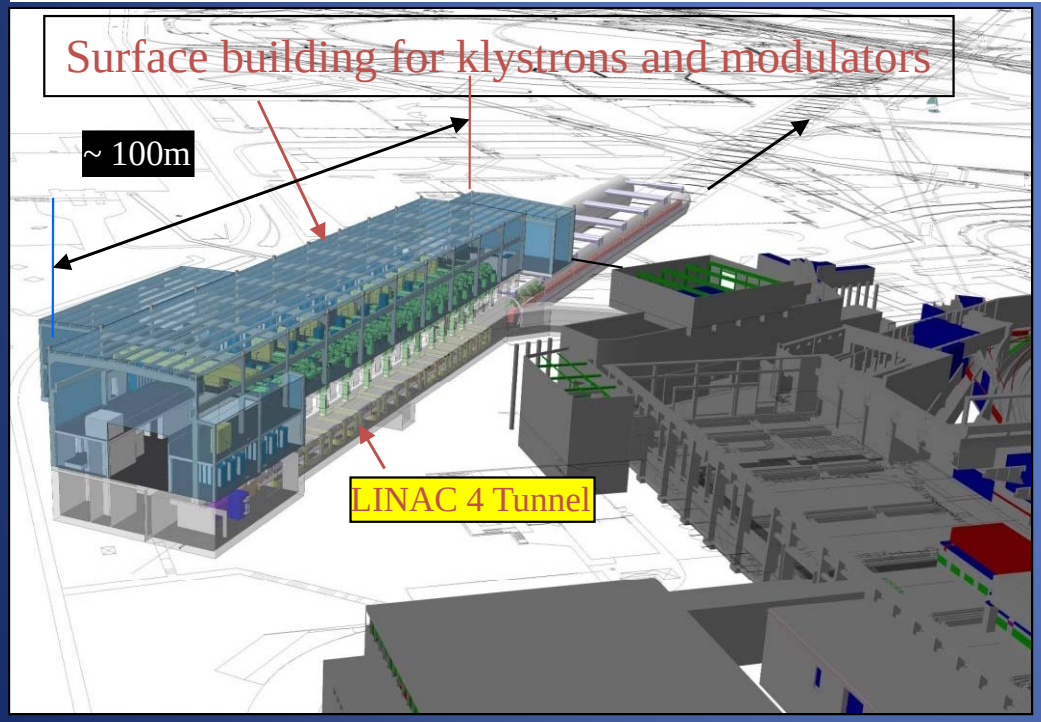
Introduction & motivations

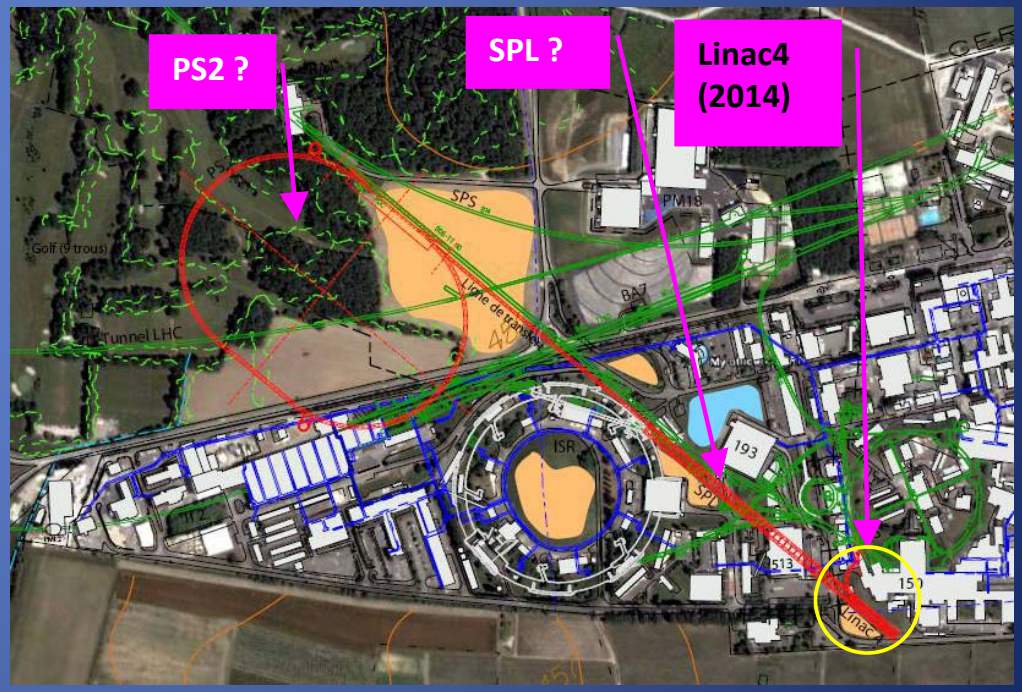
- *Linac4 Project*



-14 klystron modulators

-15 anode modulators…



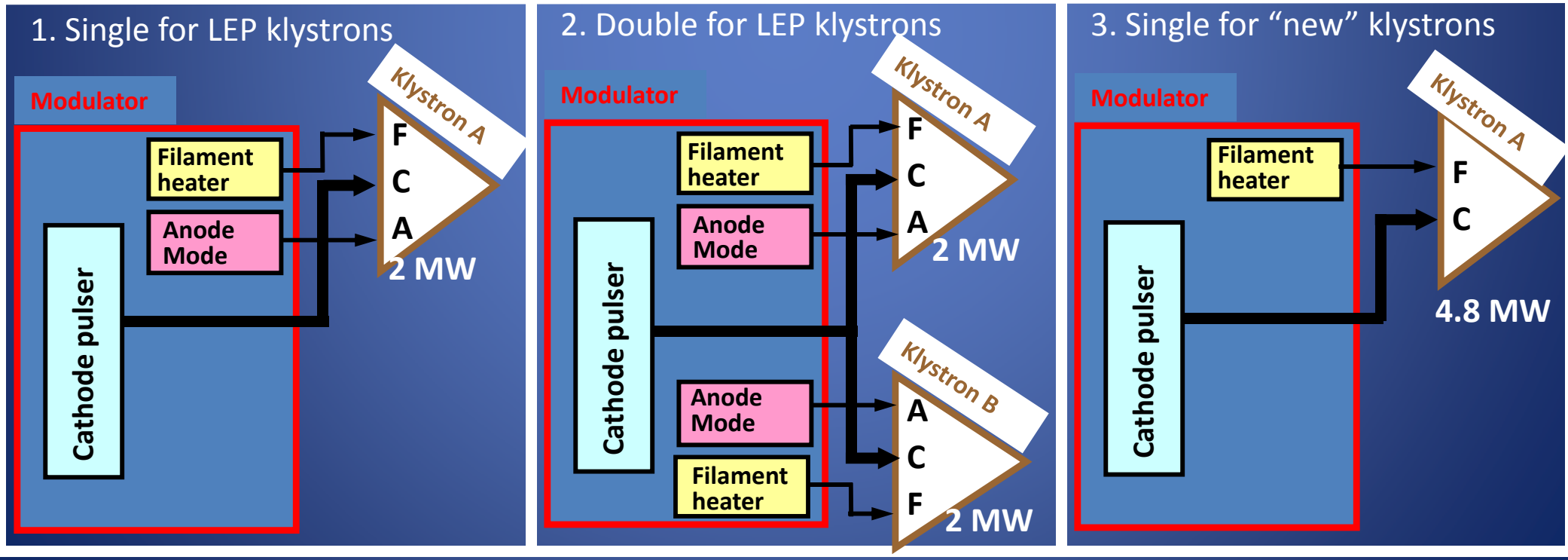


1st stage: Linac4 injects into the old PSB → increased brightness for LHC.

2nd stage: Linac4 → Future renewed and improved LHC injection chain.

Introduction & motivations

- 3 different configurations for *Linac4* Klystrons supply
  - One modulator for one “old” *LEP* klystron.
  - One modulator for 2 parallel “old” *LEP* klystron.
  - One modulator for one new klystron (no anode terminal).



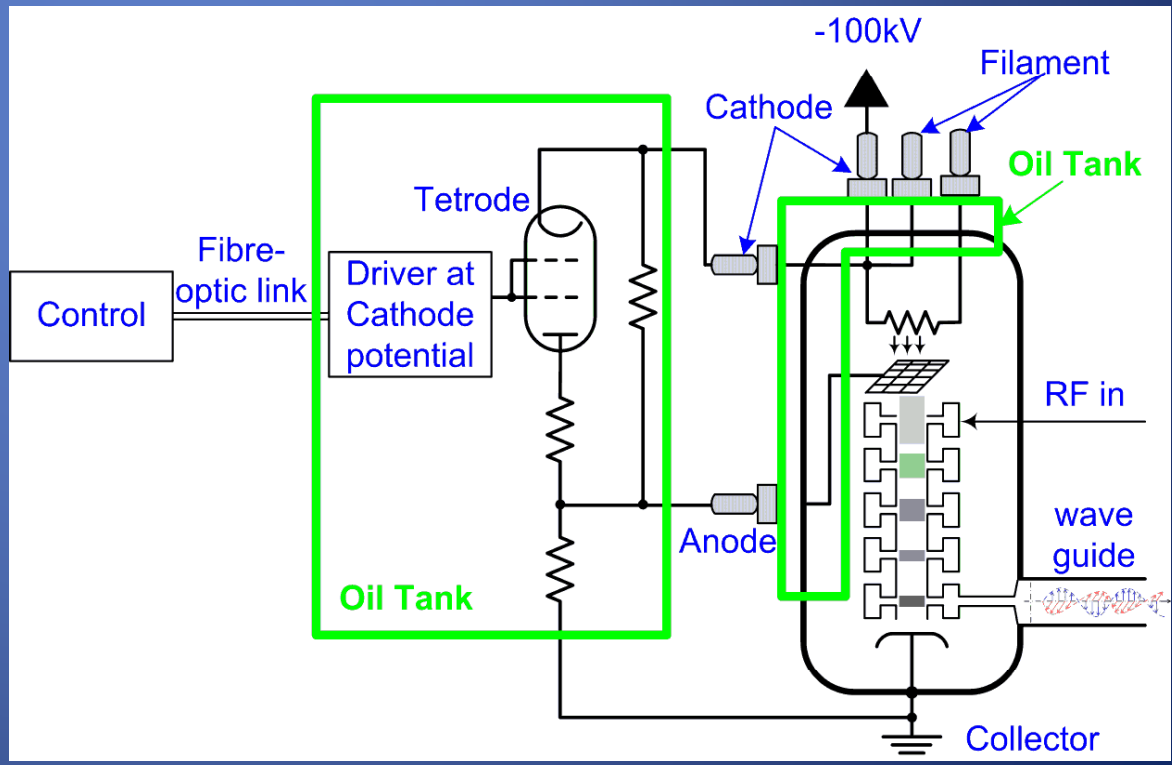
Old & new power stage topology

Old power stage based on a tetrode

- Constant Cathode voltage.
- RF power control by anode voltage modulated by a tetrode.
- Tetrode driver at cathode potential (fiber optics insulation).
- Tetrode & driver immersed in an additional oil tank.

Drawbacks:

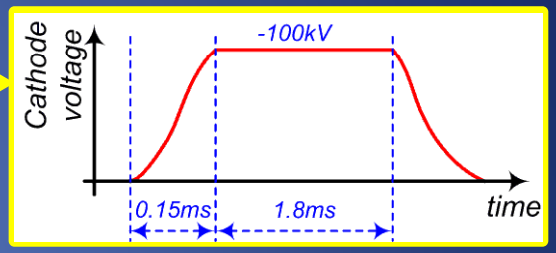
- **Tetrode:**
  - obsolete component.
  - limited lifetime.
  - low reliability.
  - high MTTR.
- **Additional oil tank.**



Old & new power stage topology

New power stage composed of a stack of 60 MOSFETs

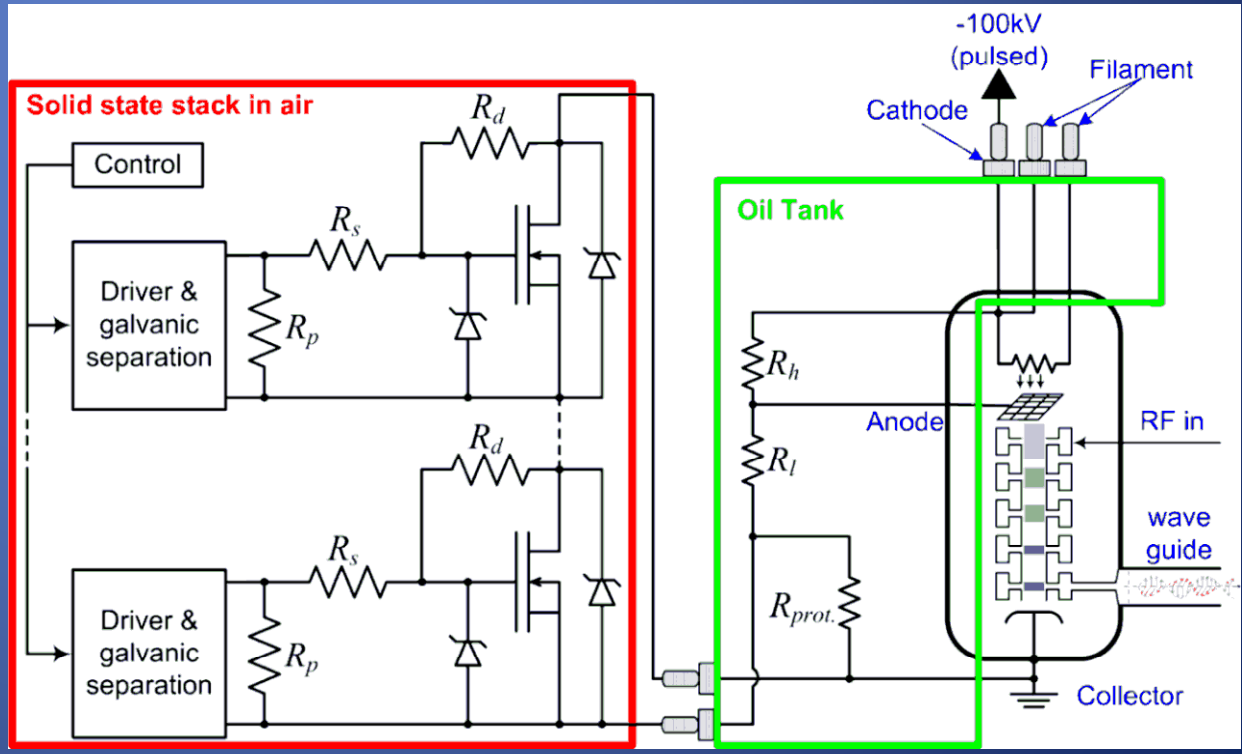
- Pulsed Cathode voltage at -100 *kV*.
- Stack placed at ground side to limit insulation requirements.
- MOSFET Stack in air, power resistors only in the klystron oil tank.



Flexibility, reliability & availability

Specifications

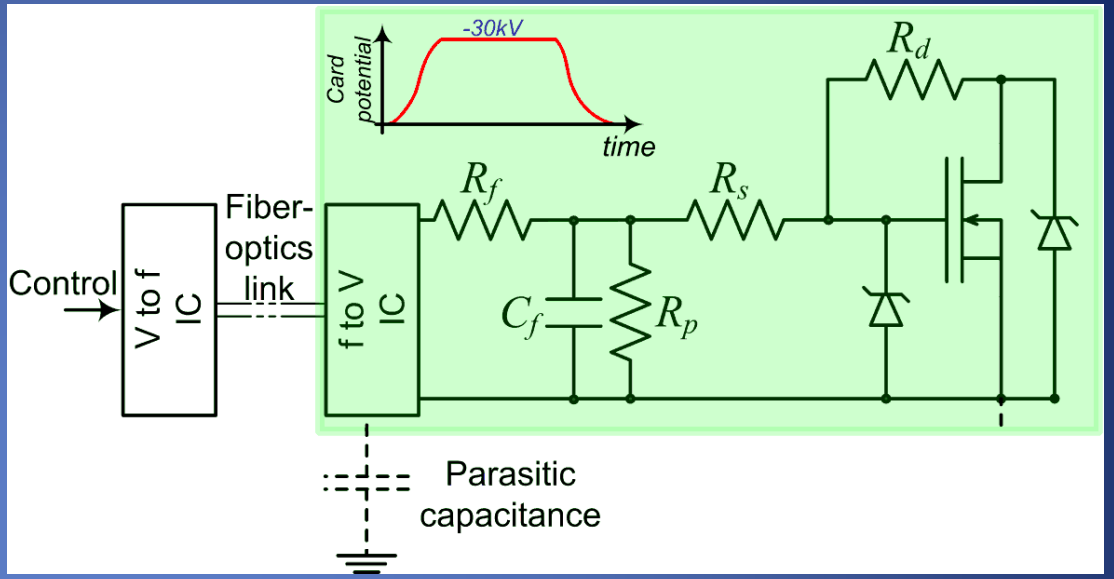
Flat-top length: 1.8 *ms*
Repetition rate: 2 *Hz*
Stability at flat-top:< 1 %
HF ripple at flat-top:< 0.1 %
Nom. voltage to cathode :50 *kV*
Voltage range: ~ 45 to 55 *kV*
Band pass: ~5 *kHz*



Driver topology choice

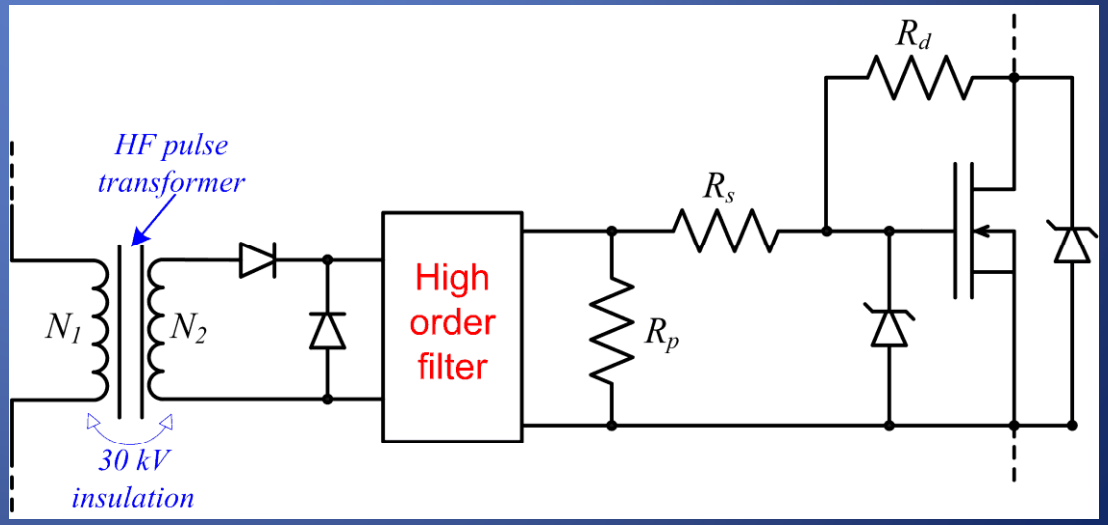
•Fiber optics based

- ➢Costly (fiber optic cables and the electronics).
- ➢Reliability: mechanical robustness, aging process.
- ➢More care: very susceptible to mishandling and dirt.
- ➢Parasitic capacitance concerns on IC.
- ➢Power supply on each card.



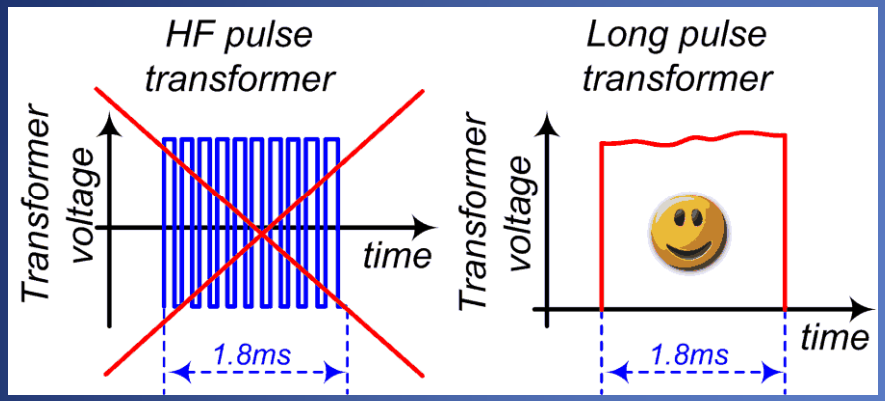
•HF pulse transformer

- ➢High order filter required to respect specifications (12th order @ 100 *kHz*).
- ➢Oscillations problems due to the filter.
- ➢Stray capacitances issues with HF pulse transformers.



Driver topology choice

- Long pulse transformer

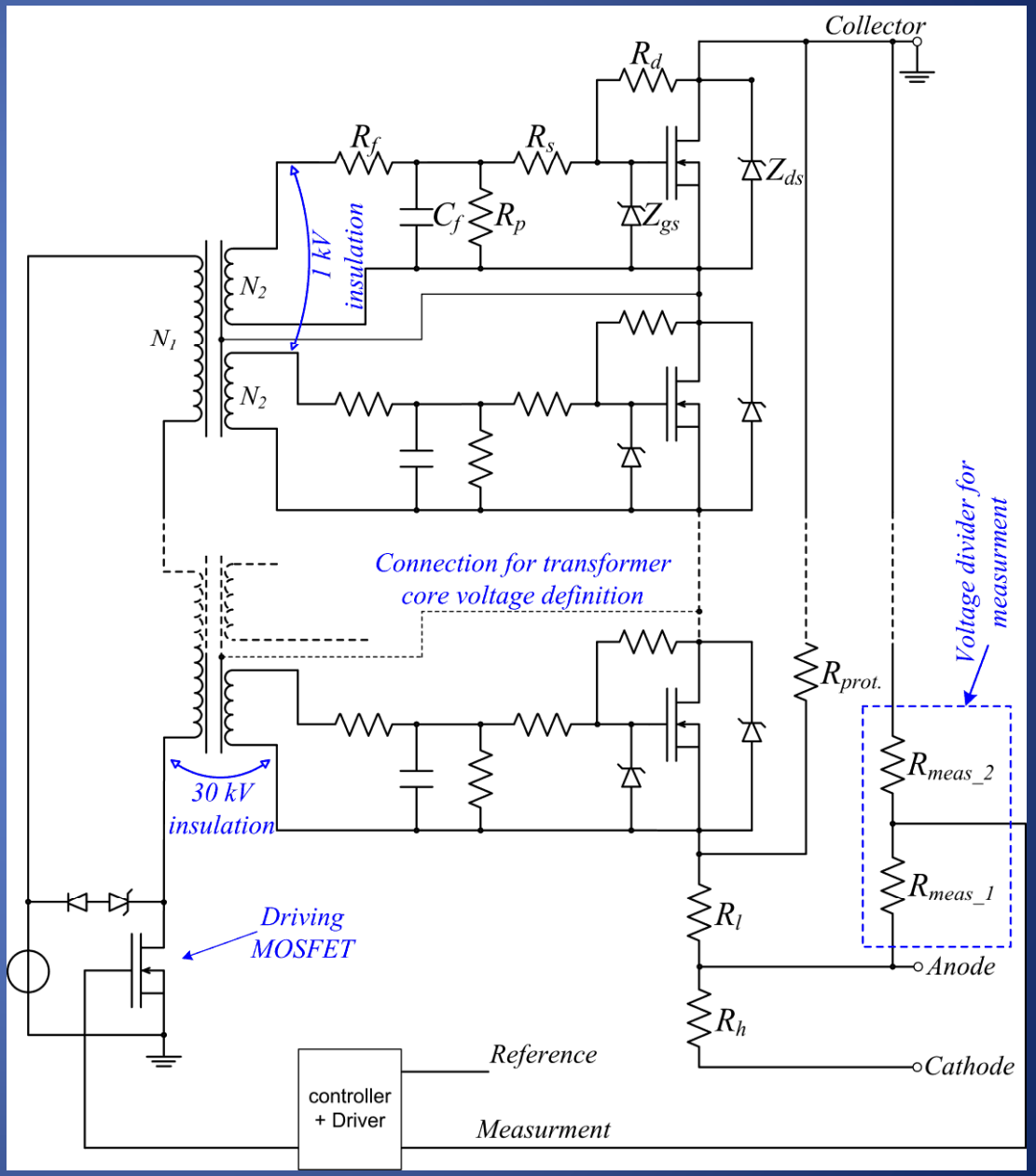


Advantages

- No ripple due to frequency modulation – no filter.
- No ICs at pulsing High Voltage potential.
- Simple control by linear variation of primary winding voltage.

Drawbacks

- Mass & volume slightly increased.



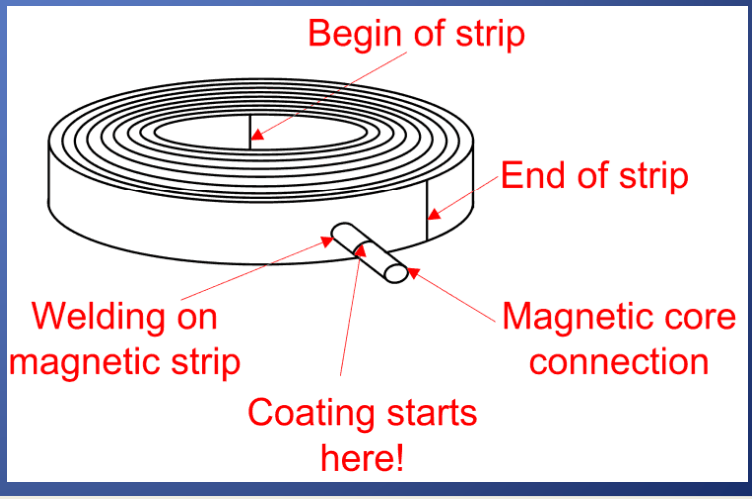
System design challenges

- Transformers design
  - Needs: Low eddy currents – Low stray capacitances – Mass & volume reduction - minimum voltage per turn (~200 *mV*) to decrease induced noise perturbations effects – High V·s value.

	Ferrite	Silicon-iron / Nickel-iron
Relative permeability μ_r	Low	High
Eddy currents insulation	Very high (HF applications)	Depends on thickness
Saturation level	Low (increased volume)	High (decreased volume)

Solution

-Use of thin strip wound cores (Silicon-iron - Nickel iron).
-Thickness of 25 μm (0.001”).
-Separated windings to reduce coupling capacitance.

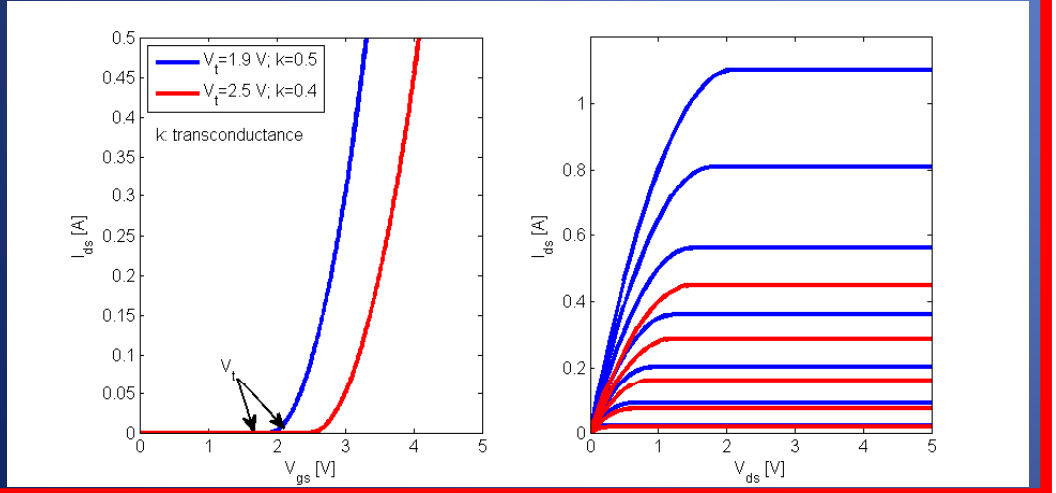


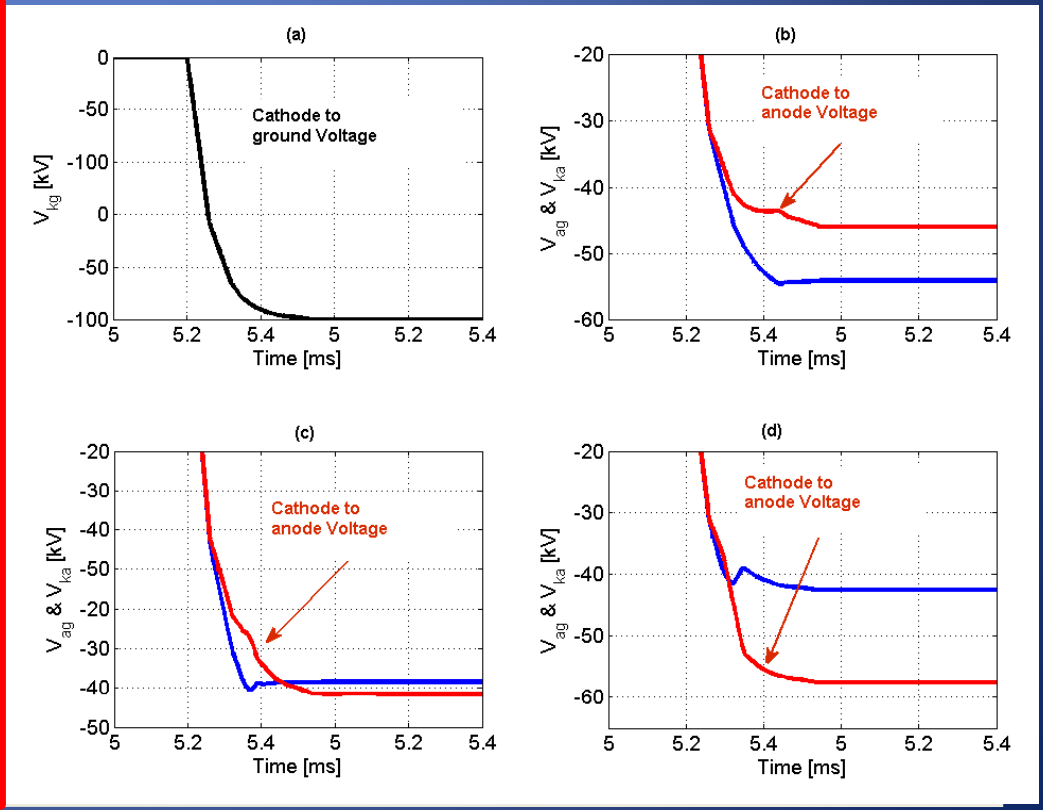
Numerical simulations

Saber simulator used to verify the system behavior

Simulation shows good dynamical response of the stack.
Transformers & MOSFETs stray capacitance were taken into account.

Differences between each MOSFET as well as differences on transformers characteristics were considered.

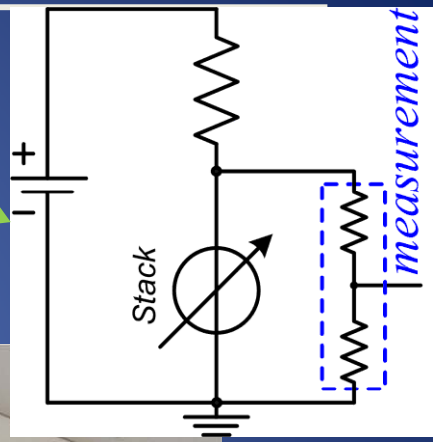


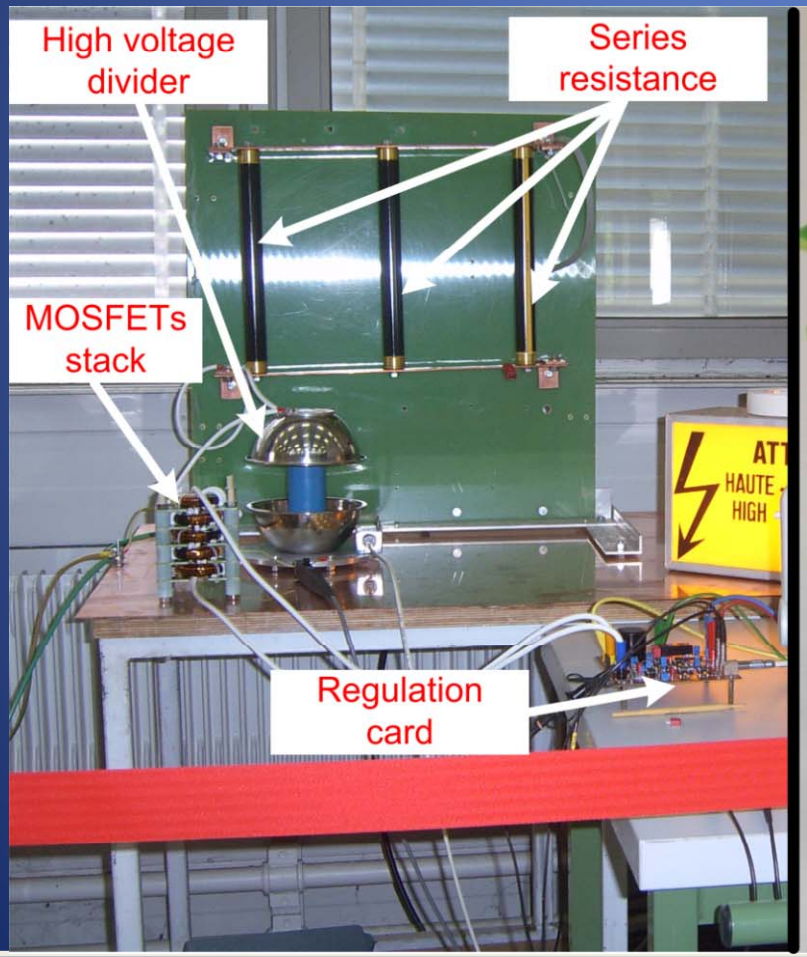


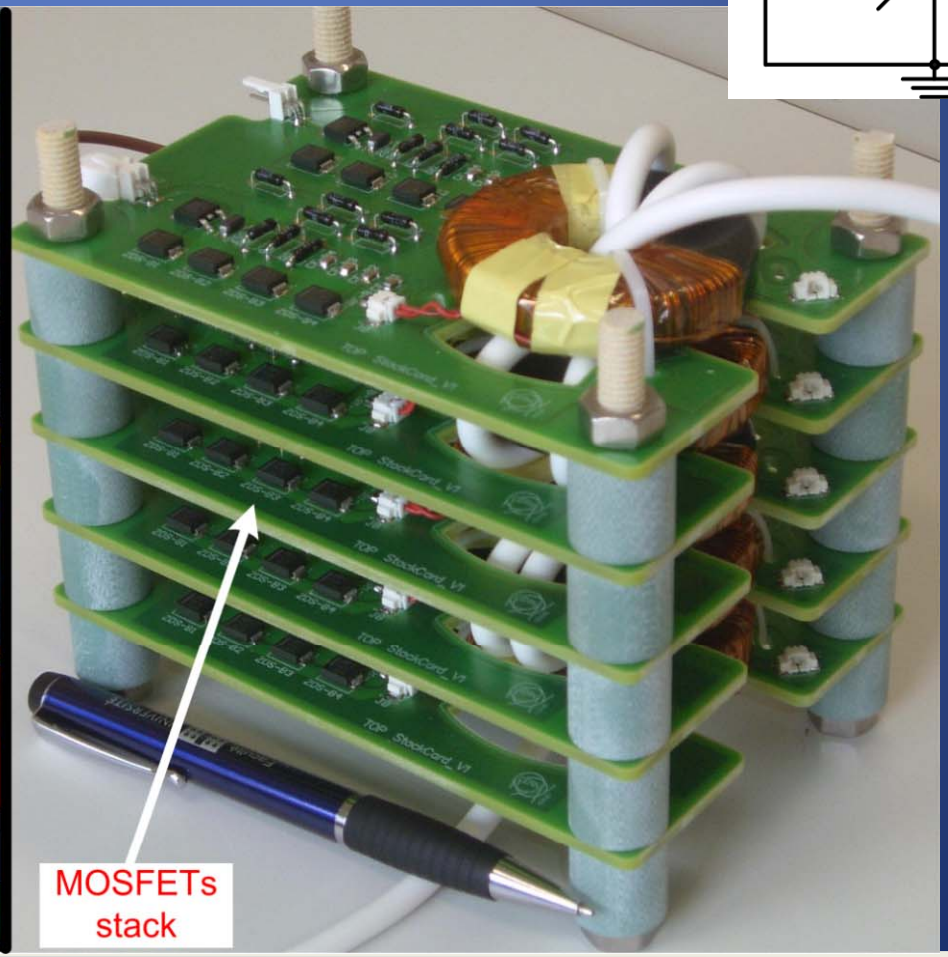
Experimental results

5*kV* stack prototype

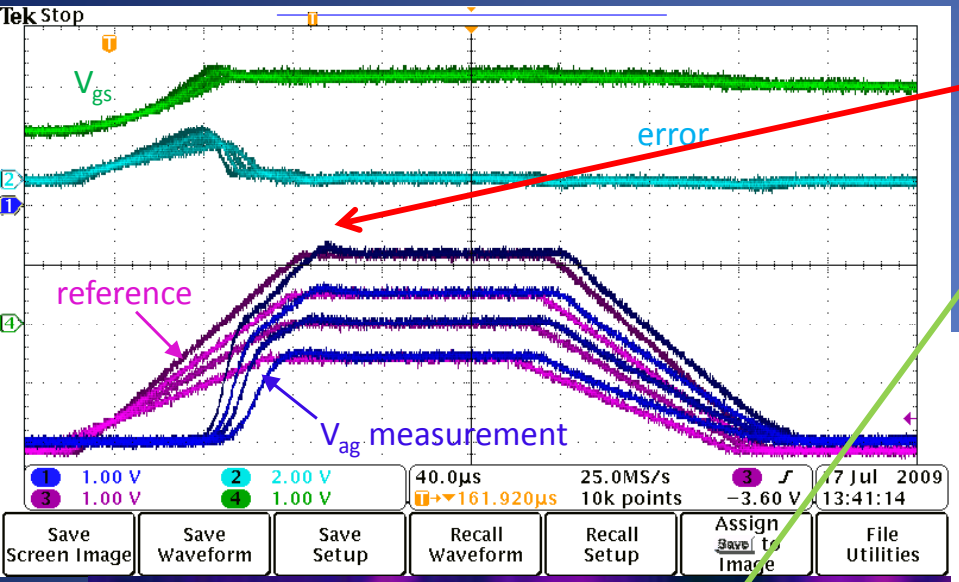
Tested circuit schematic

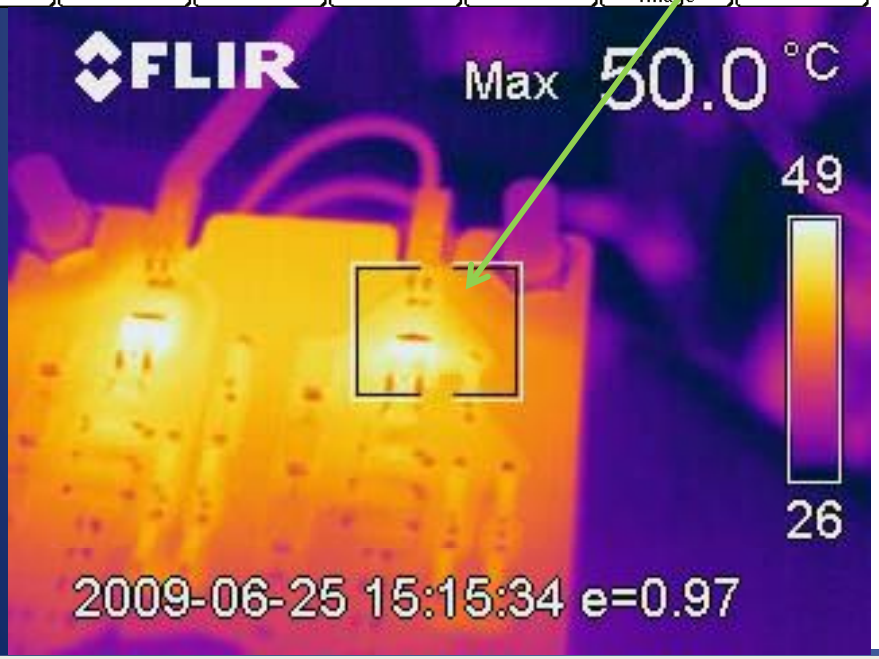






Experimental results

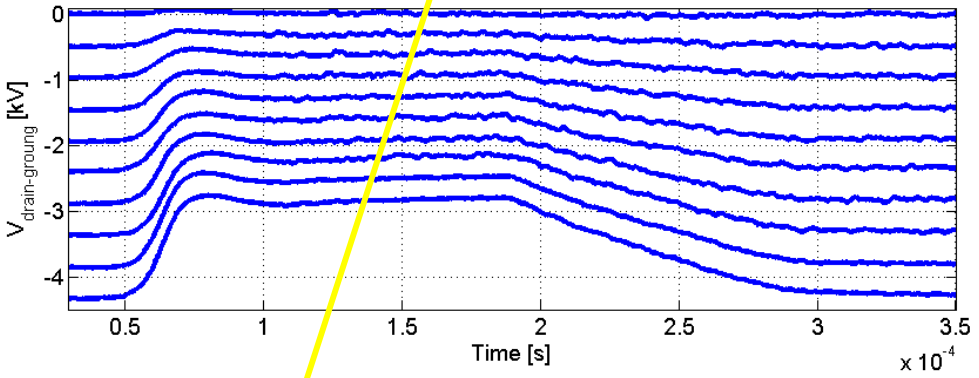


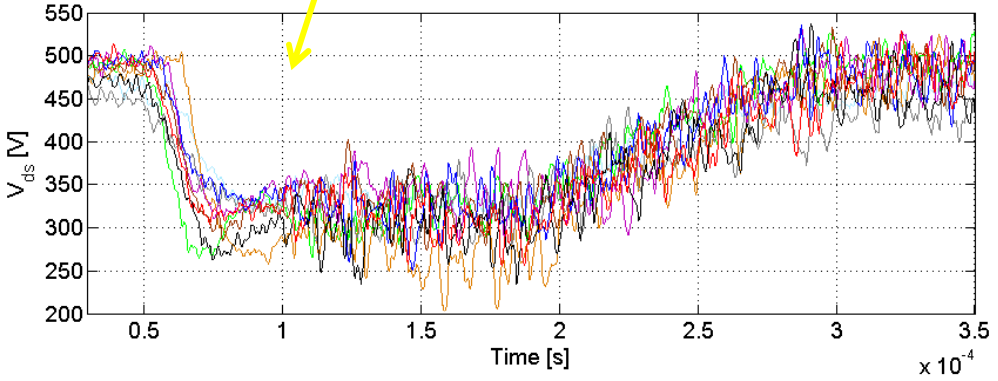


Dynamics ok!

Temperature ok, but…cycling?

Voltage sharing good!





Conclusion

- Very good voltage sharing regulation.
- Bandwidth & ripple specifications respected.
- Modular topology offering very low MTTR.
- Highly reliable system - passive components only on stack electronic boards.
- Low material cost - less than 1 k*euro* for one stack (30*kV*).
- Future: Thermal cycling impose a little reduction in the maximum junction temperature to improve lifetime – not a big deal!

Thank you!