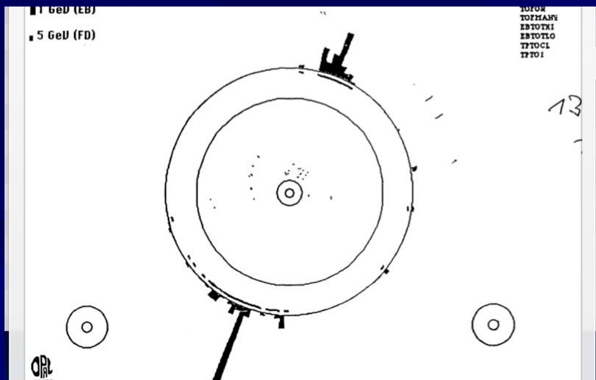
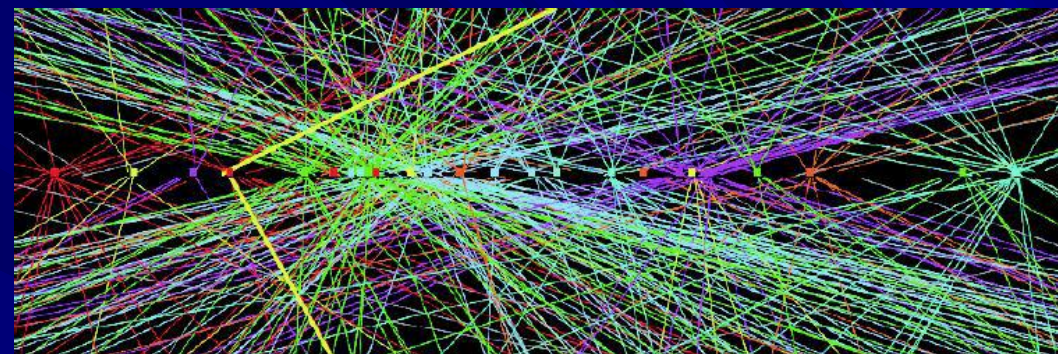
Real Time systems
Introduction



The First $Z^0 \rightarrow e^+e^-$ at LEP
OPAL-13 August 1989



Z -> μμ event at LHC ATLAS 15 April 2012

P. Le Dû

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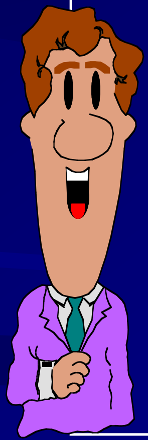
Vietnam Real Time systems School

Goals of these presentations

Introduce the concept of 'REAL TIME' and its technological evolution in HEP over the last 40 years.

Illustrated by some typical applications in various fields.



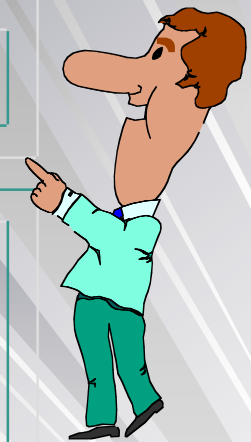
Part # 1 & 2- What is Real Time ?'

- Definition of REAL TIME ?
  - Introducing the subject of this school
  - Context & Basic definitions & terminology
- A 45 years of HEP history 1969 – 2016
  - From bubble chamber to today
- Evolution of components architectures ,tools and techniques
- A view in the the future !
- Application in other fields

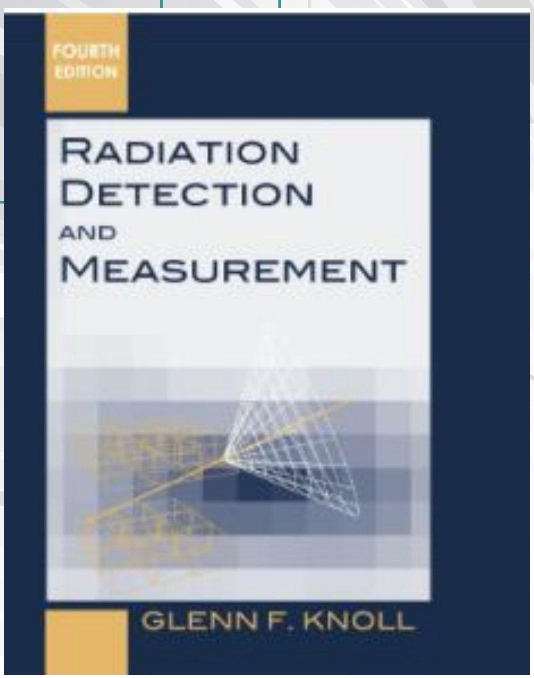
Thanks

- Some material and lots of inspiration for these lectures was taken from various lectures
  - Helmuth Speiler (LBNL)
  - Philippe Farthouat (CERN)
  - Christophe Delataille (IN2P3)
  - Ted Liu (FNAL)
  - G.Watts (UW)
  - … and many others
- Some overlap with the other lectures but it is good to see the same topic from different sides

Few words about Detectors



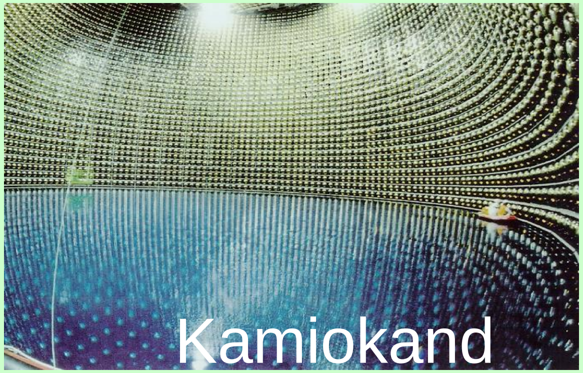
Radiation
Instrumentation
The Bible
Glenn Knoll



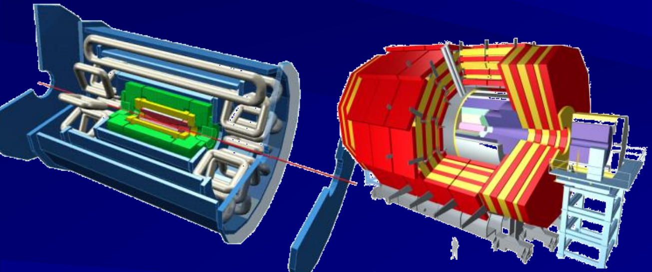
Particle detectors

- Colliders

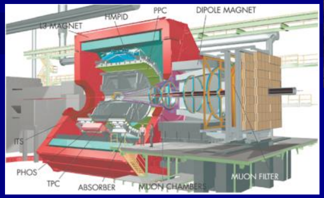
- Fixed target



- Non accelerator

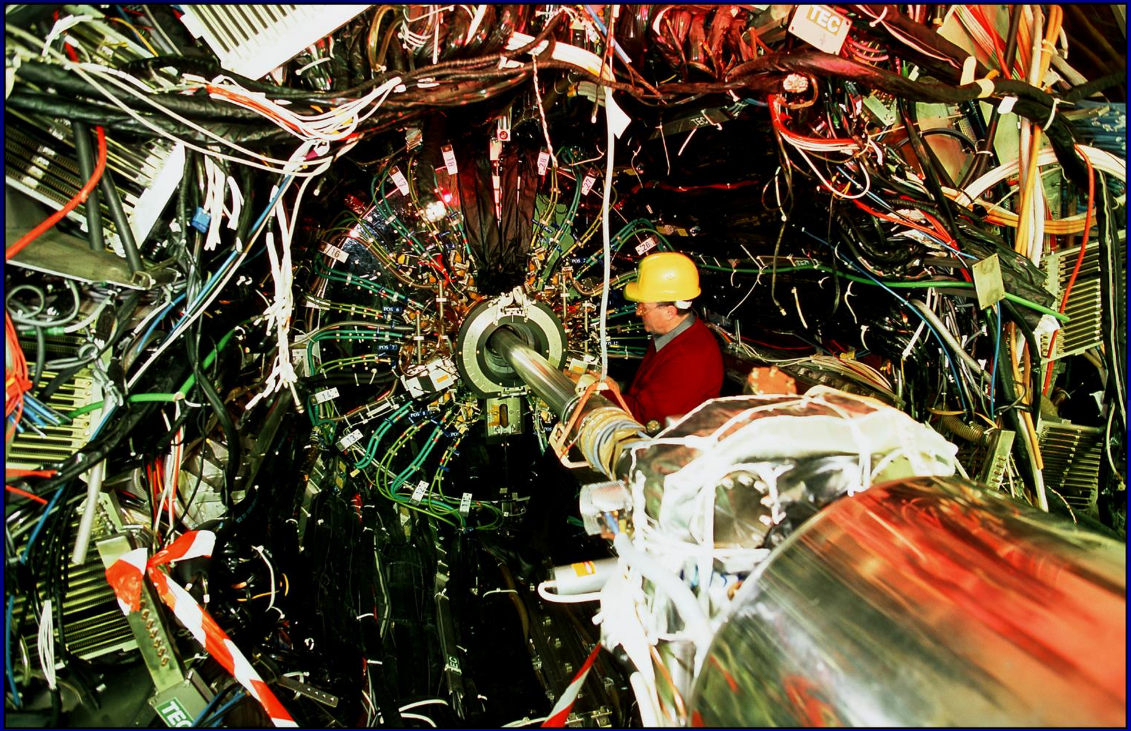


LHC

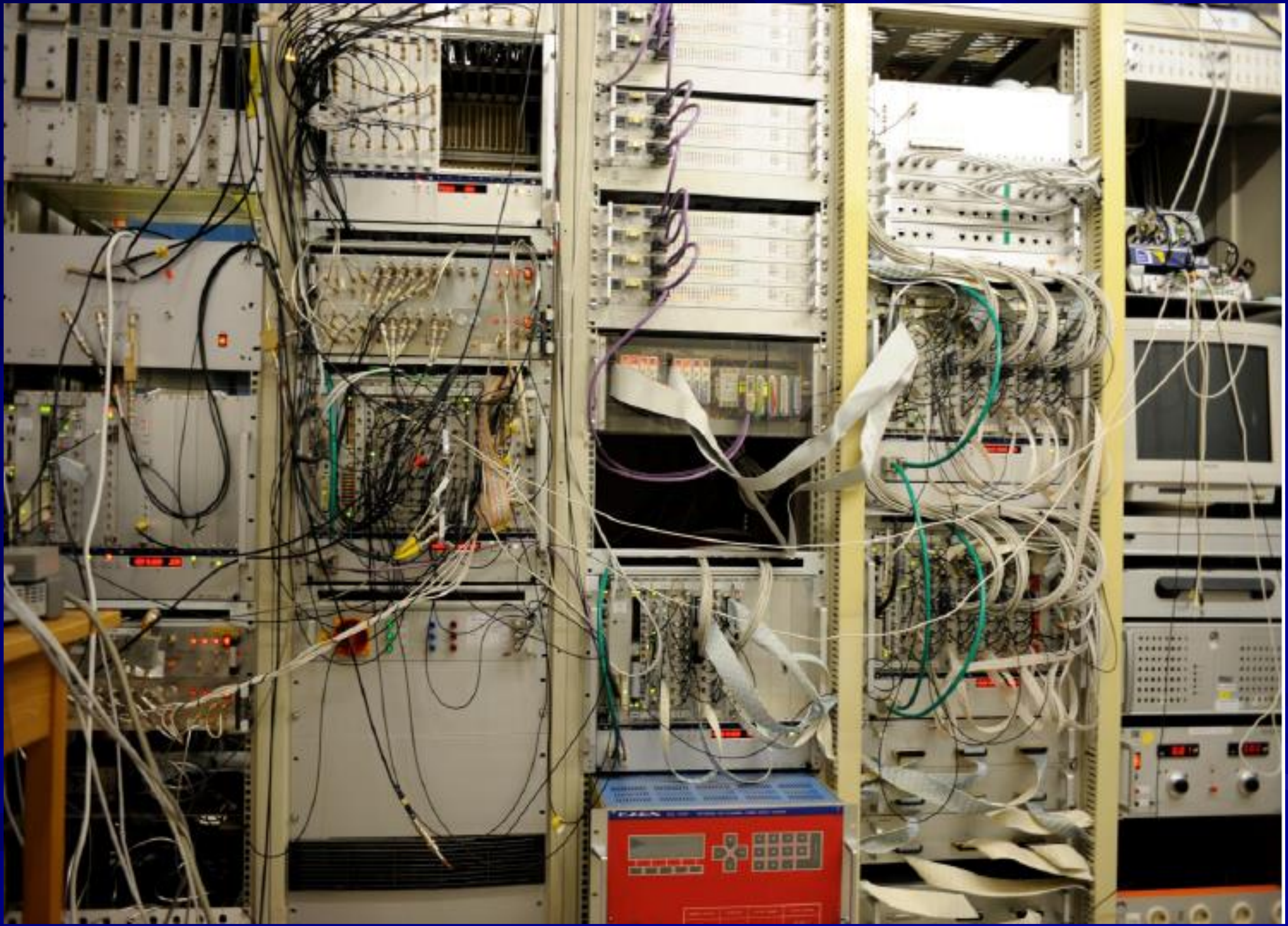


Electronics in experiments

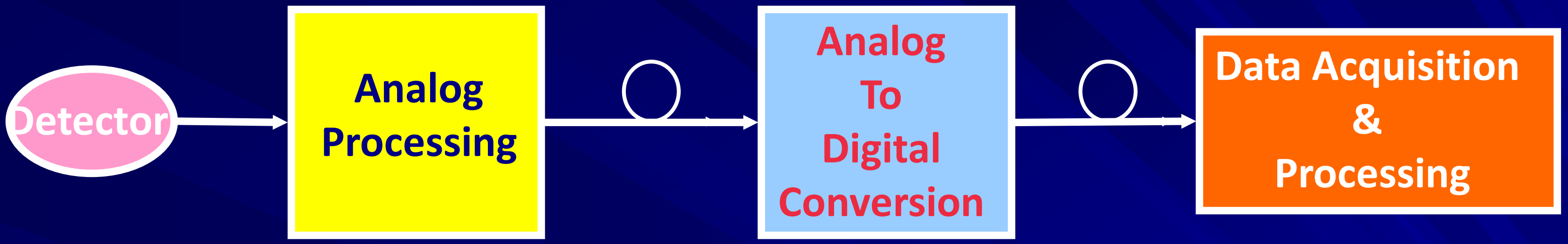
- A lot of electronics in the experiments…
  - Readout electronics :
    - amplification, filtering… : Analog electronics
    - Processing & Trigger electronics : Digital electronics (bits)



But also that !



The electronics blocks



On-detector

On-detector
Or
Off-detector

Off-detector

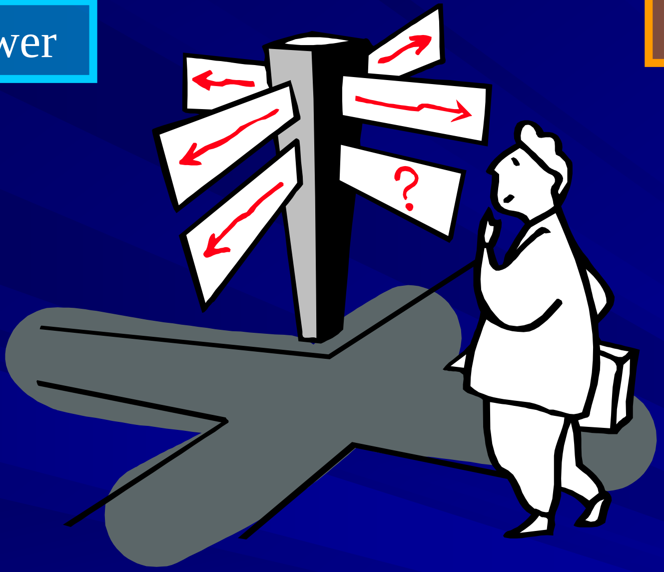
- Analog processing
- Analog to digital conversion
- Technology evolution
- Off-detector digital electronics

Readout electronics : requirements

Low noise

Low power

High speed



High reliability

Large dynamic range

Radiation hardness

Low cost !

(and even less)

Low material

Front End Electronics

Helmuth Speiler lectures

http://www-physics.lbl.gov/~spieler/

Requirements principles

- Sensors electronics must determine
  1. presence of a particle
  2. magnitude of signal
  3. time of arrival
- Some measurements depend on *sensitivity*, i.e. detection threshold, e.g.: silicon tracker, to detect presence of a particle in a given electrode
- Others seek to determine a *quantity very accurately*, i.e. resolution, e.g. : calorimeter – magnitude of absorbed energy; muon chambers – time measurement yields position

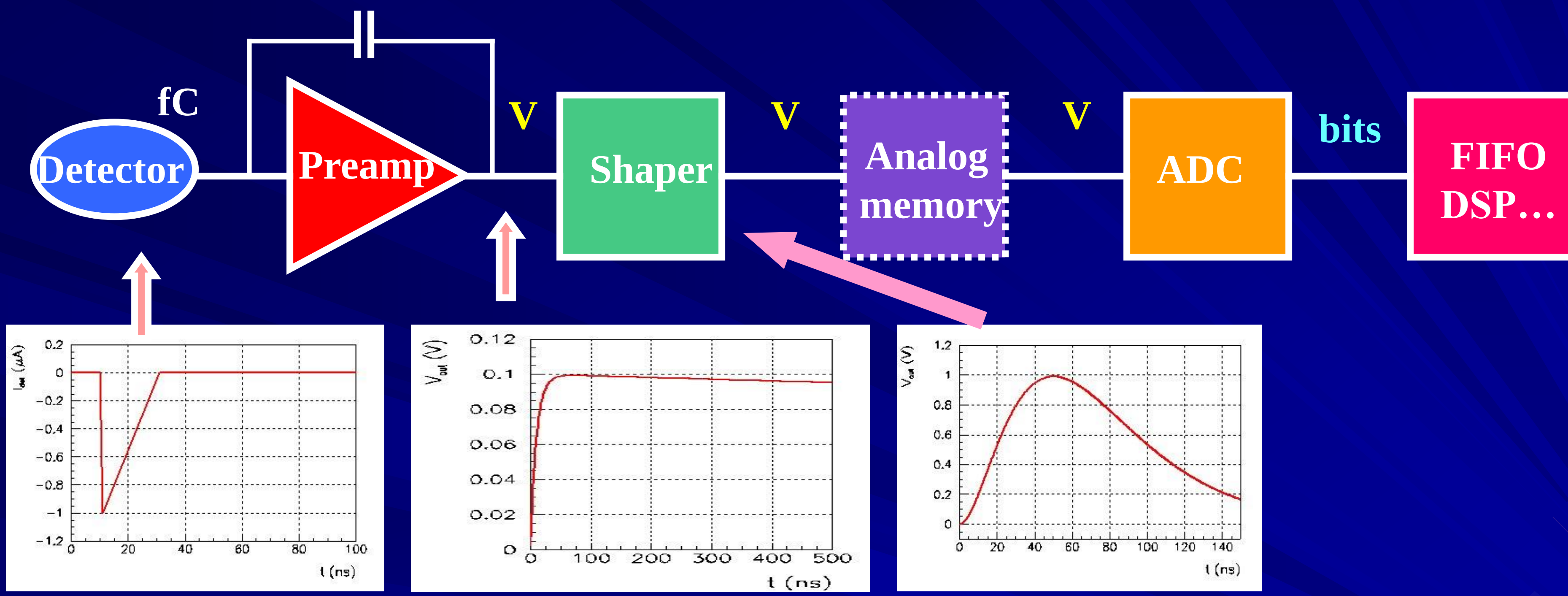
All have in common that they are sensitive to:

1. signal magnitude
2. fluctuations

What is “front-end” electronics`

- Front-end electronics is the electronics directly connected to the detector (sensitive element)
- Its purpose is to
  - acquire an electrical signal from the detector (usually a short, small current pulse)
  - tailor the response of the system to optimize
    - the minimum detectable signal
    - energy measurement (charge deposit)
    - event rate
    - time of arrival
    - insensitivty to sensor pulse shape
  - digitize the signal and store it for further treatment

Overview of Front End readout electronics chain



- Very small signals (fC) -> need amplification
- Measurement of amplitude and/or time
  - (ADCs, discris, TDCs)
- Several thousands to millions of channels

A more global view

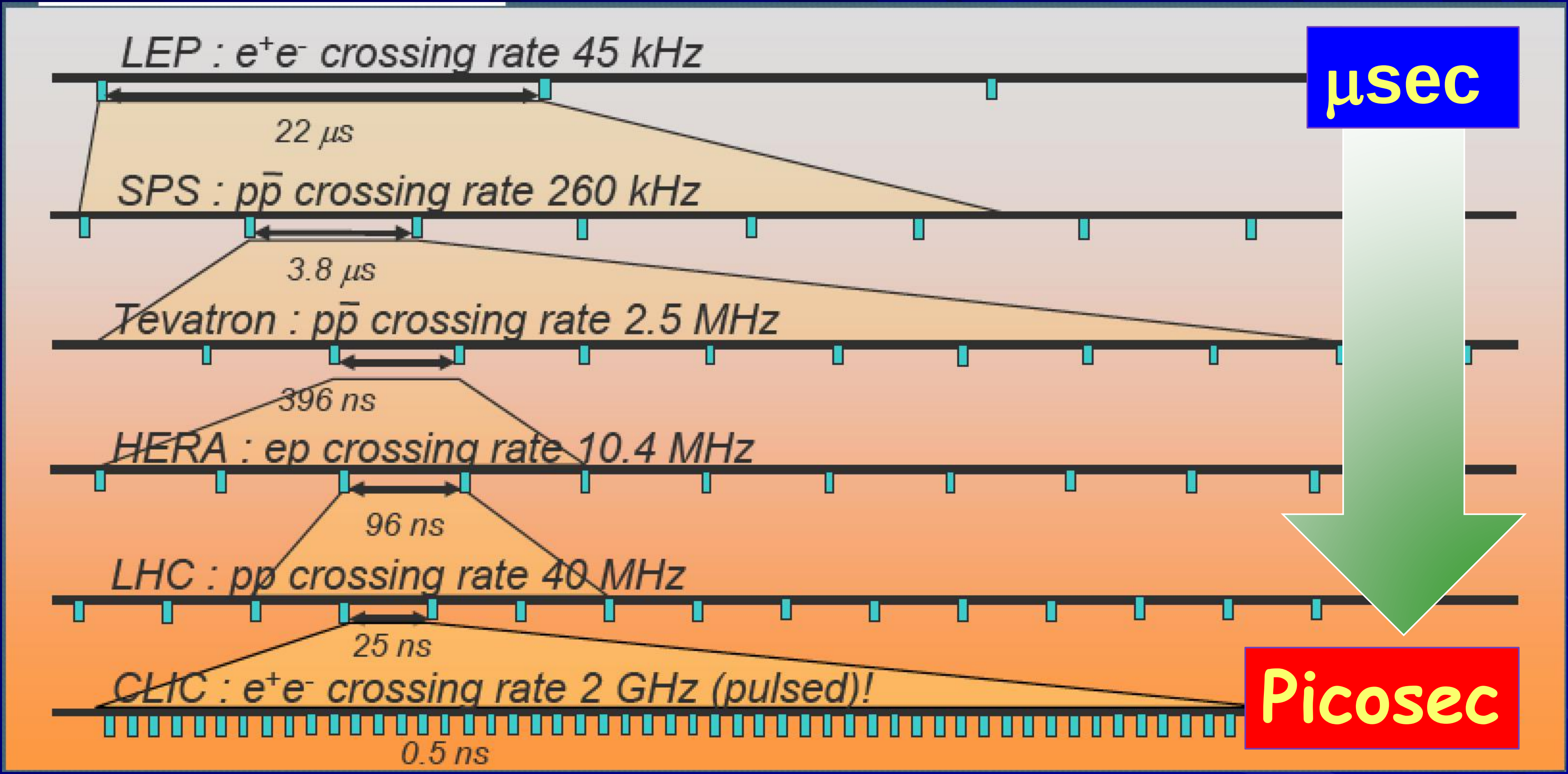
Evolution of basic parameters

Exp. *Year*	Collision rate	Channel count	L1A rate	Event building	Processin g. Power	Sociolog y
UA's *1980*	3 µsec	-	-	-	5-10 MIPS	150-200
LEP *1989*	10-20 µsec	250 - 500K	-	10 Mbit/sec	100 MIPS	300-500
BaBar *1999*	4 ns	150K	2 KHz	400 Mbit/s	1000 MIPS	400
Tevatron *2002*	396 ns	~ 800 K	10 - 50 KHz	4-10 Gbit/sec	5.10^4 MIPS	500
LHC *2010*	25 ns	200 M*	100 KHz	20-500 Gbit/s	$>10^6$ MIPS	5000
ILC *2025 ?*	330 ns	900 M*	3 KHz	10 Gbit/s	$\sim 10^6$ MIPS ?	> 3000 ?

** including pixels*

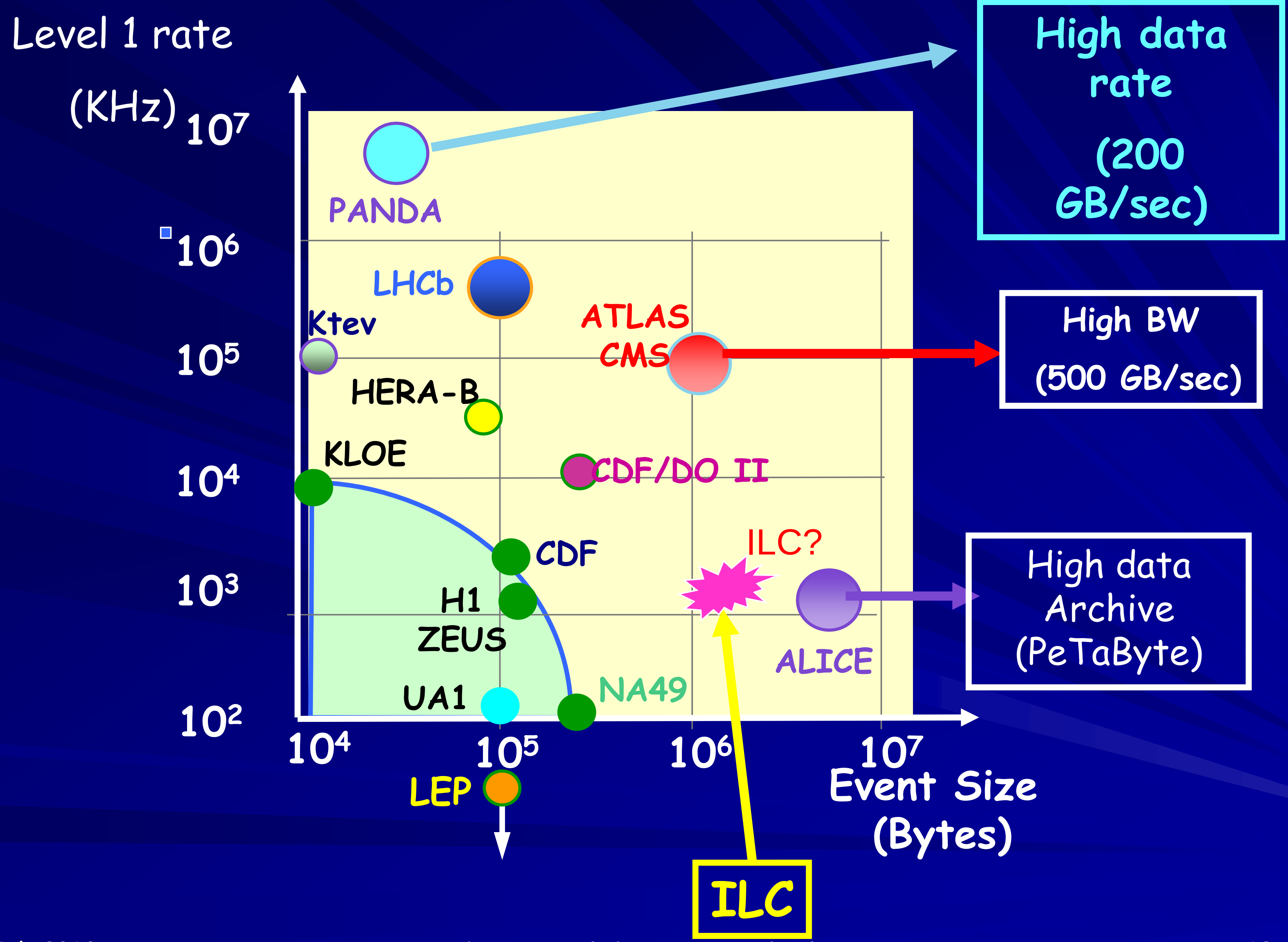
Sub-Detector	LHC	ILC
Pixel	150 M	> 800 M
Microstrips	~ 10 M	~30 M
Fine grain trackers	~ 400 K	1,5 M
Calorimeters	200 K	30 -100 M
Muon	~1 M	

Timing & synchronization issues

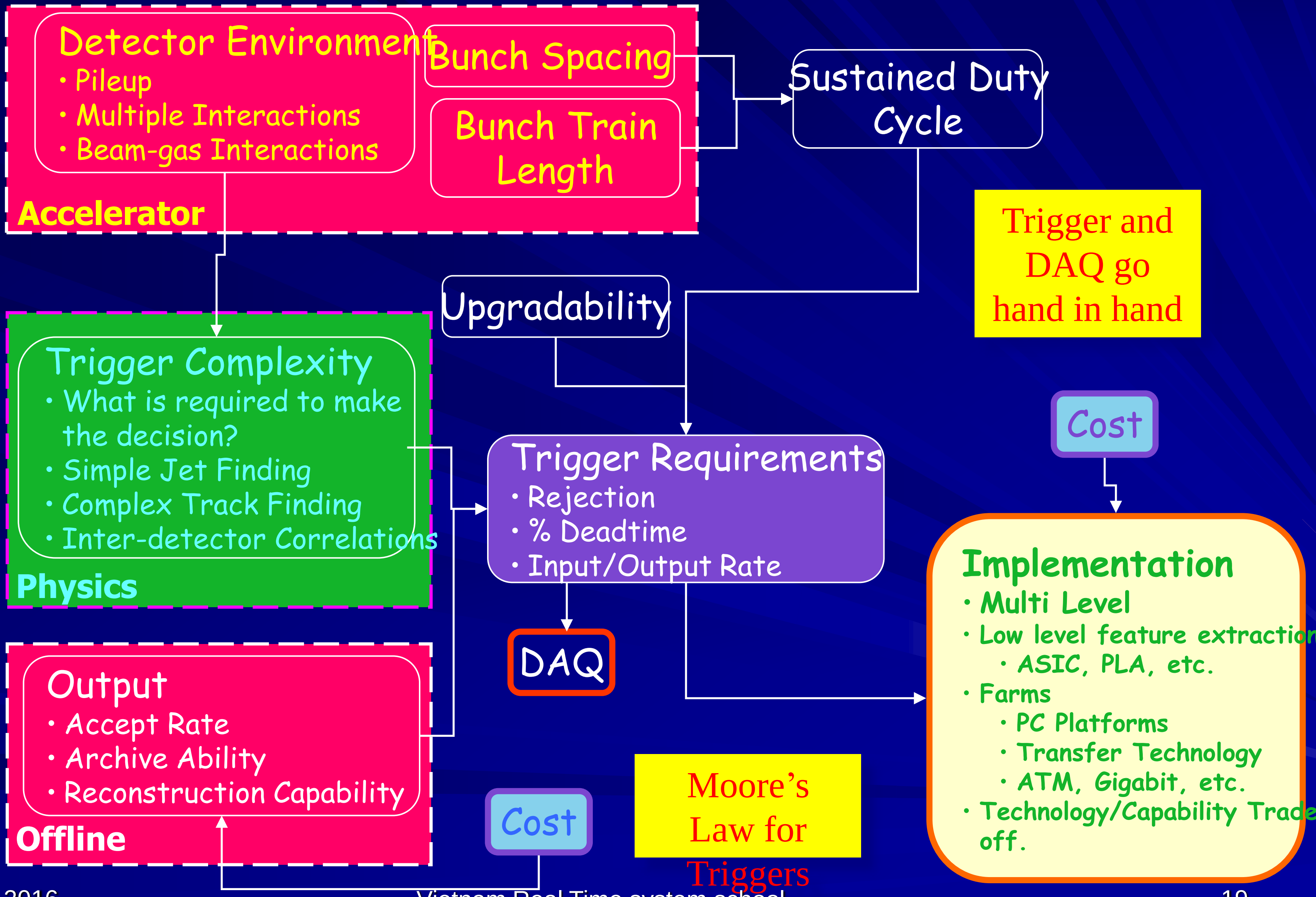


- From microseconds → to picoseconds
- How to synchronize 10^6-10^8 channels ?

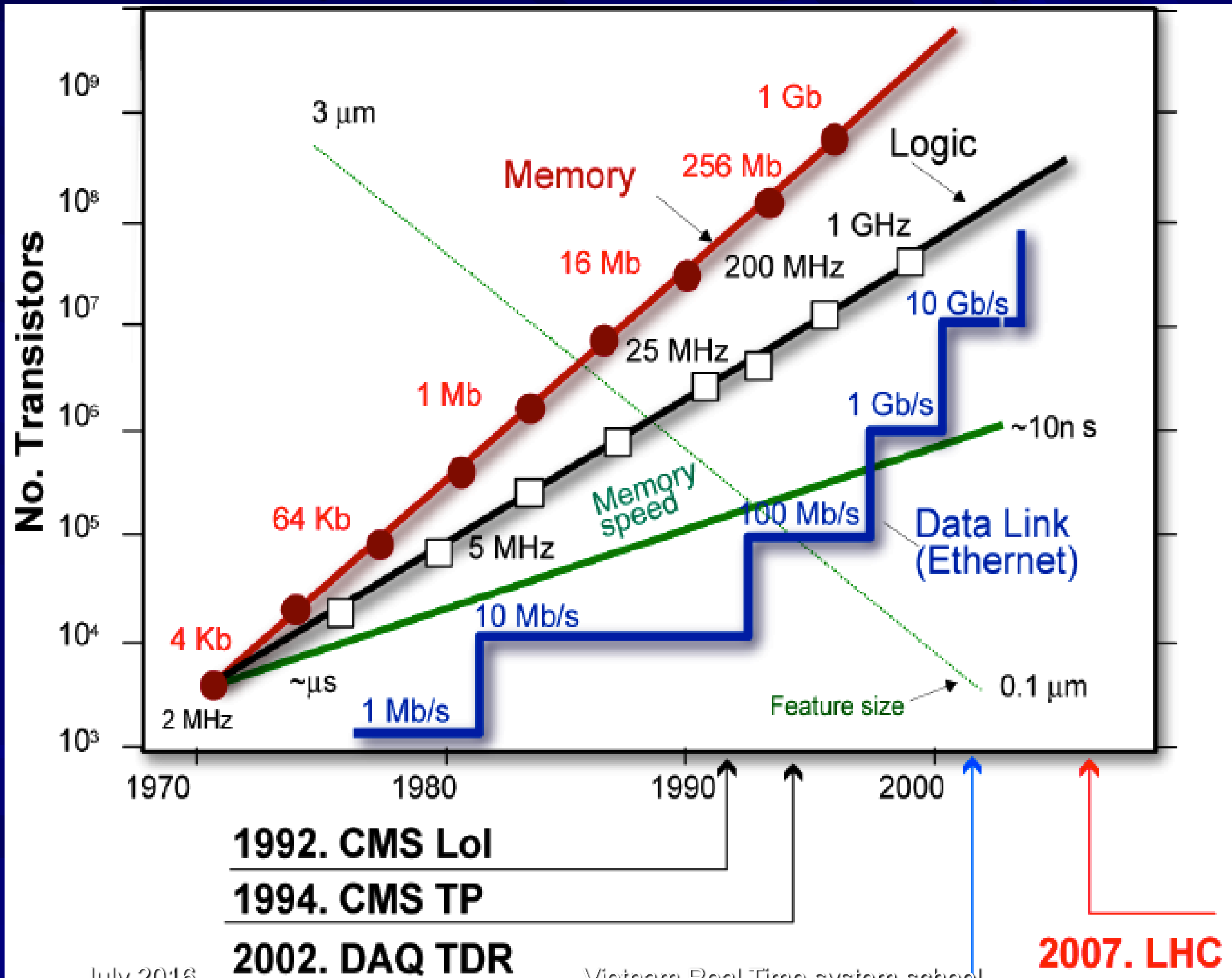
Rates and data volume



Constraints → a multiparameters problem



The Long Term issue challenge → 15 years of design-20 years of life



Tevatron
CDF/DO
1980-2012

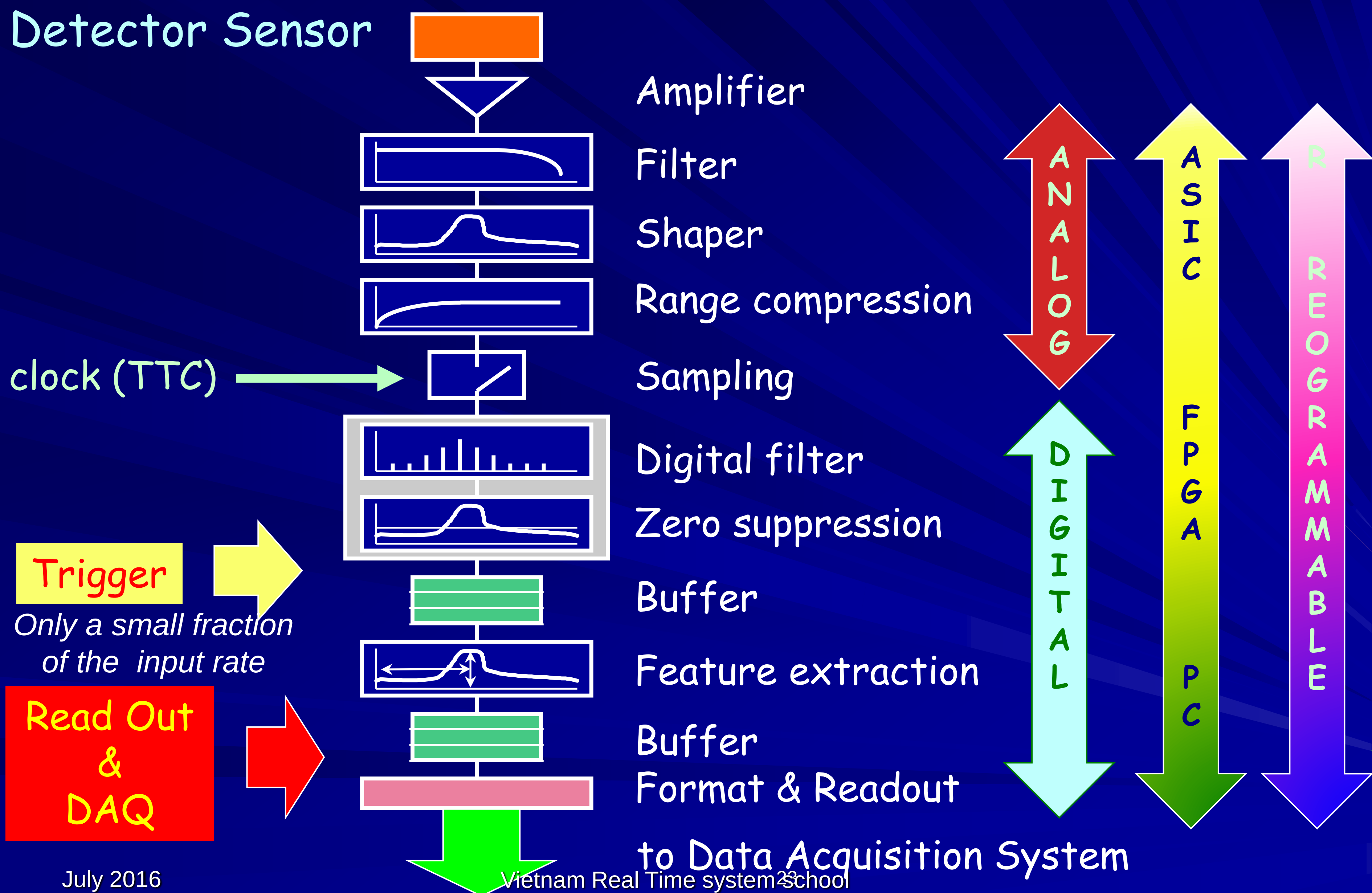
The 'More law' LHC example

Some basic terminology

What Do We Need to Read Out a Detector ?

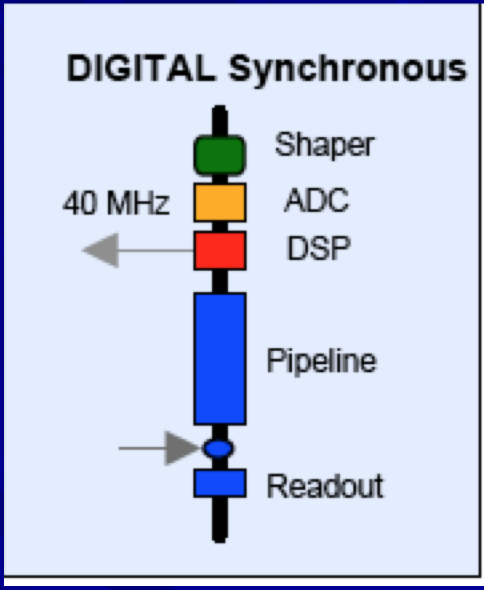
- A selection mechanism → "TRIGGER"
- Electronic readout of the sensors of the detectors →"front-end electronics"
- A system to keep all those things in sync → "clock"
- A system to collect the selected data →"DAQ"
- A Control System to configure, control and monitor the entire DAQ
- Time, money, students

The read-out chain processing flow



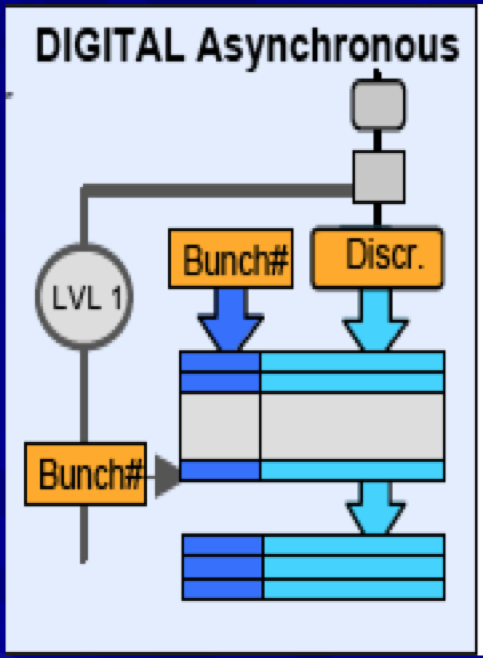
Synchronous readout

- All channels are doing the same "thing" at the same time
  - Synchronous to a global clock → *The bunch crossing*
- On-detector buffers (*de-randomizers*) are of the same size and their occupancy ("how full they are") depends only on the *trigger-rate*
- *Output* data-rate on each link is identical and depends only on *trigger -rate*
- ☹ Lots of bandwidth wasted for zero's
  - Price of links determine if one can afford this
- ☺ No problems if occupancy of detectors or noise higher than expected
  - But there are other problems related to this: spill over, saturation of detector, etc.



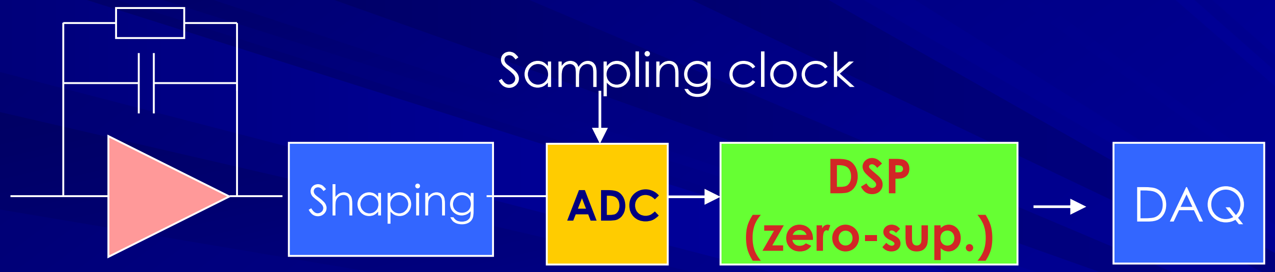
Asynchronous readout

- Remove zeros on the detector itself
  - Lower average bandwidth needed for readout links. Especially interesting for low occupancy detectors
- Each channel "lives a life of its own" with unpredictable buffer occupancies and data are sent whenever ready (asynchronous)
- In case of buffer-overflow a truncation policy is needed → BIAS!!
  - Detectors themselves do not have 100% detection efficiency either.
  - Requires sufficiently large local buffers to assure that data is not lost too often (Channel occupancies can be quite non uniform across a detector with same front-end electronics)
- DAQ must be able to handle this (buffering!)



Constantly sampled

- Needed for high rate experiments with signal pileup
- Shapers and not switched integrators
- Allows digital signal processing in its traditional form (constantly sampled data stream)
- Output rate may be far to high for what following DAQ system can handle



- With local zero-suppression this may be an option for future high rate experiments (SLHC, CLIC)

Zero-suppression

- Why spend bandwidth sending data that is zero for the majority of the time ?
- Perform zero-suppression and only send data with non-zero content
  - Identify the data with a channel number and/or a time-stamp
  - We do not want to loose information of interest so this must be done with great care taking into account pedestals, baseline variations, common mode, noise, etc.
  - Not worth it for occupancies above ~10%
- Alternative:
  - data compression

Synchronous readout

- All channels are doing the same "thing" at the same time
- Synchronous to a global clock (bunch crossing clock)
- Data-rate on each link is identical and depends only on *trigger -rate*
- On-detector buffers (*de-randomizers*) are of the same size and there occupancy ("how full they are") depends only on the *trigger-rate*
- ☹ Lots of bandwidth wasted for zero's
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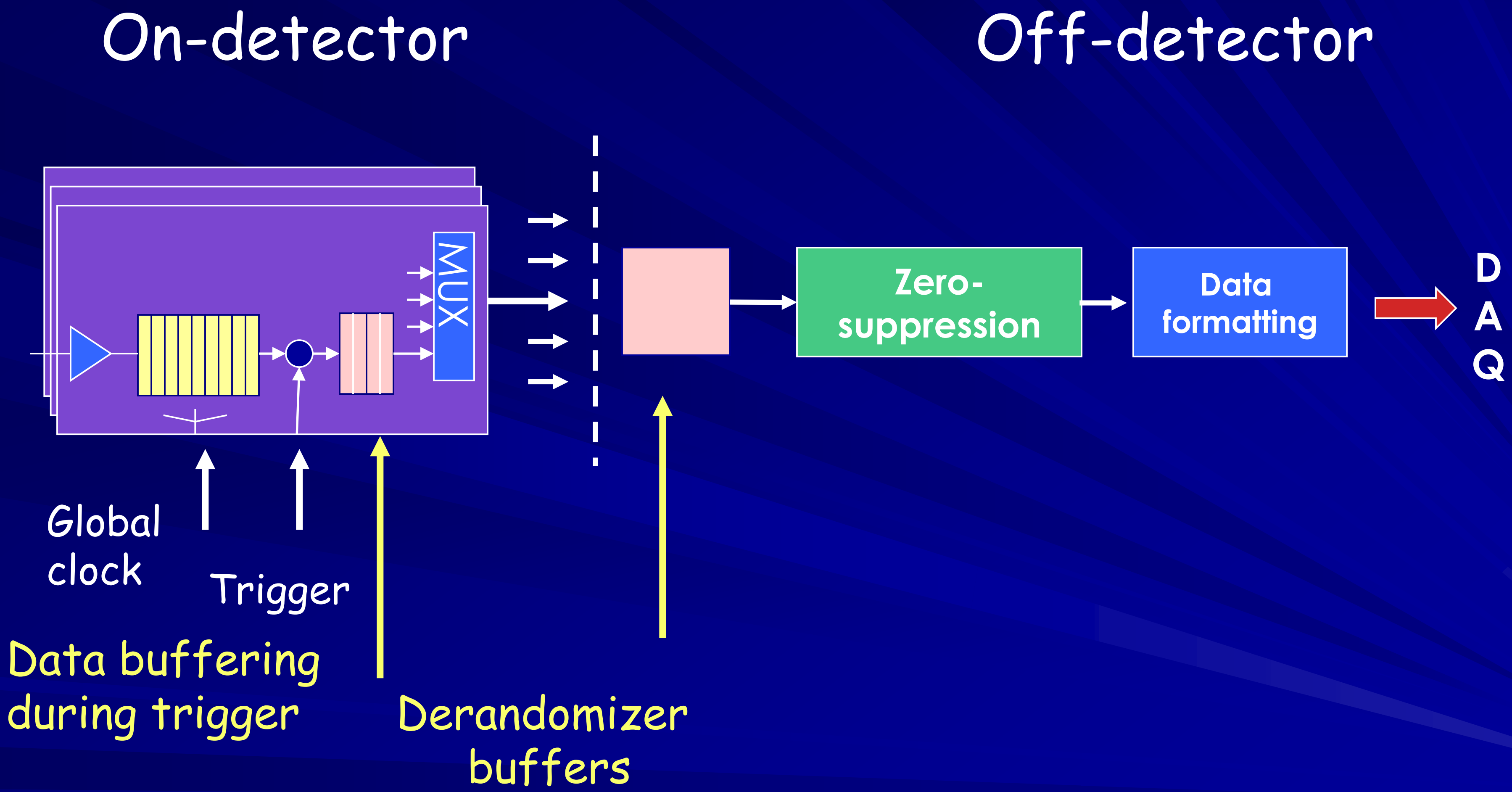
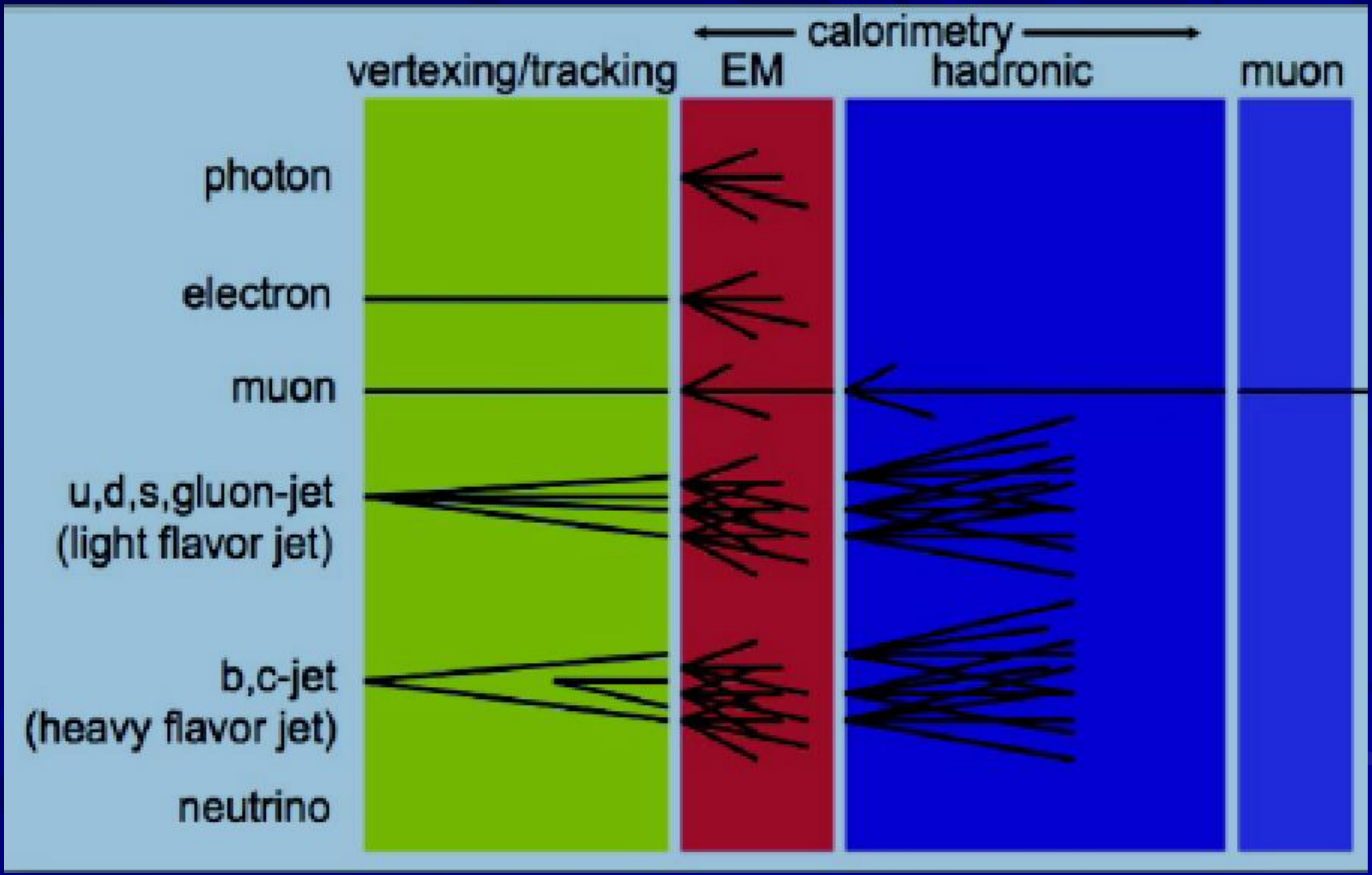
Synchronous readout



Summary: Readout to DAQ

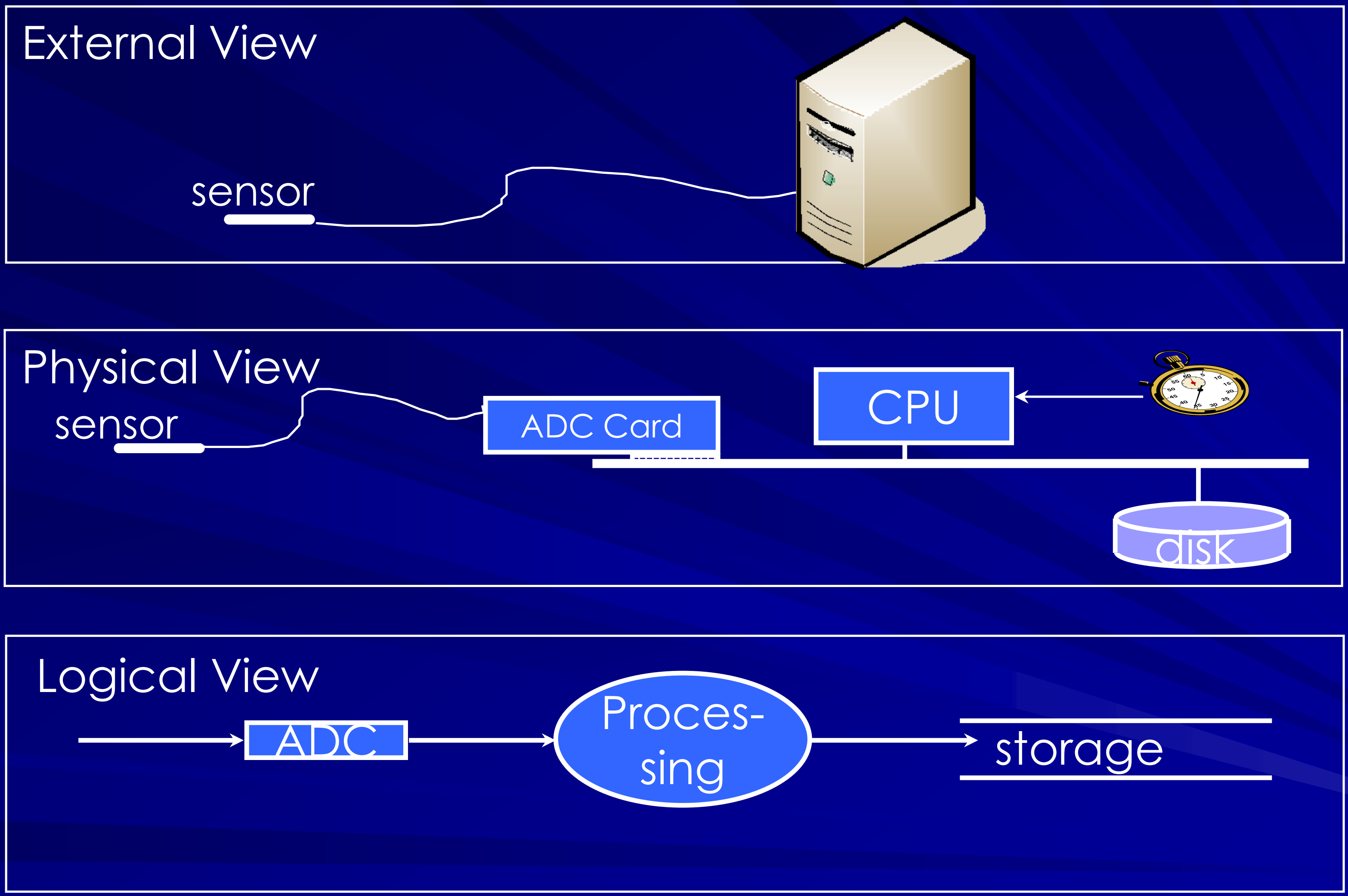
- Large amount of data to bring out of detector
  - Large quantity: ~millions in large experiment
  - High speed: Gbits/s
- Point to point unidirectional
- Transmitter side has specific constraints
  - Radiation
  - Magnetic fields
  - Power/cooling
  - Minimum size and mass
  - Must collect data from one or several front-end chips
- Receiver side can be commercially available module/components (use of standard link protocols when ever possible)

Physics signals & Trigger signatures

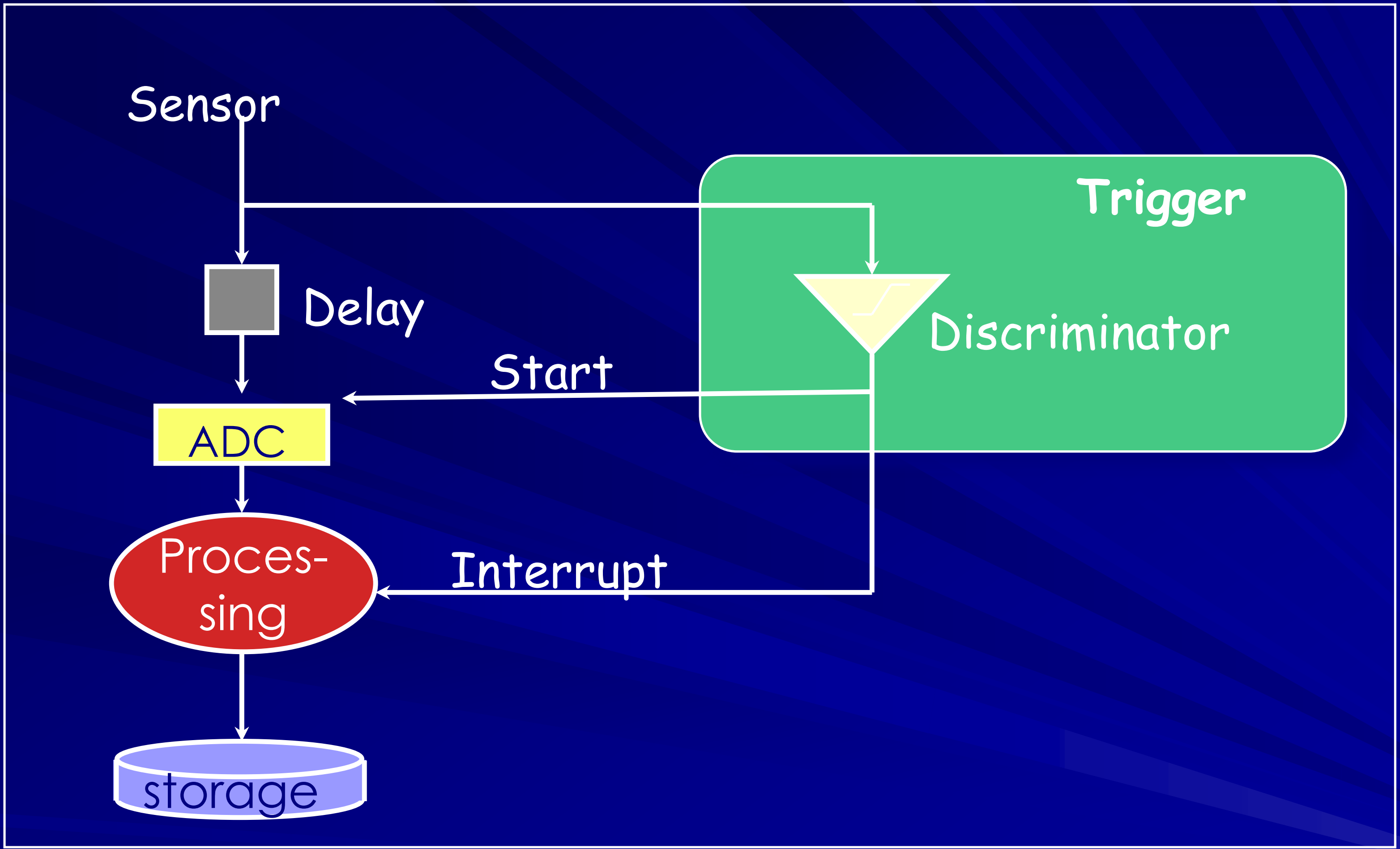


The basics of T/DAQ

Trivial DAQ

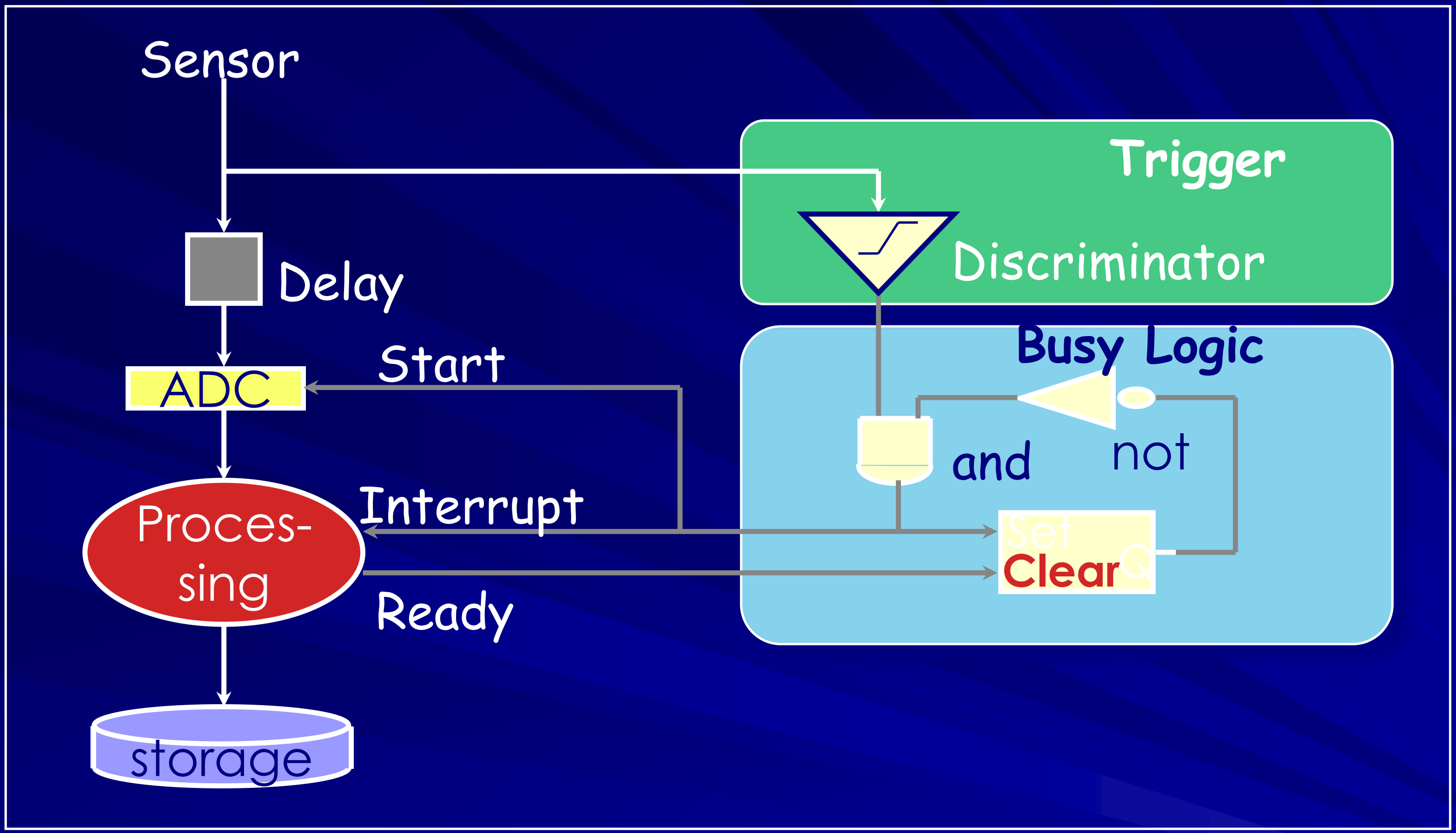

External View
sensor
Physical View
sensor
ADC Card
CPU
disk
Logical View
ADC
Proces-
sing
storage

Trivial DAQ with a real trigger



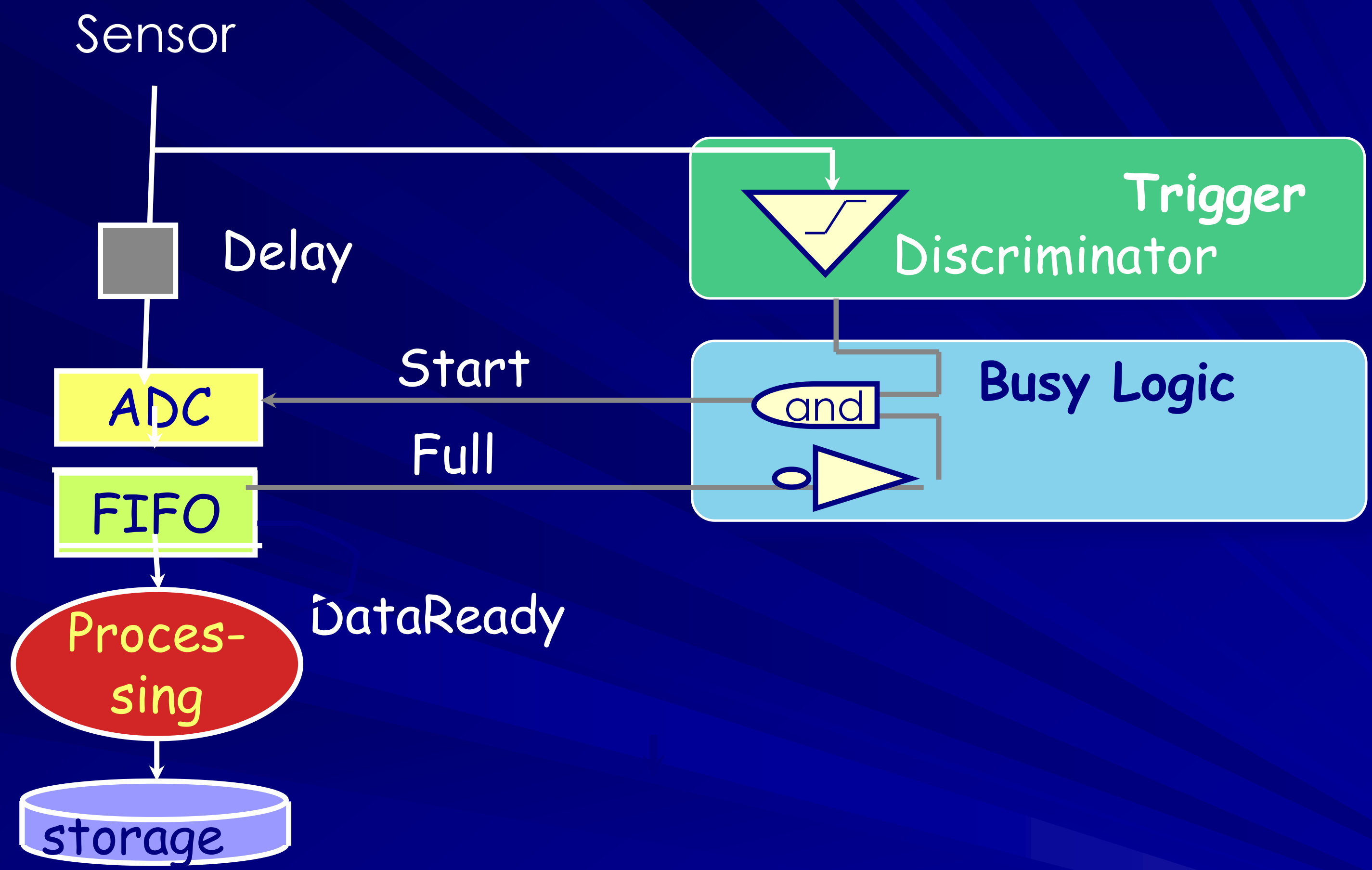
What if a trigger is produced when the *ADC* or *processing* is busy?

Trivial DAQ with a real trigger (2)



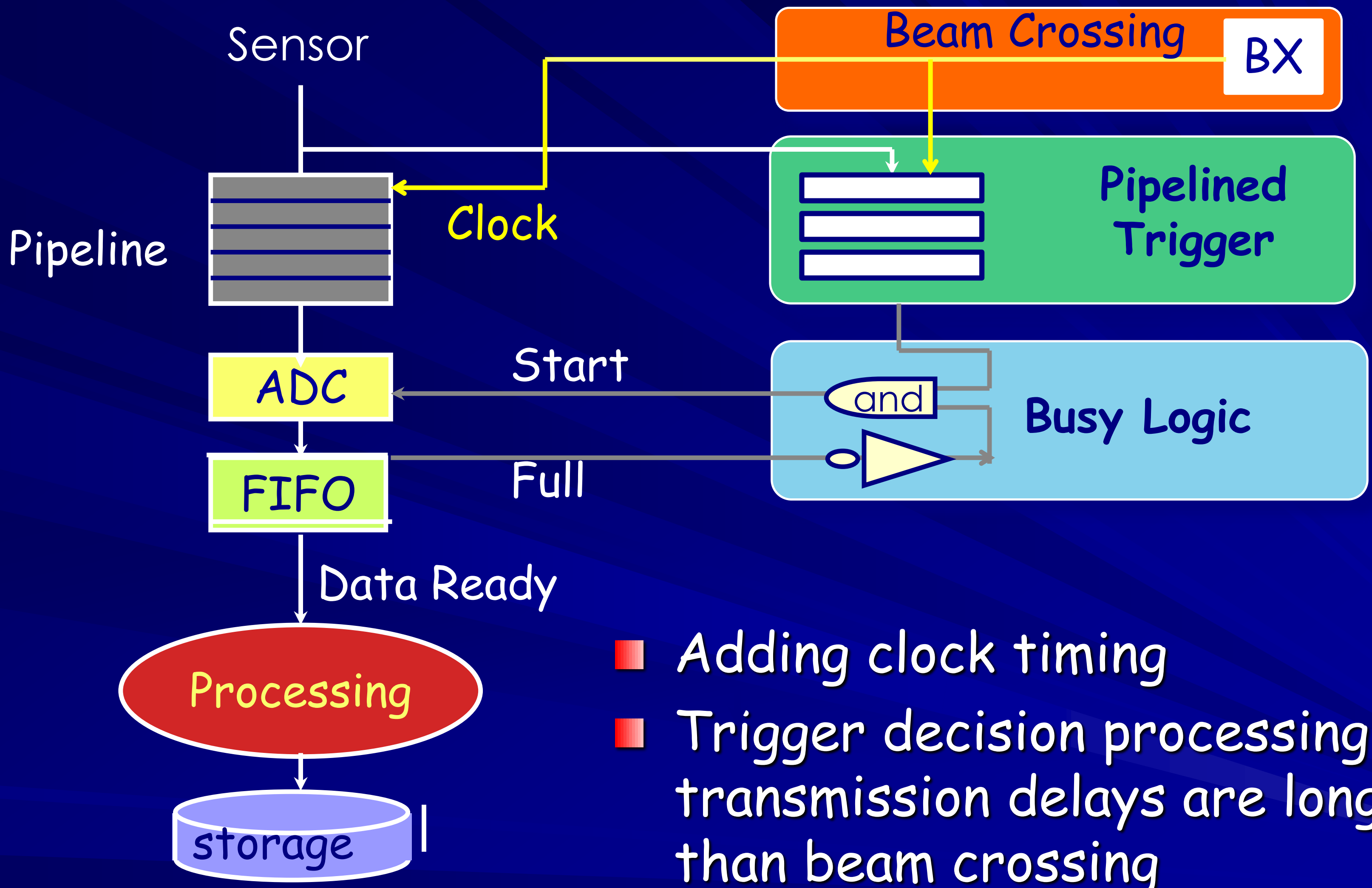
Deadtime (%) is the ratio between the time the DAQ is *busy* and the total time.

Trivial DAQ with a real trigger (3)



Buffers are introduced to de-randomize data, to decouple the data production from the data consumption.
---> **Better performance.**

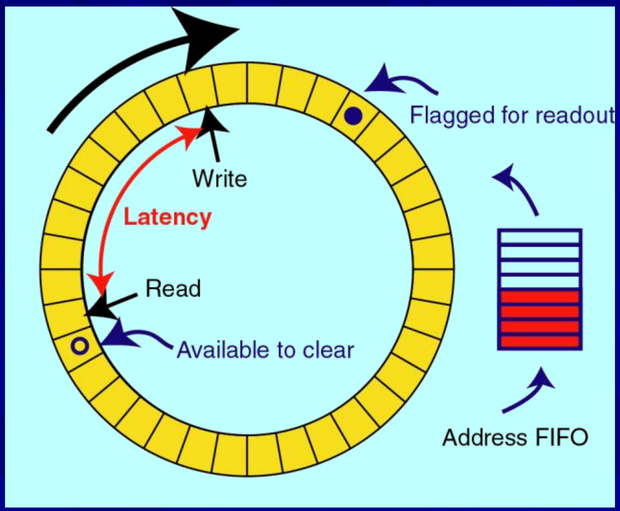
The final one



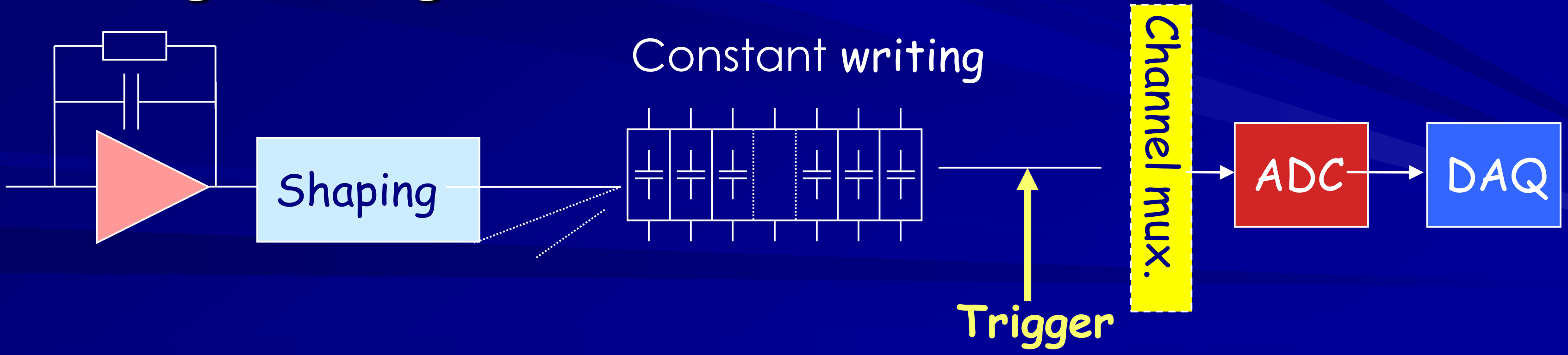
- Adding clock timing
- Trigger decision processing + transmission delays are longer than beam crossing

Terminology :buffer , pipeline & latency

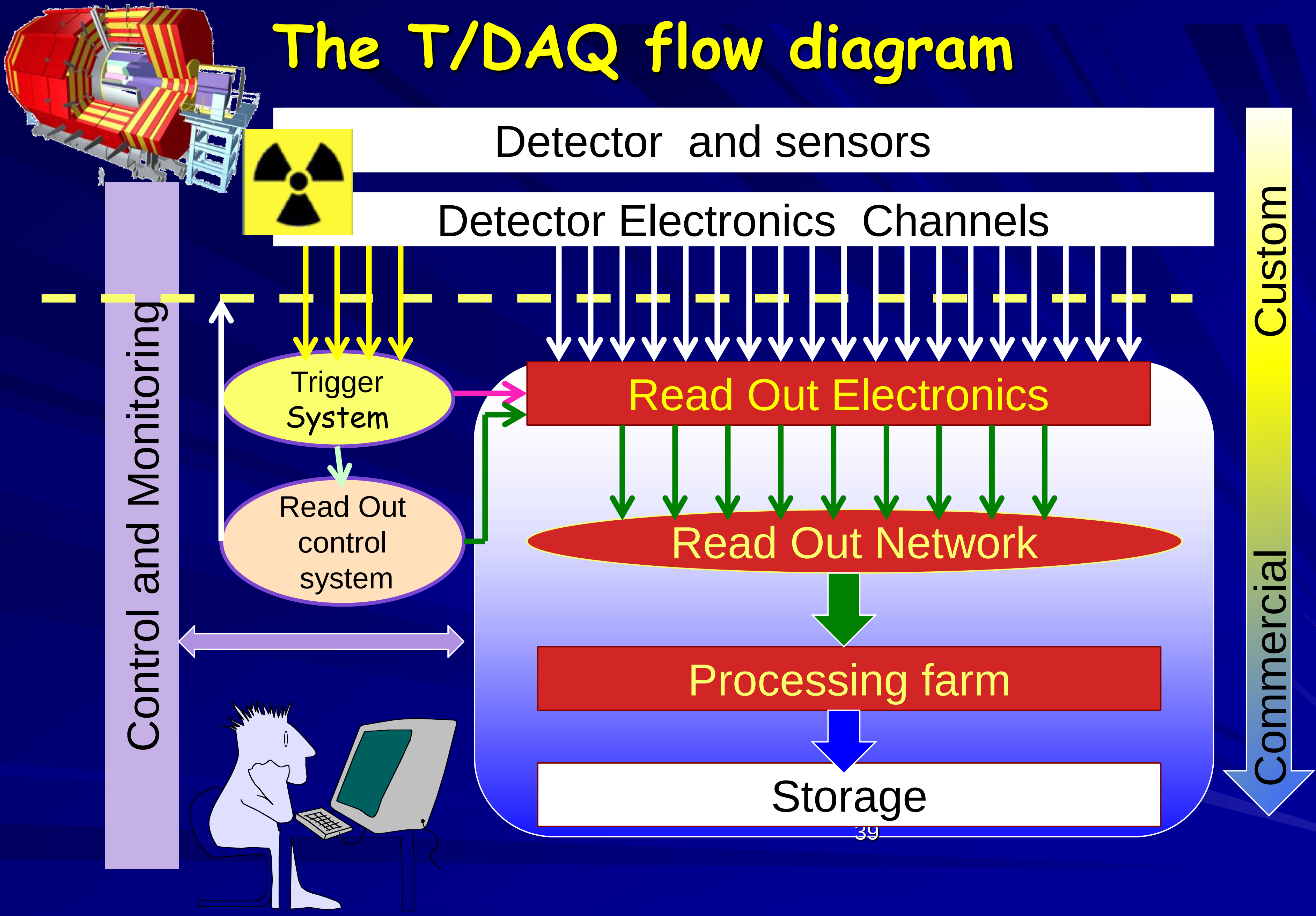
- Trigger processing requires some data transmission and processing time to make decision so front-ends must buffer data during this time. This is called the trigger latency
- For constant high rate experiments a "pipeline" buffer is needed in all front-end detector channels: (analog or digital) (e.g. circular buffer →



Circular buffer



The T/DAQ flow diagram



Trigger - Summary

- Lots of custom electronic
- Massive use of parallel processing in FPGAs (and some ASICs)
- Part of the electronics in radiation area
- Processing time typically 1 – 4 μs (limited by expensive buffer (?) memory on the detector)
- Common system for reliable transmission of timing and trigger decisions (TTC) → in the future (partially) replaced by GBT

DAQ (Read Out) summary

- Scalability
  - change in event-size, luminosity (pileup!)
- Robust
  - (very little dead-time, high efficiency, non-expert operators) → intelligent control-systems
- Use industry-standard,
  - commercial technologies (long-term maintenance) → PCs, Ethernet
- Low cost ☺ → PCs, standard LANs
- High band-width (many Gigabytes/s) → use local area networks (LAN)
- "Creative" & "Flexible" (open for new things) → use software and reconfigurable logic (FPGAs)

Now a bit of History

45 years of (r) evolution
My life!

History

SPS-NA3 — Fixed target

1975 – 1980

LEP OPAL — Collider e+ e-

1980 - 1990

Tevatron DO/CDF(SSC) — Collider P-Pbar

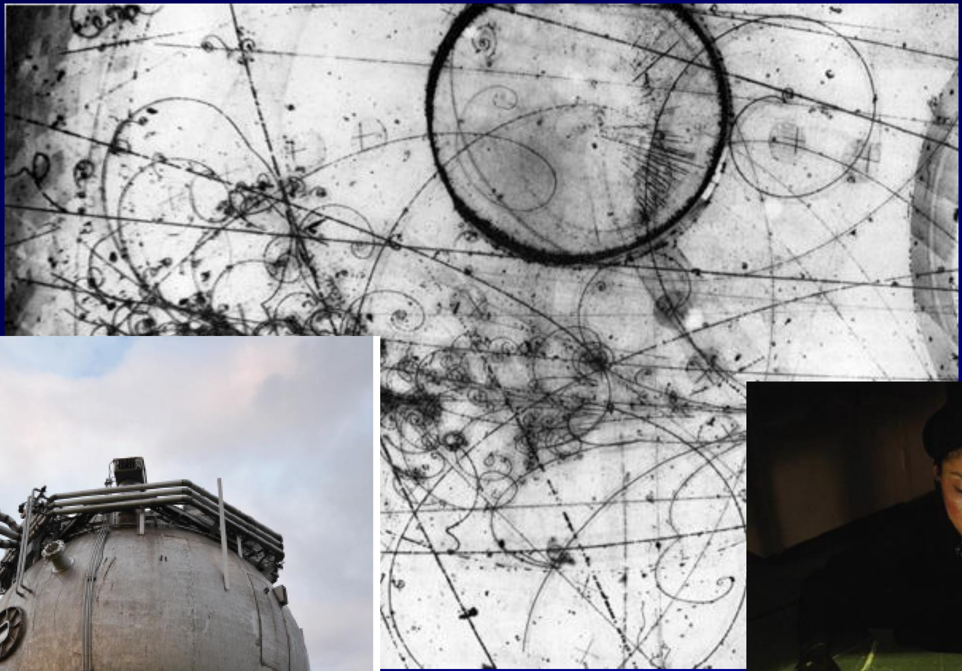
1985 - 2005

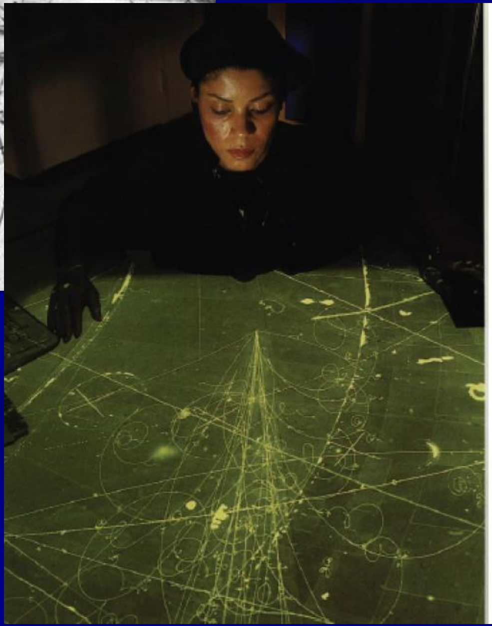
LHC-1 — 1990 – 2010

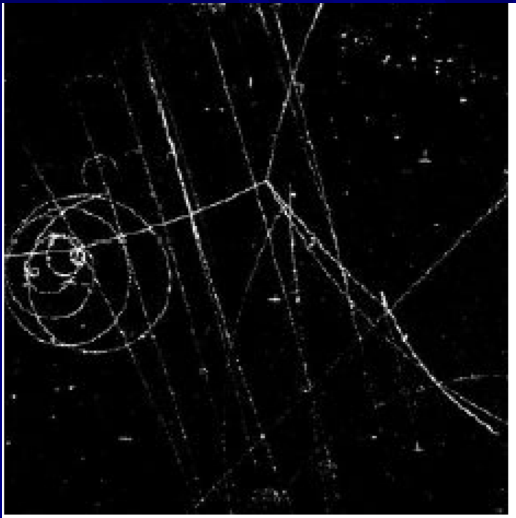
Tomorrow → LHC2-PANDA@ FAIR-Belle2 — 2016

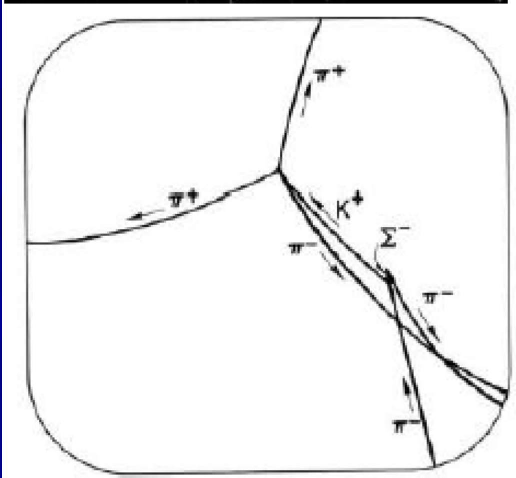
2230? — ILC ?

The prehistoric world
the Bubble Chamber -1955-1975

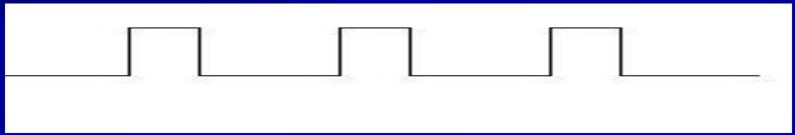


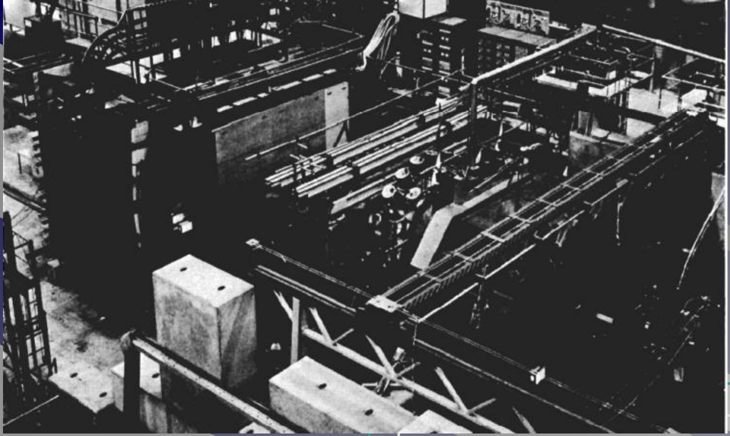






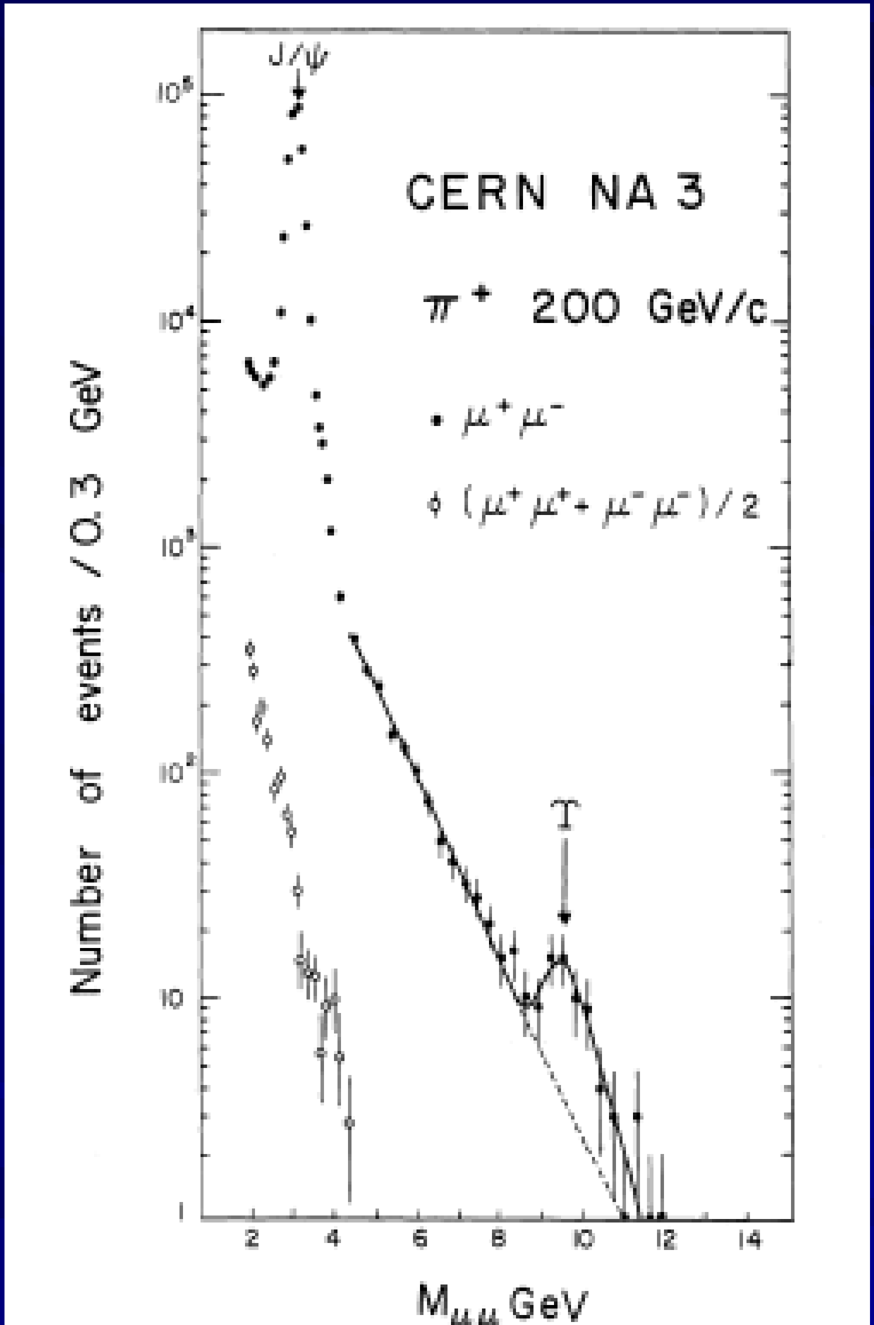
- Our Roots back to 'triggerless DAQ '



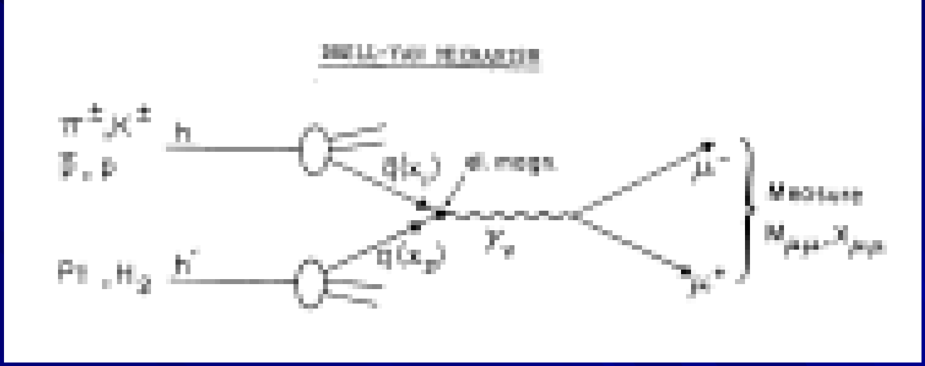


A fixe target experiment NA3

The 70's @ CERN SPS



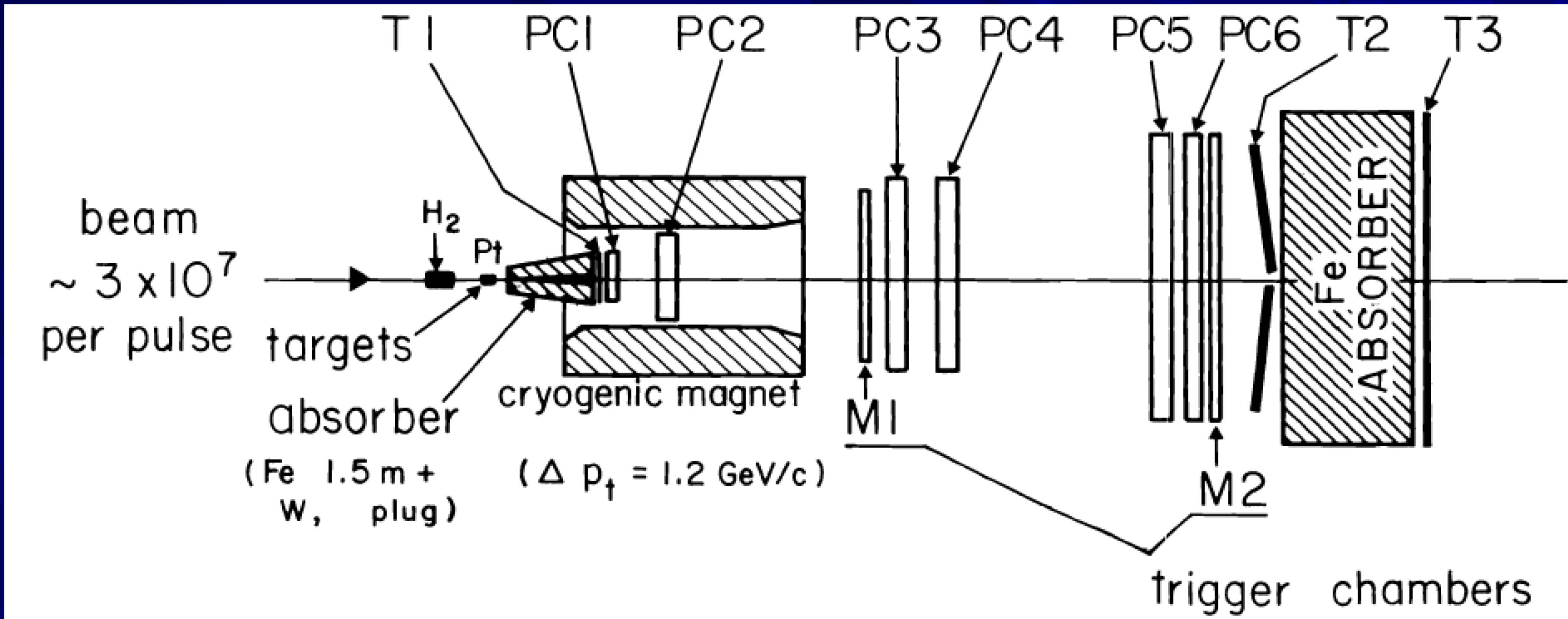
NA3 Physics



- Harwired processor

For real time calculation of dimuon mass and separate stream of data

NA3 Set Up

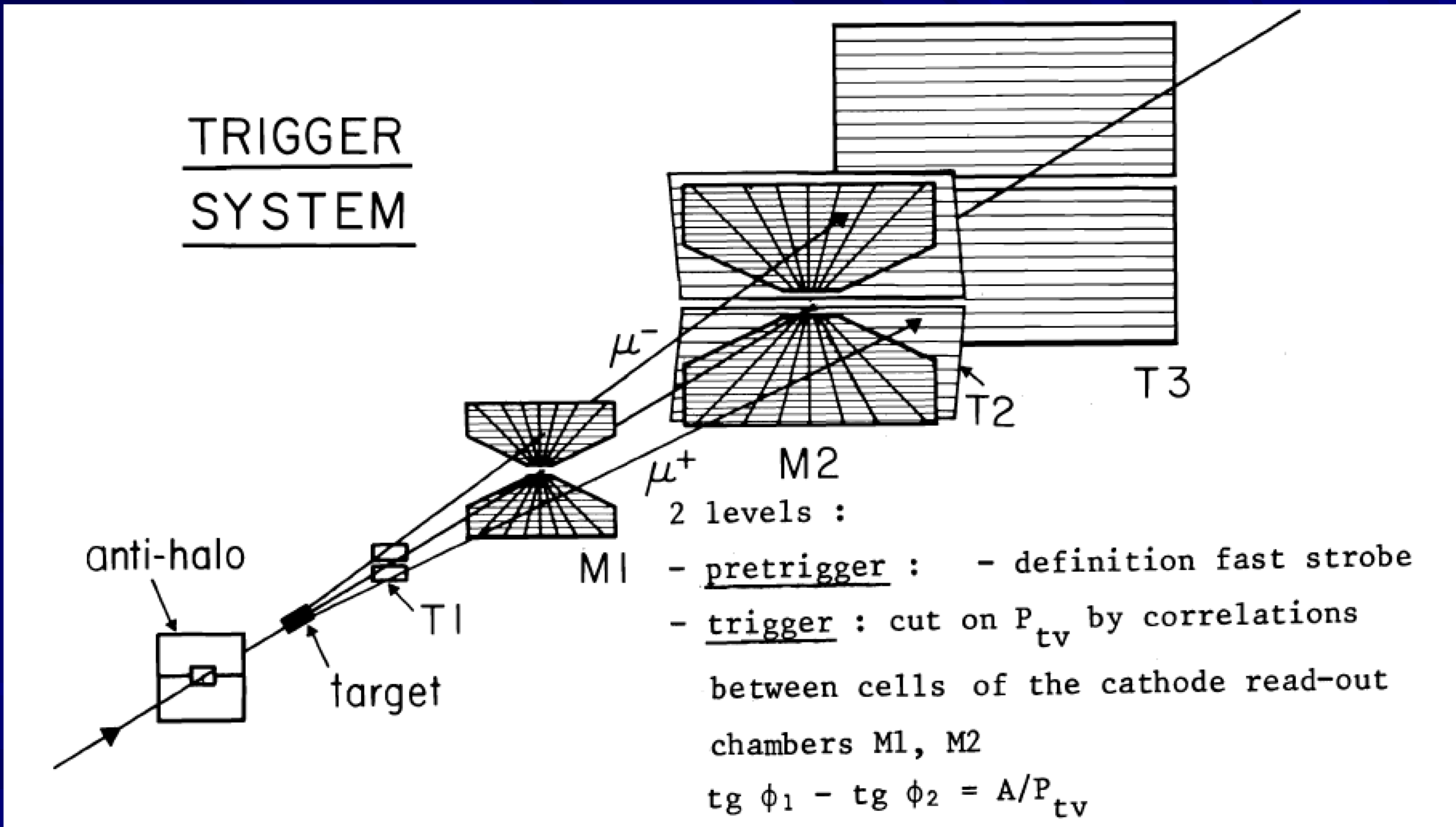


6 MWPC^s (31 planes , ~ 26 k wires)

T1, T2, T3 trigger hodoscopes

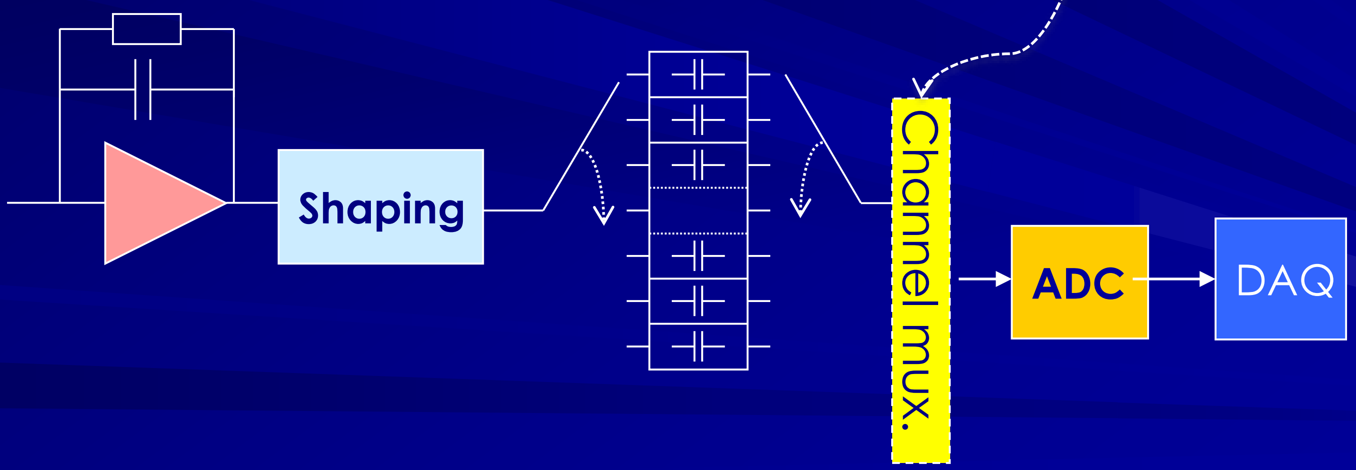
|——— 10 m ———|

NA3 Trigger

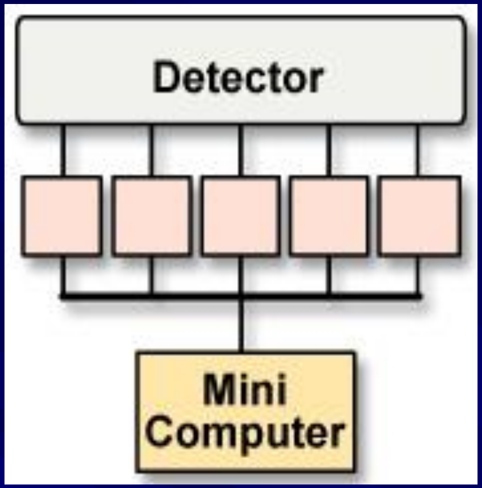

TRIGGER
SYSTEM
anti-halo
target
T1
M1
μ^-
μ^+
M2
T2
T3
2 levels :
- pretrigger : - definition fast strobe
- trigger : cut on P_{tv} by correlations
between cells of the cathode read-out
chambers M1, M2
$tg\ \phi_1 - tg\ \phi_2 = A/P_{tv}$

Electronics Multiple event buffers

- Good for experiments with short spills and large spacing between spills (e.g. fixed target experiment like SPS @ CERN) → 2 sec spill and 7 sec interburst
- Fill up event buffers during spill (high rate)
- Readout between spills (low rate)
- ADC can possibly be shared across channels (MUX)
- Buffering can also be done digitally (in RAM)



Evolution of DAQ technologies and architectures (1)
"The old time of Minicomputer"



1970-80

CERN PS/SPS

Minicomputers

Detector Readout

Event building

On-line processing

Off-line data store

- Trigger:
  - NIM logic (50 Ohms cable)
  - Hardwired custom design
  - No pipelines
  - Similar to today LVL1's
  - Large deadtime possible during read Out
- DAQ :First standard : CAMAC
  - The LeCroy time (ADC,TDC,PU)
- Rate kByte/s
- **Minicomputers (16 bits)**
  - **HP, Digital PDP 11-45, IBM 3070**

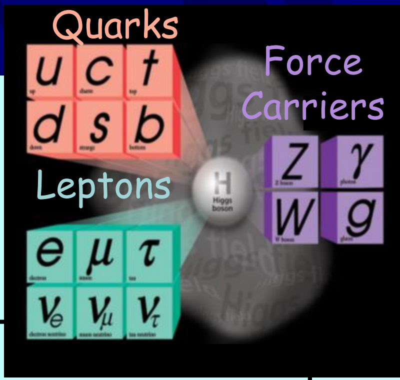
A lot of dead time & bad connections

From S. Cittolin

80's
The LEP-OPAL

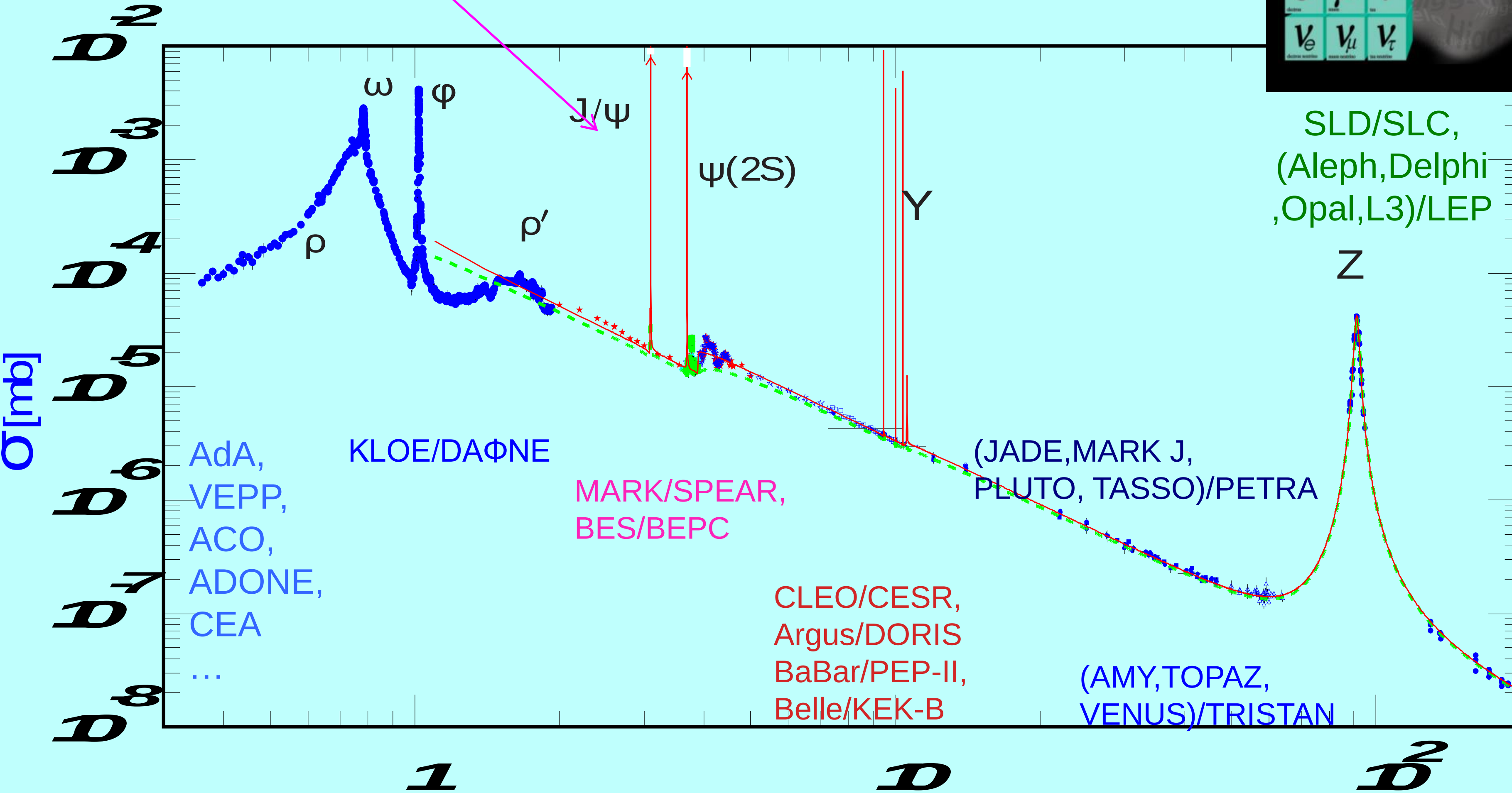
The transition world

Some past machines



"unauthorized particle on an unauthorized machine"

σ and R in e⁺ e⁻ Collisions



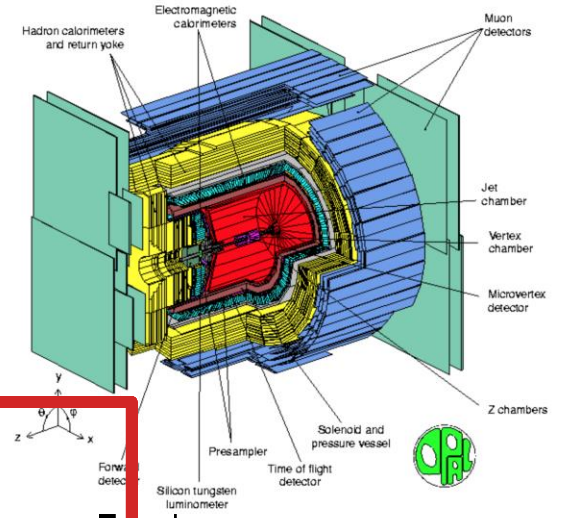
ep (H1, ZEUS, HERMES, HERA-B) /HERA
pp-bar (UA1, UA2)/SppS, (CDF,D0)/Tevatron
pp (Atlas, CMS, ALICE, LHCb)/LHC

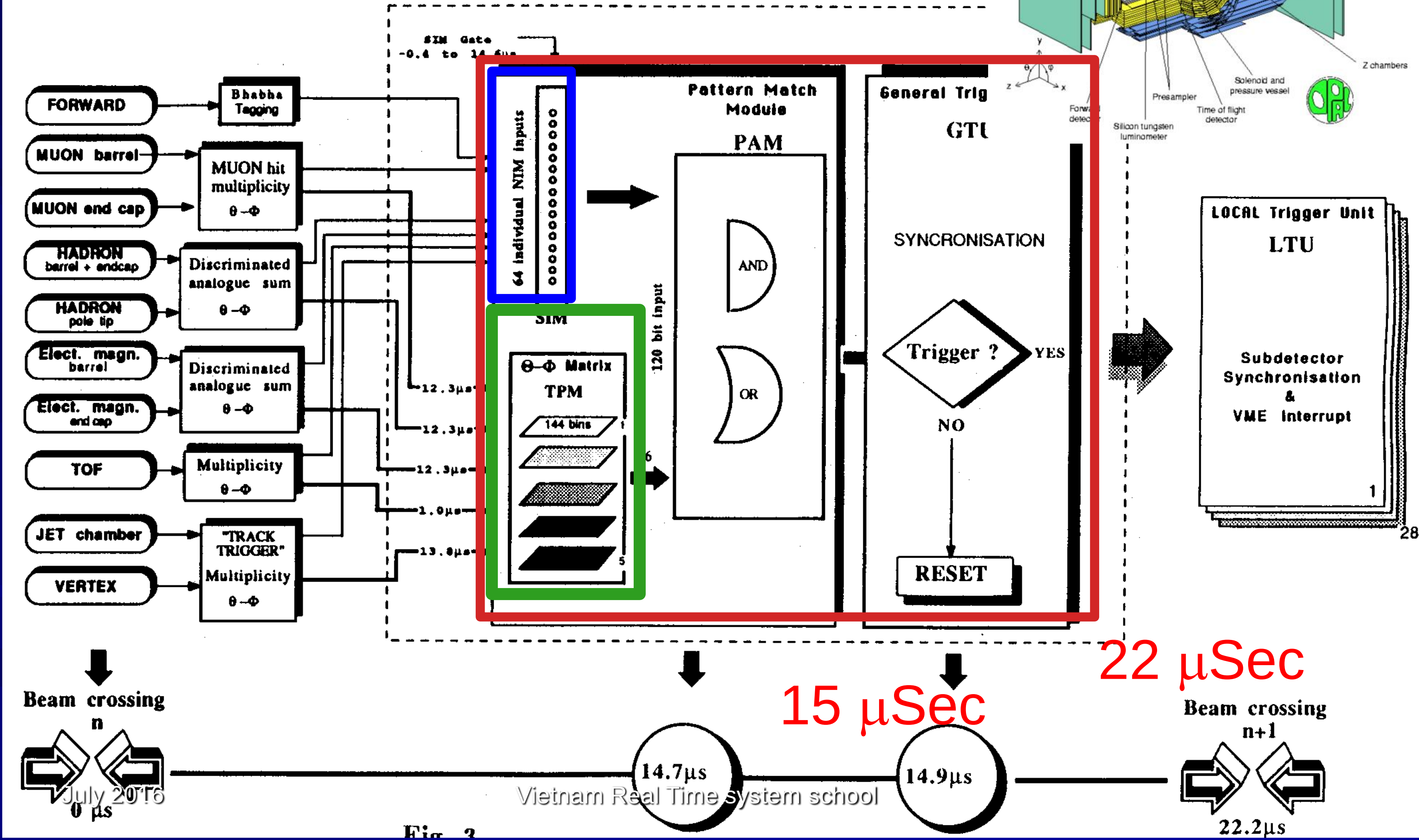
Trigger challenges at high lumi:
e+e-, ep → beam background
pp-bar, pp→ pile up

Requirements for e+e- Triggering

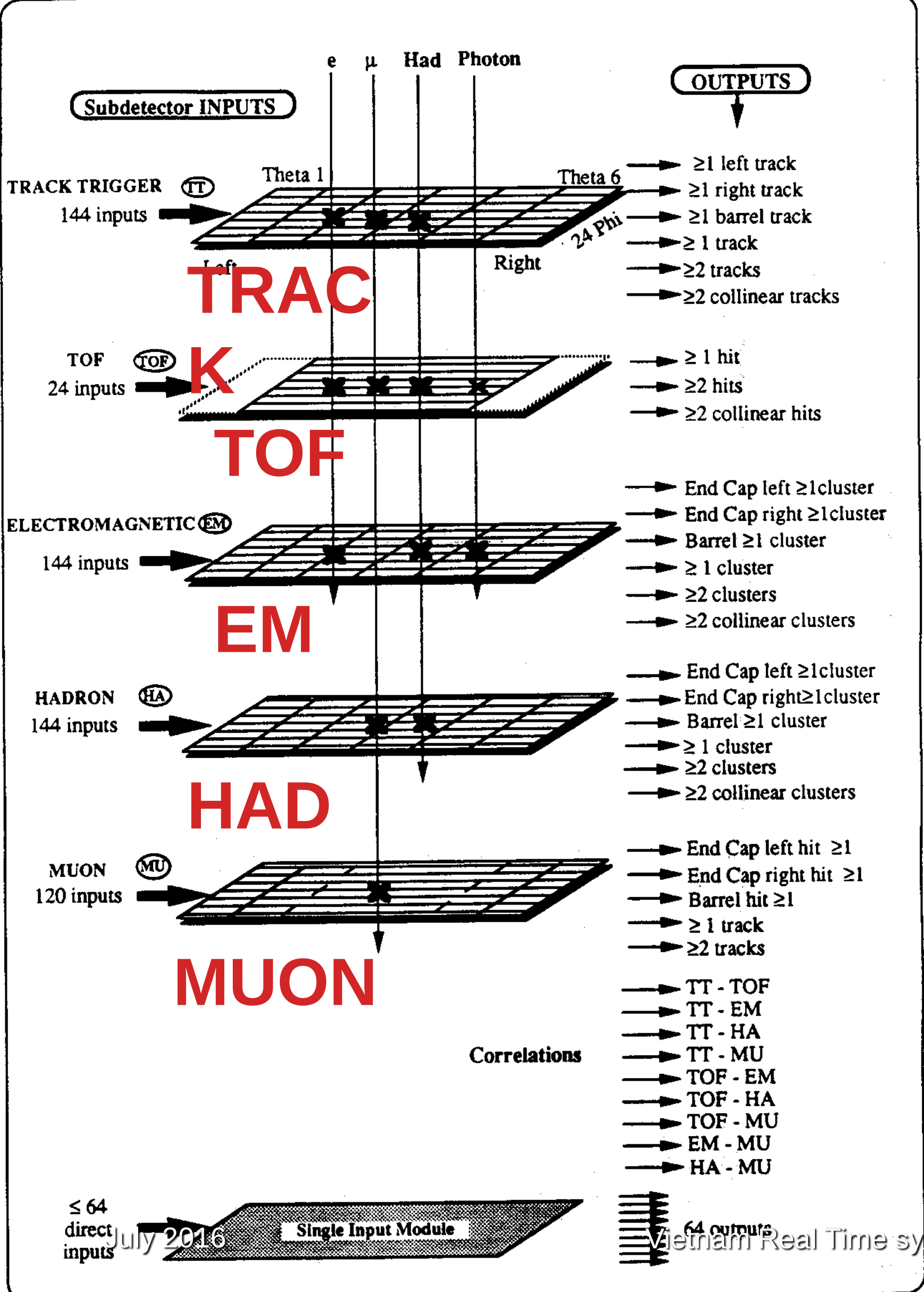
- Accept: (almost) all real collisions
- Reject:
  - very low angle e+e-
  - Beam-gas/wall events - tracks not from beam spot in r or z
- Trigger on simple event topology
  - Time-Of-Flight coincidence
  - Multiplicity of good tracks (from beam spot) – low pt cuts (100s of MeV/c)
  - Calorimeter activity: global energy and clustered energy in relative coarse spatial bins
  - Simple combinations
- Time stamping
  - Beam Xing « detector response times (few nsec vs 100-1000ns)

Simple:The LEP-OPAL TRIGGER





The OPAL Trigger

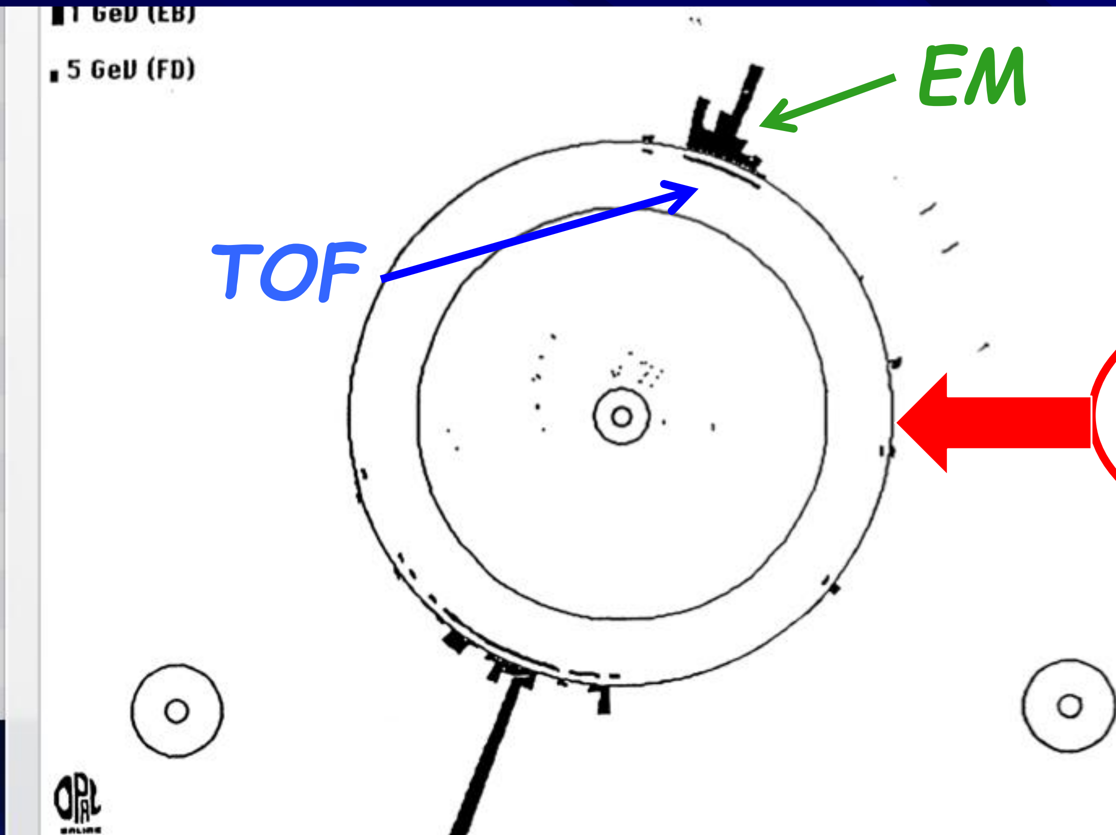


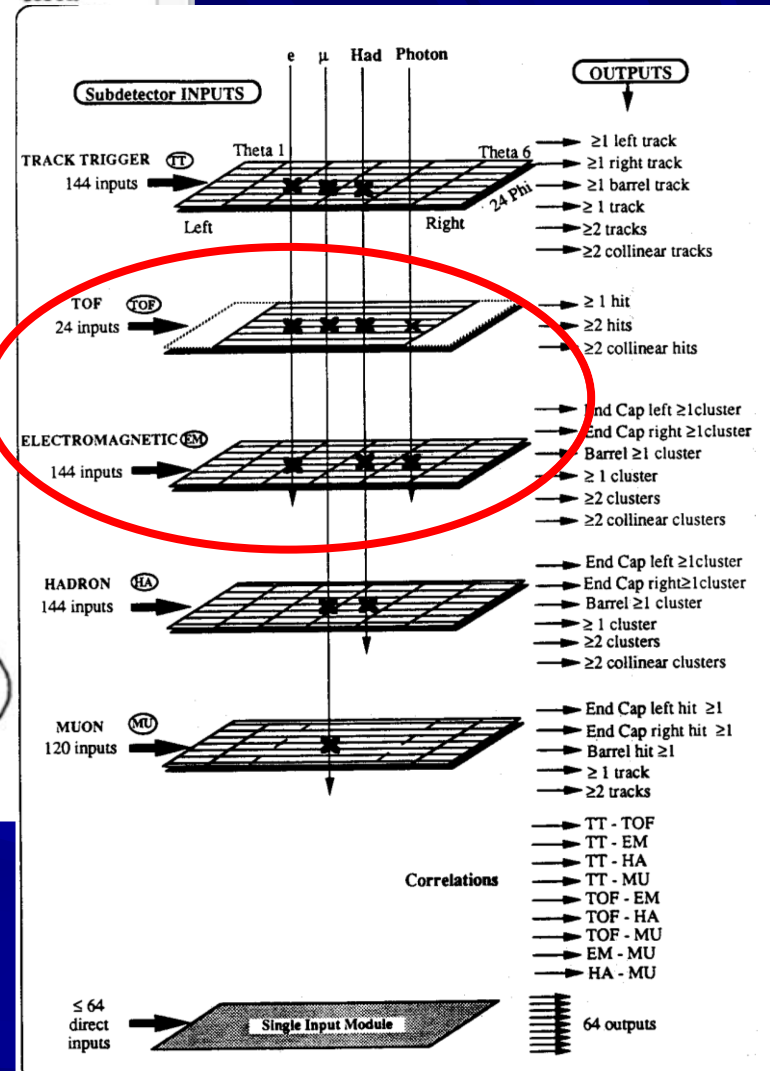
- Matrix
  - 24 Phi
  - 6 Eta
  - Total =144 trigger cells

64 'Phi' single input signals

80% of Trigger

The LEP Z0 first event

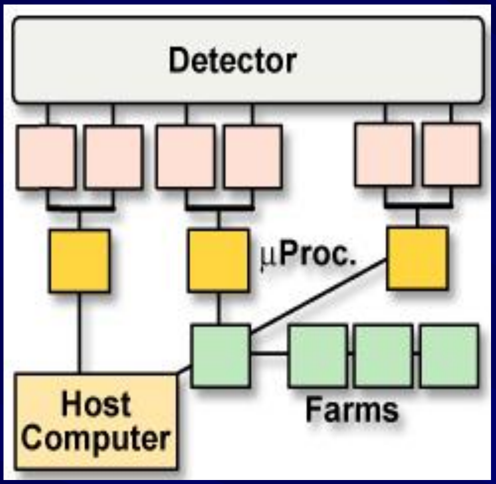




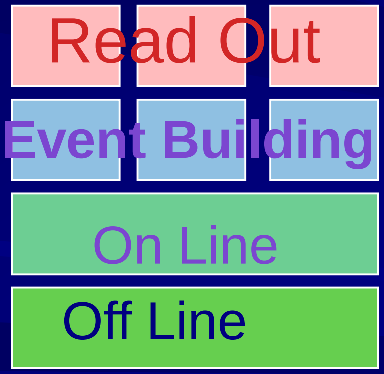
The First Z^0 → e+e- at LEP
OPAL-13 August 1989

TOF + EM Lead glass Calorimeter

Evolution of DAQ technologies and architectures (LEP) The birtday of microprocessors



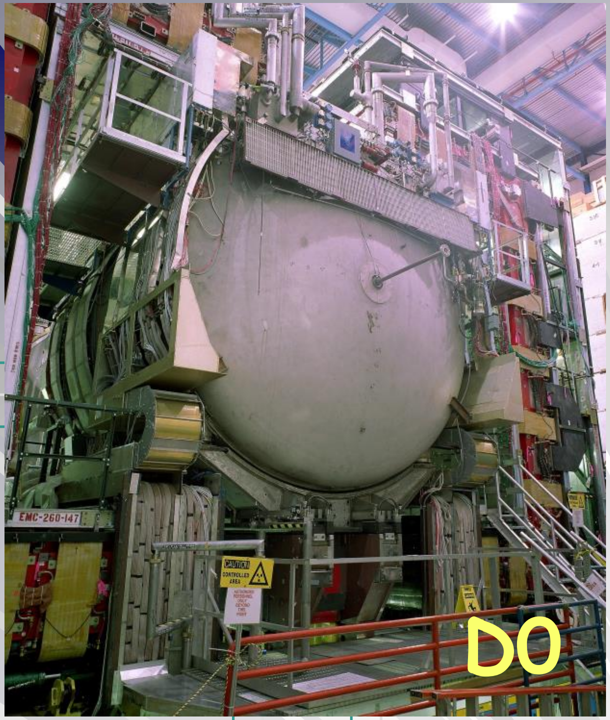
1980-90
LEP
Microprocessors

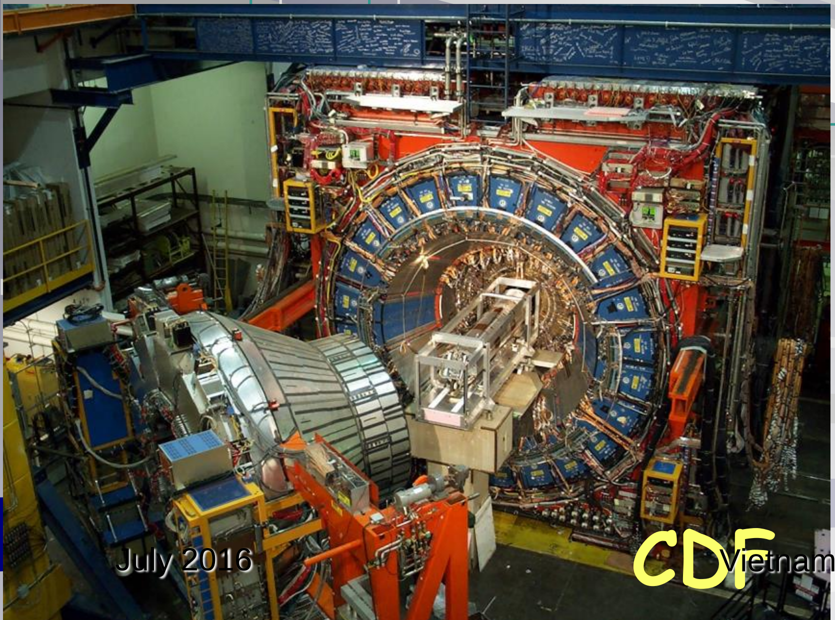


- Custom hardware triggers
- HEP Standard → FASTBUS
- Embedded CPU
  - Motorola 6800 → 68000
  - 58 to 512 KB RAM Memory
- Industry Standard (VME)
- Rate → Mbytes/sec
- On line selection → Filter
  - Emulators 3081,370E,Transputers, farms (ACP)

From S. Cittolin

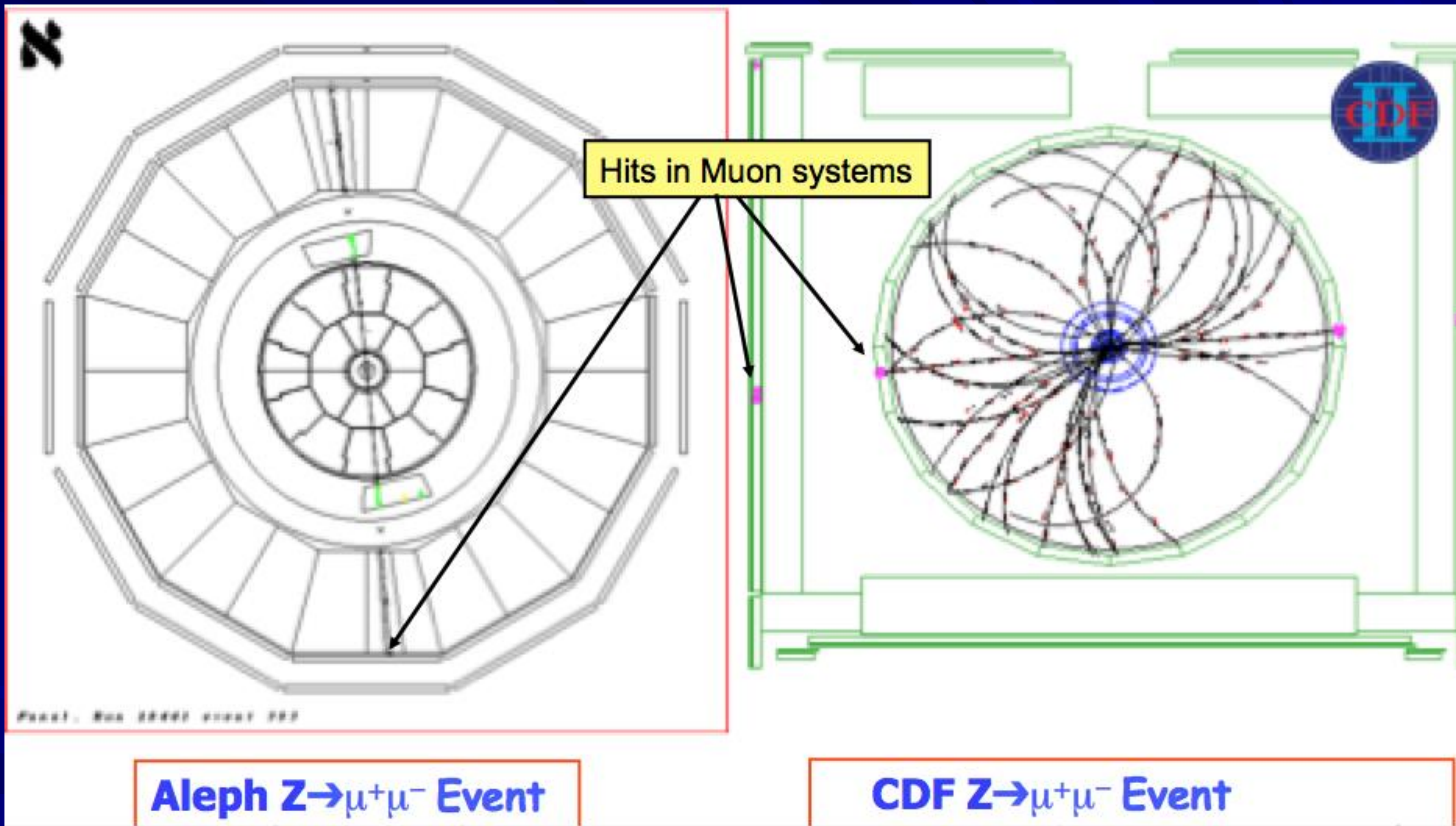
Tevatron



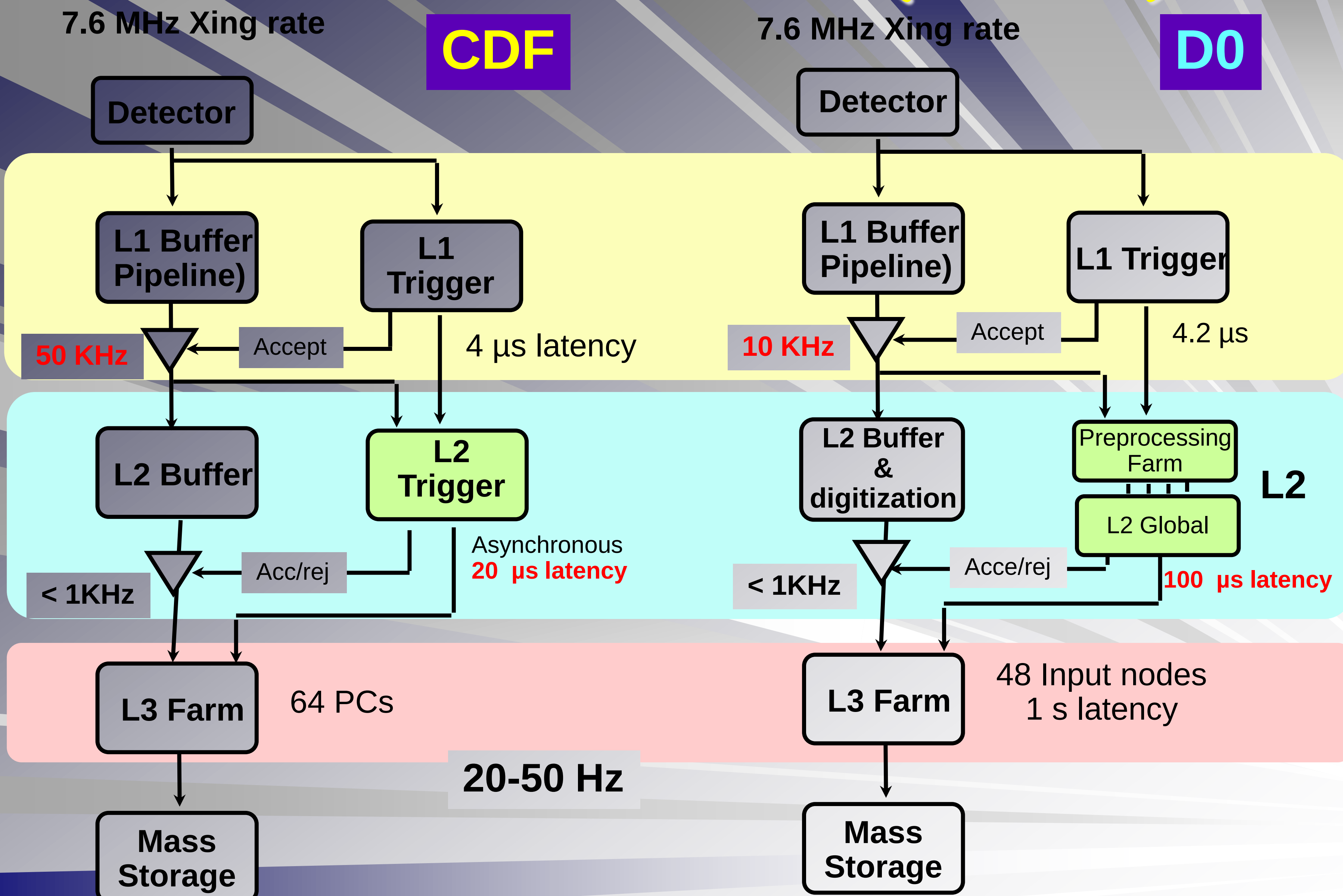


the beginning of modern time

e+e+ vs pp environment



Tevatron architectures (RUN 2)



Multilevels trigger and DAQ

- Required rejection is orders of magnitude

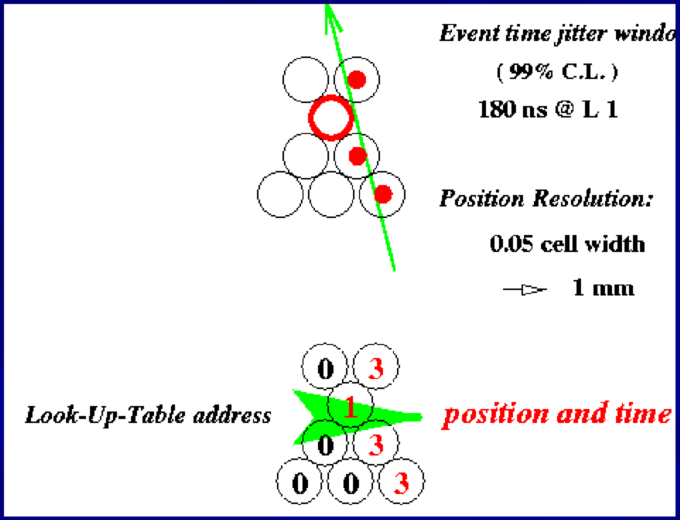
- **Level 1 is hardware based**
  - –Hardwired trigger system to make trigger decision with short latency.
  - –Constant latency buffers in the front-ends
  - –Crude signatures (hits and tracks, local energy deposit over threshold…)
  - –Operates on reduced or coarse detector data
- **Level 2 is a composite**
  - –Dedicated custom/DSP/FPGA processing or Processor based (standard CPU's or FIFO buffers with each event getting accept/reject in sequential order
- **Level 3 is a farm** → General Purpose CPUs

hundreds – thousands

Almost every one uses this scheme.

LV1 examples

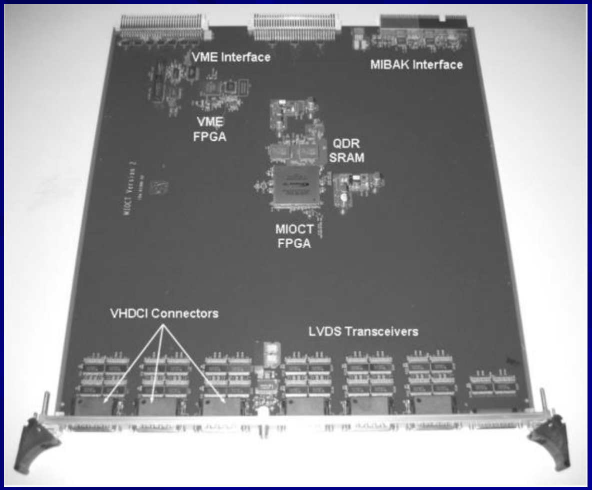
Track Segment Finder



- Large custom boards

Example of evolution

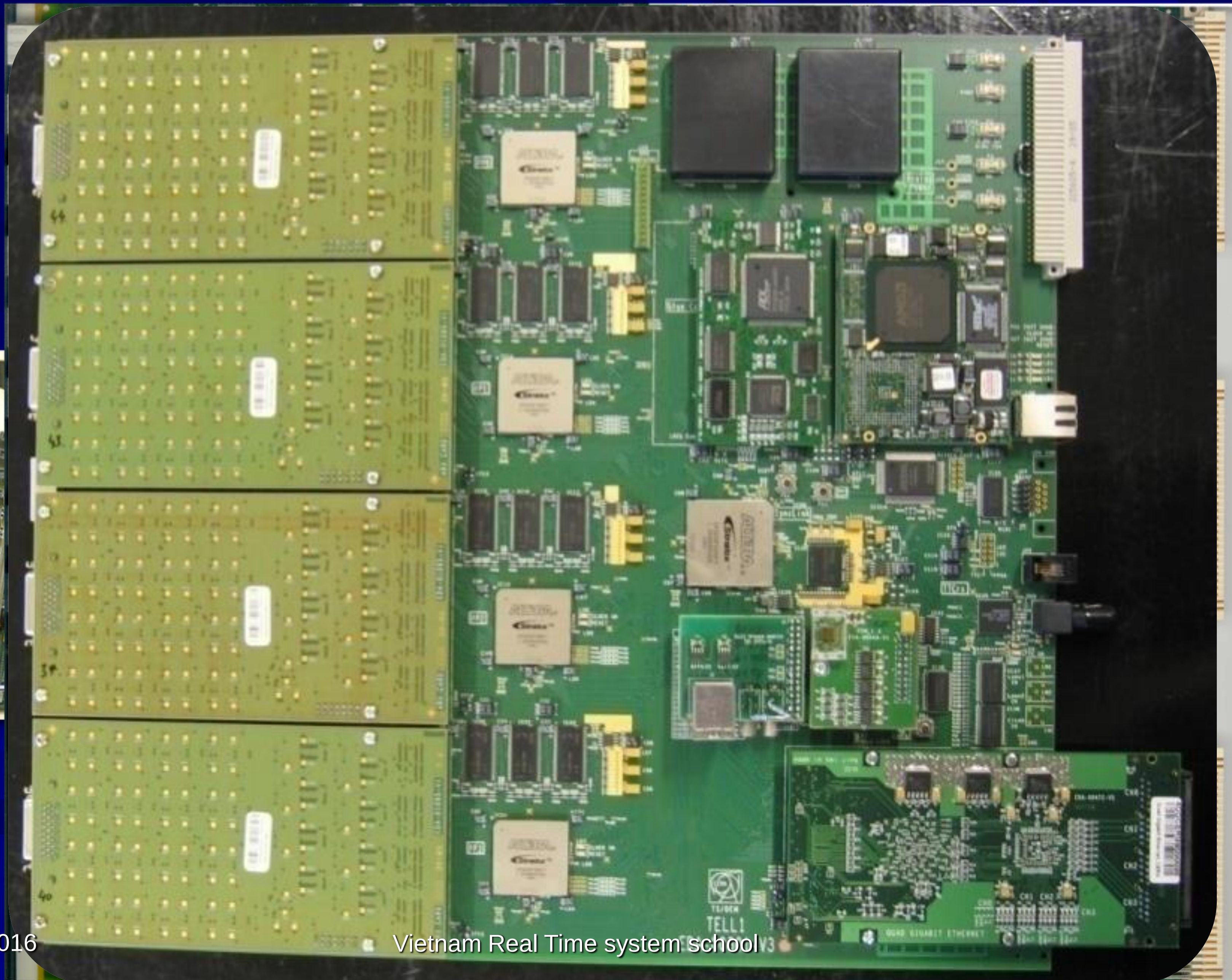
Demonstrator at
the end of the 90's



Final version
installed

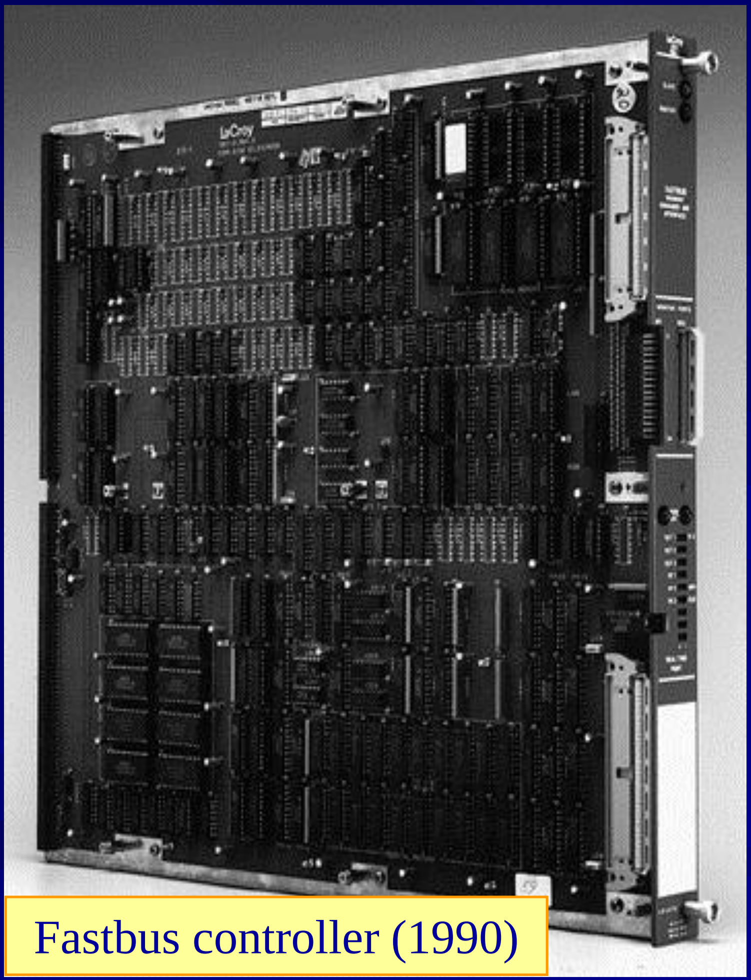
- Muon trigger board for ATLAS
  - Handles 13 input links, each of them receiving 32-bit every 25ns
  - ~17 Gb/s processed

Examples of modules

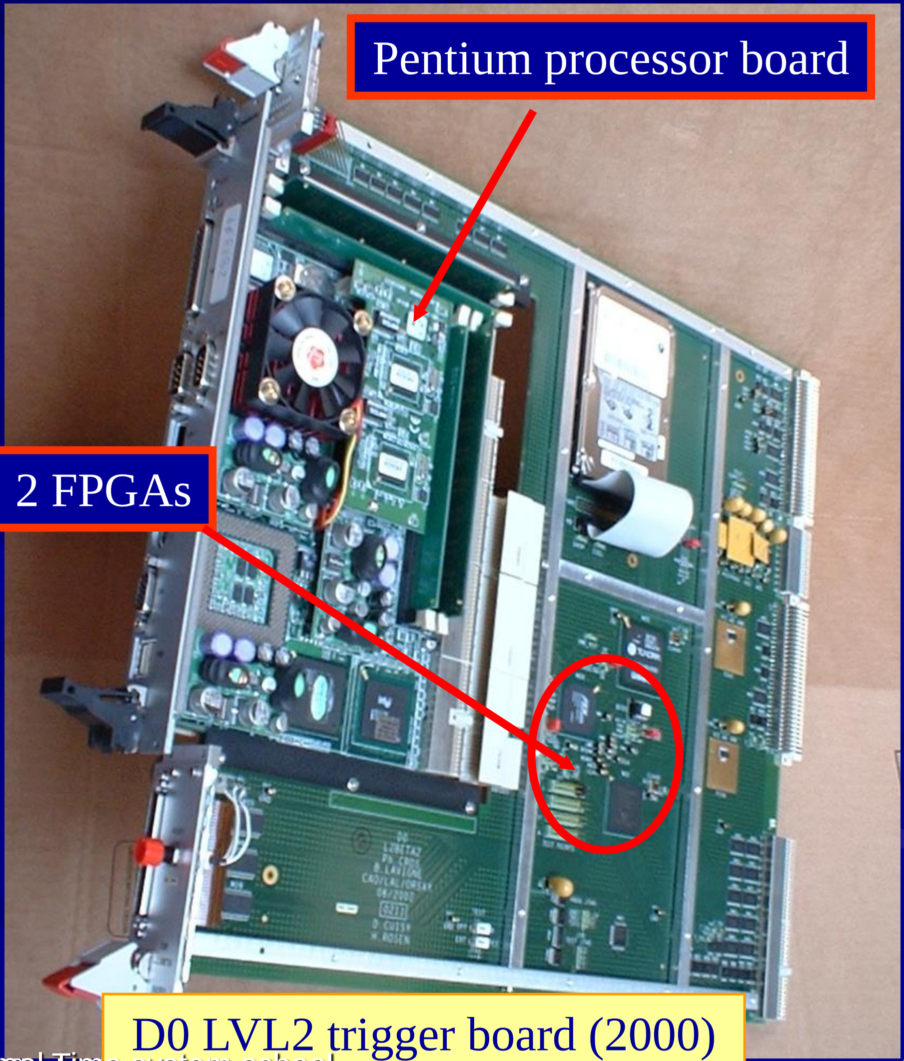


Evolution of digital electronics

- From arrays of circuits to FPGAs : programmable logic



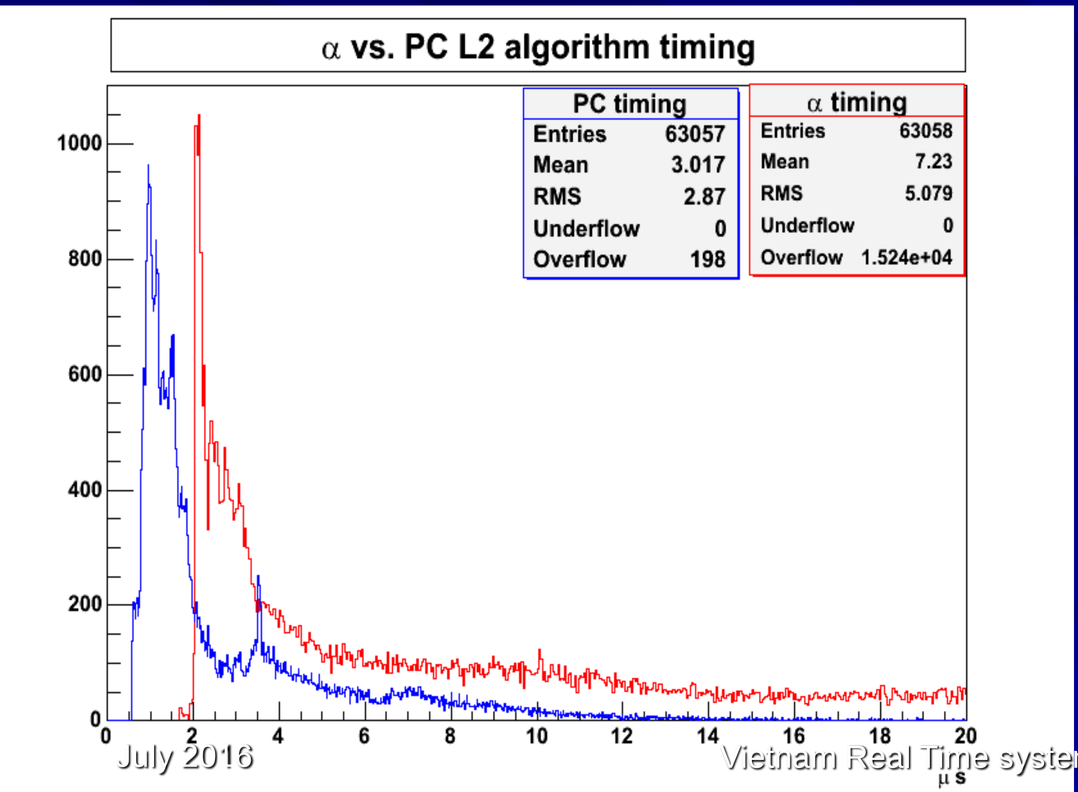
Fastbus controller (1990)

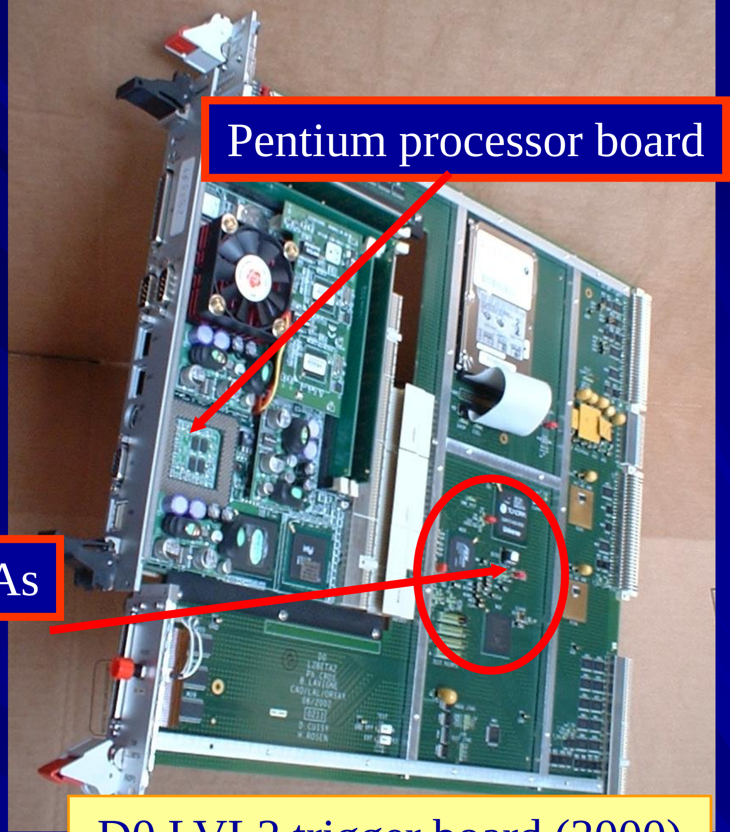


D0 LVL2 trigger board (2000)

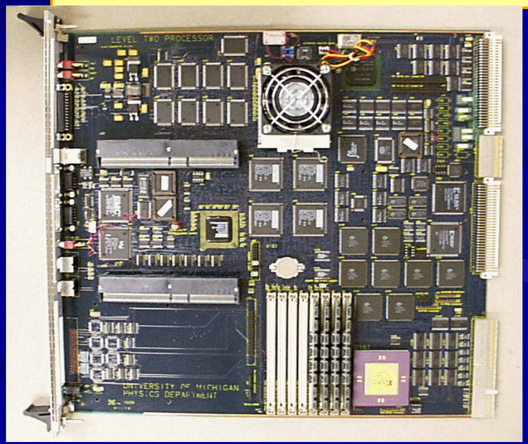
LVL2 examples

- Alpha = many years of efforts ….hardware and software
- PC (Commercial): few months to implement! No hardware !





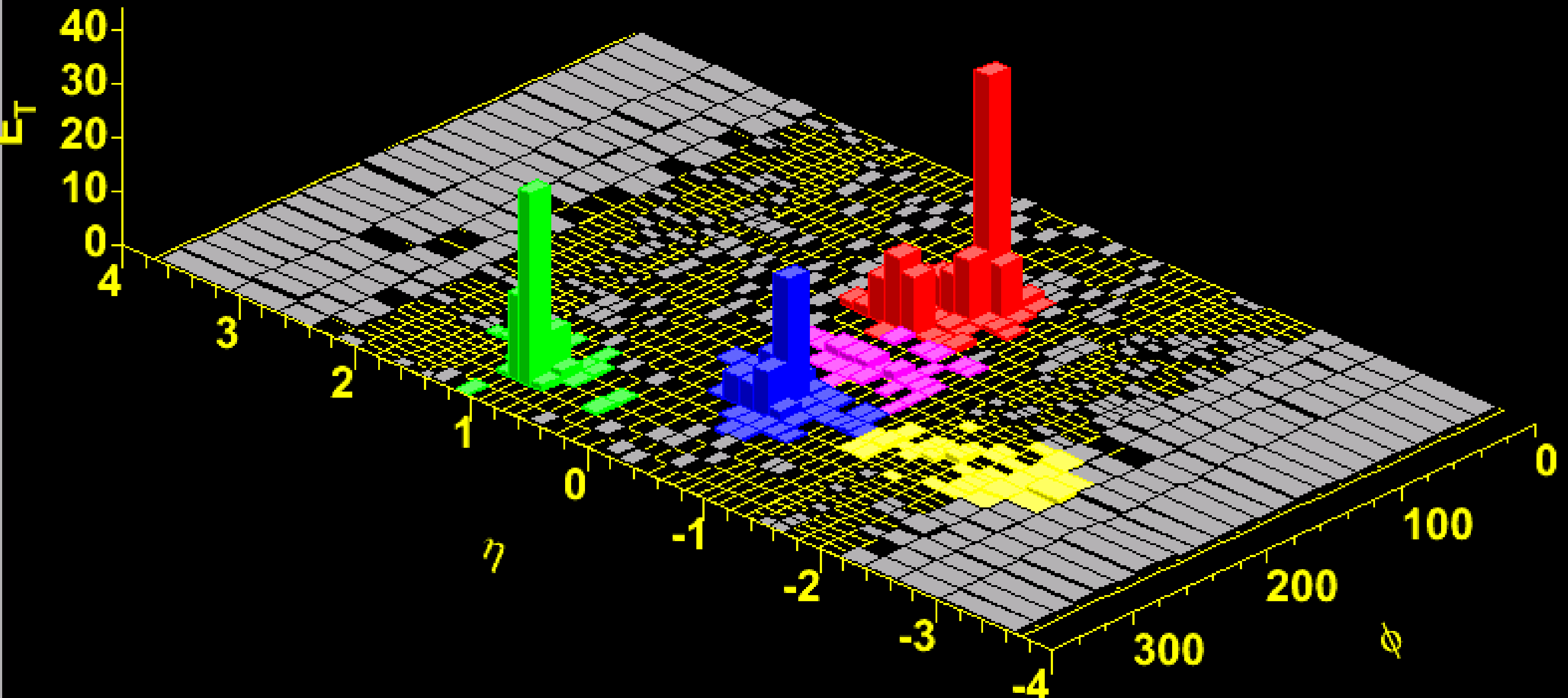
D0 LVL2 trigger board (2000)



Alpha Processor board

Event : 293170 Run : 198206 EventType : DATA | Unpresc: 0,1,5,8,9,10,11,12,13,16,51,53,23,55,24,56,25 Presc: 0,1,8,9,10,12,24,56,25

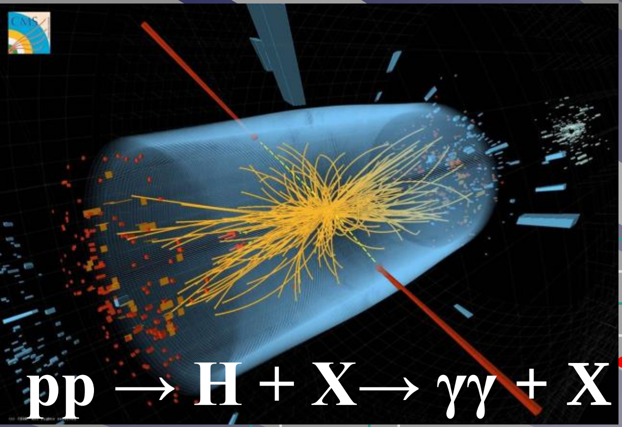
L2 Jet trigger in DO



Missing Et
IS NOT DEFINED!
Jet Collection:
JetCluModule

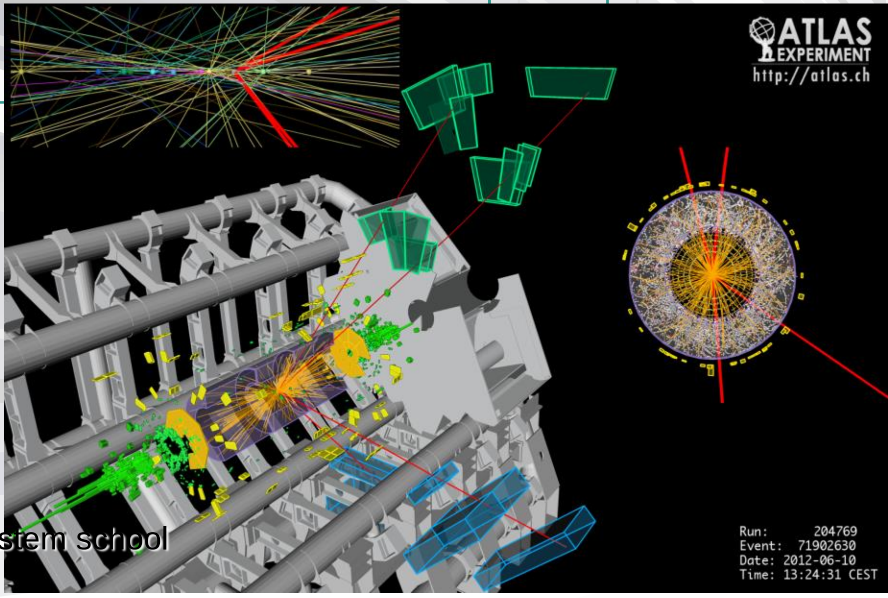
Jets(R = 0.7): first 5

Em/Tot	et	phi	eta
0.7	142.4	2.0	-0.4
0.2	70.0	5.5	0.9
0.5	64.3	4.4	-0.4
0.8	12.2	4.1	-2.0
0.6	11.0	3.3	-0.5

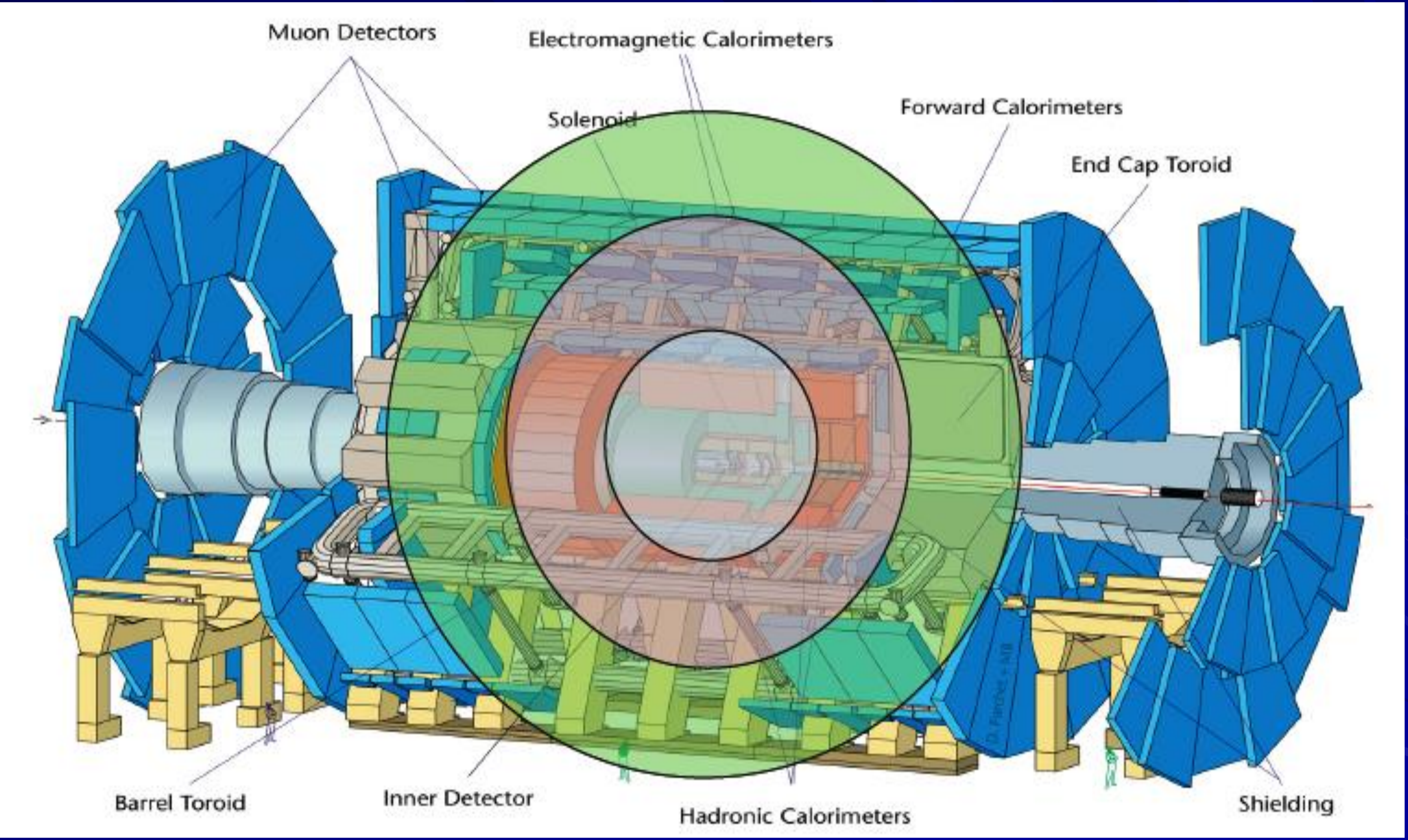


Trigger and Data Acquisition for LHC experiments

The Challenges



Challenges 1: Time of Flight

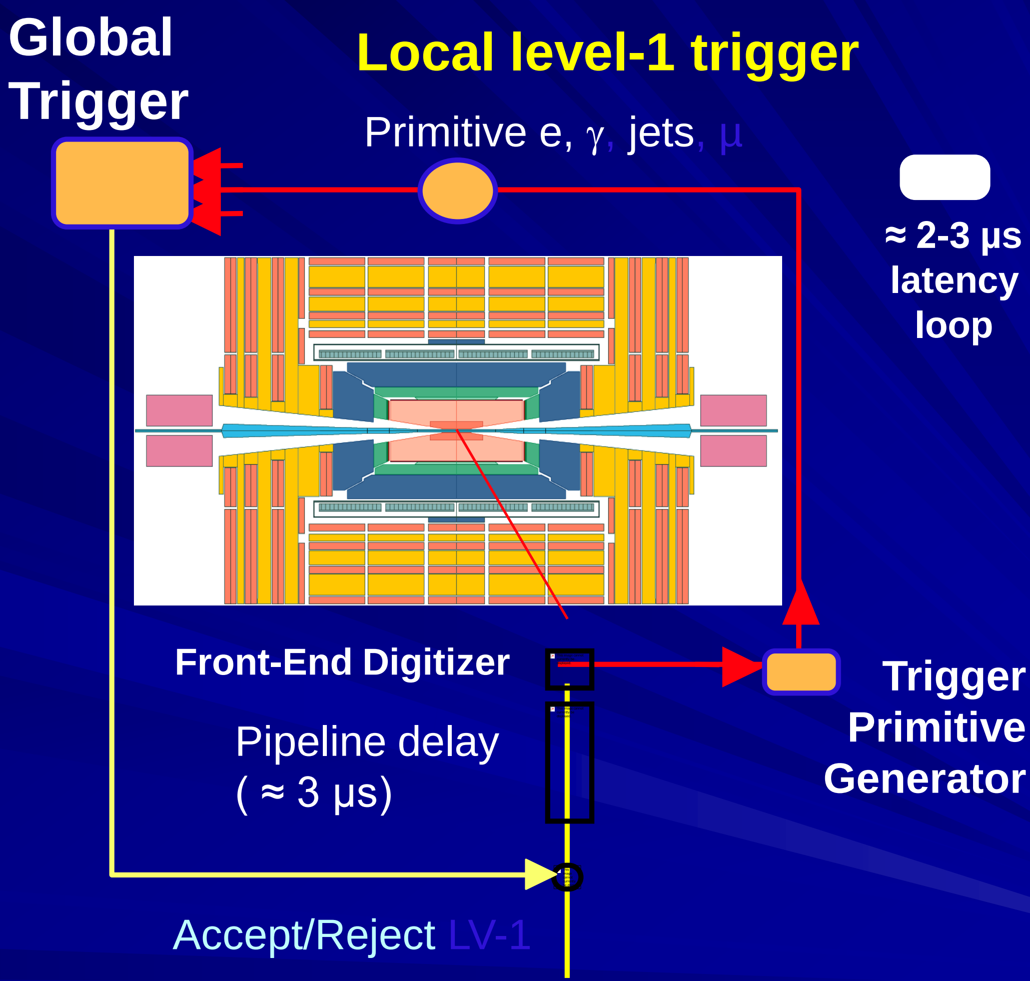


c = 30 cm/ns → in 25 ns, s = 7.5 m

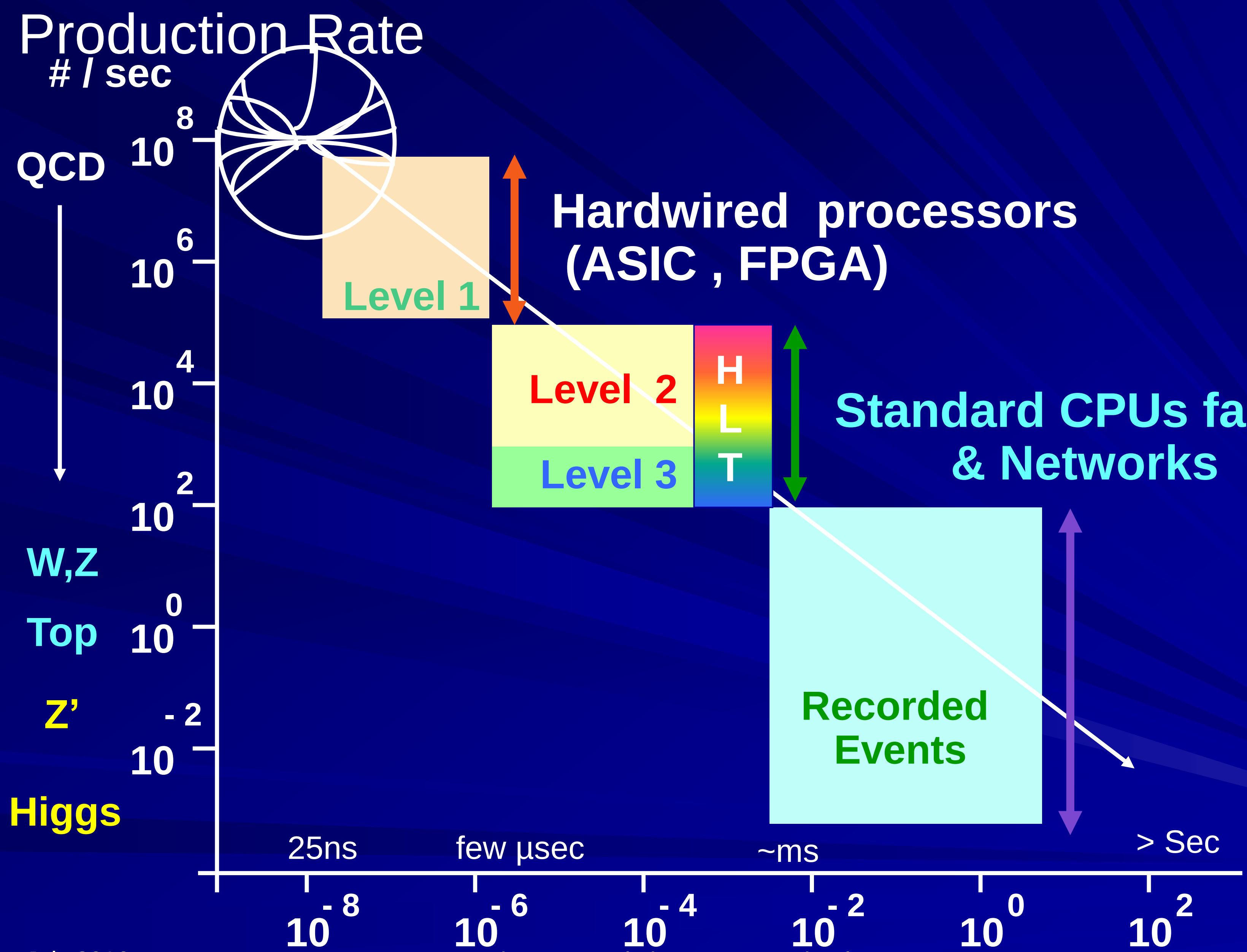
Distributing the L1 Trigger

- L1 decision has to be brought for each crossing to all the detector front-end electronics elements so that they can send of their data or discard it
- All experiments use common TTC system

L1 trigger latencies	
ALICE	No pipeline
ATLAS	2.5 us
CMS	3 us
LHCb	4 us

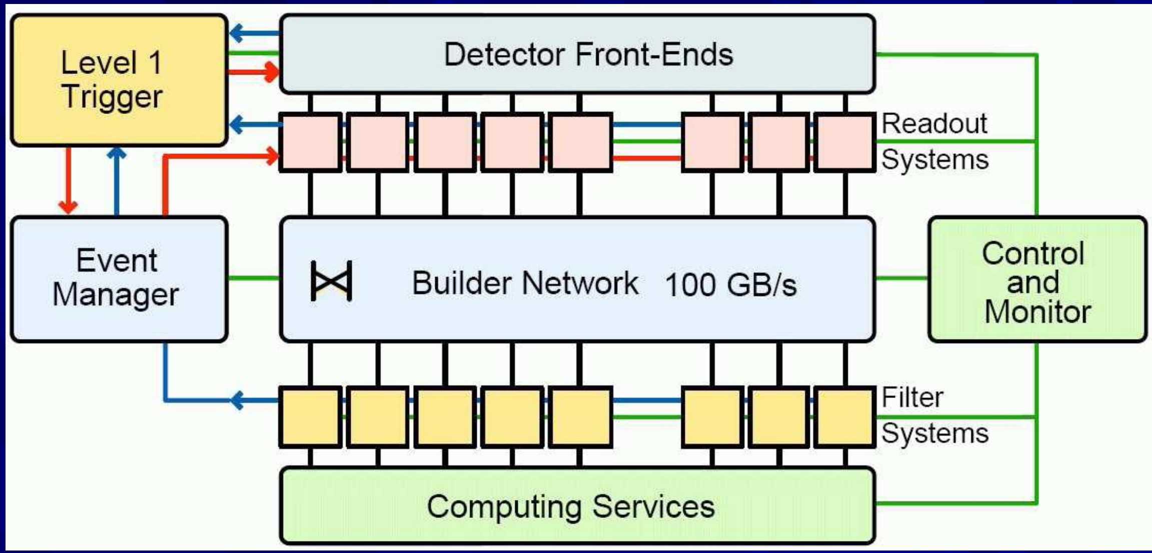


LHC Multilevels Selection scheme

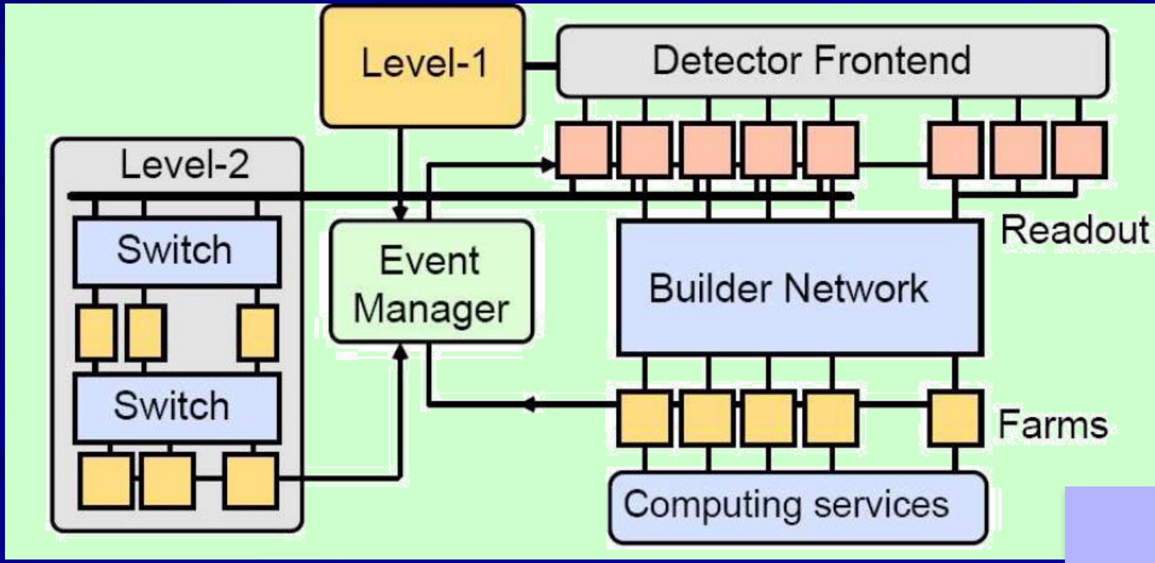


After L1 → Two philosophies

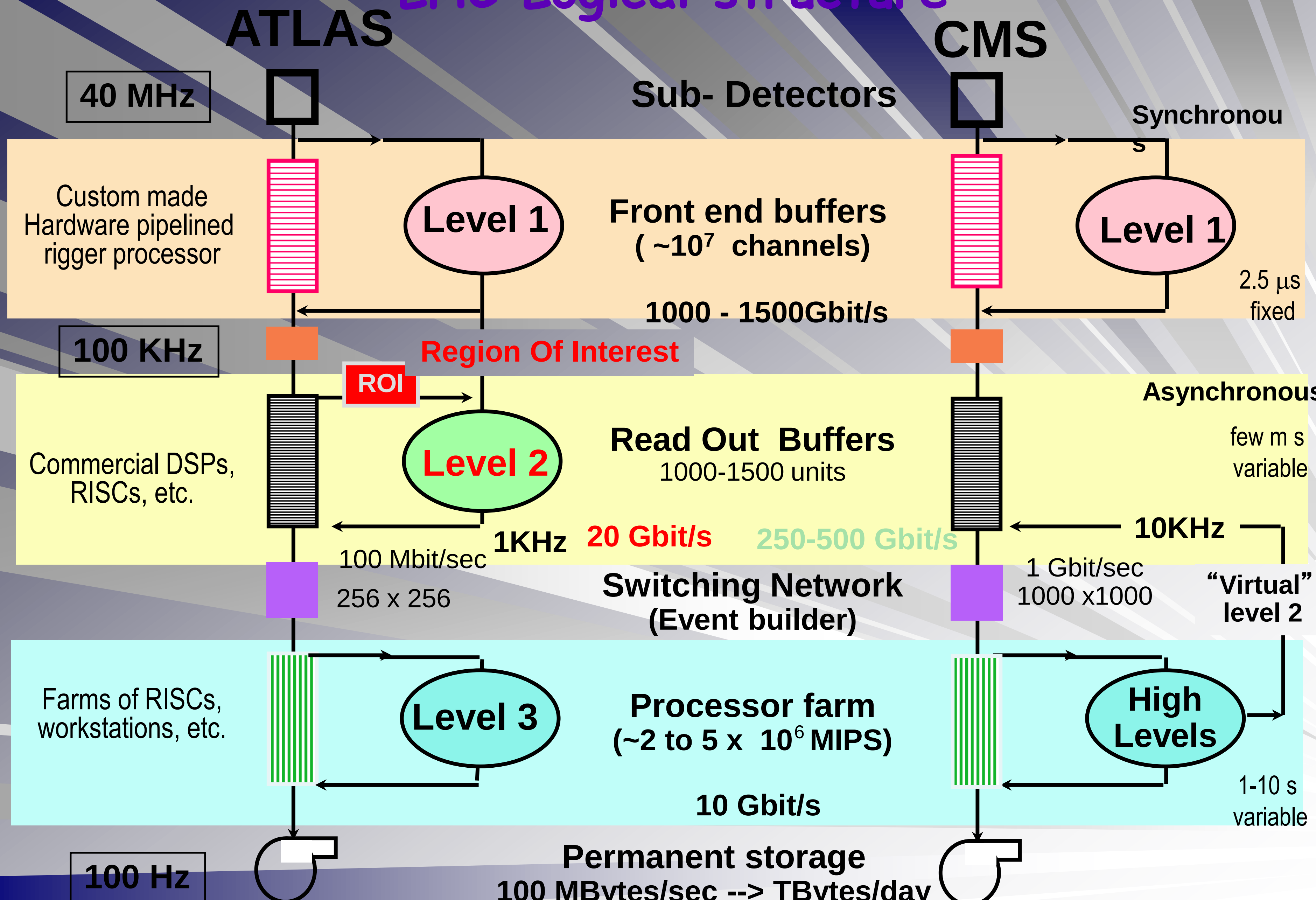
- Send everything, ask questions later (ALICE, CMS, LHCb)



- Send a part first, get better question Send everything only if interesting (ATLAS)



LHC Logical structure



"Logical Strategy" for event selection

MHz — **collision rate**

Logical steps

L1 — Coarse dedicated data

Prompt Trigger
"Identification of objects"

Local identification of
- Energy cluster
- Track segment
- Missing energy

Few µsec — **> KHz** → **Objects**

L2 — Final Digitized data *optimised code*

High Level Trigger Selection
"L 1 objects " confirm
Particle signature
Global Topology
Trigger Menu

- Refine Et and Pt cut
- Detector matching
- Mass calculation
- VTX & Impact parameters ...

Few msec — **> Hz** → **Classification of Physics/calibration**

L3 — Partial to full event *"Off-line" code type*

Event Filter
On-line processing

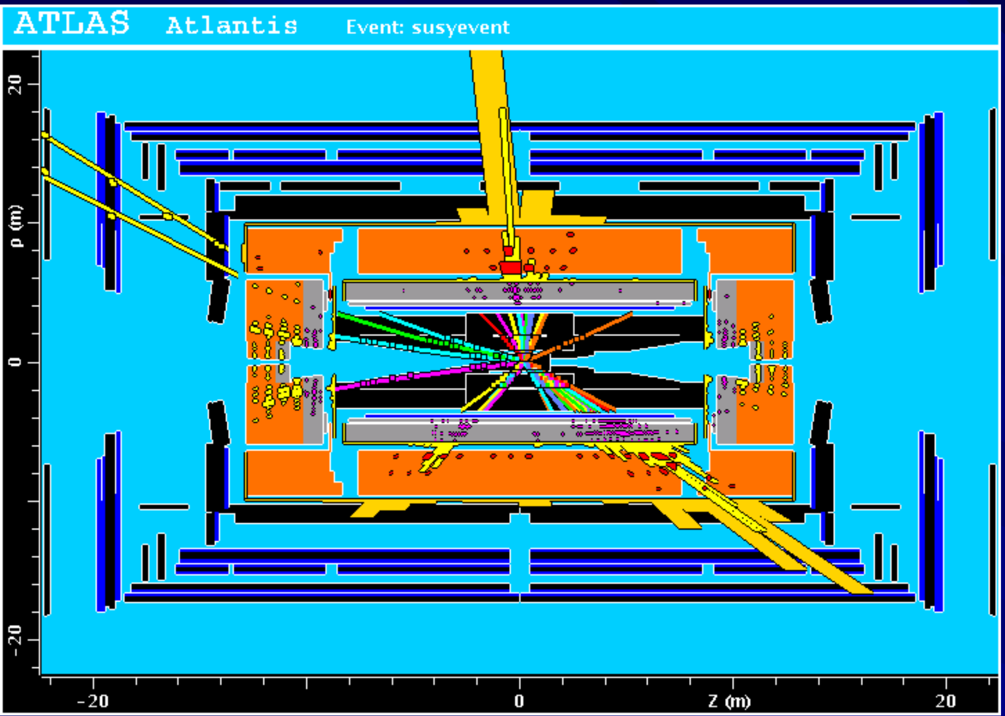
- Full or partial reconstruction
- Calibration & monitoring
- "Hot stream" physics
- "Gold platted "events
- Final formatting etc ...

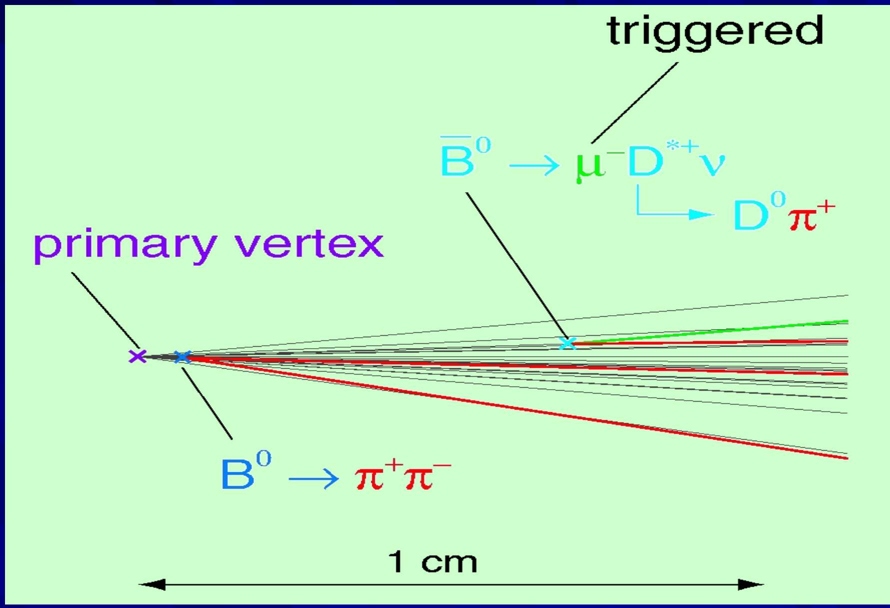
Few sec — **Data streams**

S1 **S2** **S3** **S4** **Sn** → **Storage& analy**

"off-line"

High Level Triggers

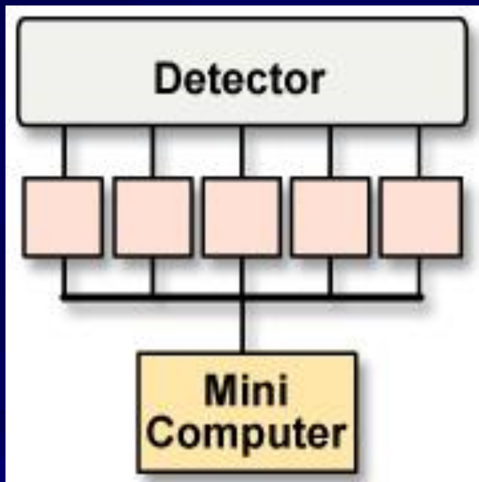




Complicated Event structure with hadronic jets (ATLAS) or secondary vertices require full detector information

Methods and algorithms are the same as for offline reconstruction

Evolution of DAQ technologies and architectures

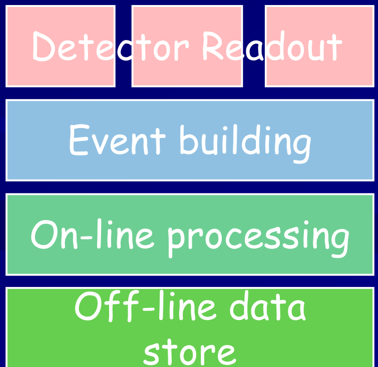


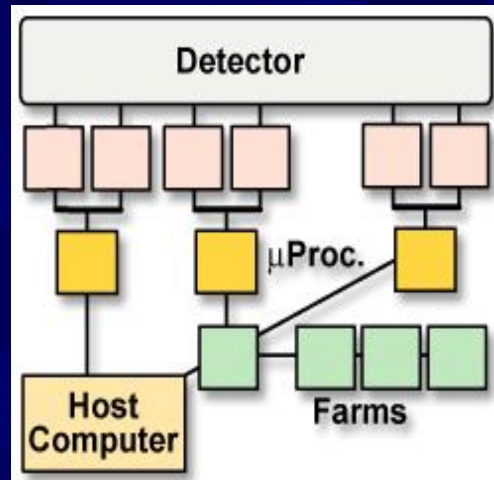
1970-80

CERN PS/SPS

Minicomputers

Readout custom design
First standard: CAMAC
kByte/s



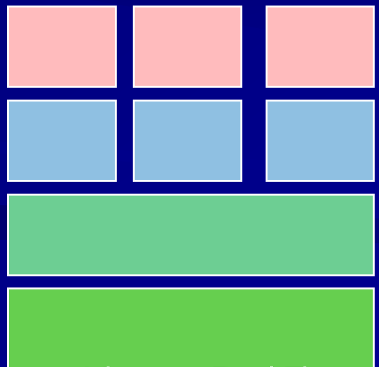


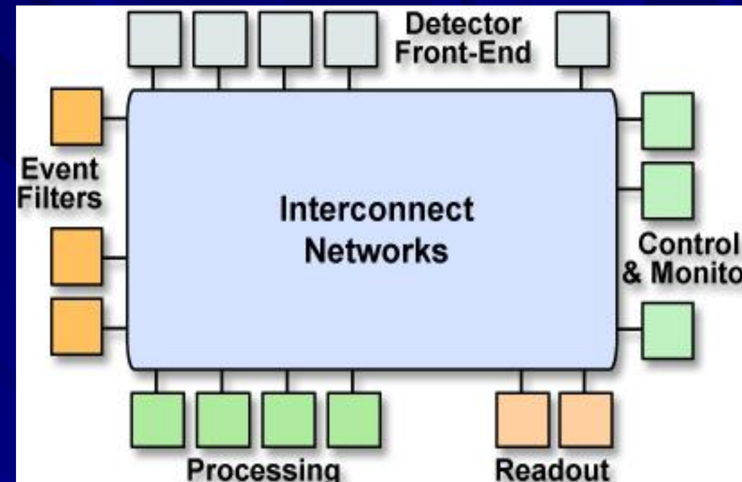
1980-90

LEP

Microprocessors

HEP standards (Fastbus)
Embedded CPU,
Industry standards (VME)
MByte/s



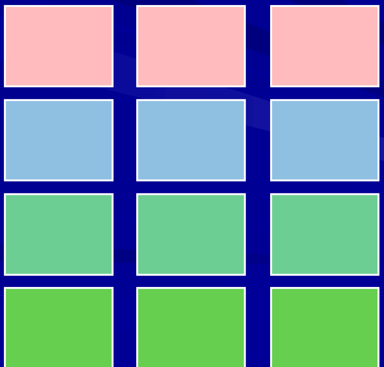


2007 …

LHC (CMS)

Networks/Grids

IT commodities, PC, Clusters
Internet, Web, etc.
GByte/s



From S. Cittolin

Conclusions

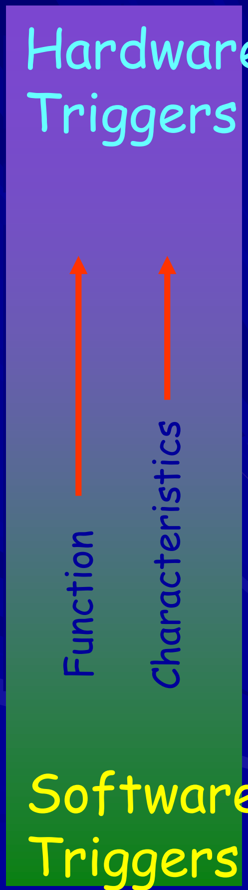
On-Off line boundaries

- **Detectors are becoming more stable and less faulty**
  - High efficiency, Low failure rate
  - Powerfull "on-line" diagnostics and error recovery (expert systems)
- **On-line computing is increasing and not doing only "data collection": More complex analysis is moving on-line**
  - "Off-line" type algorithms early in the selection chain (b tag ..)
  - Selection of "data streams" --> Important role of the "Filter"
  - Precise alignment needed for triggering
  - Detector calibration using Physics process available
  - On-line calibration and correction of data possible
- **Common aspect →**
  - Algorithms, Processing farms, Databases…
  - use similar hw/sw components (PC farms..)

Boundaries become flexible

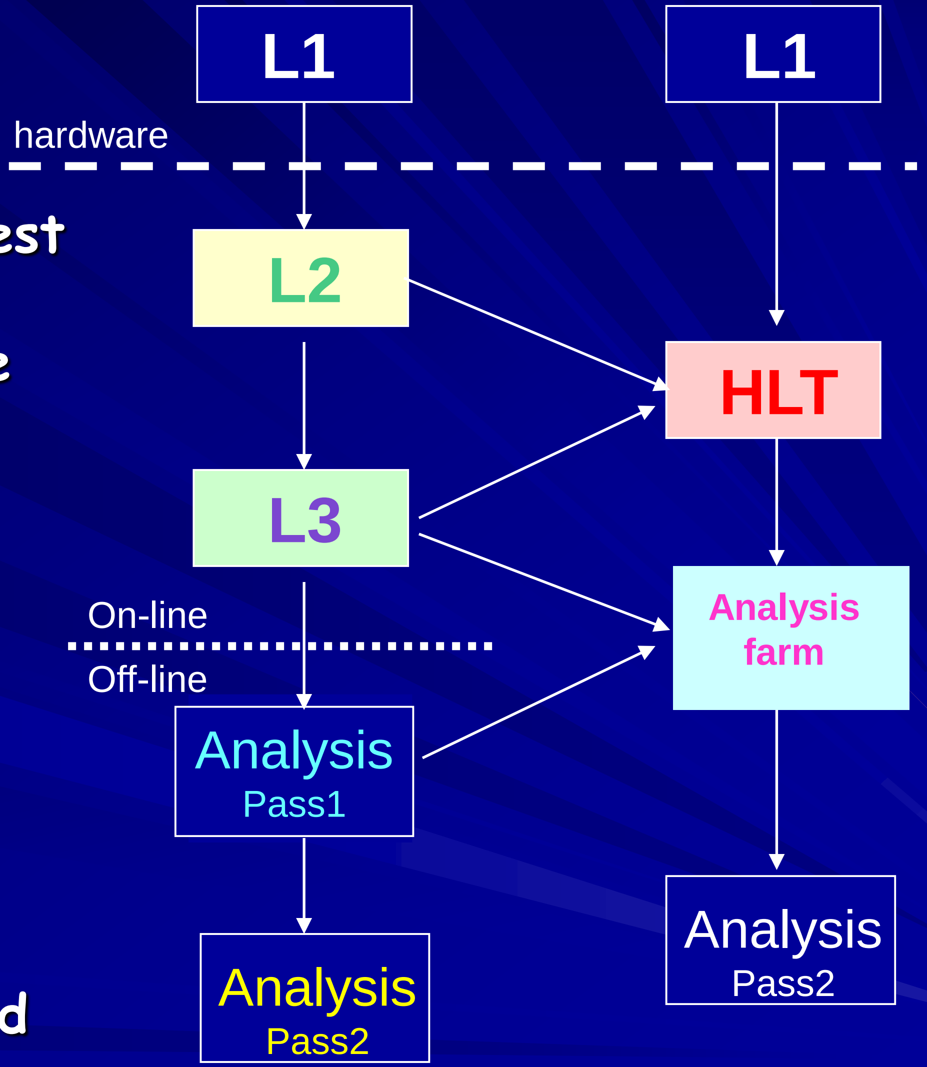
Present evolution (SLHC ...)

- Higher level trigger decisions are migrating to the lower levels → Software Migration is following functional migration
  - Correlations that used to be done at Level 2 or Level 3 in are now done at Level 1.
  - More complex trigger (impact parameter!) decisions at earlier times (HLT) → Less bandwith out of detector?
- Boundaries
  - L2 and L3 are merging into High Levels Triggers
  - DAQ and trigger data flow are merging
  - On-line and off-line boundaries are flexible
- Recent Developments in Electronics
  - Line between software and hardware is blurring
  - Complex Algorithms in hardware (FPGAs)
  - Possible to have logic designs change after board layout
  - Fully commercial components for high levels.



Summary of T/DAQ architecture evolution

- Today
  - Tree structure and partitions
  - Processing farms at very highest levels
  - Trigger and DAQ dataflow are merging
- Near future
  - Data and control networks merged
  - Processing farm already at L2 (HLT)
  - More complex algorithms are moving on line
  - Boundaries between on-line and off-line are flexible
  - Comodity components at HLT



Evolution of Standards

CAMAC BCNAF

From HEP (ESONE)

1970 - 1990
PS- ISR- SPS- LEP

From Computer INDUSTRY

FASTBUS

1980 - 1995
UA2-LEP

VME

1980 - 2007
UA1-LEP -LHC

xTCA

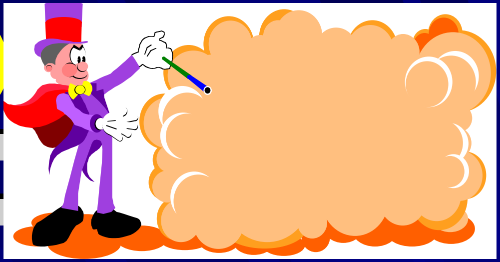
2015 - ?
PANDA
LHC/ ILC

From Telecom INDUSTRY

Technology forecast summary

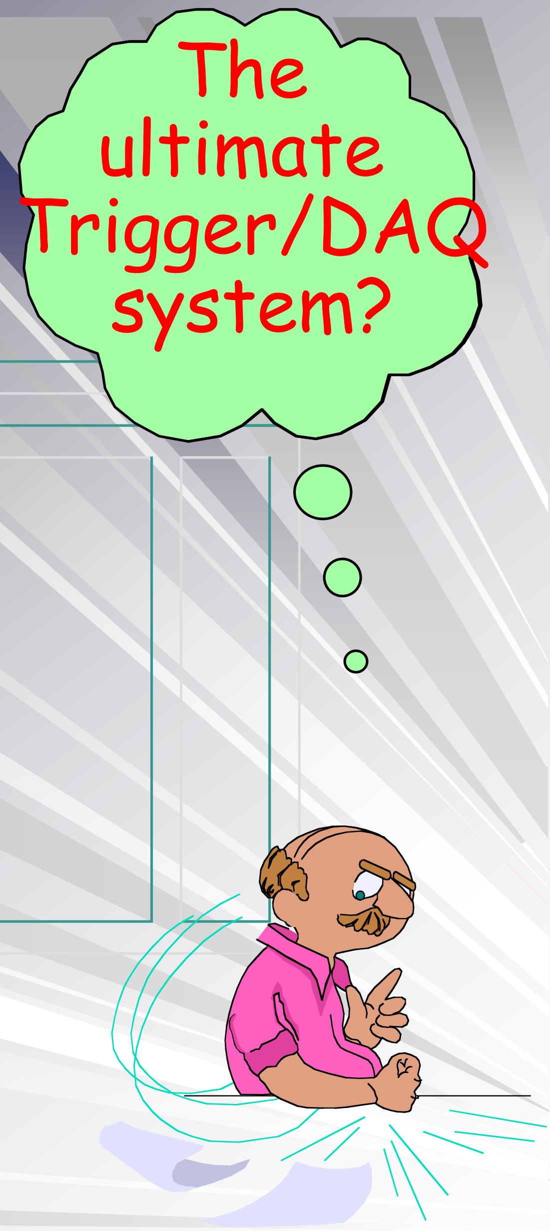
- End of traditional parallel backplane bus paradigm
  - Announced every year since ~1989
  - VME-PCI still there
    - watch PCI Express, RapidIO, ATCA
- Commercial networking products for T/DAQ
  - Conferences:
    - ATM, DS-Link, Fibre Channel, SCI
  - Today: Gigabit Ethernet (1 → 10 → 30 GB/s)
- The ideal processing / memory / IO BW device
  - The past:
    - Emulators (370E),Transputers, DSP's, RISC processors
  - Today: FPGA's →
    - Integrates receiver links, PPC, DSP's and memory

Technology forecast (Con't)



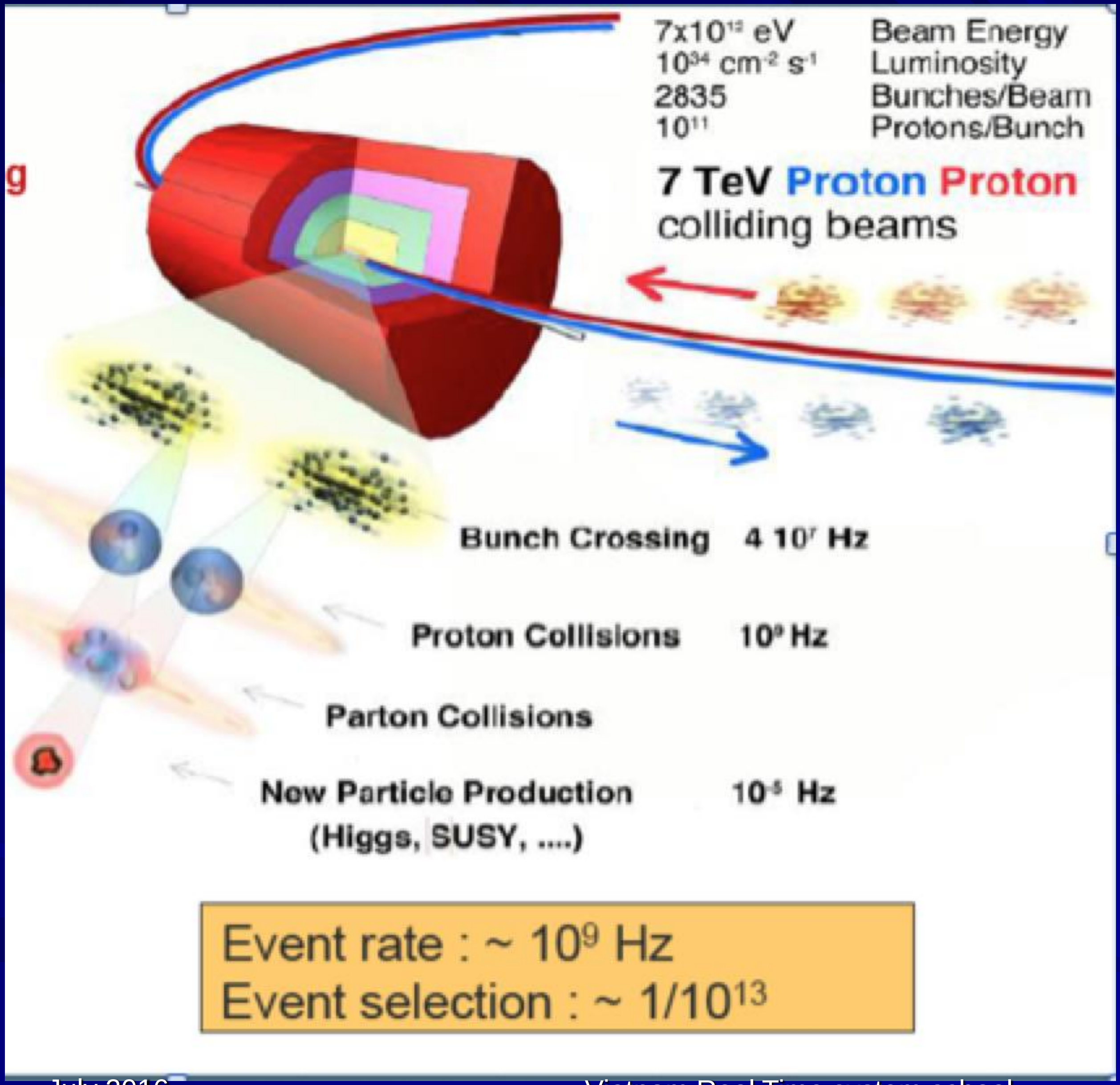
- **Point-to-point link technology**
  - The old style: Parallel Copper – Serial Optical
  - The modern style: Serial Copper – Parallel Optics
    - Today 10Gb/s → 30Gb/s
- **Processors** → Moore's law still true until 2015 ..at least!
  - Continuous increasing of the computing power (Clock)
- **Memory size → quasi illimited !**
    - Today : > 100 GBytes
    - 2015: > Tera Bytes …
- **Modern wisdom (about technology)**
  - *"People tend to overestimate what can be done in one year, and underestimate what can be done in 10 years."*

The Future will be for tomorrow



Introduction
One minute on Physics

Challenging :The LHC T/DAQ



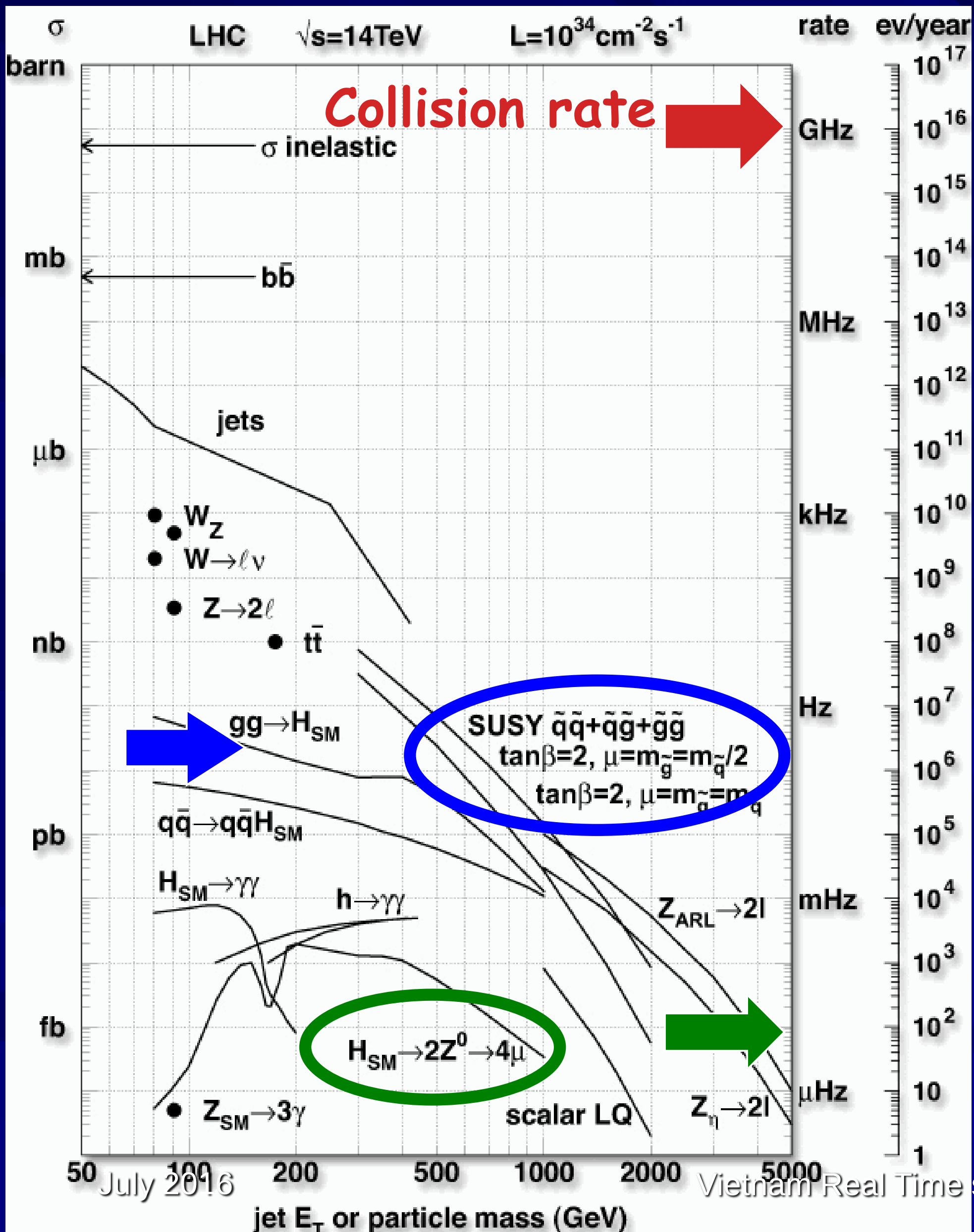
Collision Every 25 ns

Quarks

The p–p machine challenges

- pp collisions produce mainly hadrons with transverse momentum "p_t" ~1 GeV → minimum bias events
- Interesting physics (old and new) has particles (leptons and hadrons) with large p_t:
  - $W \to e\nu$: $M(W)=80\ GeV/c^2$ $\quad p_t(e) \sim 30\text{-}40\ GeV$
  - $H(120\ GeV) \to \gamma\gamma$: $\quad p_t(\gamma) \sim 50\text{-}60\ GeV$
- Impose high thresholds on the p_t of particles
  - Implies distinguishing particle types; possible for electrons, muons and "jets";
  - beyond that → need complex algorithms

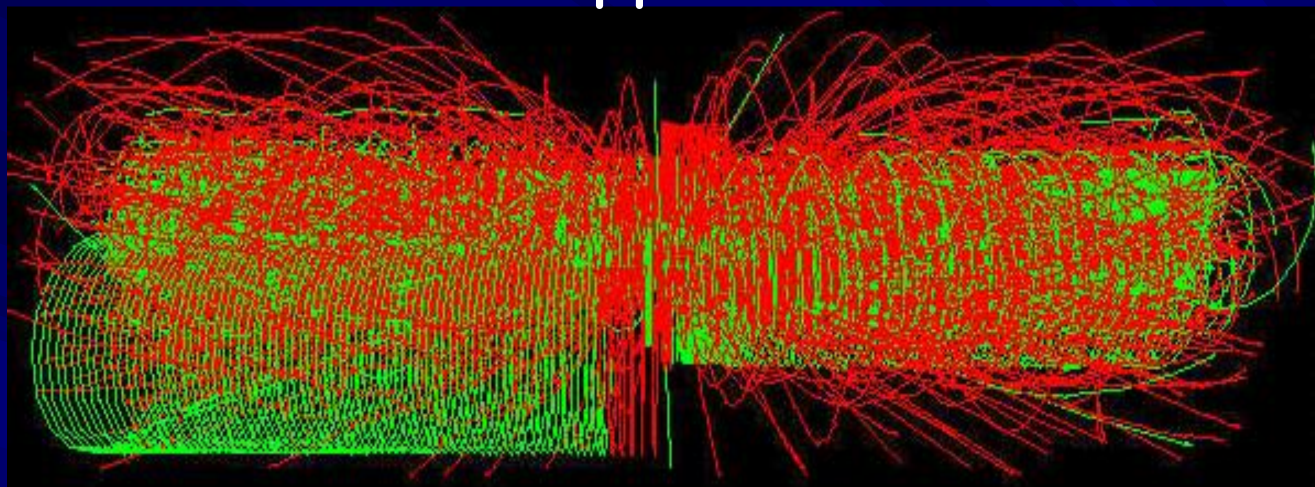
The LHC challenge

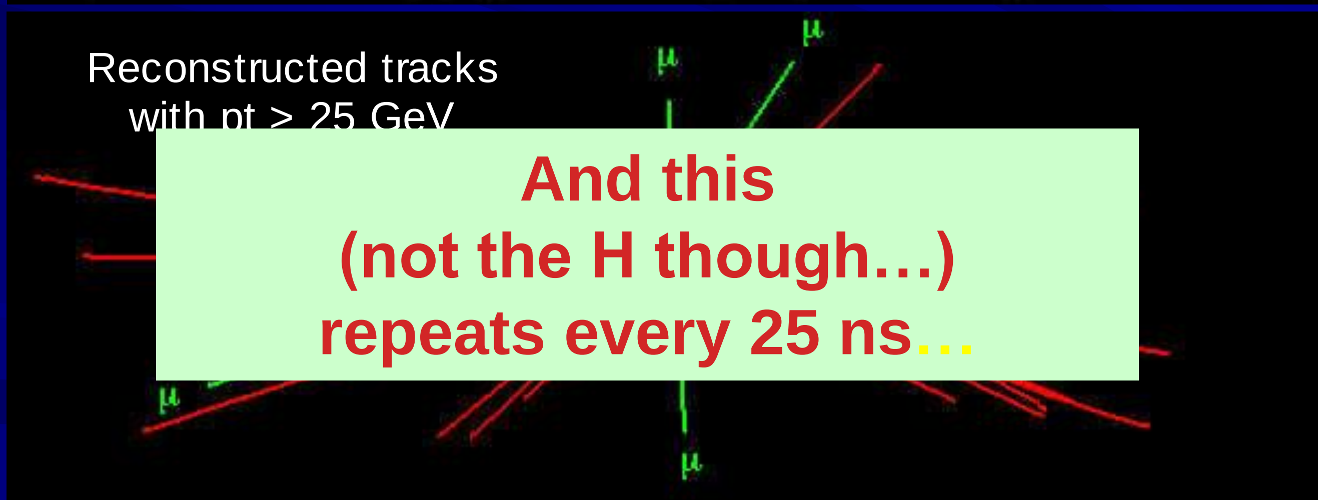


- "Interesting" physics is about 6-8 orders of magnitude below (EWK & Top)
- "Exciting" physics involving new particles/discoveries is ≥ 9 orders of magnitude below σ_{tot}
- We *just* ☺ need to efficiently identify these rare processes from the background <u>before</u> reading out & storing the whole event
- **Conclusion: Need to watch out for high transverse momentum**

pp Collisions at 14 TeV at 10^{34} $cm^{-2}s^{-1}$

Higgs→ZZ → 4 Muons + H→ 4 muons
+ 20-30 'overlapped' min bias events



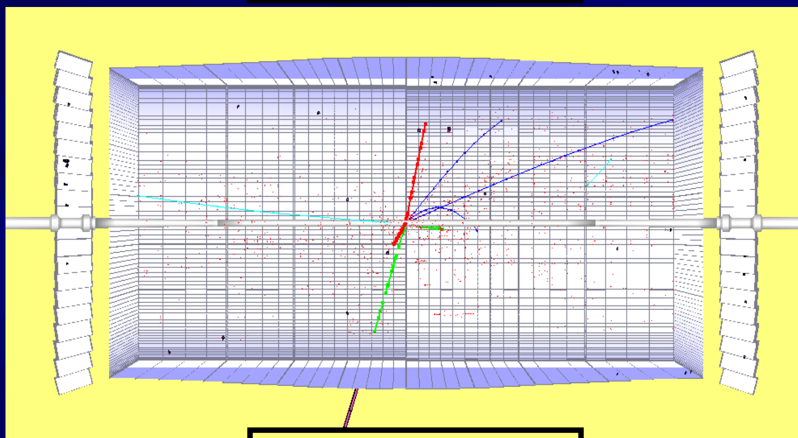


And this
(not the H though…)
repeats every 25 ns…

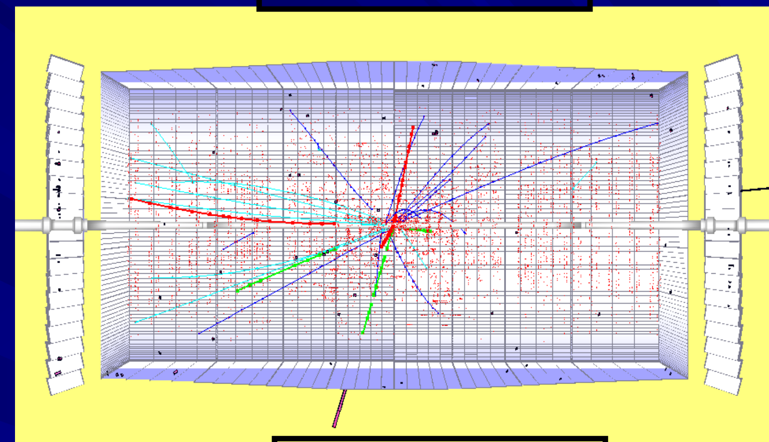
For hadron collider: increasing luminosity could get one into deep trouble …

- $H \to ZZ \to \mu\mu ee$, $M_H = 300$ GeV for different luminosities in CMS

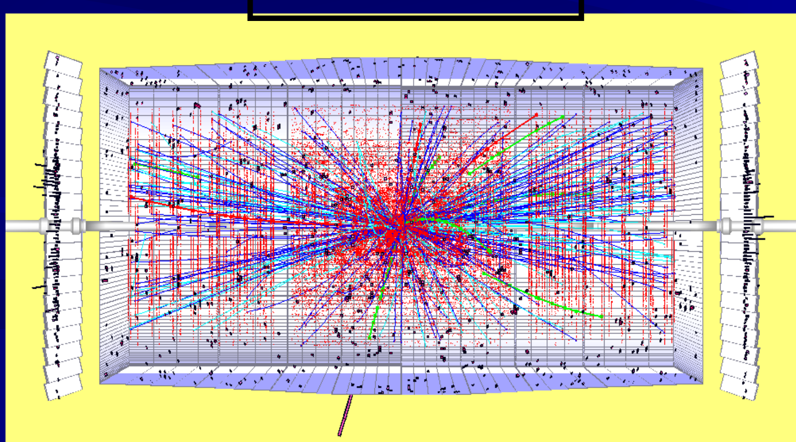
10^{32} cm^{-2}s^{-1}



10^{33} cm^{-2}s^{-1}



10^{34} cm^{-2}s^{-1}



10^{35} cm^{-2}s^{-1}