PAUL SCHERRER INSTITUT

PSI

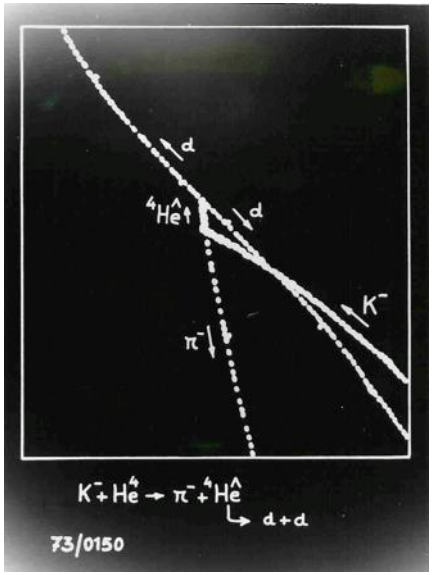
IEEE NPSS
NUCLEAR & PLASMA SCIENCES SOCIETY

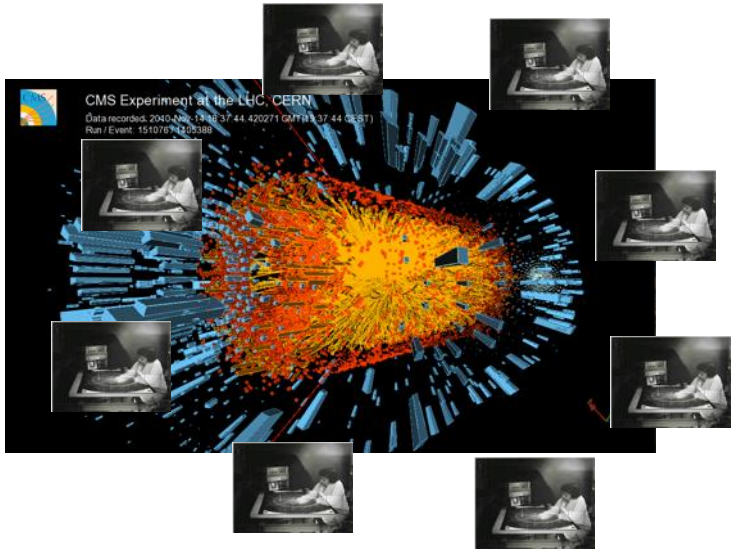
Paul Scherrer Institute, Switzerland
IEEE NPSS distinguished lecturer

Stefan Ritt

Front-end Electronics, Waveform Digitizing and Signal Processing

"Manual" DAQ



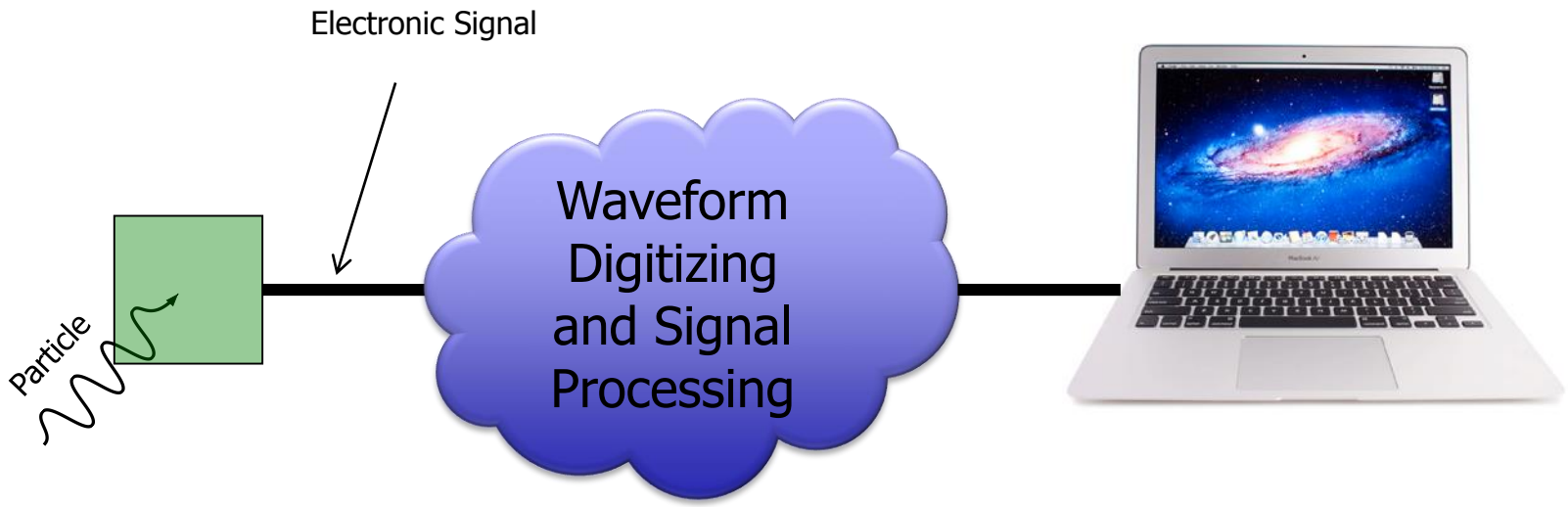


1000 tracks per 25 ns
A4 paper @ 5 g
Truck load @ 40 t

How much paper per second?

200'000 t
5000 Trucks !!!

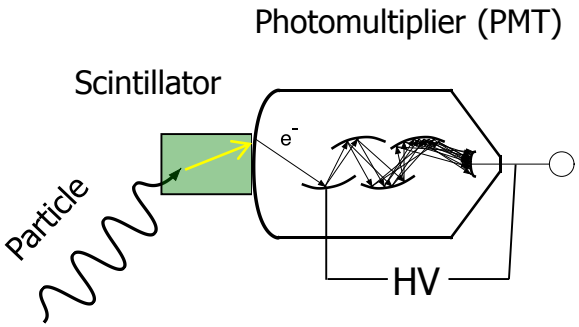
Electronic Signal Acquisition

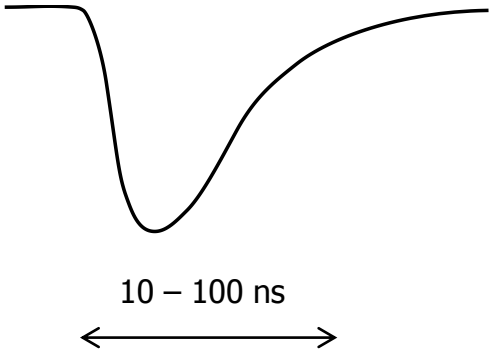


- ADC & TDC technologies
- Signal shaping
- Ultra-fast digitizing (>1 GSPS)
- Digital pulse processing
- Applications

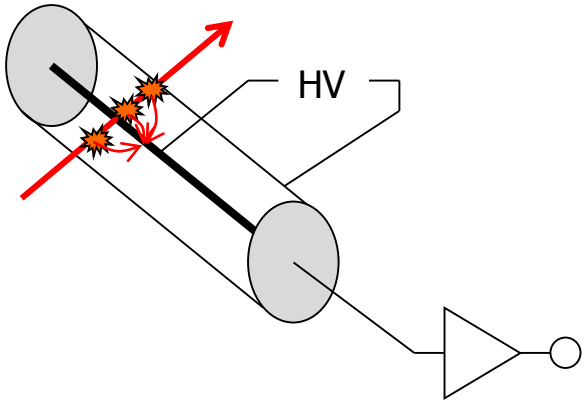
Signals in particle physics

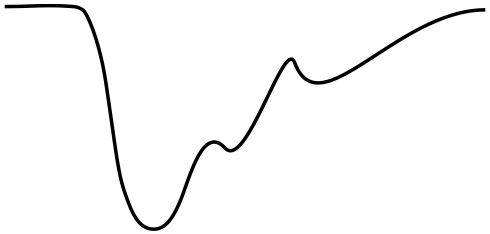
Scintillators (Plastic, Crystals, Noble Liquids, ...)



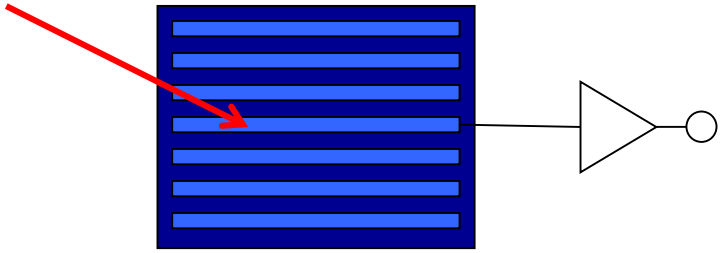


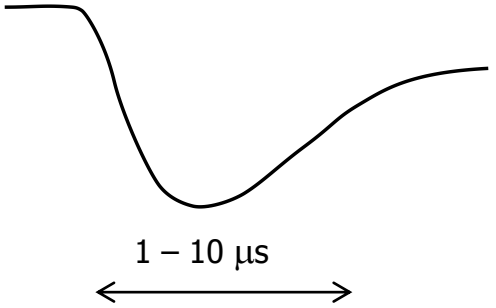
Wire chambers
Straw tubes





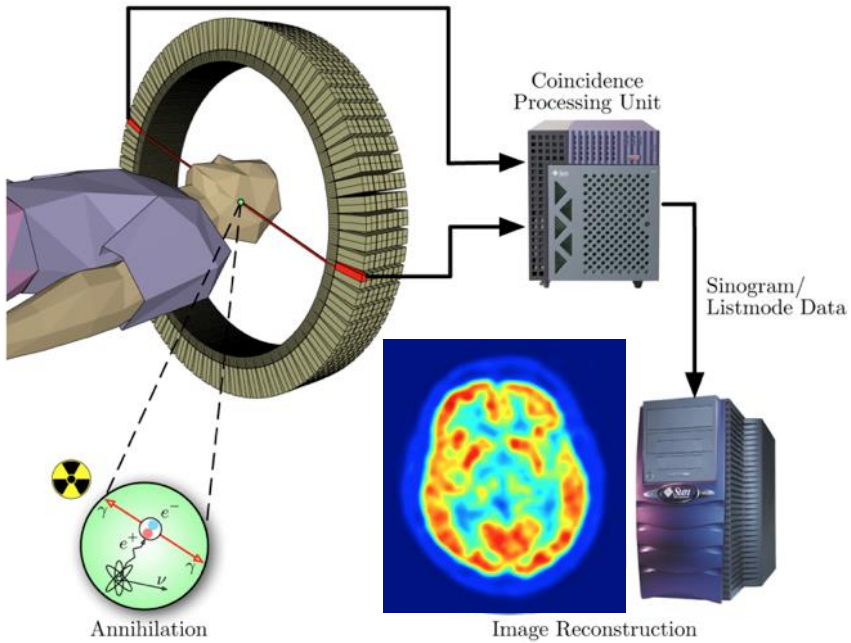
Silicon
Germanium

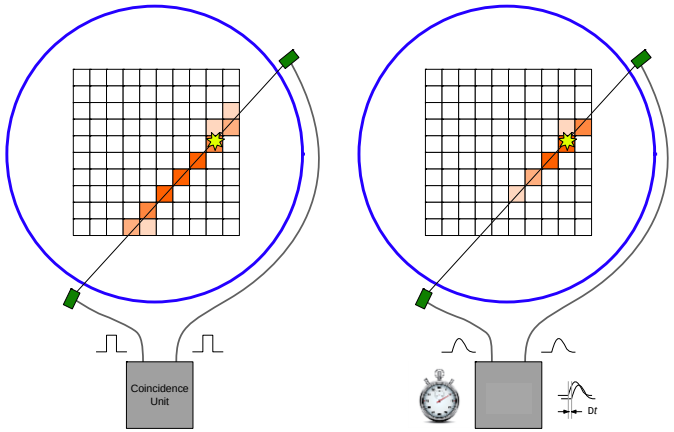




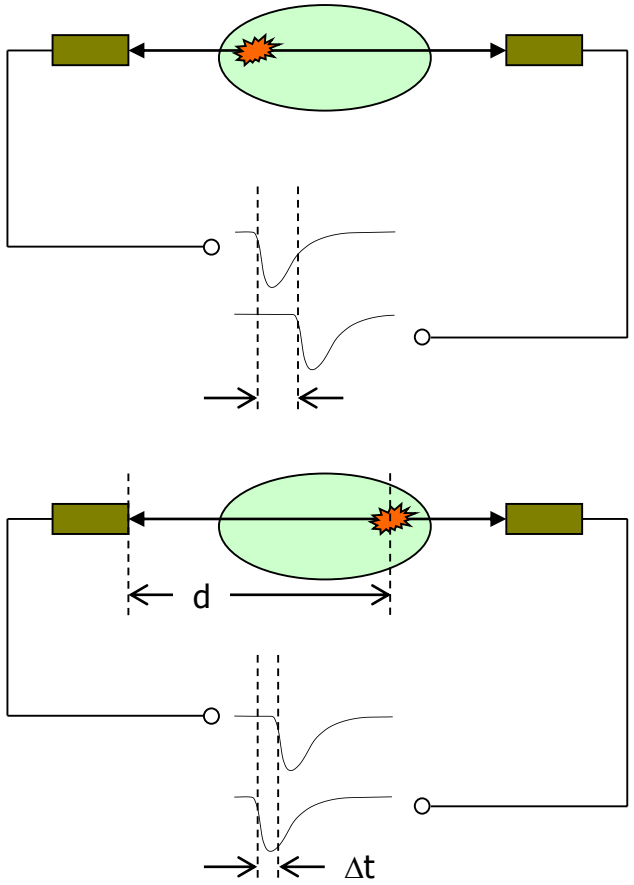
Measure precise timing: ToF-PET

Positron Emission Tomography





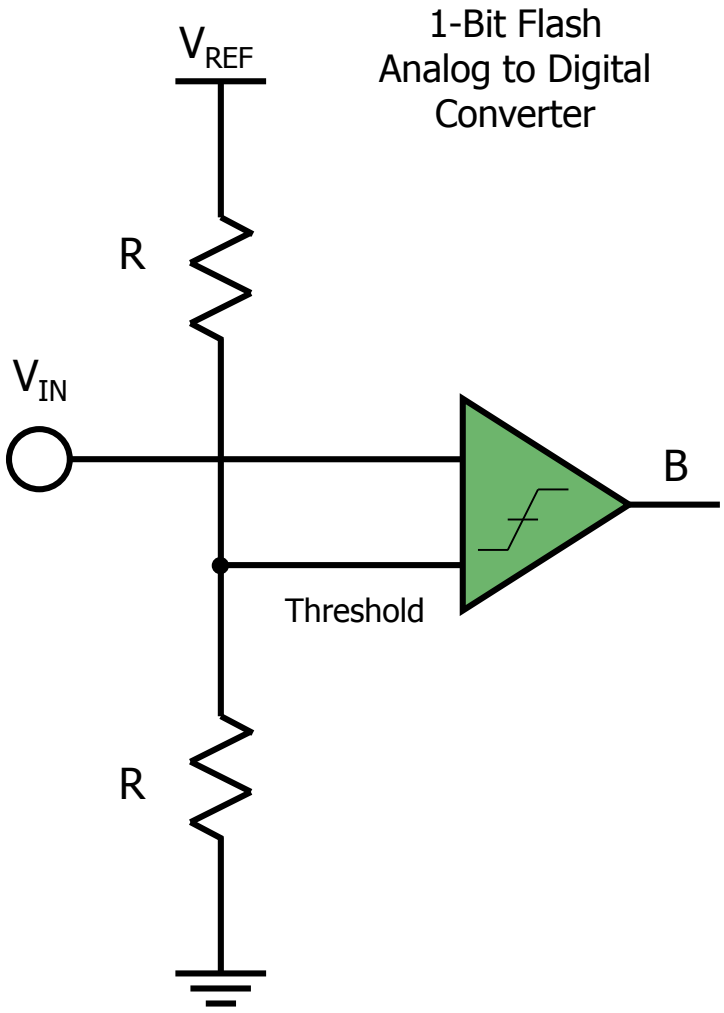
Time-of-Flight PET

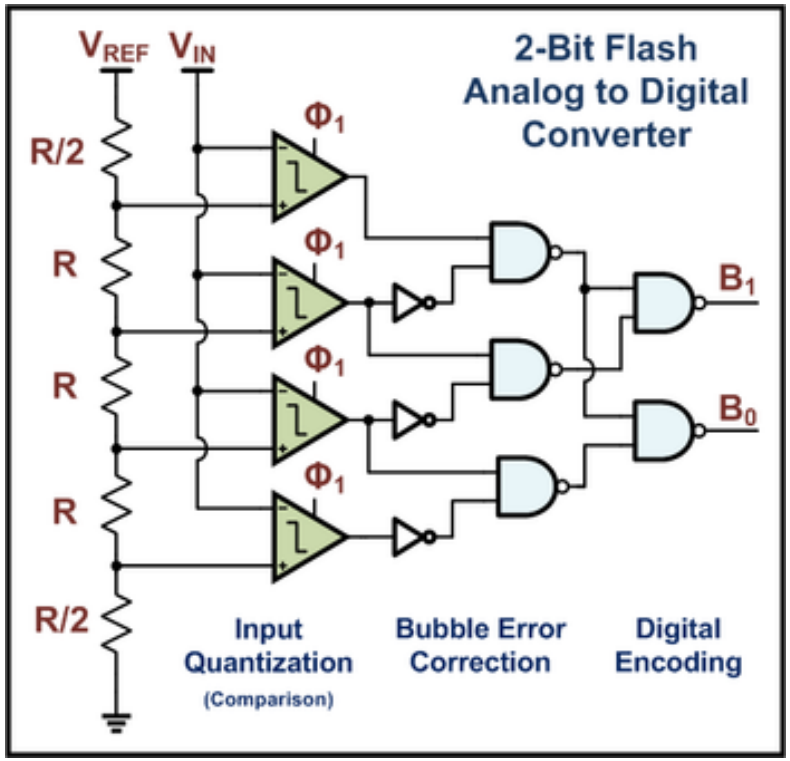


$d \sim c/2 * \Delta t$

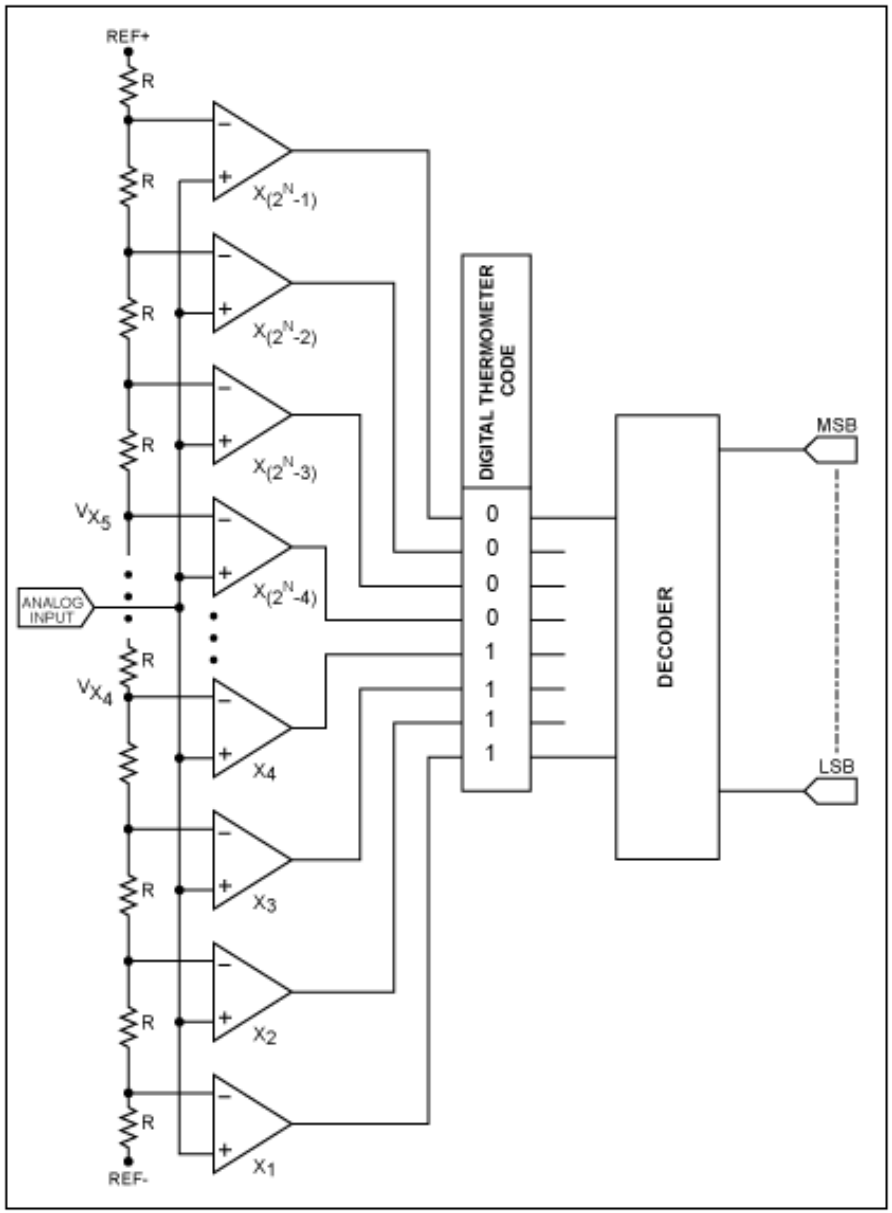
e.g.
d=1 cm → Δt = 67 ps

1-bit & 2-bit ADC



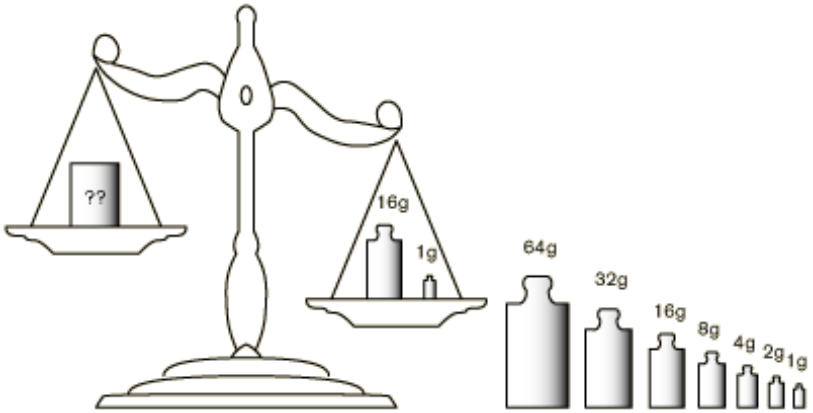


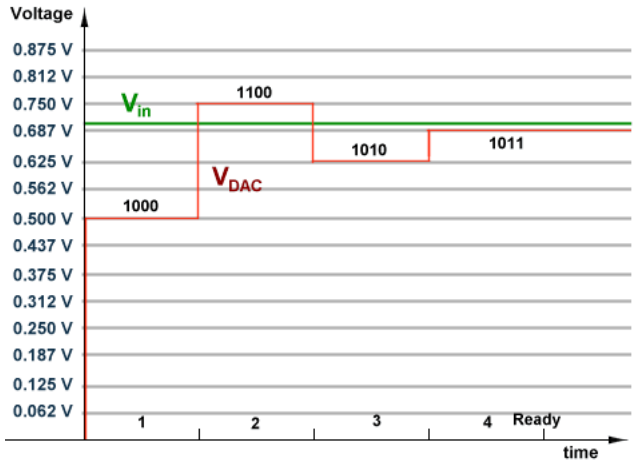
n-bit ADC

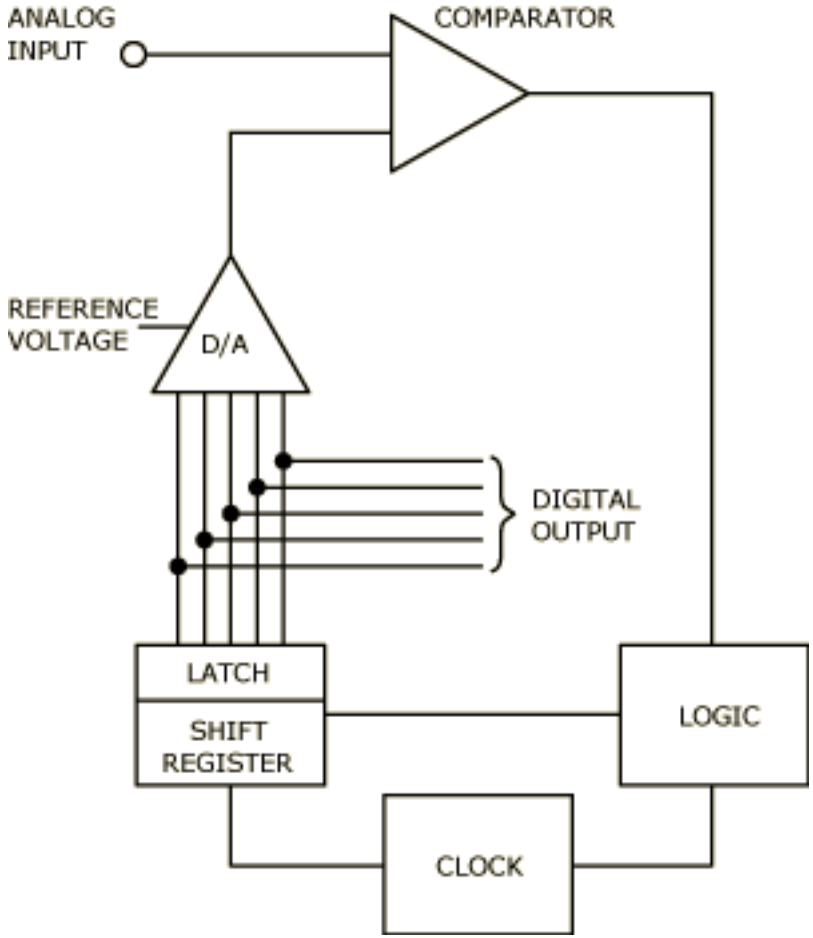


- Flash ADC very fast for small number of bits
- Requires 2^n comparators

Successive approximation ADC

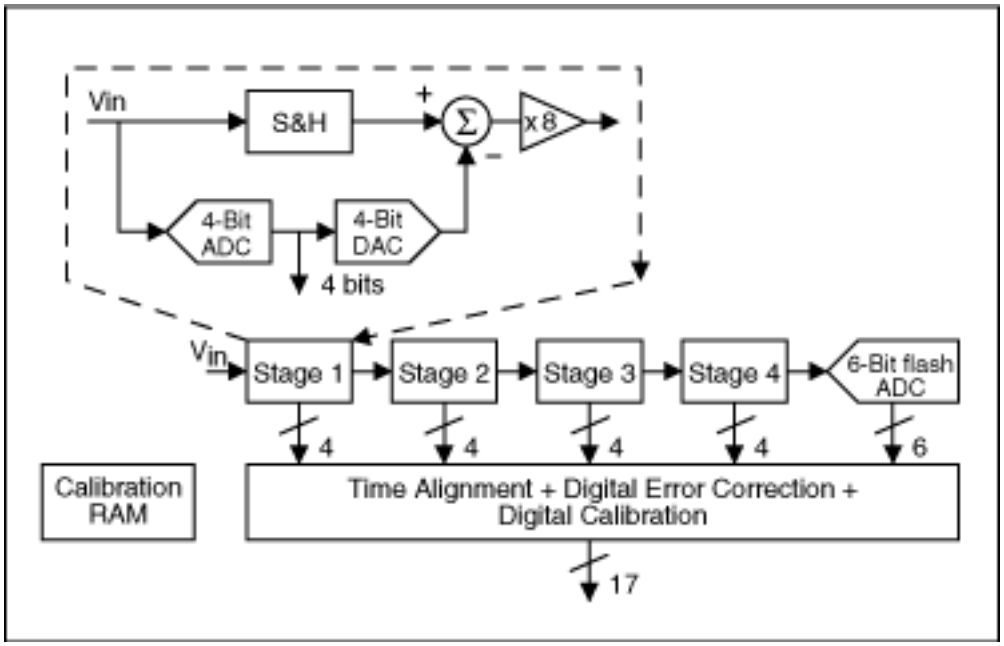


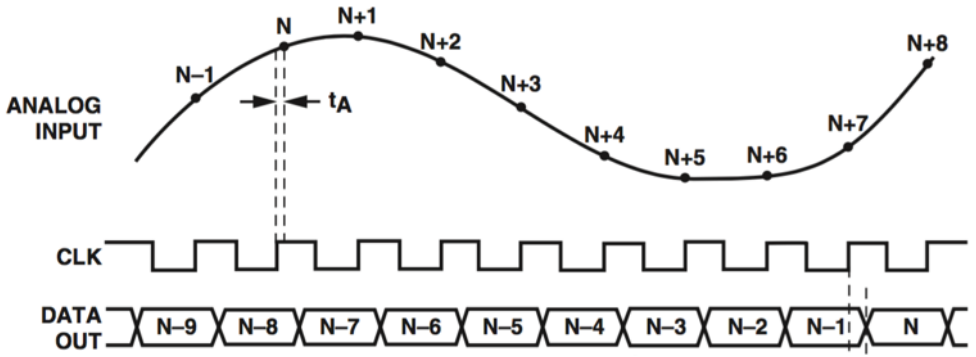




Pipeline ADC

- Combine 4-Bit flash ADC with successive approximation logic
- Only requires 4-Bit flash ADC
- Can convert one sample in each clock cycle
- Has a latency depending on the number of pipeline stages
- Most common technology for fast ADCs (> 10 MHz)

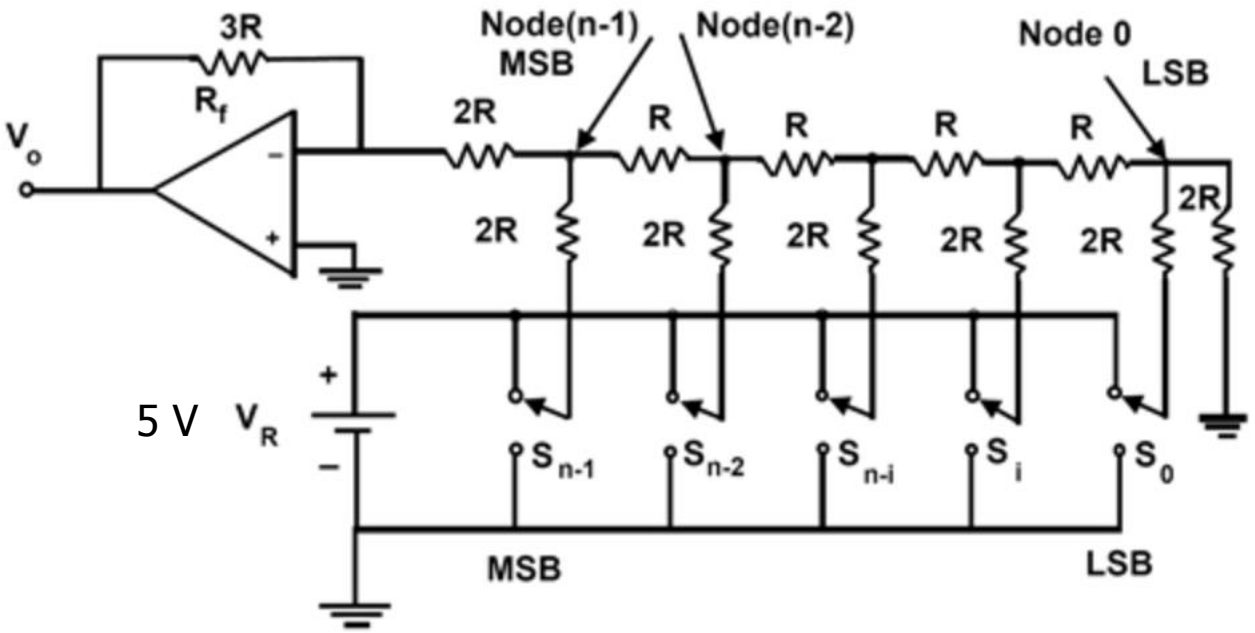




Digital-to-analog converter (DAC)

R-2R Ladder: $0/V_R$ at $S_0 \ldots S_{n-1}$ give binary weighted output $V_o = S * V_R/32$

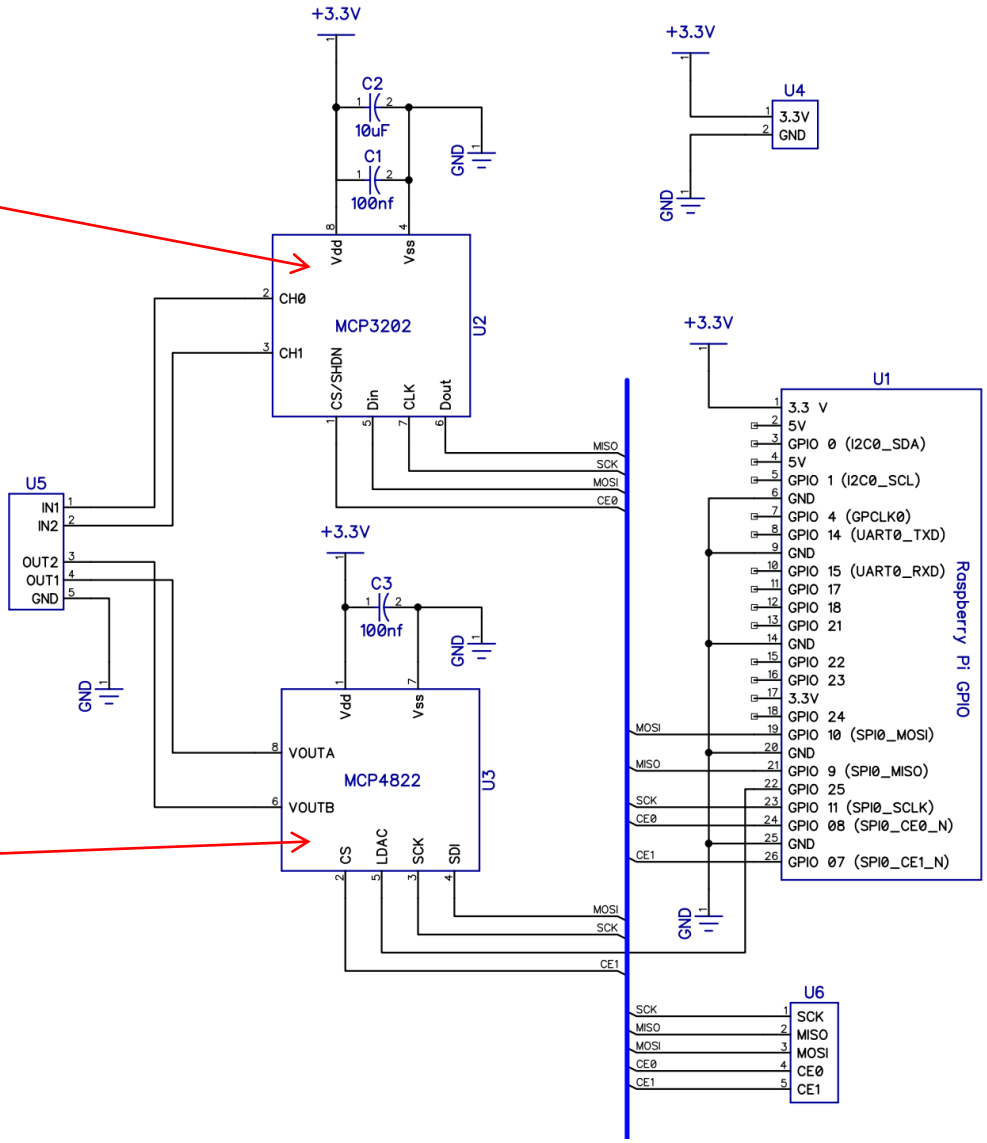
S_{n-1}-S_0	V_O [V]
00000	0
00001	0.16
00010	0.31
00011	0.47
00100	0.63
00101	0.78
...	...
11100	4.38
11101	4.53
11110	4.69
11111	4.84



Raspberry Pi ADC – DAC Board

ADC

DAC



MICROCHIP

MCP4821/MCP4822

12-Bit DACs with Internal V_{REF} and SPI™ Interface

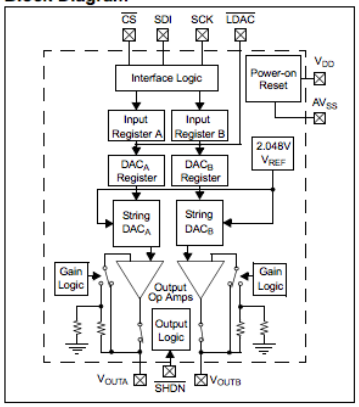
Features

- 12-Bit Resolution
- ±0.2 LSb DNL (typ.)
- ±2 LSb INL (typ.)
- Single or Dual Channel
- Rail-to-Rail Output
- SPI™ Interface with 20 MHz Clock Support
- Simultaneous Latching of the Dual DACs with $\overline{LDAC}$ pin
- Fast Settling Time of 4.5 µs
- Selectable Unity or 2x Gain Output
- 2.048V Internal Band Gap Voltage Reference
- 50 ppm/°C V_{REF} Temperature Coefficient
- 2.7V to 5.5V Single-Supply Operation
- Extended Temperature Range: -40°C to +125°C

Applications

- Set Point or Offset Trimming
- Sensor Calibration
- Precision Selectable Voltage Reference
- Portable Instrumentation (Battery-Powered)
- Calibration of Optical Communication Devices

Block Diagram



Description

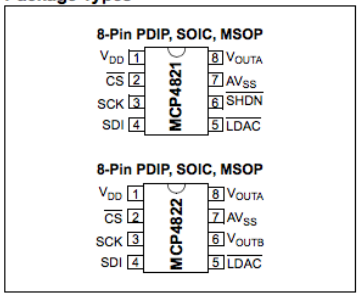
The Microchip Technology Inc. MCP482X devices are 2.7V–5.5V, low-power, low DNL, 12-bit Digital-to-Analog Converters (DACs) with internal band gap voltage reference, optional 2x-buffered output and Serial Peripheral Interface (SPI™).

The MCP482X family of DACs provide high accuracy and low noise performance for industrial applications where calibration or compensation of signals (such as temperature, pressure and humidity) are required.

The MCP482X devices are available in the extended temperature range and PDIP, SOIC and MSOP packages.

The MCP482X devices utilize a resistive string architecture, with its inherent advantages of low DNL error, low ratio metric temperature coefficient and fast settling time. These devices are specified over the extended temperature range. The MCP482X family includes double-buffered registers, allowing simultaneous updates using the $\overline{LDAC}$ pin. These devices also incorporate a Power-On Reset (POR) circuit to ensure reliable power-up.

Package Types



4.0 GENERAL OVERVIEW

The MCP482X devices are voltage-output string DACs. These devices include rail-to-rail output amplifiers, internal voltage reference, shutdown and reset-management circuitry. Serial communication conforms to the SPI protocol. The MCP482X devices operate from 2.7V to 5.5V supplies.

The coding of these devices is straight binary, with the ideal output voltage given by Equation 4-1, where G is the selected gain (1x or 2x), D_N represents the digital input value and n represents the number of bits of resolution (n = 12).

EQUATION 4-1: LSb SIZE

$$V_{OUT} = \frac{2.048V \cdot G \cdot D_N}{2^n}$$

1 LSb is the ideal voltage difference between two successive codes. Table 4-1 illustrates how to calculate LSb.

TABLE 4-1: LSb SIZES

Device	Gain	LSb Size
MCP482X	1x	2.048V/4096
MCP482X	2x	4.096V/4096

4.0.1 INL ACCURACY

INL error for these devices is the maximum deviation between an actual code transition point and its corresponding ideal transition point once offset and gain errors have been removed. These endpoints are from 0x000 to 0xFFF. Refer to Figure 4-1.

Positive INL represents transition(s) later than ideal. Negative INL represents transition(s) earlier than ideal.

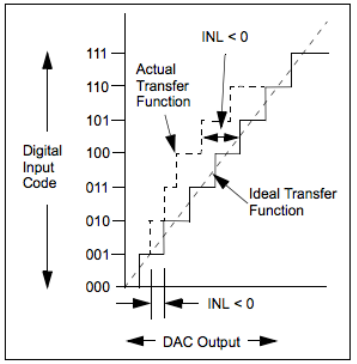


FIGURE 4-1: INL Accuracy.

4.0.2 DNL ACCURACY

DNL error is the measure of variations in code widths from the ideal code width. A DNL error of zero would imply that every code is exactly 1 LSb wide.

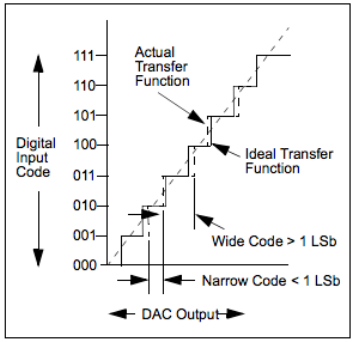


FIGURE 4-2: DNL Accuracy.

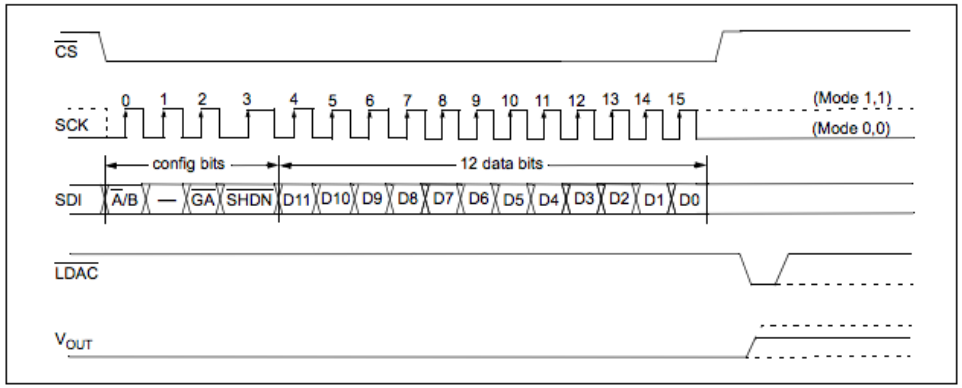
4.0.3 OFFSET ERROR

Offset error is the deviation from zero voltage output when the digital input code is zero.

4.0.4 GAIN ERROR

Gain error is the deviation from the ideal output, V_{REF} – 1 LSb, excluding the effects of offset error.

Write Command



Upper Half:							
W-x	W-x	W-x	W-0	W-x	W-x	W-x	W-x
$\overline{A/B}$	—	$\overline{GA}$	$\overline{SHDN}$	D11	D10	D9	D8
bit 15							bit 8

Lower Half:							
W-x	W-x	W-x	W-x	W-x	W-x	W-x	W-x
D7	D6	D5	D4	D3	D2	D1	D0
bit 7							bit 0

bit 15 **$\overline{A/B}$:** DAC_A or DAC_B Select bit
1 = Write to DAC_B
0 = Write to DAC_A

bit 14 — Don't Care

bit 13 **$\overline{GA}$:** Output Gain Select bit
1 = 1x ($V_{OUT} = V_{REF} * D/4096$)
0 = 2x ($V_{OUT} = 2 * V_{REF} * D/4096$)

bit 12 **$\overline{SHDN}$:** Output Power-down Control bit
1 = Output Power-down Control bit
0 = Output buffer disabled, Output is high-impedance

bit 11-0 **D11:D0:** DAC Data bits
12-bit number "D" which sets the output value. Contains a value between 0 and 4095.

Legend			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	1 = bit is set	0 = bit is cleared	x = bit is unknown

MICROCHIP

MCP3202

2.7V Dual Channel 12-Bit A/D Converter with SPI Serial Interface

Features

- 12-bit resolution
- ±1 LSB max DNL
- ±1 LSB max INL (MCP3202-B)
- ±2 LSB max INL (MCP3202-C)
- Analog inputs programmable as single-ended or pseudo-differential pairs
- On-chip sample and hold
- SPI serial interface (modes 0,0 and 1,1)
- Single supply operation: 2.7V-5.5V
- 100 ksps max. sampling rate at V_{DD} = 5V
- 50 ksps max. sampling rate at V_{DD} = 2.7V
- Low power CMOS technology
  - 500 nA typical standby current, 5 µA max.
  - 550 µA max. active current at 5V
- Industrial temp range: -40°C to +85°C
- 8-pin MSOP, PDIP, SOIC and TSSOP packages

Applications

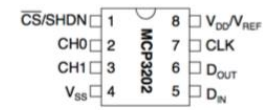
- Sensor Interface
- Process Control
- Data Acquisition
- Battery Operated Systems

Description

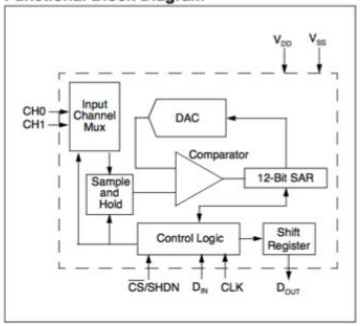
The Microchip Technology Inc. MCP3202 is a successive approximation 12-bit Analog-to-Digital (A/D) Converter with on-board sample and hold circuitry. The MCP3202 is programmable to provide a single pseudo-differential input pair or dual single-ended inputs. Differential Nonlinearity (DNL) is specified at ±1 LSB, and Integral Nonlinearity (INL) is offered in ±1 LSB (MCP3202-B) and ±2 LSB (MCP3202-C) versions. Communication with the device is done using a simple serial interface compatible with the SPI protocol. The device is capable of conversion rates of up to 100 ksps at 5V and 50 ksps at 2.7V. The MCP3202 device operates over a broad voltage range (2.7V-5.5V). Low-current design permits operation with typical standby and active currents of only 500 nA and 375 µA, respectively. The MCP3202 is offered in 8-pin MSOP, PDIP, TSSOP and 150 mil SOIC packages.

Package Types

PDIP, MSOP, SOIC, TSSOP



Functional Block Diagram



5.0 SERIAL COMMUNICATIONS

5.1 Overview

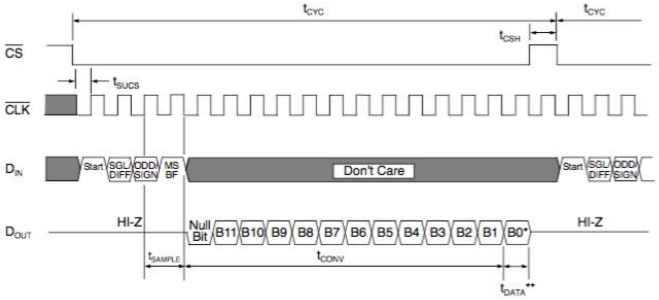
Communication with the MCP3202 is done using a standard SPI-compatible serial interface. Initiating communication with the device is done by bringing the $\overline{CS}$ line low. See Figure 5-1. If the device was powered up with the $\overline{CS}$ pin low, it must be brought high and back low to initiate communication. The first clock received with $\overline{CS}$ low and DIN high will constitute a start bit. The SGL/$\overline{DIFF}$ bit and the ODD/$\overline{SIGN}$ bit follow the start bit and are used to select the input channel configuration. The SGL/$\overline{DIFF}$ is used to select single ended or psuedo-differential mode. The ODD/$\overline{SIGN}$ bit selects which channel is used in single ended mode, and is used to determine polarity in pseudo-differential mode. Following the ODD/$\overline{SIGN}$ bit, the MSBF bit is transmitted to and is used to enable the LSB first format for the device. If the MSBF bit is high, then the data will come from the device in MSB first format and any further clocks with $\overline{CS}$ low will cause the device to output zeros. If the MSBF bit is low, then the device will output the converted word LSB first *after* the word has been transmitted in the MSB first format. See Figure 5-2. Table 5-1 shows the configuration bits for the MCP3202. The device will begin to sample the analog input on the second rising edge of the clock, after the start bit has been received. The sample period will end on the falling edge of the third clock following the start bit.

On the falling edge of the clock for the MSBF bit, the device will output a low null bit. The next sequential 12 clocks will output the result of the conversion with MSB first as shown in Figure 5-1. Data is always output from the device on the falling edge of the clock. If all 12 data bits have been transmitted and the device continues to receive clocks while the $\overline{CS}$ is held low, (and MSBF = 1), the device will output the conversion result LSB first as shown in Figure 5-2. If more clocks are provided to the device while $\overline{CS}$ is still low (after the LSB first data has been transmitted), the device will clock out zeros indefinitely.

If necessary, it is possible to bring $\overline{CS}$ low and clock in leading zeros on the D_{IN} line before the start bit. This is often done when dealing with microcontroller-based SPI ports that must send 8 bits at a time. Refer to Section 6.1 for more details on using the MCP3202 devices with hardware SPI ports.

	Config Bits		Channel Selection		GND
	Sgl/ Diff	Odd/ sign	0	1	
Single Ended Mode	1	0	+	—	-
	1	1	—	+	-
Pseudo-Differential Mode	0	0	IN+	IN-	
	0	1	IN-	IN+	

TABLE 5-1: *Configuration Bits for the MCP3202.*



* After completing the data transfer, if further clocks are applied with $\overline{CS}$ low, the A/D Converter will output zeros indefinitely. See Figure 5-2 below for details on obtaining LSB first data.

** t_{DATA}: during this time, the bias current and the comparator power down while the reference input becomes a high impedance node, leaving the CLK running to clock out the LSB-first data or zeros.

FIGURE 5-1: *Communication with the MCP3202 using MSB first format only.*

SPI Read/Write Cycle

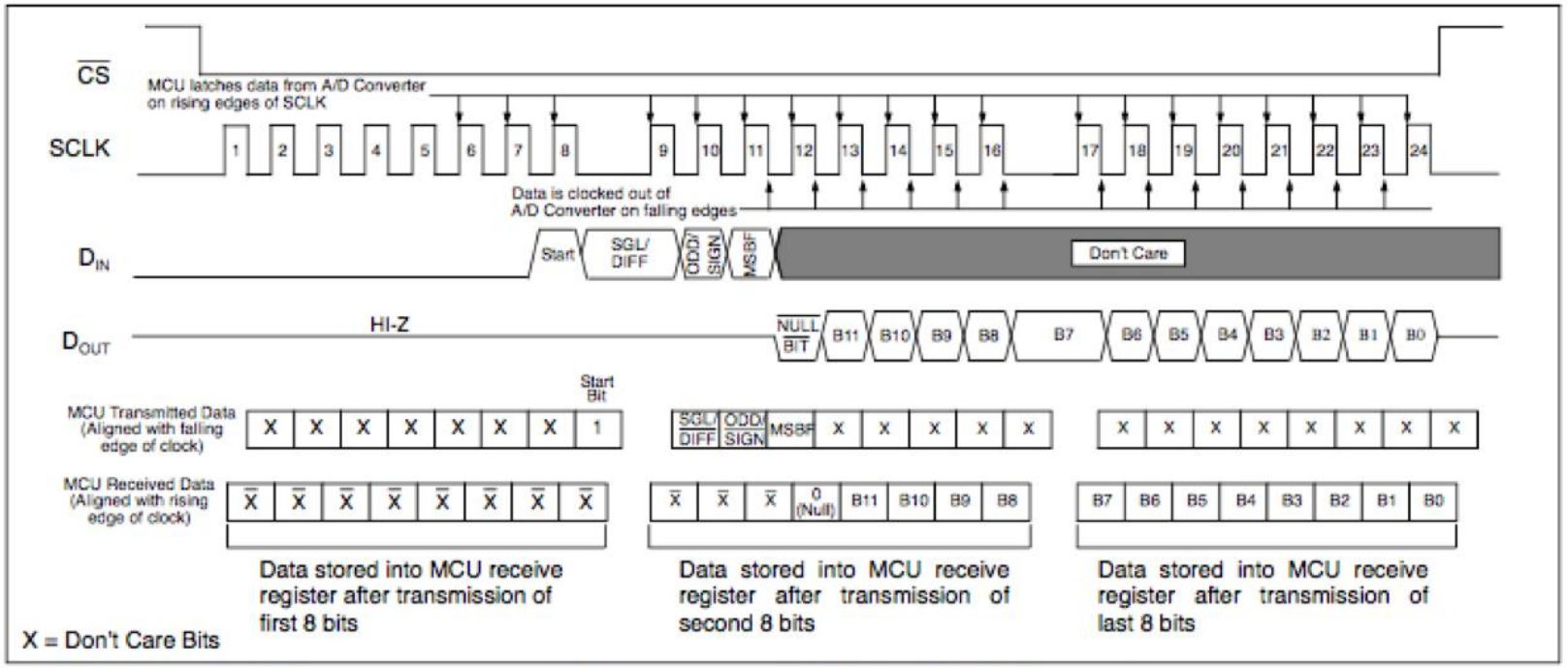


FIGURE 6-1: *SPI Communication using 8-bit segments (Mode 0,0: SCLK idles low).*

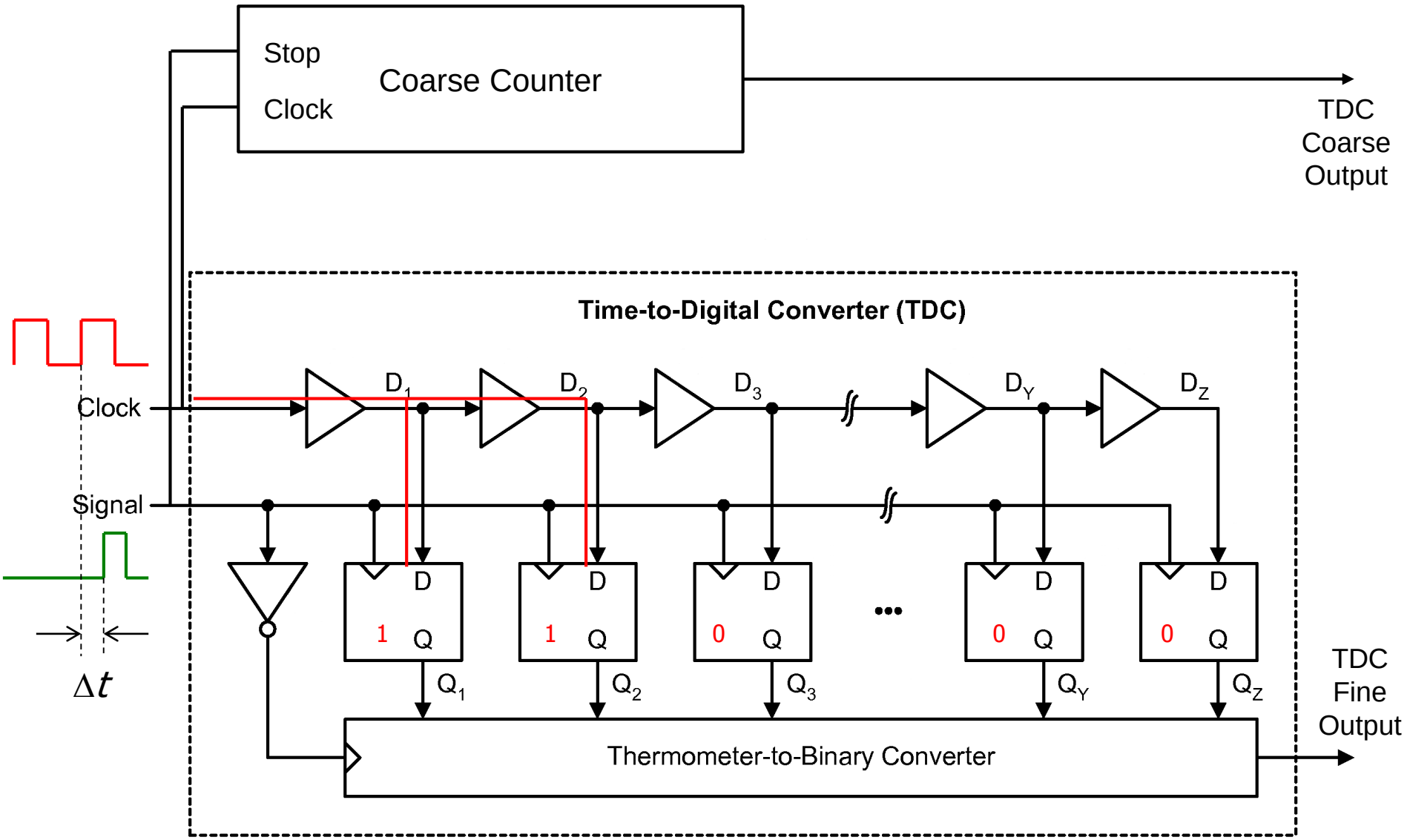
```
spi_buf[0] = 0x01; // Start
spi_buf[1] = 0xA0; // SGL/DIFF=1, ODD/SING=0, MS/BF=1
spi_buf[2] = 0x00;

wiringPiSPIDataRW(spi_fd0, spi_buf, 3);

// convert to Volts
t = (((spi_buf[1] & 0x0F) << 8) | spi_buf[2])/4096.0 * 3.3;

// convert to deg C (10 mV / deg. C)
t *= 100;
```

Time-to-Digital Converter



A 3.9 ps RMS Resolution Time-to-Digital Convertor Using Dual-sampling Method on Kintex UltraScale FPGA

Chong Liu, Yonggang Wang, Peng Kuang, Deng Li, Xinyi Cheng

Real Time 2016 Conference, Padova

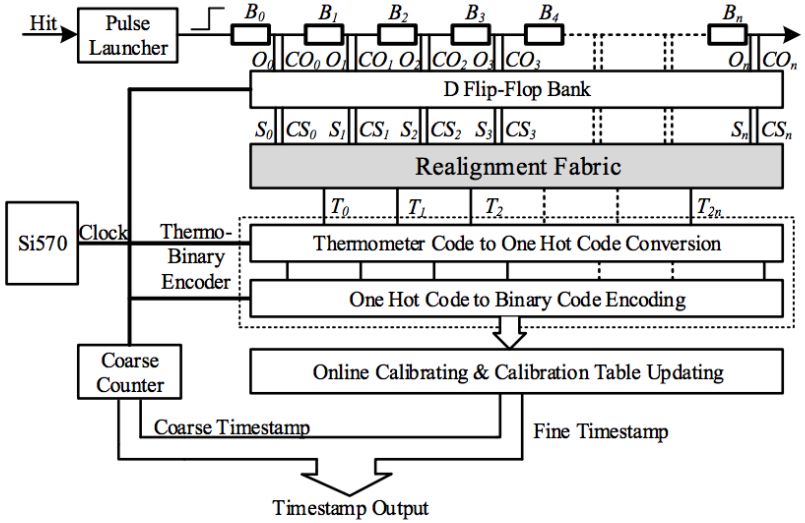


Fig. 1. Diagram of function blocks in a TDL-TDC.

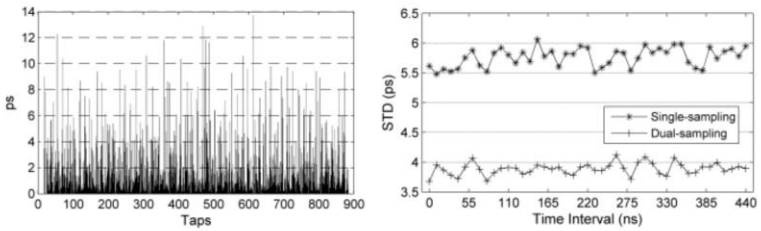
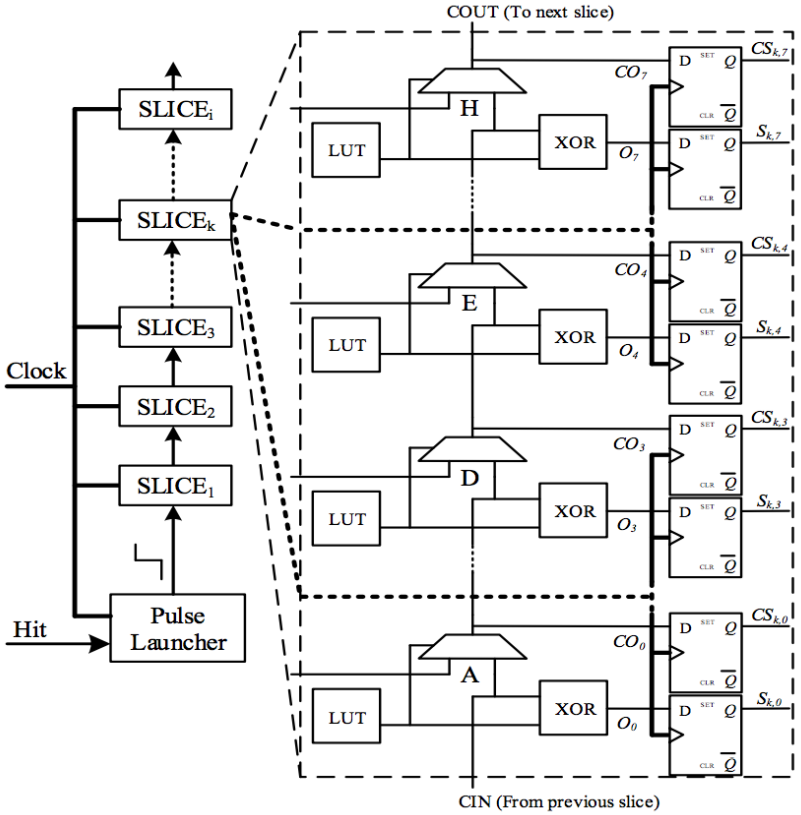
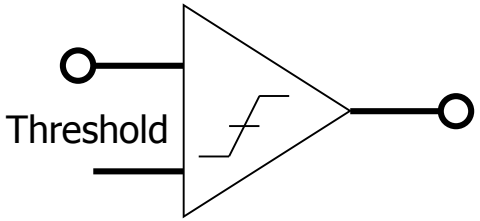


Fig. 3. (a) Bin width of dual-sampling TDC after bin realignment. (b) RMS resolution of dual-sampling TDC and single-sampling TDC.

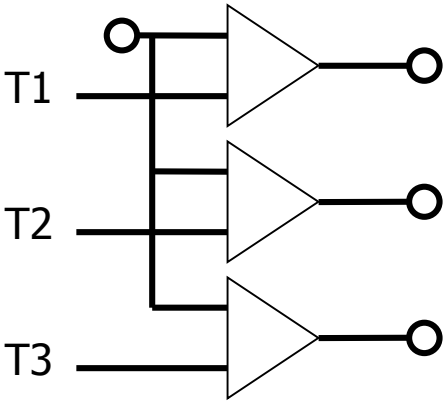


Signal discrimination

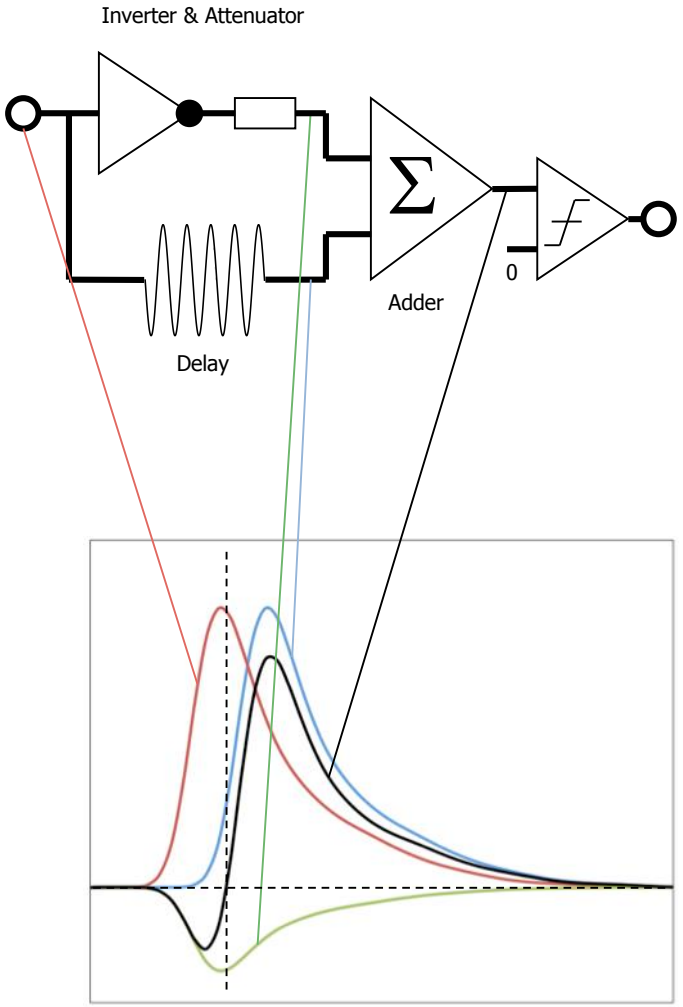
Single Threshold



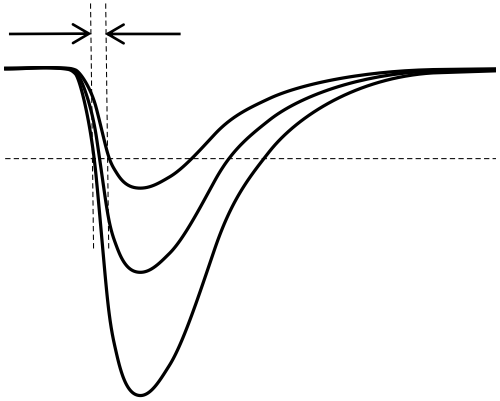
Multiple Thresholds

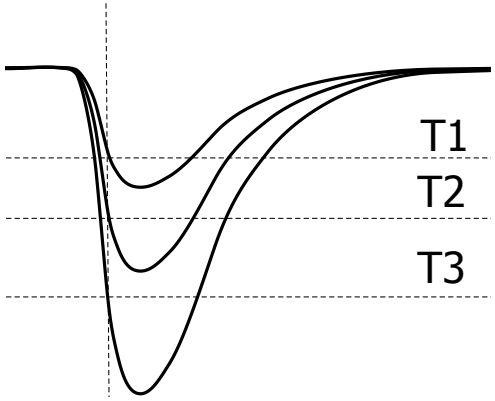


Constant Fraction (CFD)

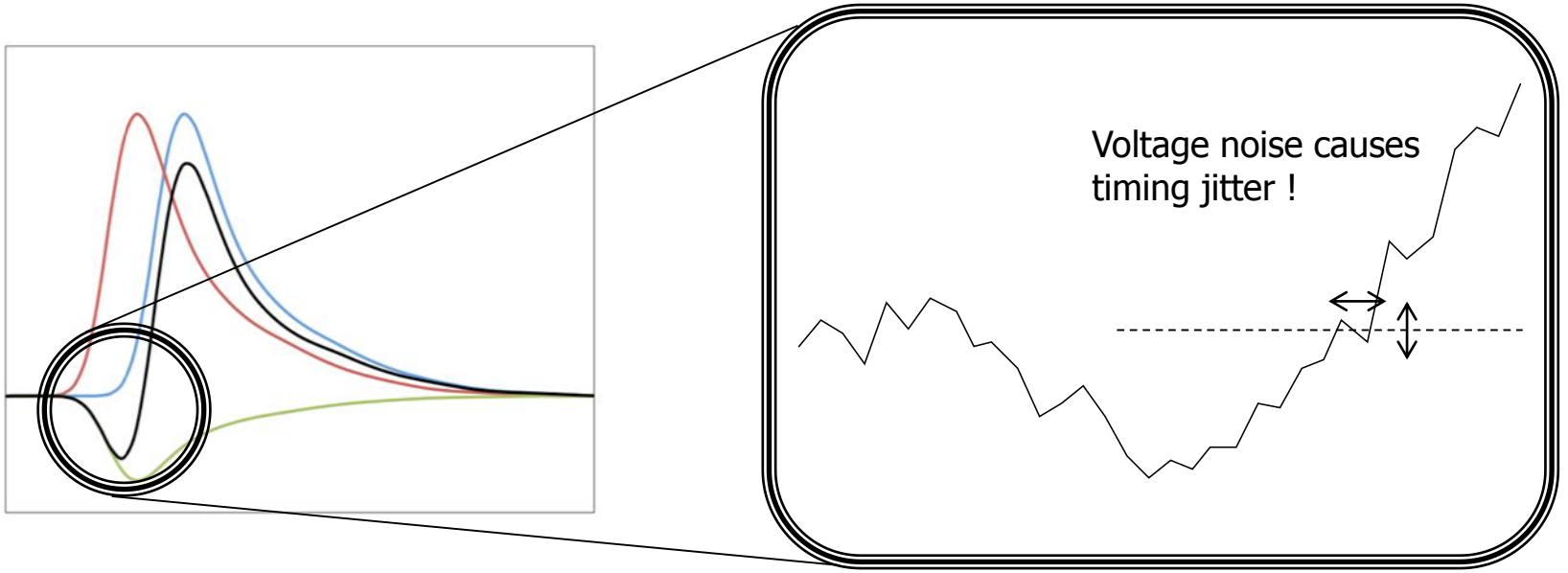


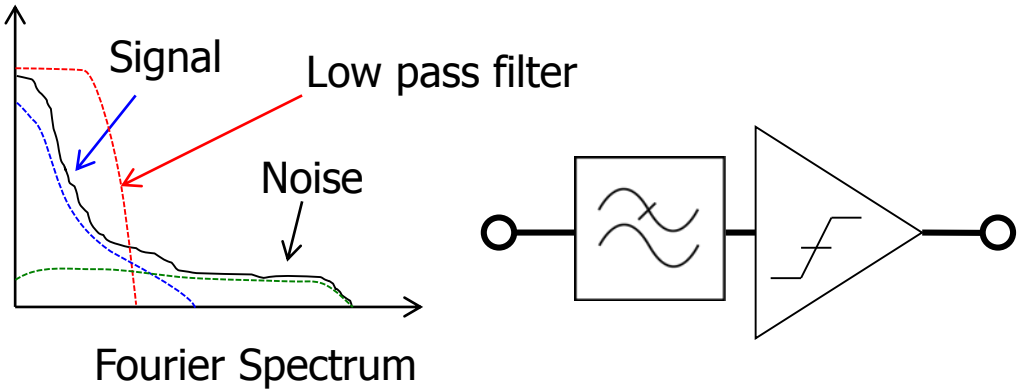
"Time-Walk"

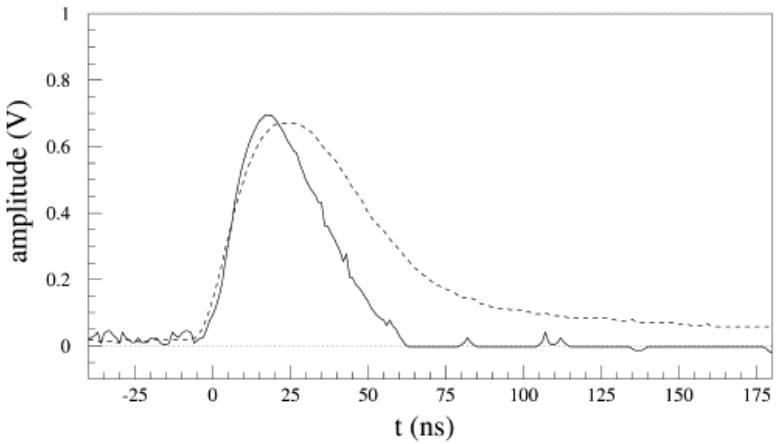




Influence of noise

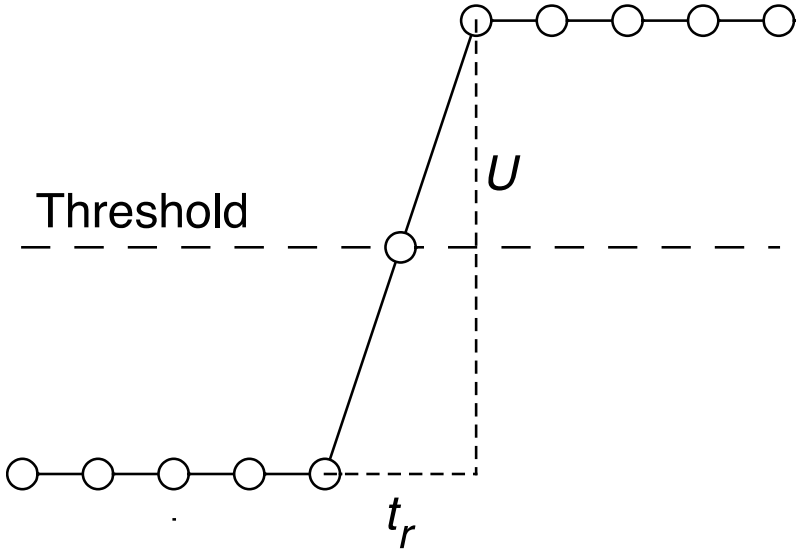


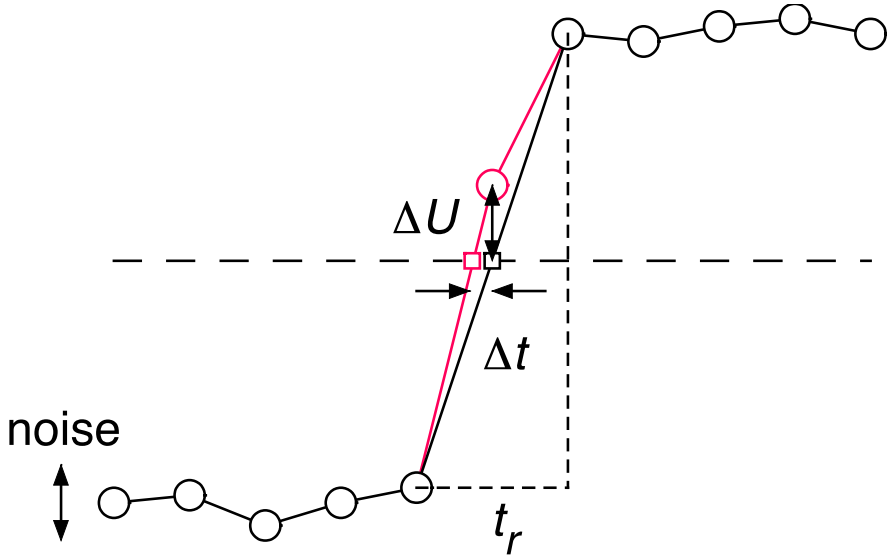




Low pass filter (shaper) reduces noise while maintaining most of the signal

Noise limited time accuracy





$$\frac{\mathrm{D}U}{\mathrm{D}t} \approx \frac{U}{t_r} \longrightarrow \mathrm{D}t = \frac{\mathrm{D}U}{U} \cdot t_r$$

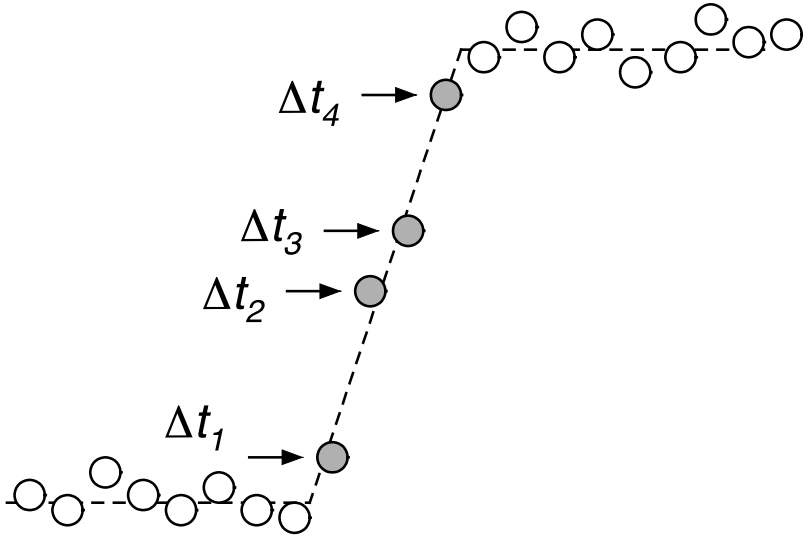
All values in **this** talk are σ (RMS) !
FHWM = 2.35 x σ

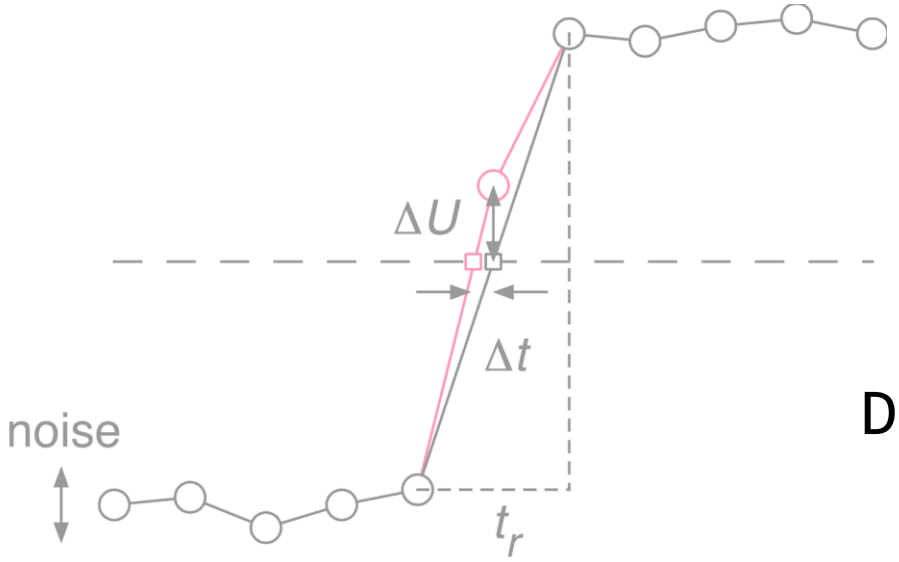
U [mV]	ΔU [mV]	t_r	Δt
100	1	1 ns	10 ps
10	1	3 ns	300 ps

Most today's TDCs have ~20 ps LSB

How can we do better ?

Noise limited time accuracy

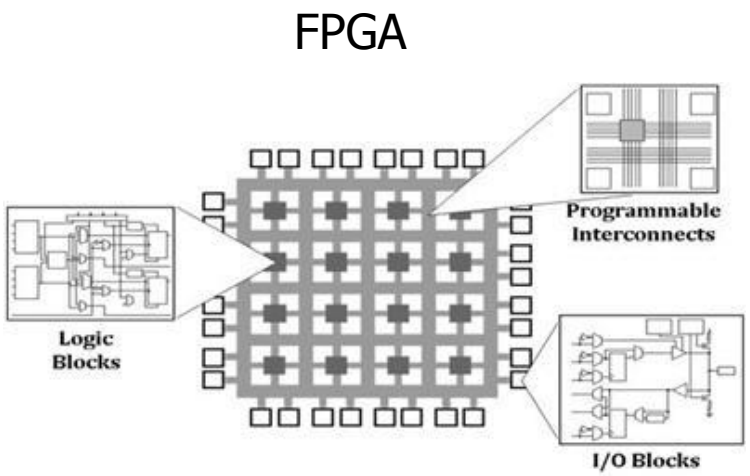


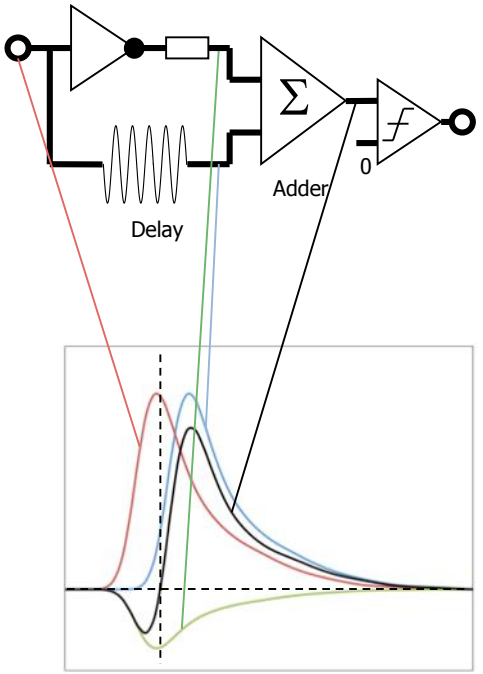


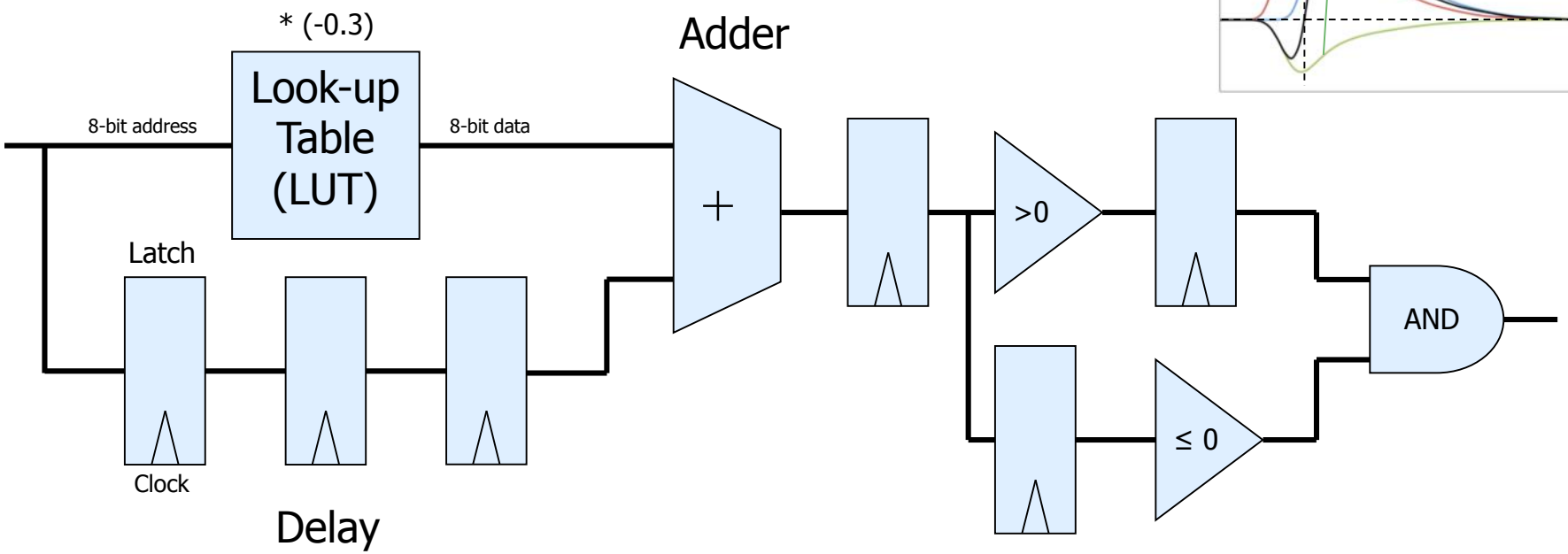
$$\frac{\mathrm{D}U}{\mathrm{D}t} \approx \frac{U}{t_r} \longrightarrow \mathrm{D}t = \frac{\mathrm{D}U}{U} \cdot t_r$$

$$\mathrm{D}t = \frac{\mathrm{D}U}{U} \cdot t_r \cdot \frac{1}{\sqrt{n}} = \frac{\mathrm{D}U}{U} \frac{t_r}{\sqrt{t_r f_S}} = \frac{\mathrm{D}U}{U} \cdot \frac{\sqrt{t_r}}{\sqrt{f_S}}$$

Example: CFG in FPGA

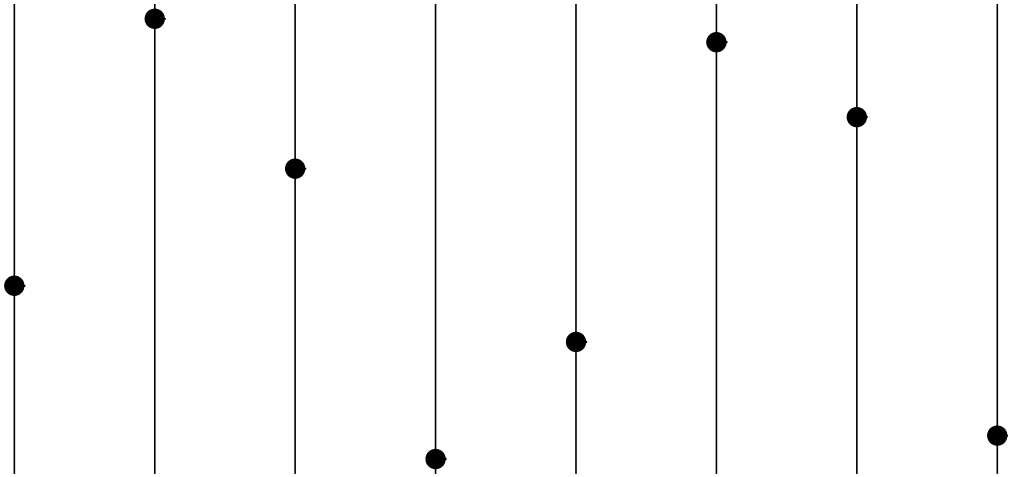




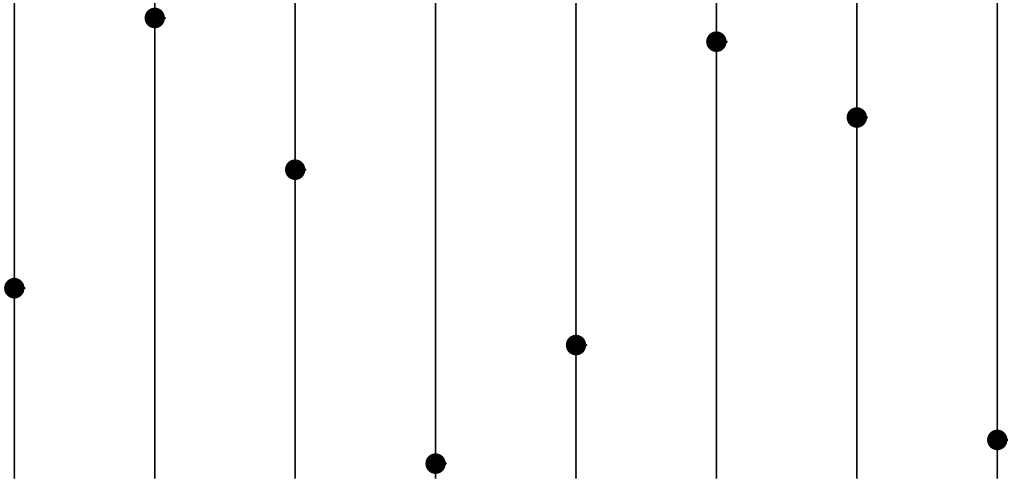


Nyquist-Shannon Sampling Theorem

$f_{signal} < f_{sampling}/2$

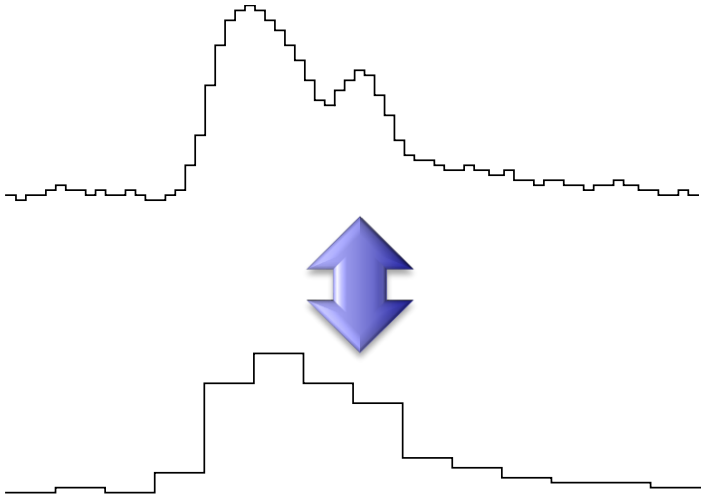


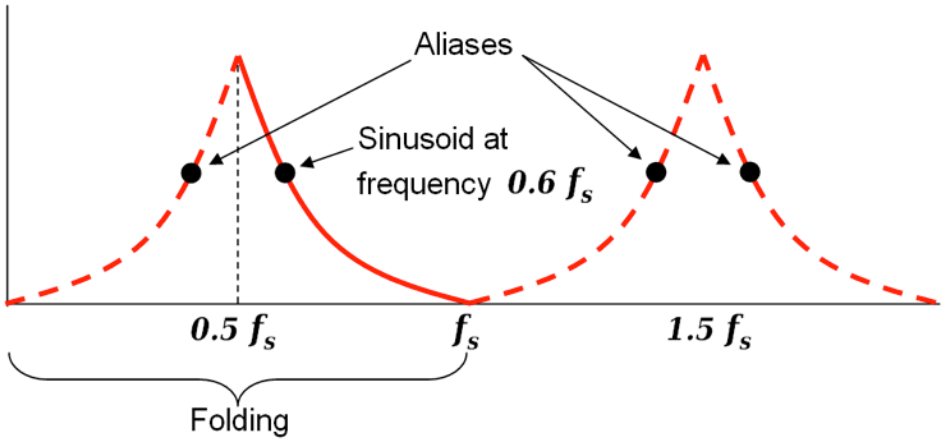
$f_{signal} > f_{sampling}/2$



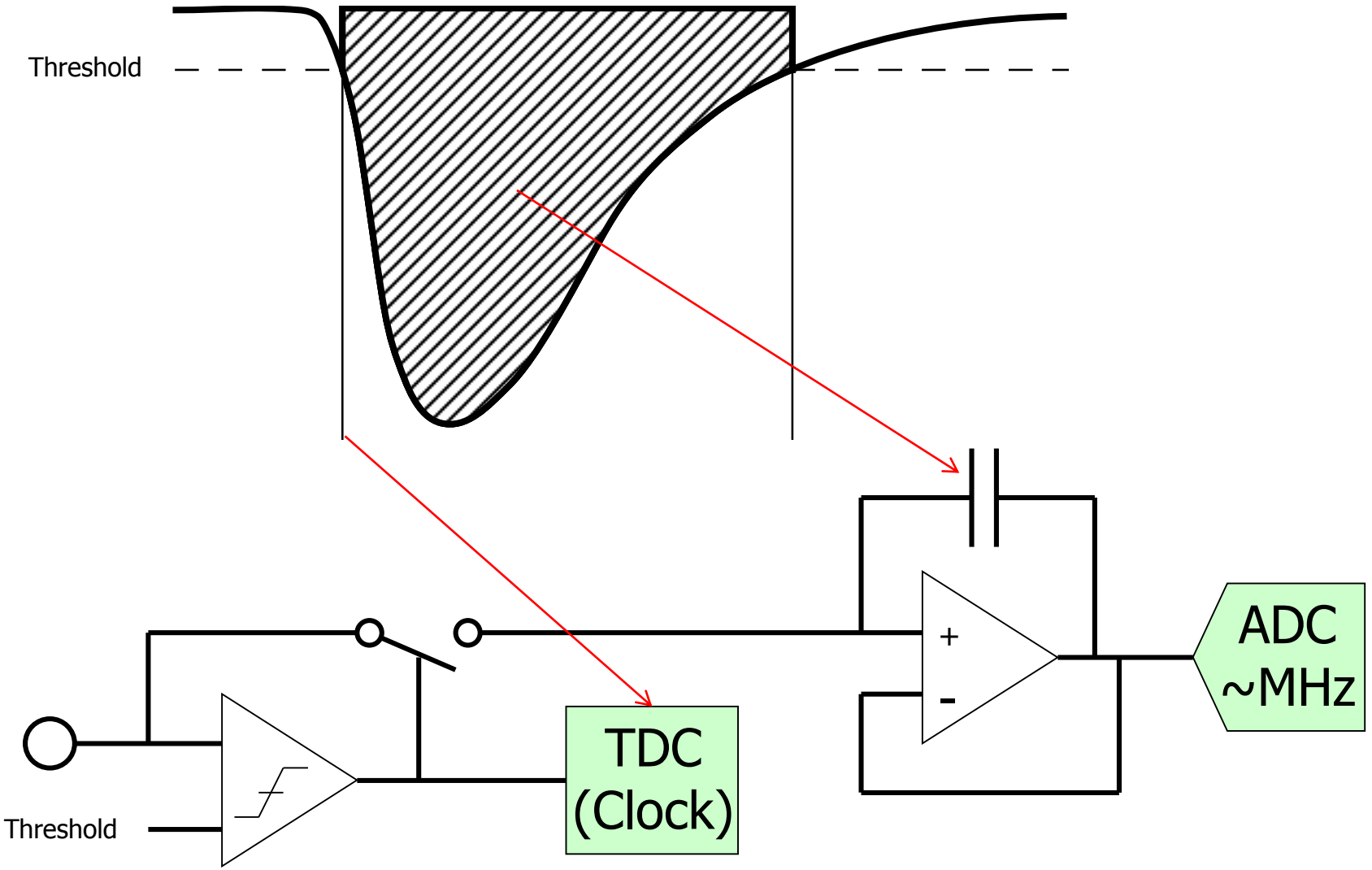
Limits of waveform digitizing

- Aliasing Occurs if $f_{signal} > 0.5 * f_{sampling}$
- Features of the signal can be lost ("pile-up")
- Measurement of time becomes hard
- ADC resolution limits energy measurement
- Need very fast high resolution ADC

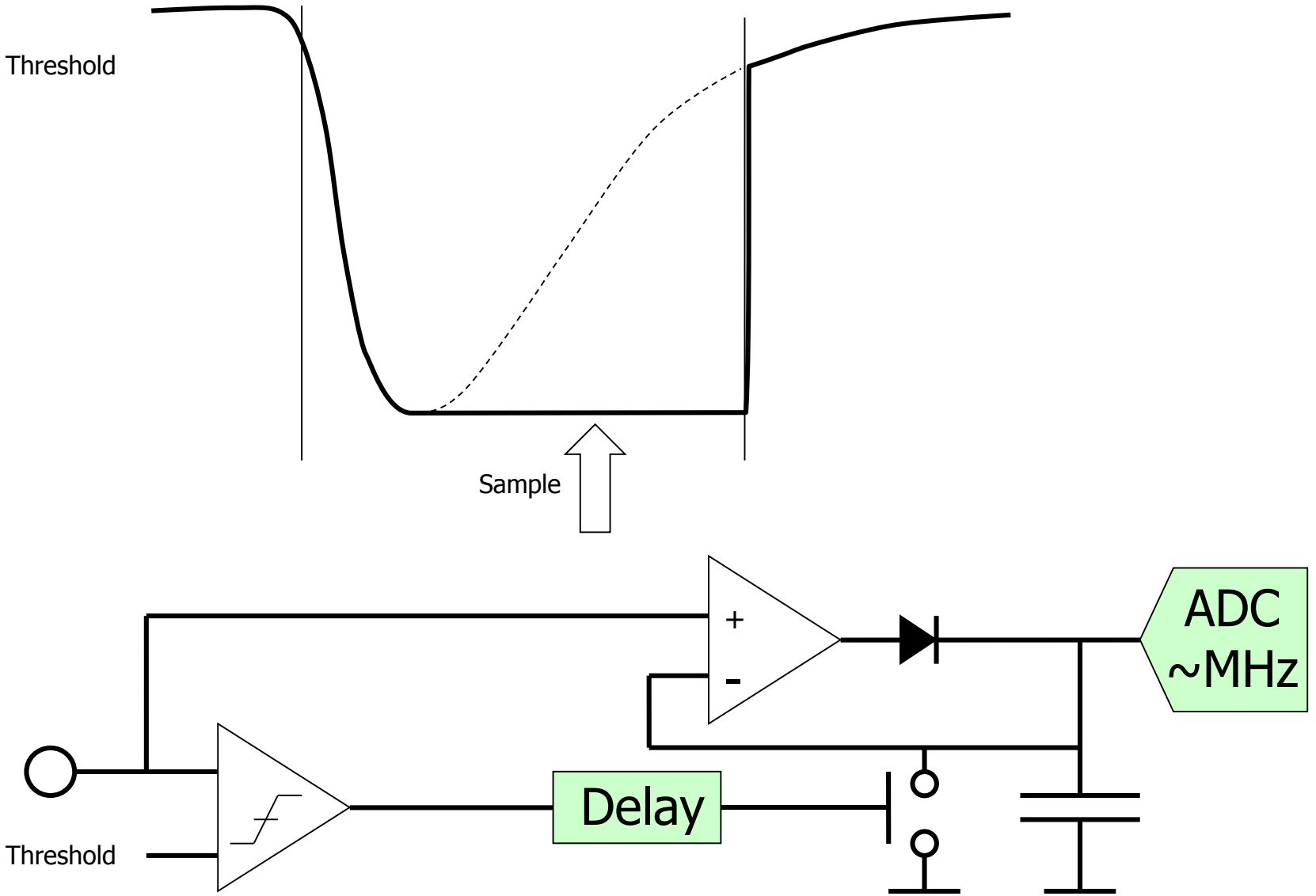




Charge ADCs (QADC)

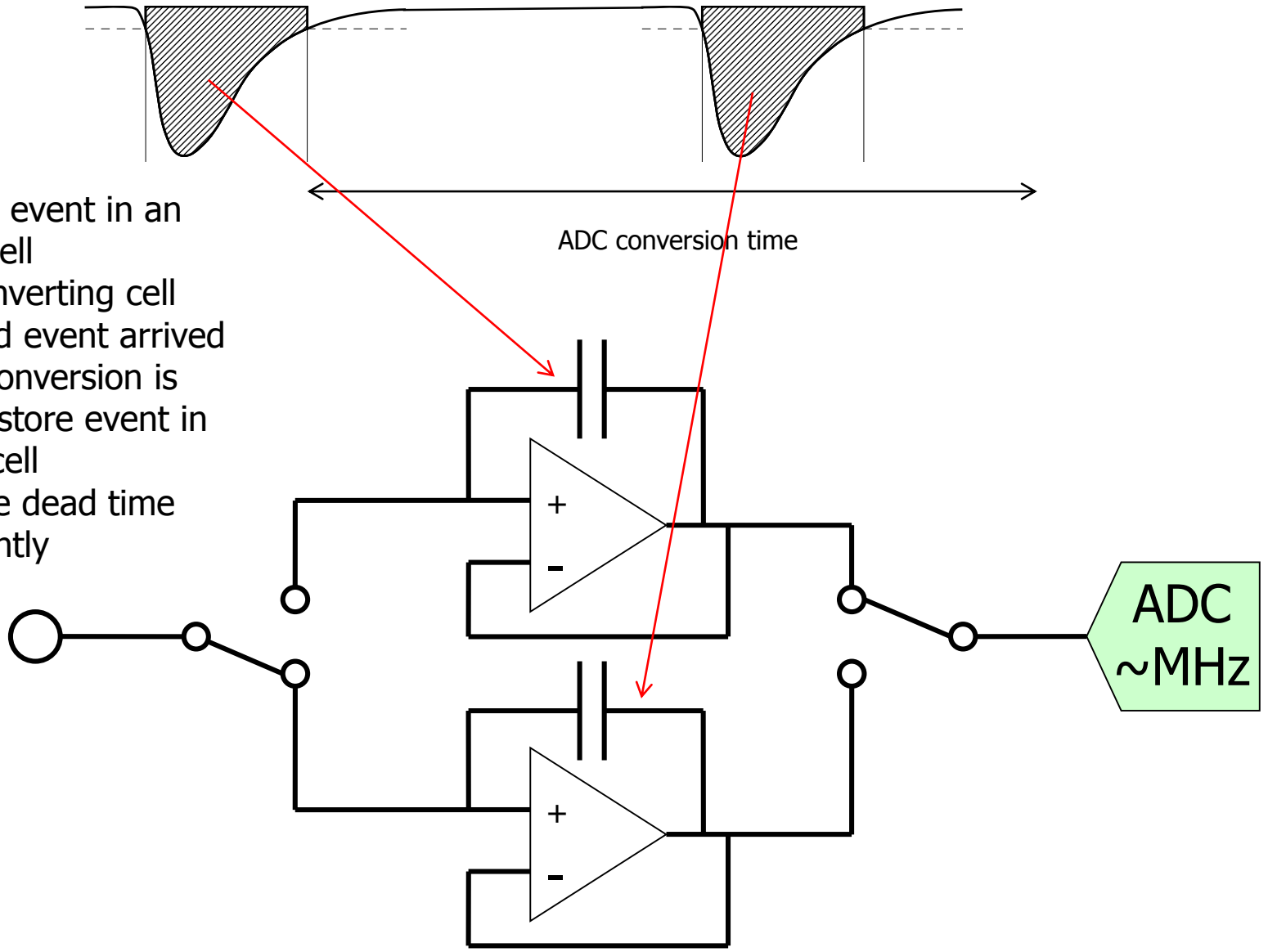


Peak sensing ADC

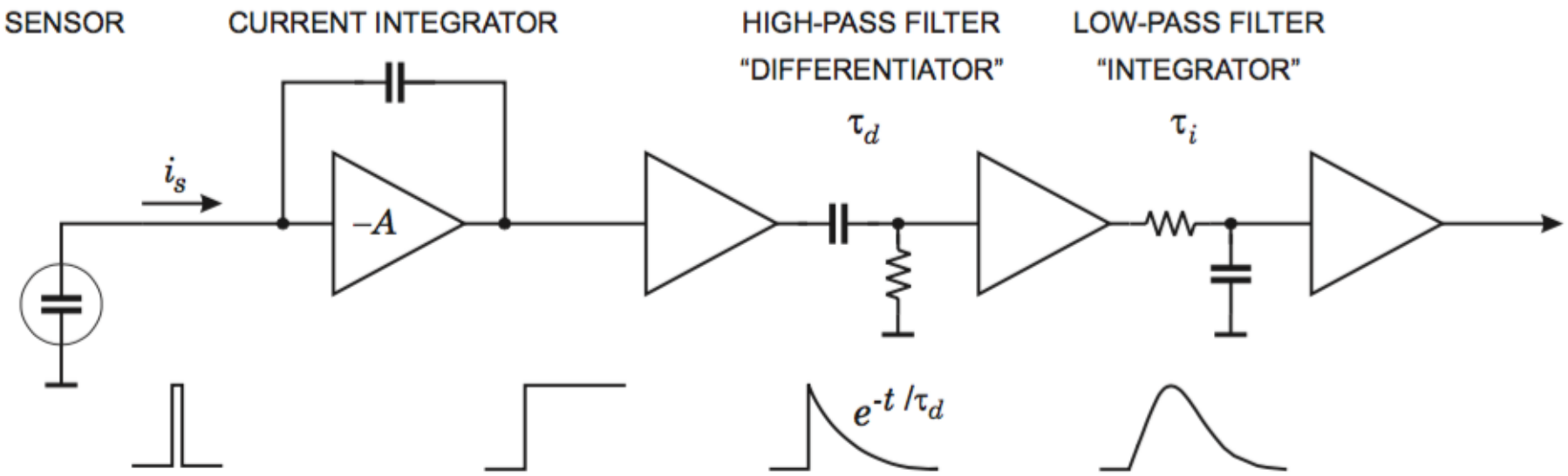


Double buffering

- Store an event in an analog cell
- Start converting cell
- If second event arrived before conversion is ready – store event in second cell
- Decrease dead time significantly

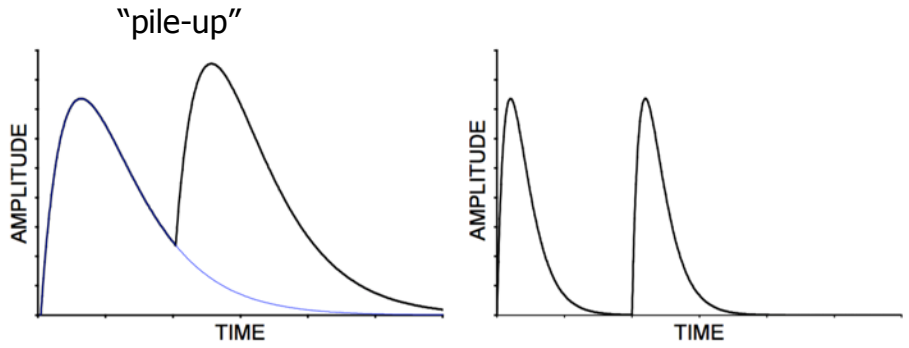


Analog readout chain

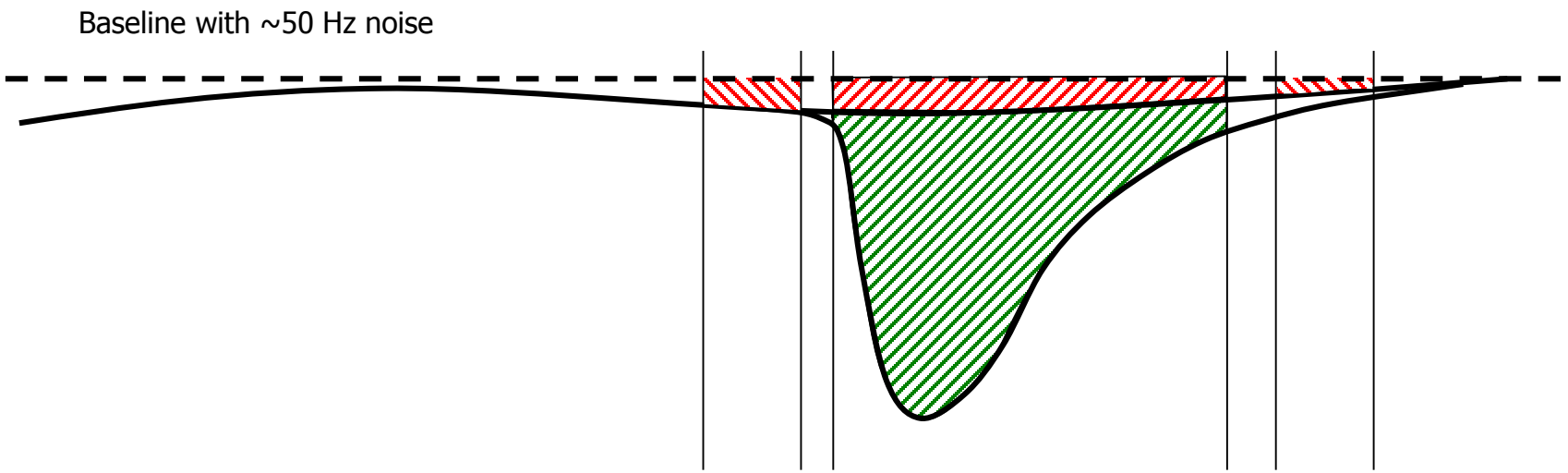


Optimal parameters can greatly improve the signal-to-noise ratio

Effect of slow shaping time:

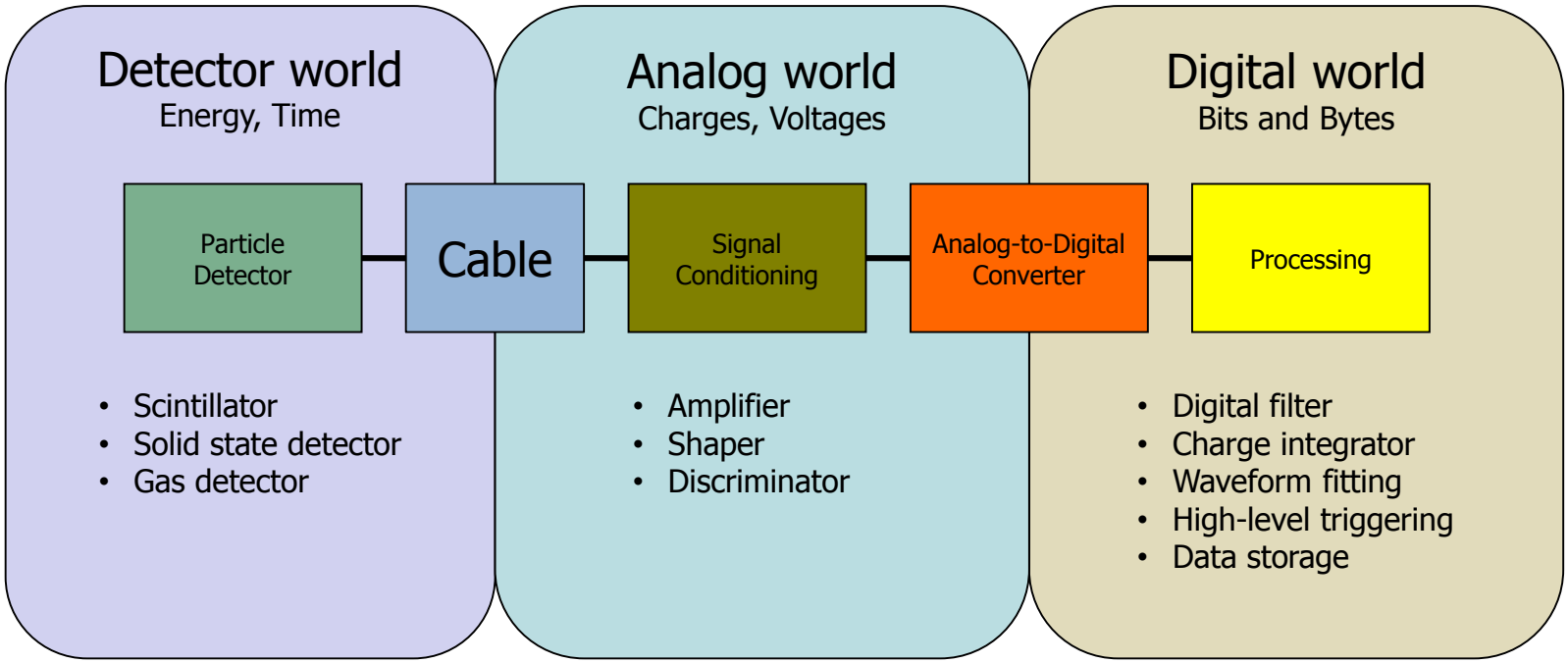


Baseline noise

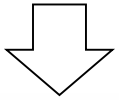


- Charge integration error due to signal "sitting" on fluctuating baseline (e.g. 50 Hz ground loop or artifact of shaper)
- Can be fixed by sampling baseline prior to signal (requires signal delay)
- Sample signal after peak for pile-up recognition

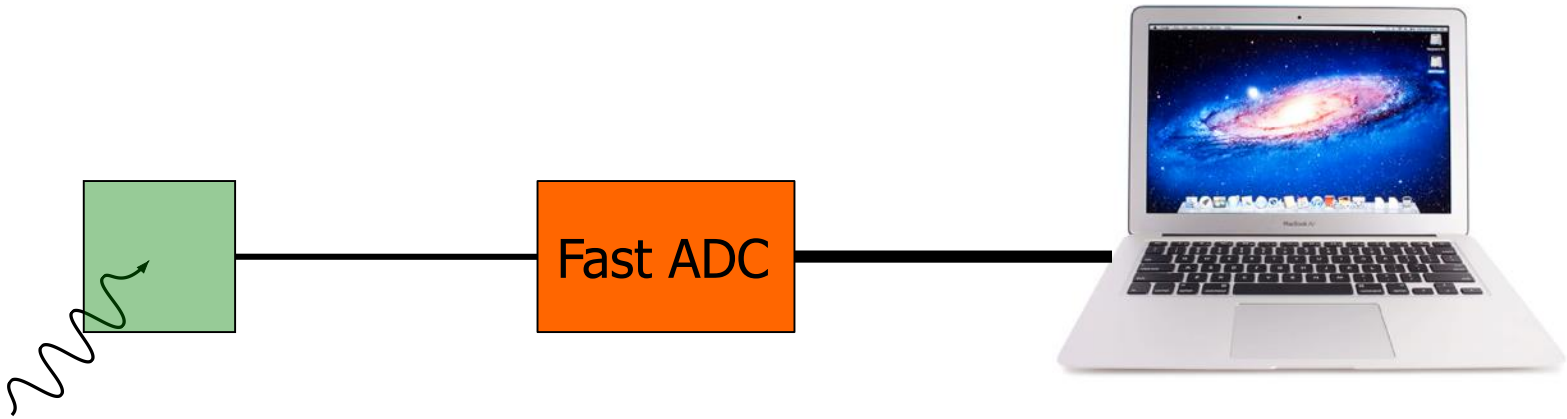
Conventional DAQ chain



Let's go a bit faster…



Ultimate sampling

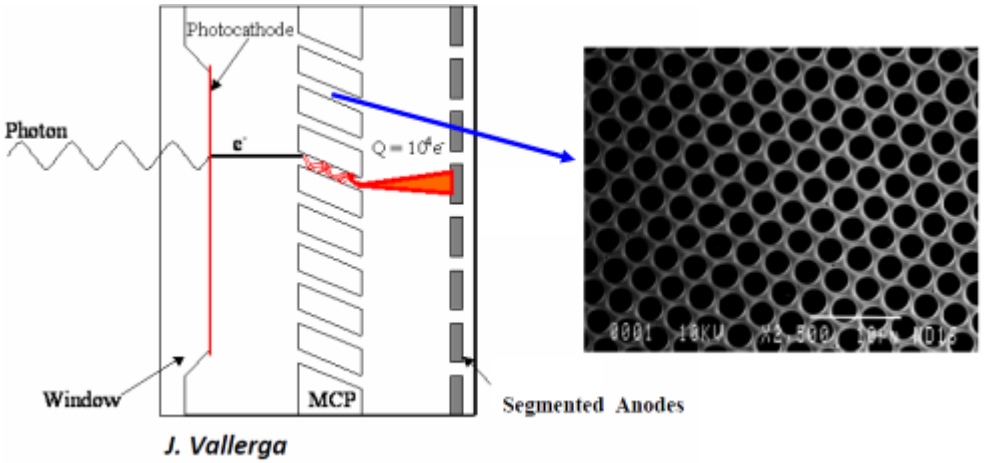


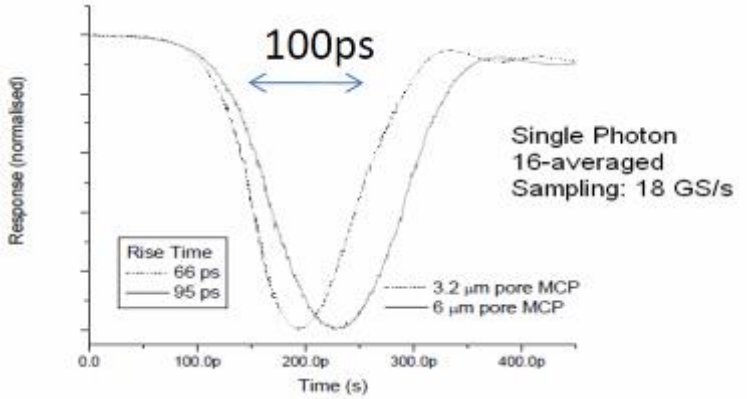
Direct fast sampling without shaping

- No shaping artifacts
- Less electronics
- All information if captured if $f_{sampling} > 2*f_{signal}$ and LSB < V_{noise}
- Any shaping circuitry can only *remove* information

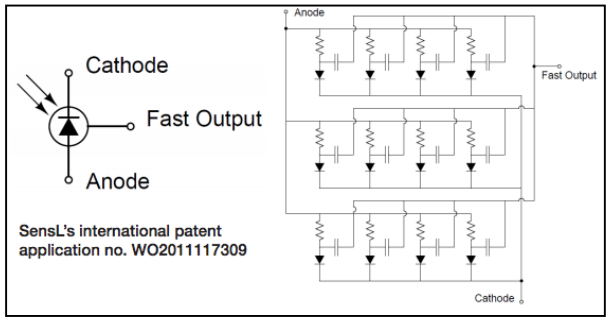
What are the fastest detectors?

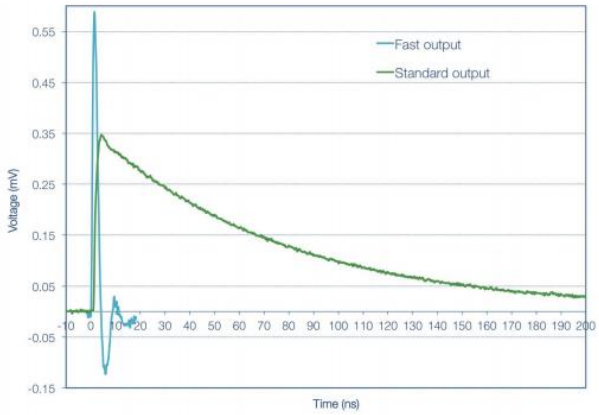
- Micro-Channel-Plates (MCP)
  - Photomultipliers with thousands of tiny channels (3-10 μm)
  - Typical gain of 10,000 per plate
  - Very fast rise time down to 70 ps
- 70 ps rise time → **4-5 GHz BW** → **10 GSPS**
- SiPMs (Silicon PMTs) are also getting < 100 ps





J. Milnes, J. Howoth, Photek

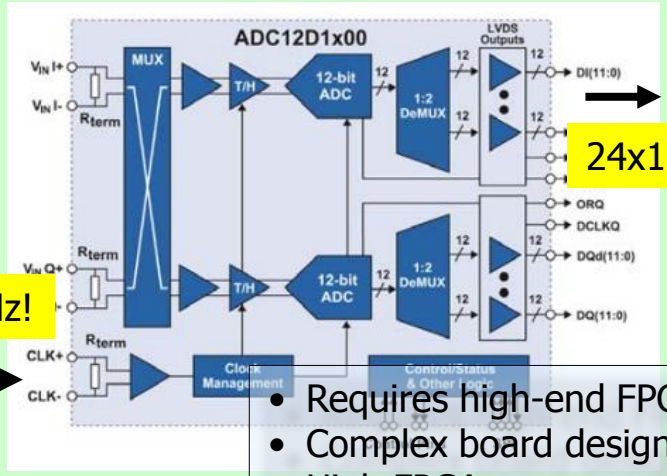




http://sensl.com

Can it be done with FADCs?

- 8 bits – 3 GS/s – 1.9 W → 24 Gbits/s
- 10 bits – 3 GS/s – 3.6 W → 30 Gbits/s
- 12 bits – 3.6 GS/s – 3.9 W → 43.2 Gbits/s
- 14 bits – 0.4 GS/s – 2.5 W → 5.6 Gbits/s



24x1.8 Gbits/s

1.8 GHz!

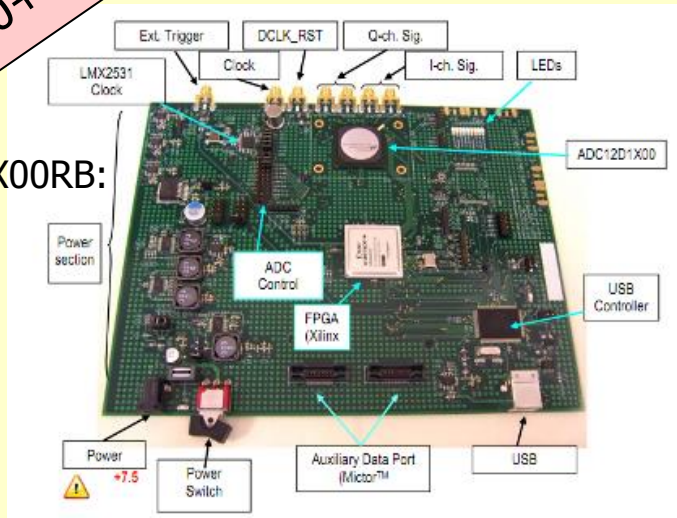
- Requires high-end FPGA
- Complex board design
- High FPGA power

1-10 k$ / channel
What about 1000+ Channels?

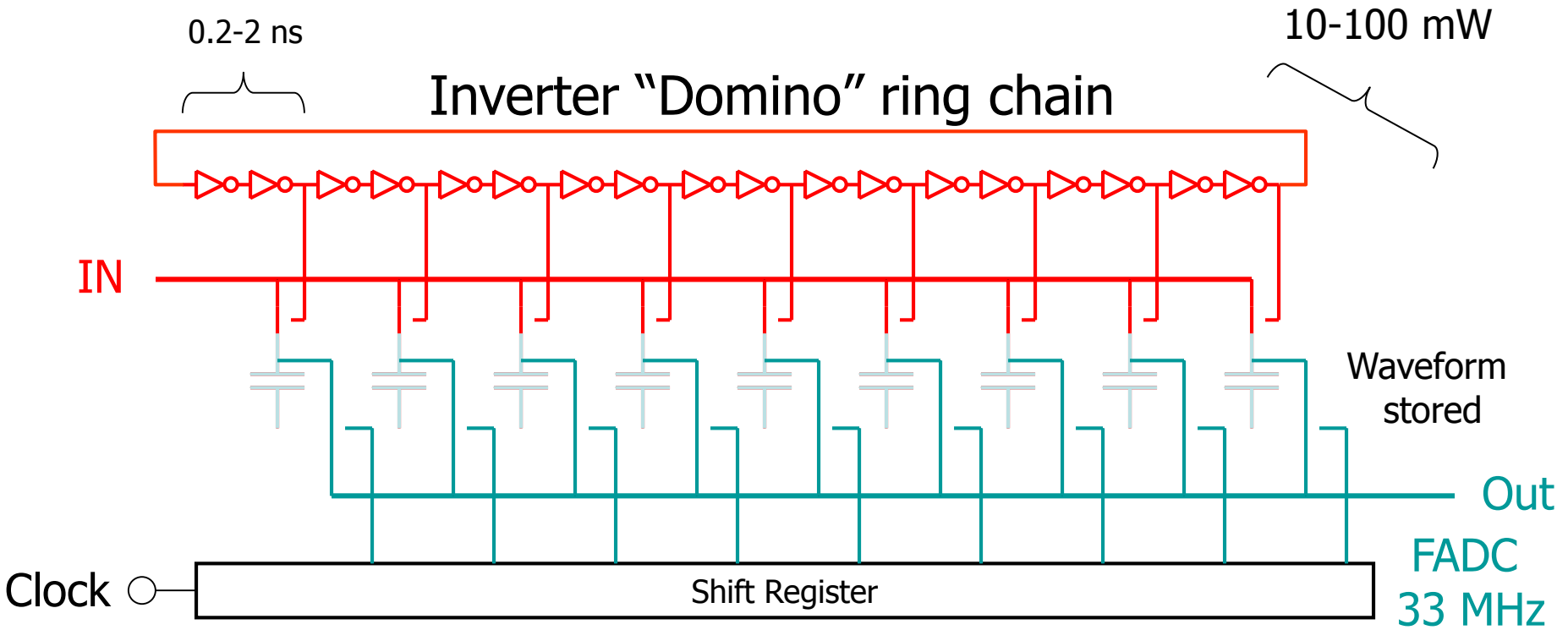
PX1500-4:
2 Channel
3 GS/s
8 bits

V1761: 2 Channels, 4 GS/s, 10 bits

ADC12D1X00RB:
1 Channel
1.8 GS/s
12 bits

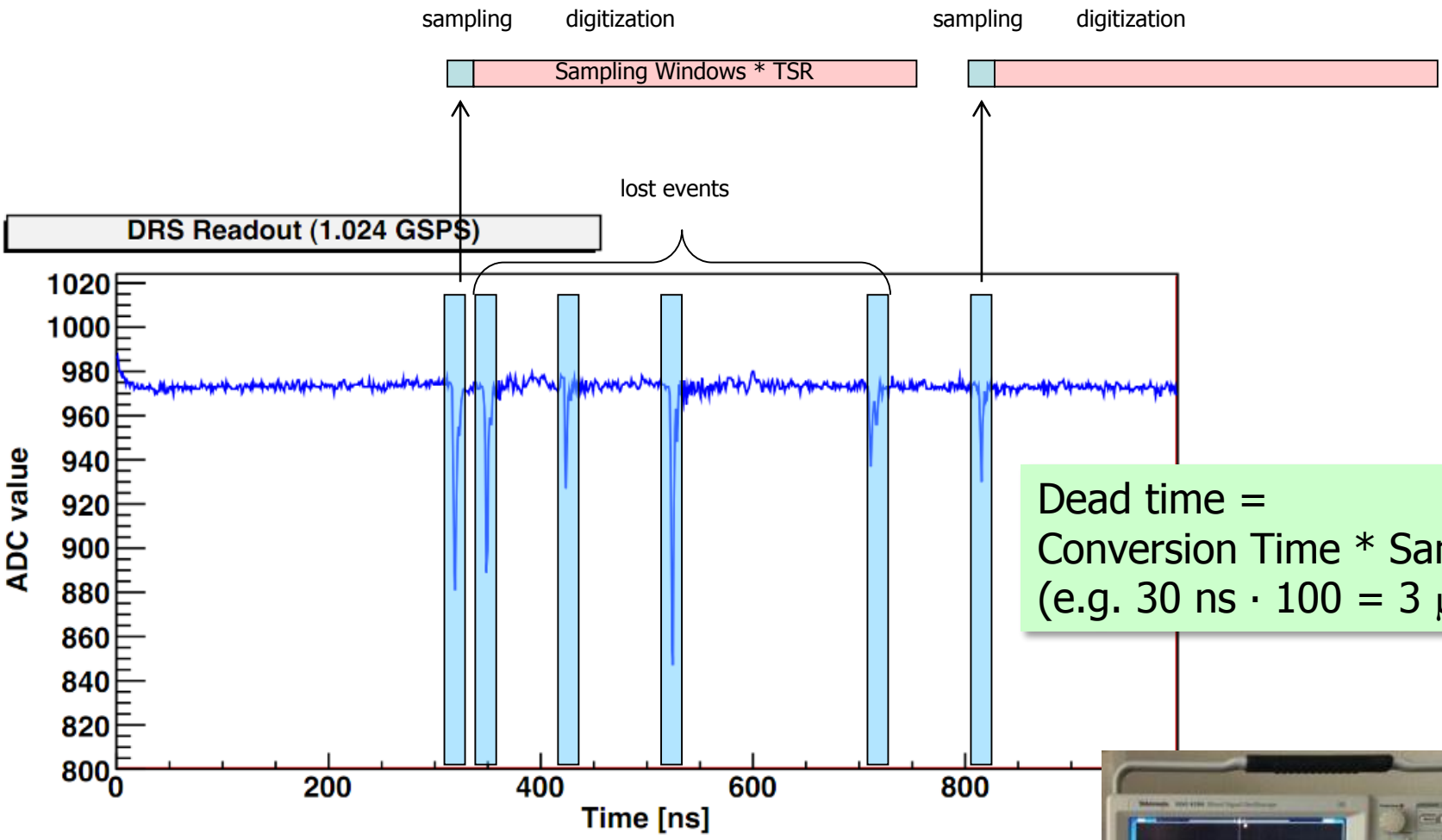


Switched Capacitor Array (Analog Memory)

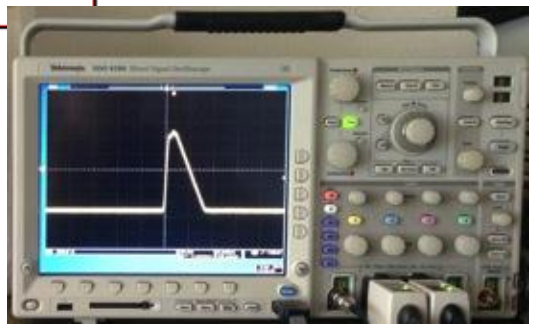


"Time stretcher" GHz → MHz

Triggered Operation



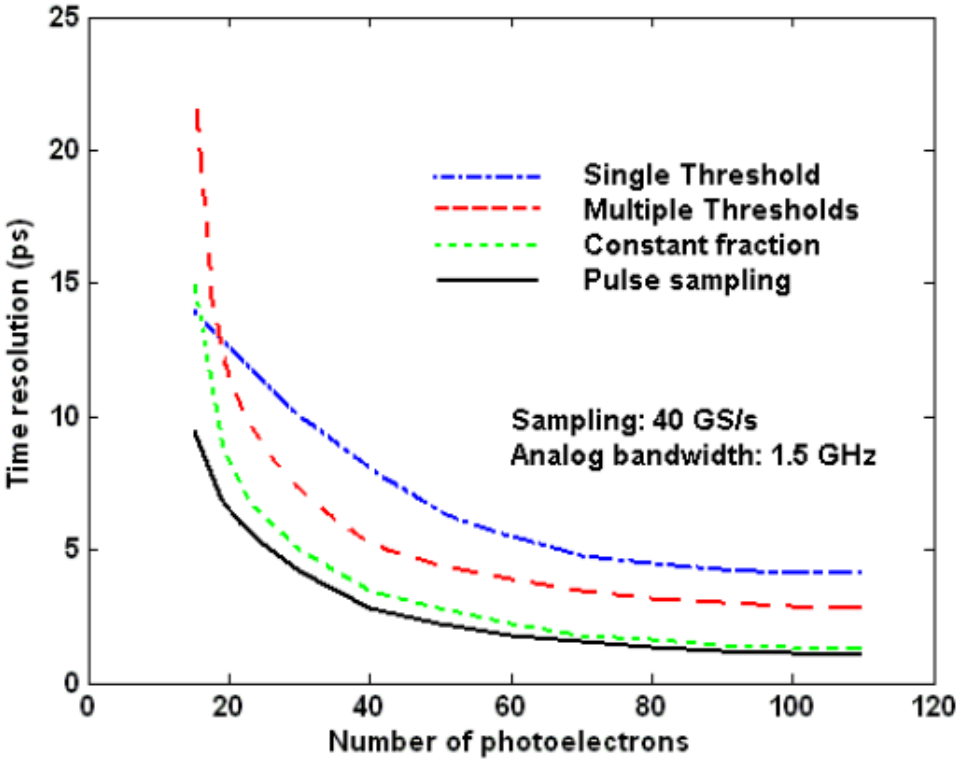
Dead time =
Conversion Time * Samples
(e.g. 30 ns · 100 = 3 μs)



Chips usually cannot sample during readout ⇒ "Dead Time"
Technique only works for "events" and "triggers"

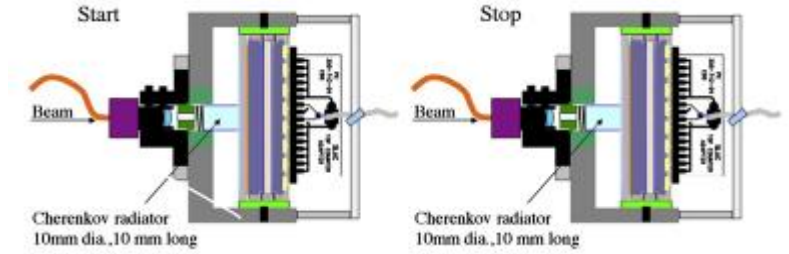
How to measure best timing?

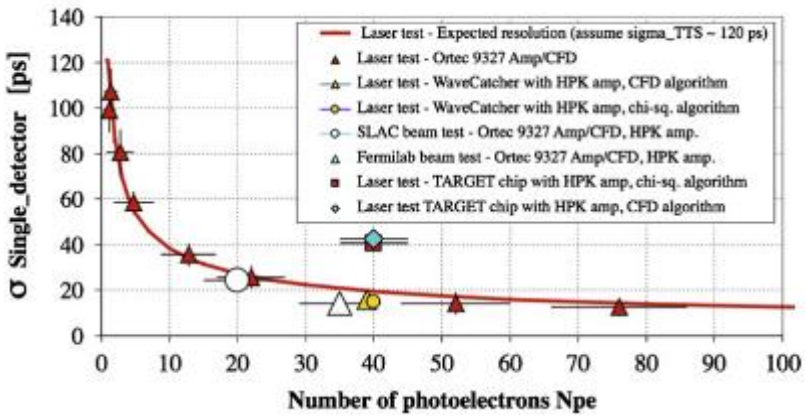
Simulation of MCP with realistic noise and different discriminators



J.-F. Genat et al., arXiv:0810.5590 (2008)

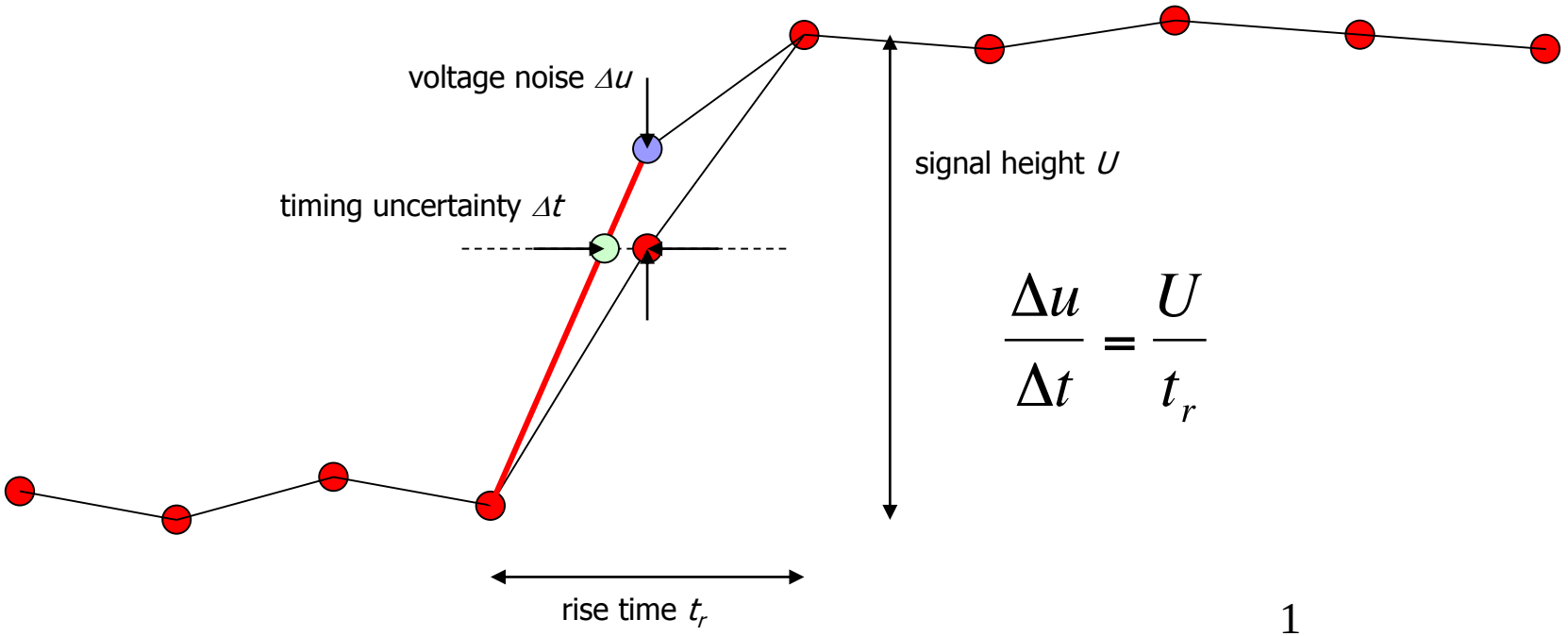
Beam measurement at SLAC & Fermilab





D. Breton et al., NIM **A629**, 123 (2011)

How is timing resolution affected?



$$\frac{\Delta u}{\Delta t} = \frac{U}{t_r}$$

$$t_r \approx \frac{1}{3 f_{3dB}}$$

$$\Delta t = \frac{\Delta u}{U} \cdot t_r = \frac{\Delta u}{U\sqrt{n}} \cdot t_r = \frac{\Delta u}{U} \cdot \frac{t_r}{\sqrt{t_r \cdot f_s}} = \frac{\Delta u}{U} \cdot \frac{\sqrt{t_r}}{\sqrt{f_s}} = \frac{\Delta u}{U} \cdot \frac{1}{\sqrt{3 f_s \cdot f_{3dB}}}$$

number of samples on slope

Simplified estimation!

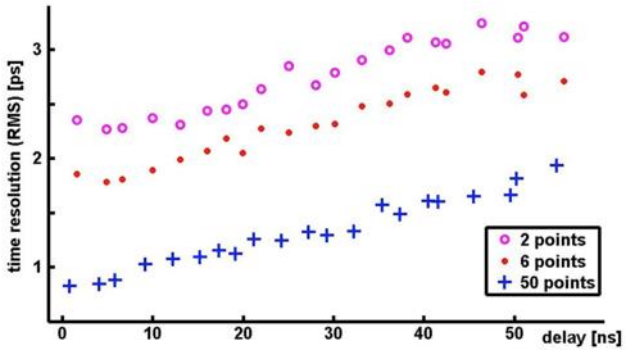
How is timing resolution affected?

$$\Delta t = \frac{\Delta u}{U} \cdot \frac{1}{\sqrt{3 f_s \cdot f_{3dB}}}$$

Assumes ideal sampling

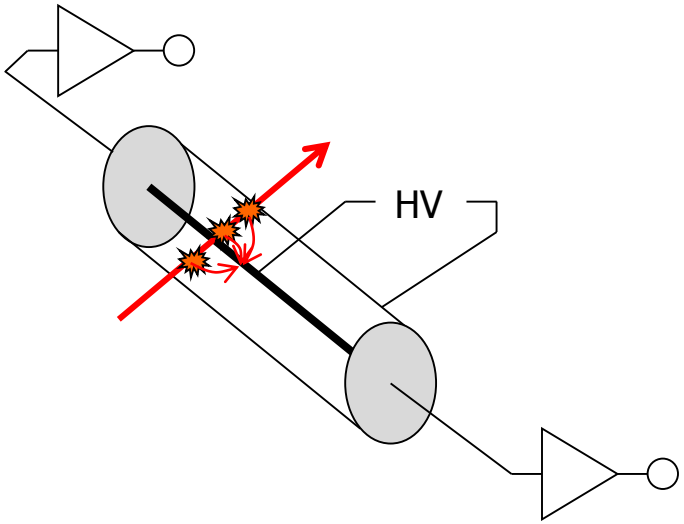
↓

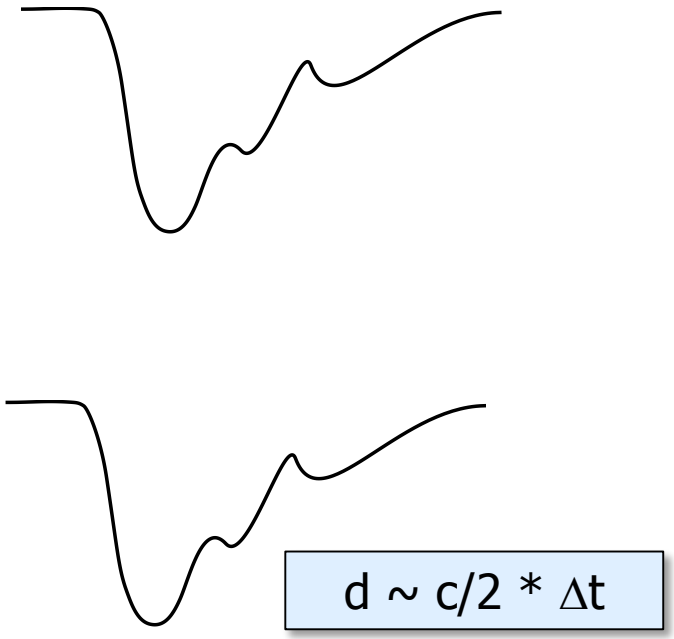
	U	Δu	f_s	f_{3db}	Δt
today:	100 mV	1 mV	2 GSPS	300 MHz	~10 ps
optimized SNR:	1 V	1 mV	2 GSPS	300 MHz	1 ps
next generation:	1 V	1 mV	10 GSPS	3 GHz	0.1 ps



"Novel Calibration Method for Switched Capacitor Arrays Enables Time Measurements width Sub-Picosecond Resolution", D.A. Stricker-Shaver, S. Ritt, B.J. Pichler, IEEE **TNS 61** (2014), 3607

Readout of Straw Tubes





$d \sim c/2 * \Delta t$

- Readout of straw tubes or drift chambers usually with "charge sharing": 1-2 cm resolution
- Readout with fast timing: 10 ps / √10 = 3 ps → 0.5 mm
- Currently ongoing research project at PSI

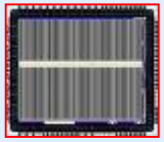
Switched Capacitor Arrays for Particle Physics

G. Varner, Univ. of Hawaii

E. Delagnes
D. Breton
CEA Saclay

H. Frisch et al., Univ. Chicago

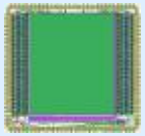
STRAW3 LABRADOR3 TARGET


- 0.25 μm TSMC
- Many chips for different projects (Belle, Anita, IceCube …)

www.phys.hawaii.edu/~idlab/

AFTER SAM NECTAR0



- 0.35 μm AMS
- T2K TPC, Antares, Hess2, CTA

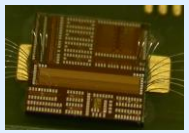
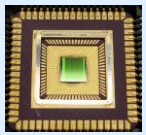
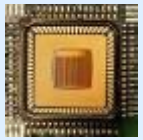
matacq.free.fr

PSEC1 - PSEC4

- 0.13 μm IBM
- Large Area Picosecond Photo-Detectors Project (LAPPD)

psec.uchicago.edu

DRS1 DRS2 DRS3 DRS4


2002 2004 2007 2008

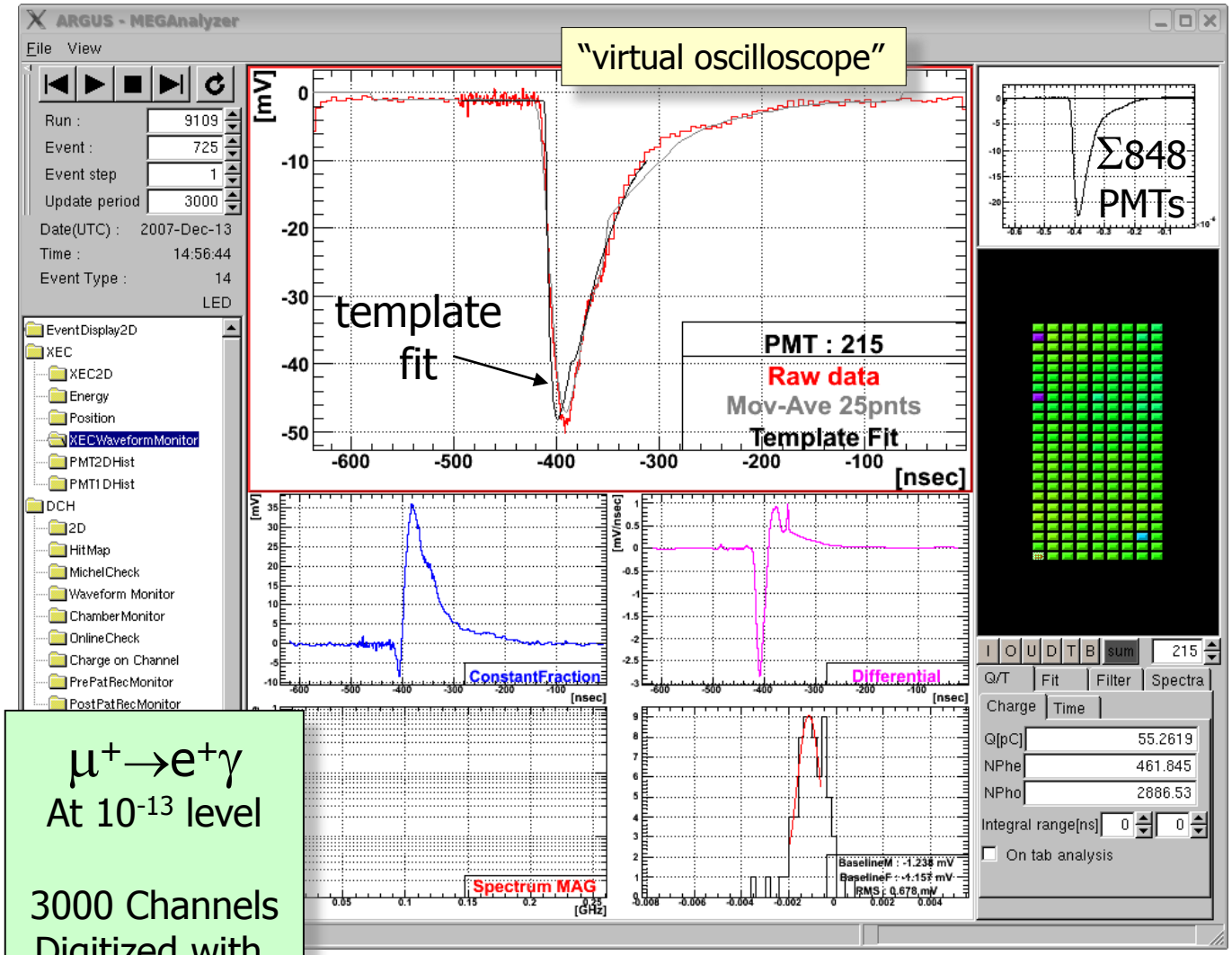
- 0.25 μm UMC
- Universal chip for many applications
- MEG experiment, MAGIC, Veritas, TOF-PET

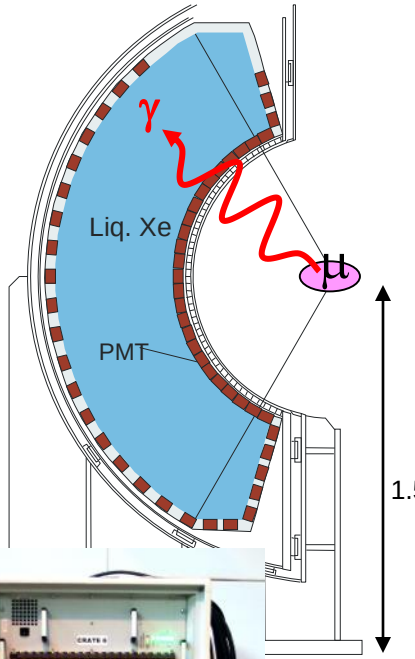
Poster 15, 106

SR
R. Dinapoli
PSI, Switzerland

drs.web.psi.ch

MEG On-line waveform display



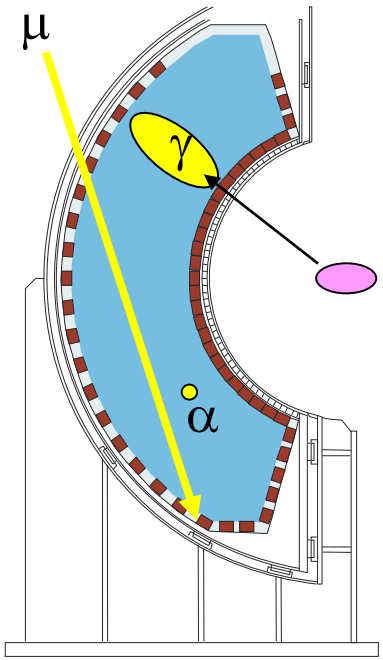


$\mu^+ \rightarrow e^+\gamma$
At 10^{-13} level

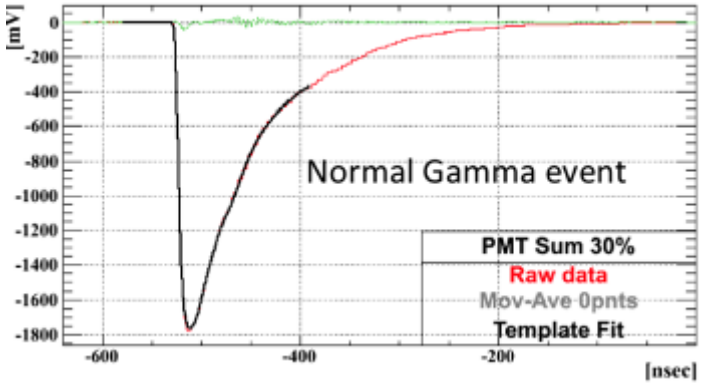
3000 Channels Digitized with **DRS4 chips** at 1.6 GSPS

Drawback: 400 TB data/year

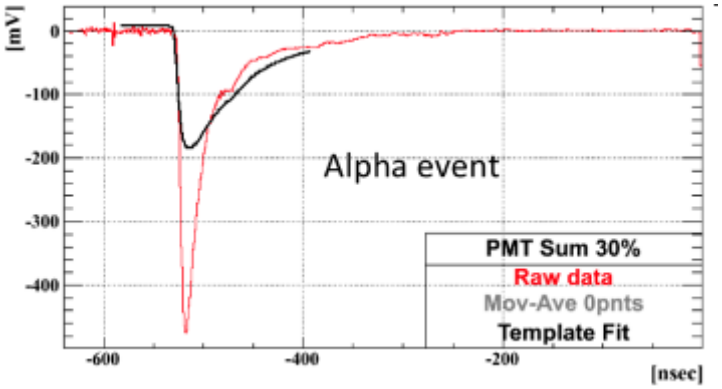
Pulse shape discrimination



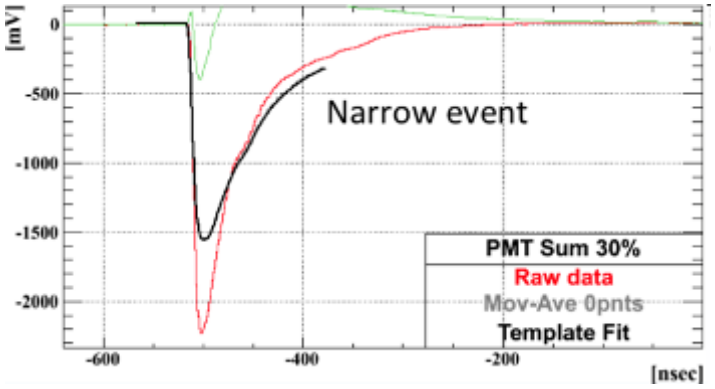
γ



α

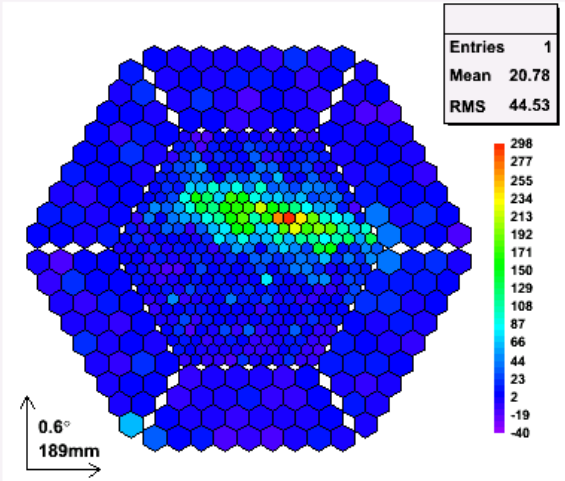


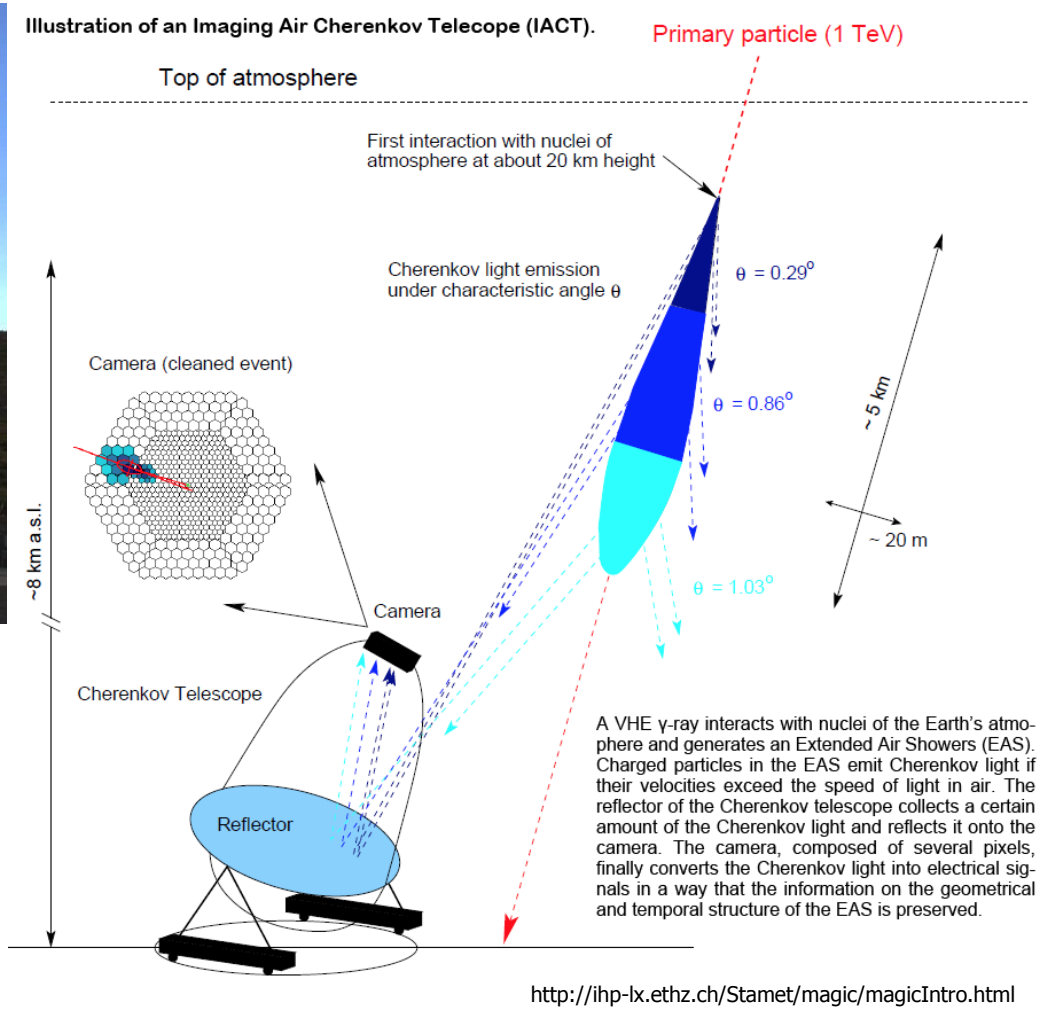
μ



Events found and correctly processed 2 years (!) after the were acquired

MAGIC Telescope





http://ihp-lx.ethz.ch/Stamet/magic/magicIntro.html

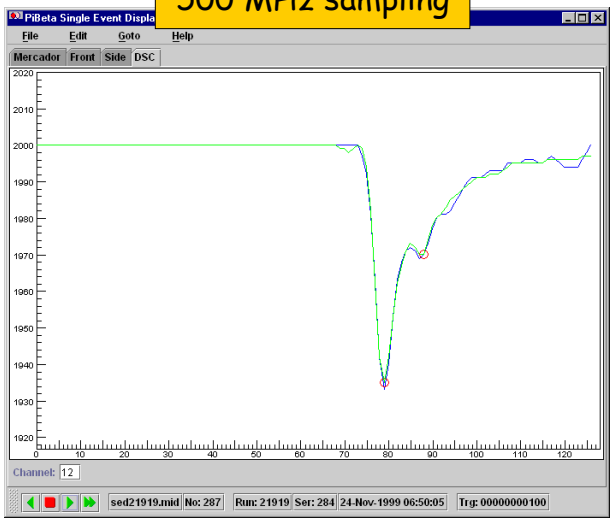
La Palma, Canary Islands, Spain, 2200 m above sea level

https://wwwmagic.mpp.mpg.de/

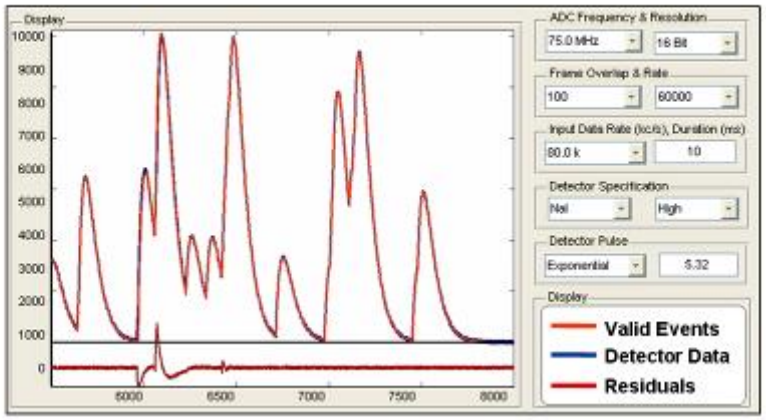
Template Fit

- Determine "standard" PMT pulse by averaging over many events → "Template"
  - Find hit in waveform
  - Shift ("TDC") and scale ("ADC") template to hit
  - Minimize χ^2
  - Compare fit with waveform
  - Repeat if above threshold
- Store ADC & TDC values

πβ Experiment
500 MHz sampling



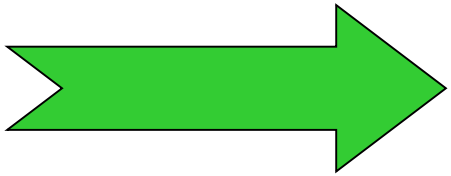
- At 1,000 kc/s less than 10% of events cannot be decoded.



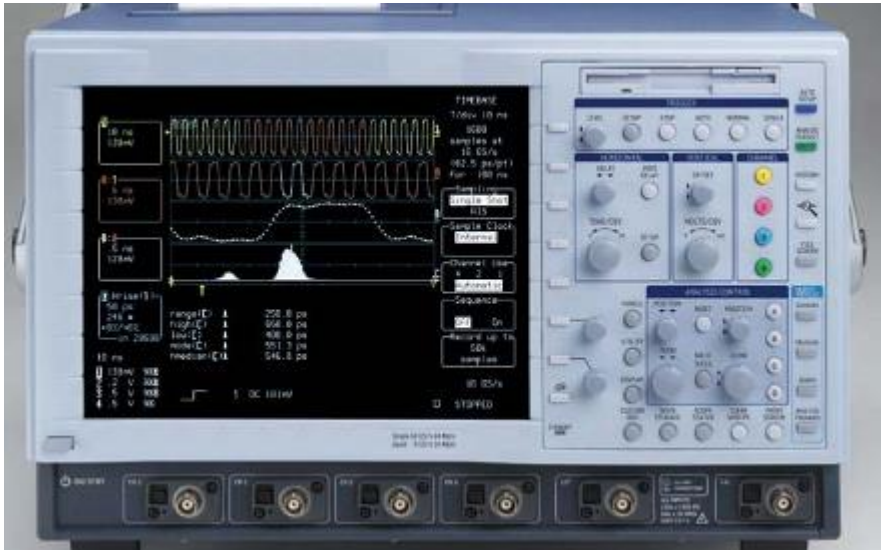
14 bit
60 MHz

High speed USB oscilloscope

4 channels
5 GSPS
1 GHz BW
8 bit (6-7)
15 k€



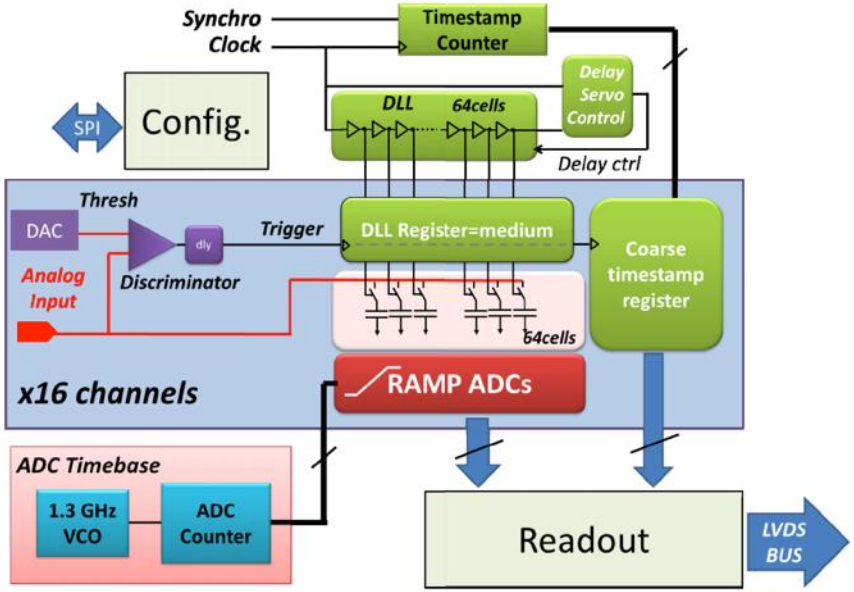
4 channels
5 GSPS
1 GHz BW
11.5 bits
1170 €
USB Power



New chips

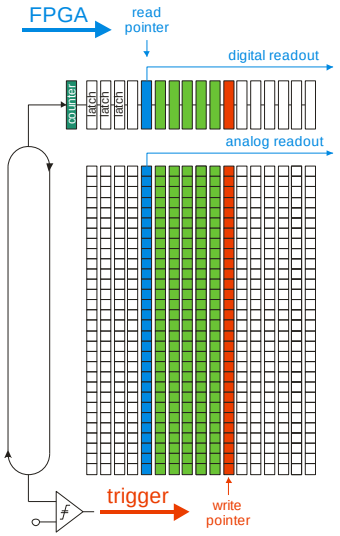
CEA/Saclay

- SAMPIC Waveform TDC
- Record short (64 bins) waveforms
- Digitize on-chip
- Data-driven read out



DRS5 (PSI, planned)

- Self-trigger writing of 128 short 32-bin segments (4096 bins total)
- Storage of 128 events
  - Accommodate long trigger latencies
  - Quasi dead time-free up to a few MHz,
  - Possibility to skip segments
    → second level trigger



Summary

- Digitization is a key element of all particle physics experiments
- General trend to faster digitization and waveform analysis in digital domain (embedded CPUs, FPGAs)
- This talk can only give you a glimpse
- Further information
  - H. Spieler, "Semiconductor Detector Systems", Oxford Univ. Press, 2005
  - G. Knoll, "Radiation Detection and Measurement", Wiley, 2010
  - Conferences (with short courses):
    IEEE NSS-MIC (Strasbourg, France, Nov. 2016)
    IEEE Realtime (Williamsburg, VA, June 2018)
  - Become IEEE NPSS member

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- Radiation Effects (Nuclear and Space Radiation Effects Conference)
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IEEE Transactions on Nuclear Science

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