# Mitigation of SPS timing synchronization issues

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# Outline

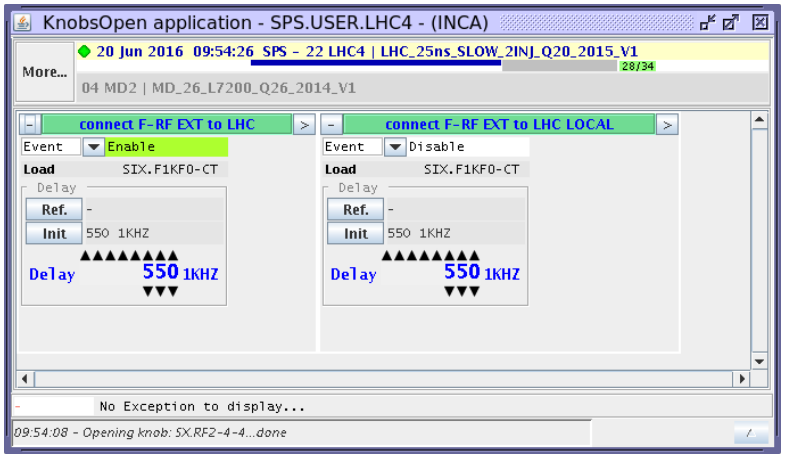
- Introduction & motivation
- Mitigations being implemented
- Conclusion

# Introduction

- Synchronisation of extraction SPS->LHC requires reference clocks from LHC to SPS Faraday cage.
- For setting-up while LHC is not at injection, local clocks are generated in the FC.
- Switching between LHC/local clocks is controlled by enabling/disabling the relevant LTIM timings.
- On the 5$^{th}$ of May, a single nominal bunch was sent on the TDI because the SPS frequency was locked on the local frequency instead of the LHC.
- A number of mitigations have been/are being put in place to avoid this occurring in the future:
  - Improved LHC injection sequencer checks
  - Modifications to the SPS LHC/Local Clock Selection application
  - Hardware checks of clock selection in the SPS Faraday Cage

# Injection sequencer checks

- Before allowing the injection request, the injection sequencer checks that the SPS frequency is locked on the LHC frequency.



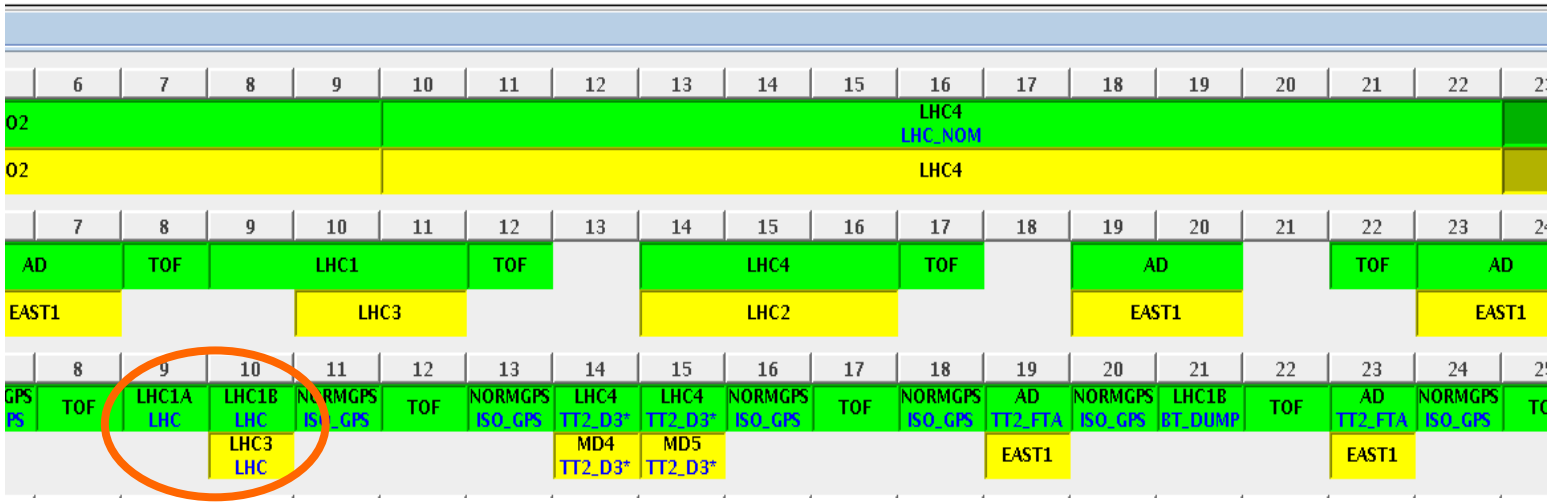

2 RF local timings are checked.
Their values are user dependent.

- When the check was implemented, it was only possible to have one user tagged TO_LHC programmed in the SPS supercycle.
- Therefore, the code only checked the first cycle tagged TO_LHC found in the supercycle.

D. Jacquet

# Injection sequencer checks

- In the CBCM, introduction of the NOMINAL tag that allows to have 2 LHC cycles in the same supercycle, with any users.
- Injection sequencer check not adapted: only one user was checked.
- Nominal and the 12 bunches cycles have the same user, and most of the time programmed  in the same supercycle. This configuration was still safe.




D. Jacquet

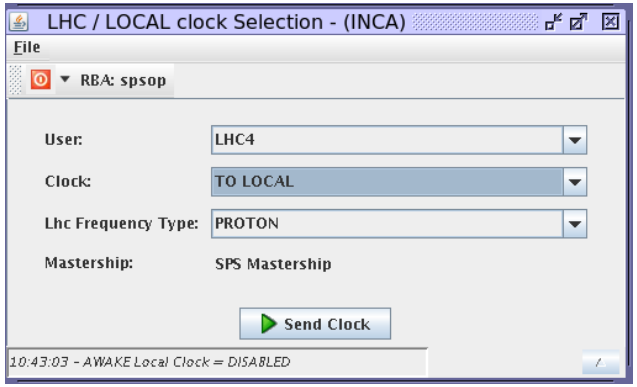
# Injection sequencer checks

- On the 5th of May, a single nominal bunch was sent on the TDI because the SPS frequency was locked on the local frequency instead of the LHC.
- The INDIV cycle is most of the time programmed with the pilot, and only the frequency for the pilot user was checked.

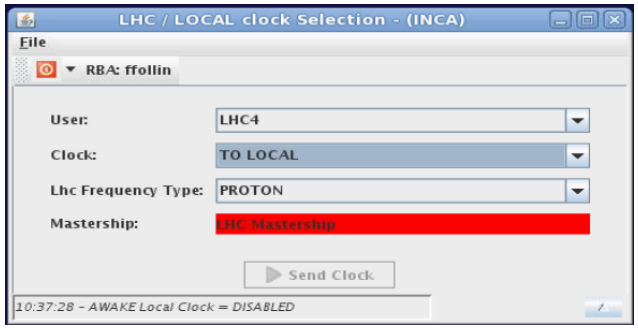

- The code has been updated, now all the users tagged TO_LHC in the supercycle are checked by the injection sequencer, and the injection is prevented if one of them is not correct.

D. Jacquet

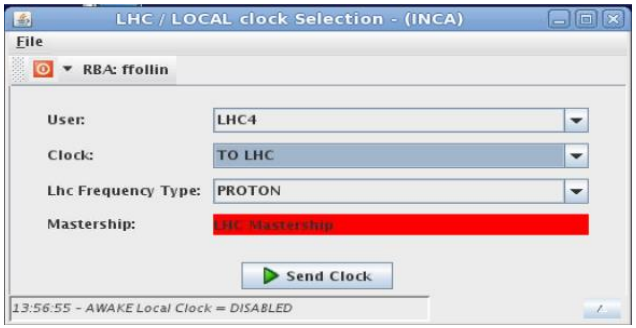
# SPS Clock Selection application




If SPS has the Mastership, switch to the LOCAL clock is allowed




**If LHC has the Mastership, switch to the LOCAL clock is not allowed**



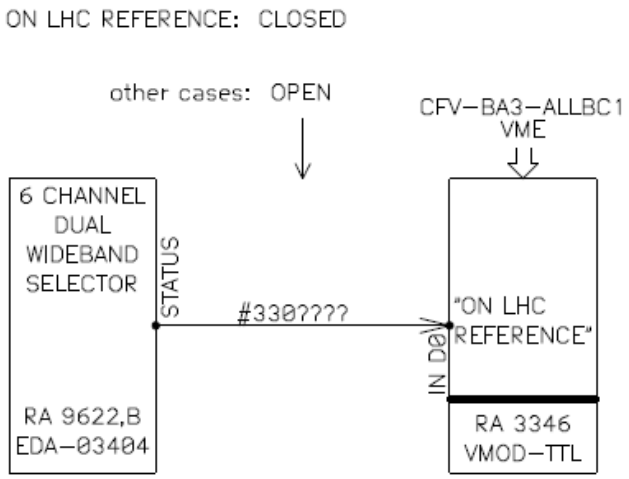

Switch  to the TO LHC clock is always allowed

F. Follin

# Faraday Cage HW checks

- Currently being implemented: checks of HW status of clock selector using dedicated FESA class

Local/LHC clock selector



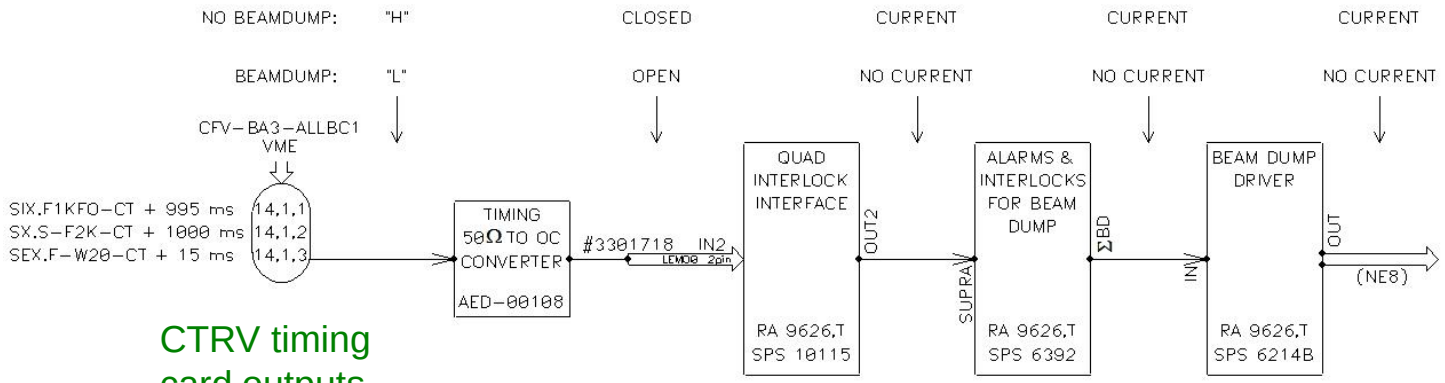

Read in VME crate by FESA class via VMOD-TTL interface

HW module being modified to allow reading of switch status

U. Wehrle, A. Pashnin, N. Stapley

# Faraday Cage HW checks

- 3 checks during cycle: before injection, at start of ramp, before extraction
- At each check, a timing is started which will fire the beam dump unless disabled




CTRV timing card outputs

Beam dump interface

- FESA class checks clock status and the dynamic destination and disables timing except when

  (NOT on LHC reference) AND (DDEST == LHC1_TI2 or LHC2_TI8)

- "Fail-safe" in case of FESA class failure
- Similar mechanism already used by BQM

U. Wehrle, A. Pashnin, N. Stapley

# Conclusion

- The code in the LHC injection sequencer to check the remote/local clock switching timings has been updated to allow multiple TO_LHC tagged cycles
- The LHC/Local clock selection panel has been modified to disallow switching to Local when LHC has mastership
- Hardware to detect the clock switching status and a pre-emptive dump trigger mechanism similar to that used by the BQM is being prepared for the SPS Faraday cage