Development of Tracking and Timing Detectors

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Outline

- FCC - hh tracking environment (highest demands)

- Current status and advances in Si detectors (focus “pixels”)
  - Radiation -> radiation hard sensors and chips
  - Current “Large System” layouts
  - Hybrid Modules: Pros&Cons

- Depleted CMOS pixels

- Timing with silicon pad/pixel detectors
The environment: FCC versus LHC and HL-LHC

- “today” ... HL-LHC trackers of ATLAS and CMS
- FCC - Radiation ... fluence = $6 \times 10^{17} \text{n}_{eq} \text{cm}^{-2}$; TID $\approx 0.4$ GGy
  - LHC = 1
  - HL-LHC $\times 20$
  - FCC $\times 600 = 30 \times$ HL-LHC
- Demands ...
  - highest hit-rate capability
  - highest radiation tolerance
  - not much more power
  - larger area (esp. pixels) -> cheaper price tag

~200 m² silicon (strips & pixels)

- peak and integrated: L $\rightarrow$ 10 $\times$ HL-LHC
- charged particle rates
  - @ r=2.5 cm (pix): 20 GHz/cm²
    $\approx 20 \times$ HL-LHC
  - @ forward: up to 100 GHz/cm²

N. Wermes, FCC-2017 Berlin, 6/2017
Demands on good tracking

- Pattern recognition and identification of particle tracks at large background and pile-up levels
- Measurement of primary and secondary vertices
- Multi-track separation and vertex-ID in the core of (boosted) jets
- Momentum measurement
- Measurement of specific ionization.

**note**

✧ Vertex and $p_T$ resolutions only improve with $1/\sqrt{N_{\text{layers}}}$ while material increases with $N_{\text{layers}}$

✧ Philosophy change: from “Hits become tracks”
  -> “cluster orientations contain tracklet information”
Radiation

- FCC fluence => every Si lattice cell sees about 1500 particles

- From defect investigation -> defect engineering (example: oxygen enrichment) make VO to happen more likely than VP

Recipe

- Readout at n⁺ electrodes (e⁻ collection)
- Operate at high bias voltages
- Carefully plan the annealing scenario
- Provide proper electrode design and guard rings
- Use p-substrates (rather than n)
Huge progress in understanding radiated Si-sensors

Most defects show linear fluence dependence. Cooling helps to keep \( I_{\text{leak}} \) and reverse annealing smaller. \( N_{\text{eff}} \) changes

Most studies with n-type material


E(30K)

V

E4-

E5-

BD= bistable donor (e-trap)

positive space charge

strongly produced in oxygen rich DOFZ material

V2O complex (?)

negative space charge

causes leakage current, strongly produced in oxygen lean STFZ

extended acceptor defects produced equally by n,p

negative space charge

-> reverse annealing

 triple vacancy, small cluster

negative space charge

-> high leakage current

V2O complex (?)

negative space charge

causes leakage current, strongly produced in oxygen lean STFZ

extended acceptor defects produced equally by n,p

negative space charge

-> reverse annealing

most defects show linear fluence dependence

cooling helps to keep \( I_{\text{leak}} \) and reverse annealing smaller

\( N_{\text{eff}} \) changes

Radiation hard Si sensors -> (thin) planar pixel sensors

- thin $n^+$ in $p$ sensors after high fluences (neutrons)

- 6000 – 7000 e-
  for 100 - 200 µm sensors @ 300 V – 600 V bias

- hit efficiencies still reasonable at $\Phi > 10^{16}$

Terzo, Andricek, Macchiolo, Nisius et al, JINST 9 (2014) C05023
Radiation hard Si sensors -> 3D-Si sensors

- particle path (signal) different from drift path
- high field w/ low voltage

- radiation tolerance
- Q still 50% @ 10^{16} cm^{-2}

- slightly larger $C_{in}$ (noise)
- now also in diamond, CdTe

Development for HL-LHC:
- thin (100 µm)
- 6” wafers
- electrodes thin (5µm) & narrowly spaced
- slim or active edges

- 3D sensors have been put to reality in ATLAS IBL detector since 2015 -> so far reliable and well performing
Pixel R/O-Chip for HL-LHC rates (and radiation)

- Effort and costs so large that joint approach (cross experiments) is needed -> **RD53** (20 Institutes)
- Higher hit rate (not smaller pixel size) requires higher logic density -> **65nm TSMC** -> **5nm (FCC)**?

### Pixel R/O-Chip Characteristics

<table>
<thead>
<tr>
<th>Technology</th>
<th>Pixel Size</th>
<th>Transistors</th>
<th>Hit Rate</th>
<th>Power Consumption</th>
<th>Radiation Tolerance</th>
</tr>
</thead>
<tbody>
<tr>
<td>250 nm</td>
<td>400 × 50 µm²</td>
<td>3.5 M.</td>
<td>&lt; 400 MHz/cm²</td>
<td>1.8 mW/mm²</td>
<td>&lt; 100 M rad</td>
</tr>
<tr>
<td>130 nm</td>
<td>250 × 50 µm²</td>
<td>70 M</td>
<td>2-3 GHz/cm²</td>
<td>&lt; 1 MHz trigger @12µs</td>
<td>2x10¹⁵/cm²</td>
</tr>
<tr>
<td>65 nm</td>
<td>50 × 50 µm²</td>
<td>~ 1000 M</td>
<td>&lt; 400 MHz/cm²</td>
<td>3.5 mW/mm²</td>
<td>200 M rad</td>
</tr>
</tbody>
</table>

- **FE-65** prototypes (2016) -> RD53A (full size chip) -> 2017
- Deep submicron (250 nm & 130 nm) saved LHC pixel R/O chips
- 65 nm has its **own** – geometry induced – **radiation effects** to deal with
- Requires long and tedious study program ...

RINCE = Radiation Induced Narrow Channel Effects
RISCE = Radiation Induced Short Channel Effects

see e.g. F. Faccio, TWEPP 2015, Proceedings

N. Wermes, FCC-2017 Berlin, 6/2017
Pixel R/O philosophy changes -> better architectures

1\textsuperscript{st} generation
- column drain R/O
- FE-I3 like

2\textsuperscript{nd} generation
- 4-pixel region logic
- efficient for clusters
- FE-I4 like

3\textsuperscript{rd} generation
- region architectures with grouped logic
  -> regional hit draining
- surrounded by synthesized logic ("digital sea")
- RD53A like

"analog islands in digital sea"
Current favorite large system layouts ...

- **n in p strip modules**
- **depl. CMOS pixels**
- **large modules planar n in p pixels / CMOS?**
- **3D silicon**
- **dedicated rad.-hard detectors**

N. Wermes, FCC-2017 Berlin, 6/2017
Can one do better than “hybrid”?  

**Hybrid Pixel Detectors**

- **PROs (split functionality)**
  - complex signal processing in readout chip
  - zero suppression and hit storage during L1 latency
  - radiation hard chips and sensors to $>10^{15}$ n$_{eq}$/cm$^2$
  - high rate capability (~MHz/mm$^2$)
  - spatial resolution $\approx 10 - 15$ µm
  - **NEXT:** 3D integration (TSVs) ... from C2W to W2W assemblies

- **CONs**
  - relatively large material budget: $>1.5\%$ X$_0$ per layer
  - sensor + chip + flex kapton + passive components
  - support, cooling (-10°C operation), services
  - resolution could be better
  - complex and laborious module production
  - bump-bonding / flip-chip
  - many production steps
  - expensive

- hence: Monolithic pixels relying on commercial CMOS processes have come in focus (first outside LHC-pp -> also for HL-LHC)

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N. Wermes, FCC-2017 Berlin, 6/2017
Non – Hybrid
-> Monolithic
From HYBRID to monolithic CMOS pixels

Monolithic Active Pixel Sensors

- **MAPS** using CMOS with Q-collection in epi-layer: developed for > 10 yrs
  Q by diffusion → recent advances
  not sufficiently radhard

- **DMAPS** (Depleted CMOS pixels)
  - using **HR** substrates and **HV** add-ons to create some depletion region
  - CMOS on **SOI**

- **STAR** + **ALICE**

- **HL - LHC**
  \[ d \sim \sqrt{\rho \cdot V} \]
  for high rate/rad environment

N. Wermes, FCC-2017 Berlin, 6/2017
Current **DMAPS** explorations

- **HV/HR technologies**
  - **HV CMOS**
    - AMS 350 nm
    - AMS 180 nm
  - **HR CMOS**
    - LFoundry 150 nm
    - Global Foundry 130 nm
    - ESPROS 150 nm
    - Toshiba 130 nm
    - **TowerJazz** 180 nm
    - IBM T3 130 nm
    - STM 180 nm
    - ON Semiconductor 180 nm

- **SOI – CMOS Pixel**
  - XFab 180 nm
The question of the fill-factor

Electronics inside charge collection well
- Collection node with large fill factor
  - no low field regions
  - on average short(er) drift distances
- Full CMOS with isolation between NW&DNW

- Larger (~100 fF) sensor capacitance (due to DNW/PW junction!)
  - noise & speed or power penalties
  - x-talk easier (from digital to sensor)
  - needs dedicated IC design

Electronics outside charge collection well promises
- Very small sensor capacitance (~5 fF)
  - noise low, speed high, power low
- on average longer drift distances and low field regions
  - not radhard ? or see later !!
- also full CMOS with addn’l deep-p implant
- see later -> TowerJazz design
What is needed to realize depleted CMOS pixels?

\[ d \sim \sqrt{\rho \cdot V} \]

“High” Resistivity Substrate Wafers (100 Ωcm – kΩ cm)

“High” Voltage add-ons to apply 50 – 200 V bias

Multiple (3-4) nested wells (for full CMOS and for shielding)

Backside Processing (for thinning and back bias contact)


from: www.xfab.com

N. Werms, FCC-2017 Berlin, 6/2017
Important prototyping results

• radiation hardness

LFoundry
edge-TCT measurements

$5 \times 10^{15} n_{eq}/cm^2$

Bias voltage (V)

0 20 40 60 80 100 120 140 160 180 200

FWHM (µm)

Bias [V]

Preliminary

LFoundry

Bias $[V]$ 1x10$^{15}$

AMS180

99.7%
(time integrated)

Bias $[V]$ 1x10$^{15}$

AMS180

• efficiency

I. Mandić et al., JINST 12 (2017) no.02, P02021

• timing

TID 1 MGy

AMS180 after $1 \times 10^{15} n_{eq}/cm^2$

gain

noise

labeled with jitter reduction

w/o jitter reduction

$\sigma = 1.96 \text{ ns}$

$\rightarrow 2.78 \text{ ns} @ 10^{15} n_{eq}/cm^2$

TowerJazz (small fill factor)
Development lines so far ...

- small prototypes
  - stand alone
  - bonded or glued to FE-I4

- full size **demonstrator**
  - stand alone testable
  - bonded or glued to FE-I4 readout chip

- fully monolithic version
  - includes complete R/O architecture
  - column drain (**FE-I3 type**) or alternatives

- AMS 350/180nm development line
- LFoundry 150nm development line
- (TowerJazz 180 nm follow-up on ALICE)

very good results so far
ALICE -> ATLAS follow up: small FF w/ TowerJazz

- **TowerJazz** 180 nm CMOS CIS
- deep PW full CMOS in pixel
- Gate oxide 3 nm good for TID
- epi thickness: 18 – 40 µm
- Resistivity: 1 – 8 k Ohm-cm
- Reverse substrate bias
- **Modified process** to improve lateral depletion
- Design derived from ALICE development

**Pixel dimensions:**
- 50×50 µm² pixel size
- 3 µm diameter electrodes
- **Measured capacitance <5fF** (C. Gao et al., NIM A (2016) 831)
  (20 times smaller than large fill-factor pixel)

- Large fully monolithic chip with two different R/O architectures (asynchronous and column drain) ready for submission -> June 2017.

N. Wermes, FCC-2017 Berlin, 6/2017
For the very cheap & large area .... passive CMOS sensors

hybrid again but cheap

C4 bumps: come with chip fabrication at low cost

- no bumping
- do flip-chipping in-house (large pitch)
- cheap large feature size technology
- large sensors (reticle stitching)
- wafer based flip-chipping (8“)
- can have in-pixel AC coupling
- fancy RDL possibilities by metal layers (watch C !)

- Question: how good are these CMOS sensors?

also for strip sensors

N. Wermes, FCC-2017 Berlin, 6/2017
Performance of sensor fabricated in CMOS

- break down at 110 – 120 V
- leakage $20 \mu A / cm^3$ (assuming 220 $\mu m$ depletion, estimated from simulation and indep. measurements)
- compare w/ ATLAS IBL planar sensors: $15 \mu A/cm^3$ (200 $\mu m$ depletion depth)

Noise of LFoundry passive CMOS sensor on ATLAS FE-14

compare IBL
- planar sensors ($C_D = 117$ fF): ENC = 120 e-
- 3D-Si sensors ($C_D = 180$ fF): ENC = 140 e-

D.-L. Pohl et al., arXiv:1702.04953, subm. to JINST
Testbeam performance unirradiated

Setup
- 2.5 GeV electron beam (ELSA)
- threshold: 1500 e- (tuned)

Resistivity

- Resistivity: 2.0 kΩ – cm
- Resistivity: 5.5 kΩ – cm
- Resistivity: 6.0 kΩ – cm
- Data

5.5 kΩ cm
2 kΩ cm

Efficiency

Mean efficiency of LF0ndry passive CMOS pixel sensor unirradiated, center pixels only

DC: efficiency lost in punch-through bias dot

high ohmic substrate
Testbeam performance after $1.14 \times 10^{15} \text{n}_{eq}/\text{cm}^2$

Efficiency of LFoundry passive CMOS pixel sensor after irradiation

- **AC**
  - $0.18 \times 10^{15} \text{n}_{eq}/\text{cm}^2$
  - $1.14 \times 10^{15} \text{n}_{eq}/\text{cm}^2$

- **DC**
  - $0.18 \times 10^{15} \text{n}_{eq}/\text{cm}^2$
  - $1.14 \times 10^{15} \text{n}_{eq}/\text{cm}^2$

In-time efficiency requirement

N. Wermes, LBNL Seminar, 08/16
Time measurement

Low Gain Avalanche Detectors (LGAD)

$\Delta t = 30 \text{ ps} \leftrightarrow \Delta x = 1\text{ cm}$
How to obtain fast timing with Si detectors?

- How would one go about getting into the 10 ps range with (structured) Si detectors?
  - => exploit “in-silicon” charge amplification
    - in “Geiger Mode” fashion (like in gas RPCs)

\[ \sigma_t \approx \frac{1.4}{(\alpha - \eta) v_D} \approx 50\text{ps} \]

\( \sigma_t \) governed by avalanche fluctuations

- OR .... in “linear mode” fashion
  -> Low Gain Avalanche Detectors

see e.g. W. Riegler, C. Lippmann, R. Veenhof
NIM A 500 (2003) 144

N. Cartiglia et al., NIM A796:141–148, 2015; NIM A845 (2017) 47-51
Towards 4D tracking ... Low-Gain Avalanche Detectors

- Separate the "collection" of charge from the signal gain
- Figure of merit for $\sigma_t$ is the "slew rate" $\frac{dV}{dt} \approx \text{Signal}/\tau_{\text{rise}}$

$$
\sigma_t^2 = \left( \frac{V_{th}}{\sqrt{\langle \frac{dV}{dt} \rangle_{\text{rms}}}^2} \right)^2 + \left( \frac{\text{Noise}}{\langle \frac{dV}{dt} \rangle} \right)^2 + \sigma_{\text{arrival}}^2 + \sigma_{\text{dist}}^2 + \sigma_{\text{TDC}}^2
$$

**Need:** fast drift - large signals – low noise
- e- drift in sat. ($E = 20 \text{ kV/cm}, v_D \approx 10^7 \text{ cm/s}) \Rightarrow \text{HV}$
- collect electrons fast $\Rightarrow \text{thin}$
- get large signals $\Rightarrow$ from amplified holes (!)
- small $C$, small $i_{\text{leak}}$, low noise $\Rightarrow$ small electrodes
- broad-band (non-CSA) amplifier & e.g. CF discr.

**Ultimate Goal:** simultaneous space ($\sim 10\mu\text{m}$) and time resolution ($< 50 \text{ ps}$) $\Rightarrow$ pile-up killer

**Options for ATLAS** (HighGranularityTimingDetector; Forward)
and **CMS-TOTEM** (in Roman Pots)
LGAD – successes so far ... and current problems

- LGAD pad detectors

G. Pellegrini et al., NIM A 765 (2014) 12–16.
G. Pellegrini et al., HSTD 2015, arXiv:1511.07175

N. Cartiglia et al., NIM A796:141–148, 2015; NIM A845 (2017) 47-51

- main problem: gain variation with fluence (due to high doping of amplification region) especially annoying in varying radiation fields

- current directions:
  1. substitute B with Ga as acceptor dopant
  2. use Carbon-enriched p-silicon wafers
Silicon detectors are the working horse for tracking detectors in high rate and radiation environments and currently THE choice for experiments at the FCC.

The main foci: "addressing the weak points"
- material in all aspects (thickness, rad. hardness)
- large area coverage at low cost
- integration
- addition of time measurement
BACKUP
Radiation effects in 65 nm CMOS small channel devices

**W** = moderate size

**W** = minimum size

**L** = moderate size

**L** = minimum size

heating  trap release

Regions strongly influenced by the trapped charge

cartoons: F. Faccio, TWEPP2015

N. Wermes, FCC-2017 Berlin, 6/2017
### Rate and Radiation Levels

#### Numbers for innermost layers ($r \approx 5\,\text{cm}$) -> scale by 1/10 for typical strip layers ($r > 25\,\text{cm}$)

<table>
<thead>
<tr>
<th></th>
<th>STAR</th>
<th>Belle II</th>
<th>ALICE-LHC heavy ion</th>
<th>ILC</th>
<th>LHC pp</th>
<th>HL-LHC-pp</th>
</tr>
</thead>
<tbody>
<tr>
<td>BX-time (ns)</td>
<td>110</td>
<td>2</td>
<td>20 000</td>
<td>350</td>
<td>25</td>
<td>25</td>
</tr>
<tr>
<td>Particle Rate (kHz/mm$^2$)</td>
<td>4</td>
<td>400</td>
<td>10</td>
<td>250</td>
<td>1 000</td>
<td>1 000</td>
</tr>
<tr>
<td>$\Phi$ ($n_{eq}/\text{cm}^2$)</td>
<td>few $10^{12}$</td>
<td>$3 \times 10^{12}$</td>
<td>$&gt; 10^{13}$</td>
<td>$10^{12}$</td>
<td>$2 \times 10^{15}$</td>
<td>$10^{15}$</td>
</tr>
<tr>
<td>TID (Mrad)*</td>
<td>0.2</td>
<td>20</td>
<td>0.7</td>
<td>0.4</td>
<td>80</td>
<td>50</td>
</tr>
</tbody>
</table>

*per (assumed) lifet ime
LHC, HL-LHC: 7 years
ILC: 10 years
others: 5 years

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- **in need for**
  - much less material
  - higher resolution
  - thinner strips & monolithic pixels

- **state of the art**
  - large area strips
  - hybrid pixels
  - even larger area
  - radhard sensors
  - higher rates R/O
  - R&D of new types

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N. Wermes, FCC-2017 Berlin, 6/2017
CMOS Pixels for HL-LHC -> DMAPS

- driven by the need/hope for
  - low cost large area detectors ... more pixel layers in trackers .... commercial
  - less material ... ? less power ... not clear
- but facing the rate/radiation challenges of the HL-LHC
- **goal:** some (40 – 80 µm) depletion depth for ...
  - fast charge collection (< 25ns “in-time” efficient)
  - a reasonably large signal ~4000 e-
  - not too large a travel distance to avoid trapping (rad hardness)

- **need**

low resistivity, low voltage

![Graph showing charge vs. time with two curves for NW and PW, and different radiation levels.](image)

high res. plus (high) voltage

![Graph showing charge vs. time with two curves for NW and PW, and different radiation levels.](image)

\[ d \sim \sqrt{\rho \cdot V} \]

from Tomasz Hemperek

N. Wermes, FCC-2017 Berlin, 6/2017
Important prototype results

- radiation hardness

**LFoundry**
edge-TCT measurements

Bias voltage (V)

**Preliminary**

Bias voltage (V)

$5 \times 10^{15} n_{eq}/cm^2$

- (50μm) depletion after $10^{15} n_{eq}/cm^2$

M. Mandic, B. Hiti (Ljubljana)

**AMS350**

Charge collection map @ V = 50V

1.5e15$n_{eq}/cm^2$

**AMS180**

- 99.7%
(time integrated)

9x10$^{15}$

Bias [V]

Thresh = 0.870V

**LFoundry**

gain

TID 100 Mrad

Tokio Hirono (UBonn)

**AMS350**

- 99.7%
(time integrated)

9x10$^{15}$

Bias [V]

Thresh = 0.870V

**LFoundry**

noise
Current DMAPS approaches

**CMOS on SOI**

- **FD-SOI**
- **OKI/LAPIS/KEK**
  Y. Arai et al., e.g. NIM. A636 (2011) 1, S31-S36
- **issues**
  - back gate effect
  - radiation issues due to BOX
- cures invented in recent years
- proposed for ILC
- but not suited for LHC - pp

- **HV-SOI (thick film)**
  Hemperek, Kishishita, Krüger, NW, NIM A796 (2015) 8-12
- a promising alternative
- doped, non-depleted P- and N-wells prevent back gate effect and increase the radiation tolerance

N. Wermes, FCC-2017 Berlin, 6/2017