
FCC WEEK 2017

# TOPOLOGIES FOR SUPPRESSING ERRATIC TRIGGERING OF SOLID STATE SWITCH STACKS

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## Introduction

The proposed FCC Beam Dump architecture consists of a large number of kicker magnets to assure a fast and safe beam deflection. The High Voltage (HV) pulse generators will produce fast controlled capacitor discharges through HV power switches into lumped inductance magnets. As for the LHC Beam Dump System (LBDS), an erratic triggering (i.e. self-trigger) of one or more of the 300 generator switches would deflect the circulating beam and could significantly damage the machine. A possible mitigation is a corrective retrigger mechanism that ensures the triggering of the remaining generators, but the kicker rise time is then unsynchronised with the beam abort gap(s) and hence several bunches will be steered on the machine extraction and downstream equipment.

To improve reliability, two alternative generator topologies for tackling the problem of erratic triggers at the source are studied: the use of additional shorting crowbar or series blocking switches. Both topologies can limit the current in the kicker magnet with the aim to reduce or eradicate the impact on the beam. This can result in a higher system reliability but the impact on availability needs to be acceptable. The results of electrical simulation models are presented in addition to topology advantages and disadvantages. Furthermore the corresponding impact on an FCC beam is presented.

## Problem outline

A self-trigger of an extraction kicker magnet (MKD) generator is a failure mode that cannot be ignored because:

- Semiconductor switches are blocking a high voltage close to their nominal value in order to reduce the number of switches;
- Leakage currents during long physics runs heat the switches which lower the gate threshold voltage;
- Large internal surfaces can make the switches susceptible to electrostatic discharges (LHC experience).

Two approaches to reduce this failure mode are: 1/ lowering the blocking voltage seen by a single device and 2/ using alternative switch topologies as discussed here. The first approach requires studies in a irradiation facility which is a topic for future research.

In case of self-triggering of one generator and the resulting beam deflection/ destabilisation, one possibility is to trigger the remaining(299) generators and thus perform an asynchronous beam dump. The effects were described during FCCW16 (ref. B. Goddard) and can be summarised as follows:

| Parameters (per module) | Value |
|---|---|
| Number of modules | 300 |
| B.dl [T.m] | 0.025 |
| k [μrad] | 0.150 |
| Length [mm] | 300 |
| Inductance [μH] | 0.38 |
| Current [kA] | 2.1 |
| Magnet current rise-time | 1 μs |

*Table 1: FCC dump module parameters*

- Miskicked bunches swept across collimators, aperture and septum;
- Damage reduction by (sacrificial) septum and QD protection devices.

This research focuses on reducing the magnetic field in the magnet in case of a single semiconductor device self-firing. The extraction magnet generator parameters from last year's baseline have been taken into consideration (ref. T. Kramer) with modifications for a changed extraction zone layout, see Table 1.

## Simulation Model

This research focusses on different semiconductor switch architectures and the following notes/assumptions are important:

- Capacitor discharge in a lumped inductance magnet: small HV capacitor for fast magnet current rise-time
- Bigger capacitor to provide flat-top kick, ignored for the moment as this is a non-critical component
- Cable inductance ignored to allow the use of this COTS product and comply with the 1 μs rise-time; several other simplifications
- An isolated IGBT gate driver with pulse transformer has been modelled as well to incorporate realistic triggering delays and gate currents
- Single IGBT switches used for studies: Mitsubishi CM1000HA-24H has a complete PSpice model with parasitic components; max $I_C$=2kA; max $V_{CES}$=1.2kV
- Simulating with complete model needed because fast collector voltage surges (dV/dt) can trigger the switch, simple switch model serves no use
- Parasitic capacitances $C_{GE}$, $C_{GC}$ (Miller capacitance) and $C_{CE}$ found correctly modelled, $C_{GC}$ ref. $V_{CE}$ verified with PSpice

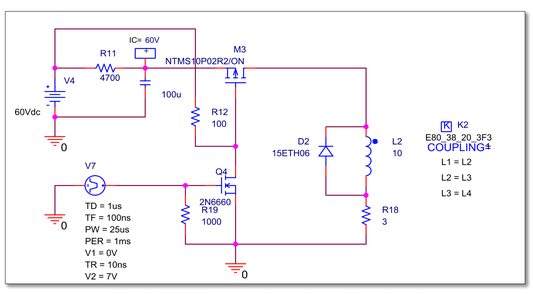


*Fig. 1: IGBT gate driver simulation circuit*

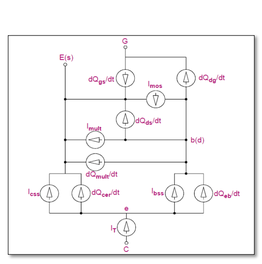


*Fig. 2: NIGBT simulation model*

## Conclusions

- Promising results for the series connected switch, the 1% leakage current (~30A top) reduces significantly the beam oscillation and impact on the machine in case of a module self-firing.
- Reliability gain to be compared to series switch with reducing blocking voltage (Single Event Effects (SEE) cross-section shown to decrease with voltage, ref. Viliam Senaj).
- Reliability studies needed to estimate the probability of (simultaneous) module self-triggering to have conclusive results of the miskicked beam's impact on the machine.

## Switch series connection

Two discrete IGBT devices in series can inhibit magnet current in case of a single device self-triggering. However because of the parasitic capacitances and fast transient at the collector, the second device might be turned on as well.

In case the top-side IGBT self-triggers, a high dV/dt is applied at the bottom-side IGBT's collector and the Miller capacitance will form a voltage divider with the $C_{GE}$. Depending on gate-emitter threshold voltage, this can turn the bottom IGBT on (undesired). Several mitigations can been applied to avoid this:

- Limit of the transient amplitude by lowering the device's blocking voltage
- Selection of IGBTs with higher $C_{GE}$, contradictory with the fast rise-time requirement
- Lowering of the gate resistance and connections

A second source for unwanted bottom-side IGBT turn-on can be the internal parasitic NPN transistor which can be turned on by a fast transient as well due to its base-emitter Miller capacitance. This can be mitigated by a PNP transistor to clamp $V_{GE}$ to zero in the off state.

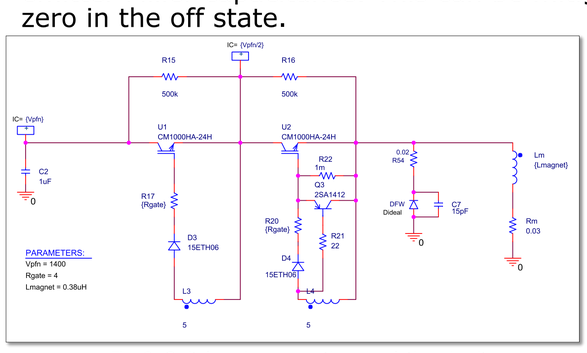


*Fig. 3: Switch series connection simulation circuit*

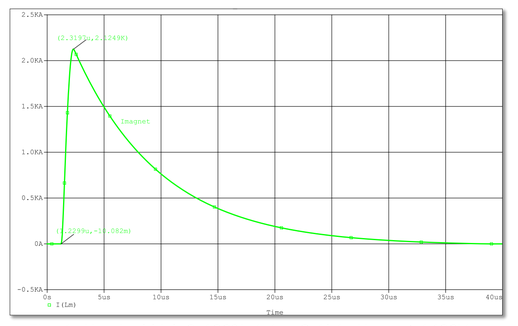


*Fig. 4: Nominal kick 0-100% 1.1μs 2.1kA; $U_{CAPA}$ at 1400V so each IGBT is blocking 700V*

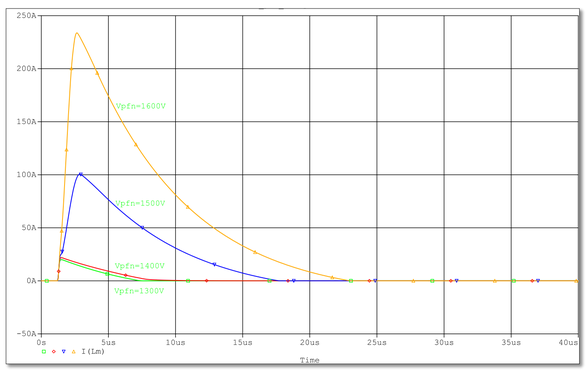


*Fig. 5: Bottom-side IGBT blocking full capacitor voltage; effect of capacitor voltage on leakage current (self-conduction) of that IGBT*

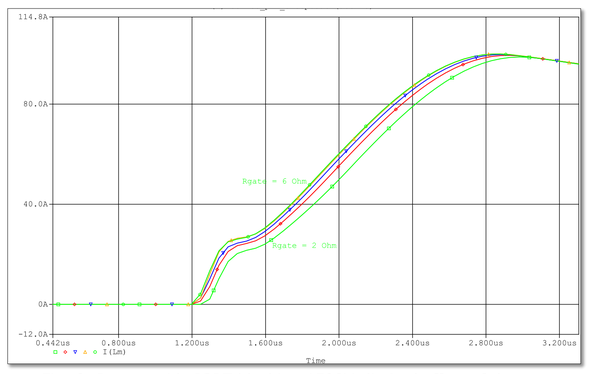


*Fig. 6: Bottom-side IGBT blocking 1500V; limited effect of the gate impedance on the leakage current*

## Switch crowbar connection

The two discrete IGBT devices can be configured so that the bottom-side device can short-circuit the charge to the ground (a.k.a crowbar connection). This circuit has some inconveniences:

- Self-triggering of the top-switch has to be detected to trigger the crowbar switch
- Single device to block the capacitor voltage: nominal MKD kick cannot be reached with device used
- Failure mode of crowbar switch self-triggering on dump request might will impact reliability

Anyhow interesting to study circuit behaviour. Trigger delay (kick 5% - trigger) is about 350ns and simulations show that the crowbar gate current is not sufficient to charge the gate capacitances after the fast voltage transient at its collector.

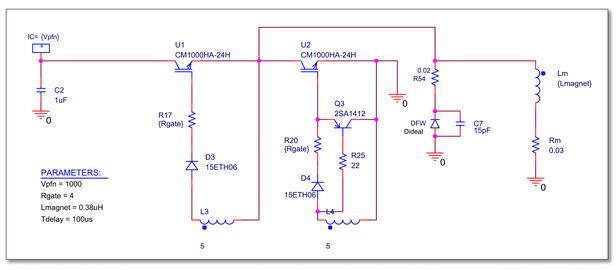


*Fig. 7: Switch crowbar connection simulation circuit; $U_{CAPA}$ at 1000V so FCC extraction parameters not met*

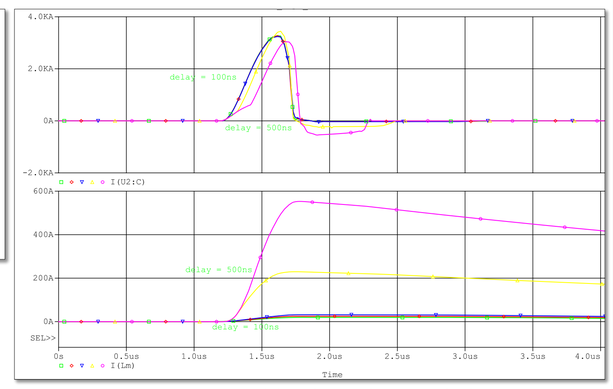


*Fig. 8, 100ns - 500ns delayed cross-bar IGBT (U2) trigger.*
*Top: U2 collector current; Bottom: magnet current*

## Self-trigger impact on FCC beam

The impact of a single module self-triggering has been evaluated for a FCC beam for two cases: nominal pulse (2.1kA at 1400V) and reduced pulse (~30A with 1400V). From both the beam oscillation and the proton loss studies it is clear that the topology reduces the kick significantly with minor impact on the machine. A Gaussian beam distribution is assumed and collision optics used for calculation of the impact of a self-trigger of the first (out of 300) module.

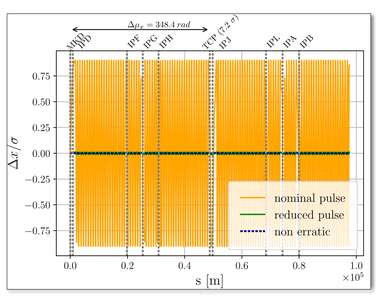


*Fig. 9: introduced transverse offset size vs. machine position*

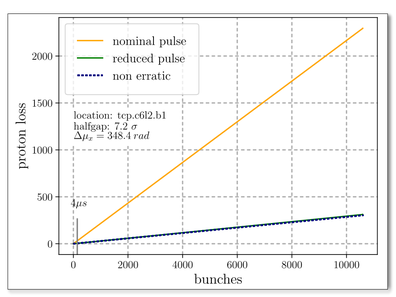


*Fig. 10: proton loss vs. bunches impacted on TCP*