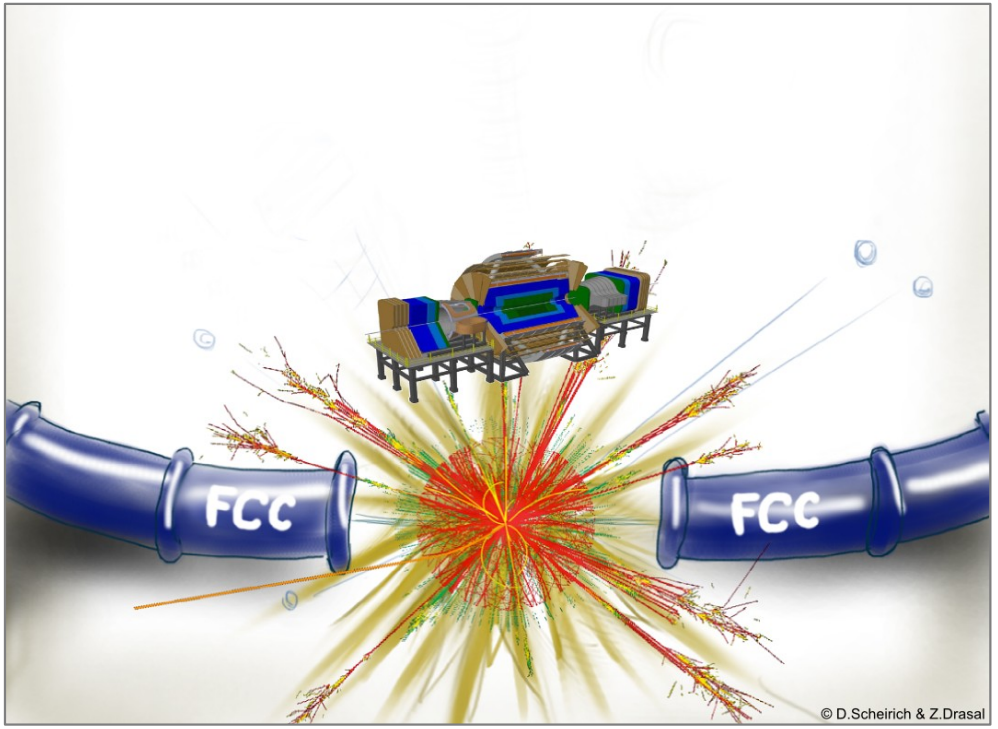
FCC-hh Tracker: Update on Data Rates & Occupancy



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With thanks to: M.I.Besana & F.Cerutti

Introduction

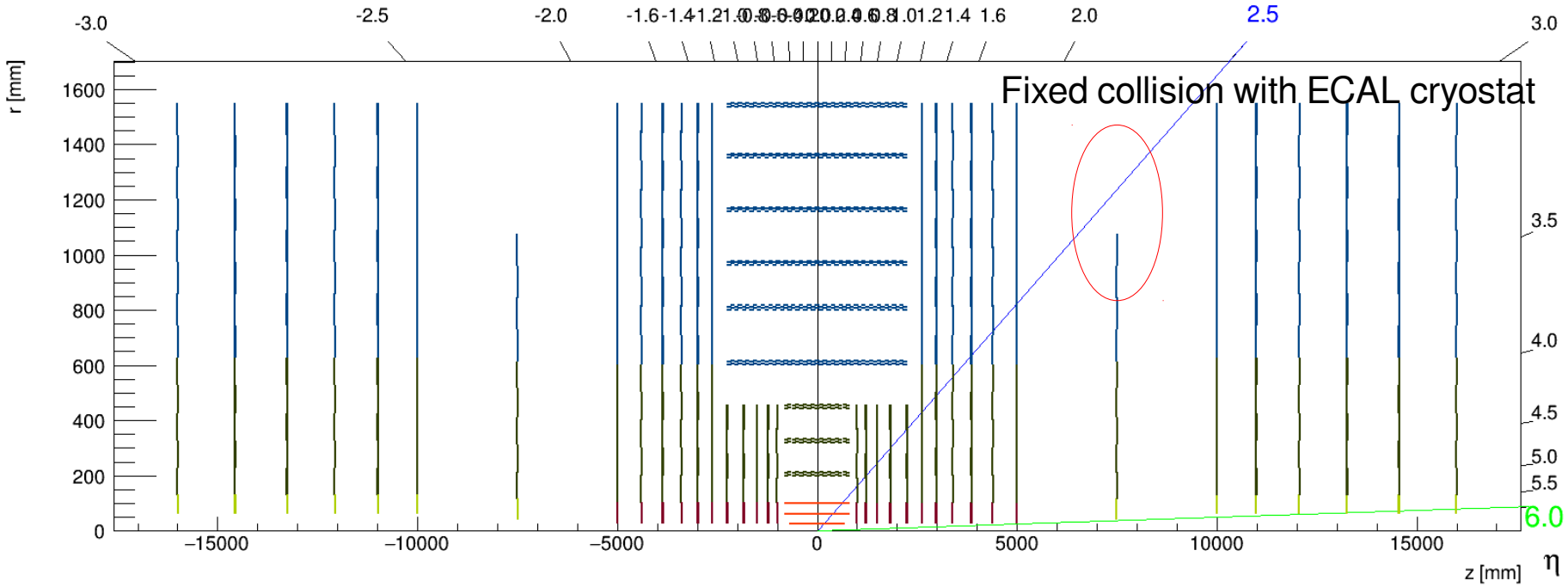
- **Update on tracker data rates & occupancy using new detector layout in B=4T**
  - Geometry layout details
  - Fluka fluence map (by M.I.Besana & F.Cerutti) & occupancy estimates
  - Data addressing scheme & expected data rates
- **Summary & Conclusions**

Geometry Layout Details

- **Currently 2 official layouts being studied:**
  - **Option3_v02**: http://fcc-tklayout.web.cern.ch/fcc-tklayout

    → Frozen geometry for full/fast simulations for Berlin, i.e. applied in Delphes & FCCSW

    → Only urgent “patches” accepted



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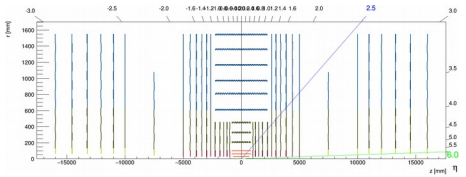


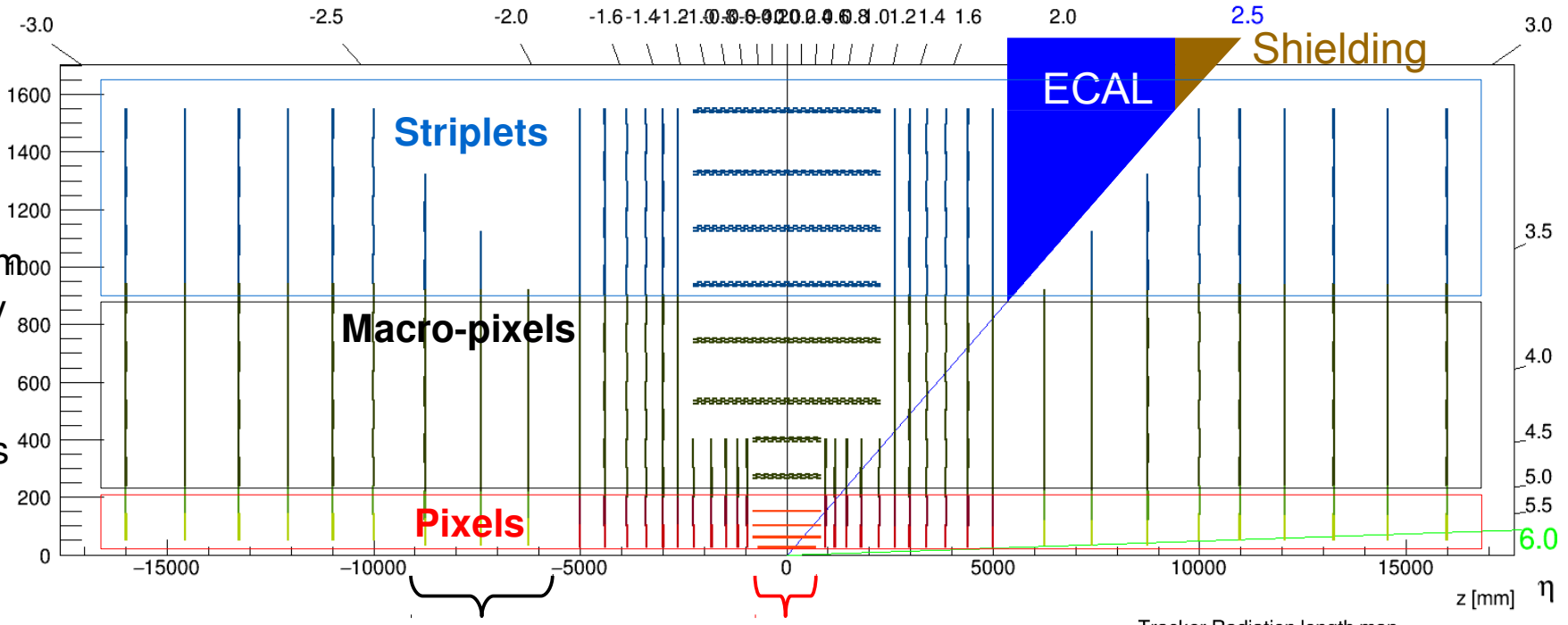
  - **Option3_v03** → currently being studied:
    - → Optimized module sizes with respect to pitch (to have $\mathbf{2^n}$ read-out channels & realistic modules)
    - → Optimized layout in terms of low occupancy & optimal pattern recognition
    - → Optimized channels for services etc.
    - → Design of tilted layout ongoing (non-tilted finished)
    - → Still missing optimization of wedge-shaped module sizes
    - → Still missing more realistic supports & services materials
    - → **All data rates results are based on this version**

Geometry Layout: Option3_v03

4 x **4** x **4** BRL layer structure

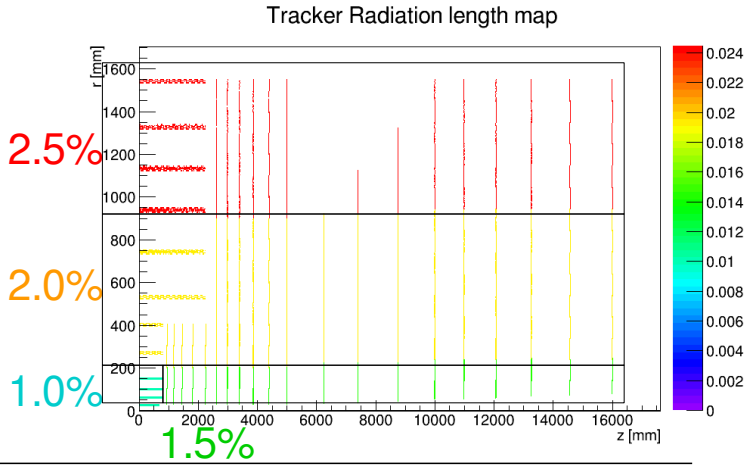
Pixel R↗0.9 (0.6) m due to occupancy (6T → 4T)

Layer/Ring R/Zpos optimized by pattern-reco



3 (1) needed by pattern-reco

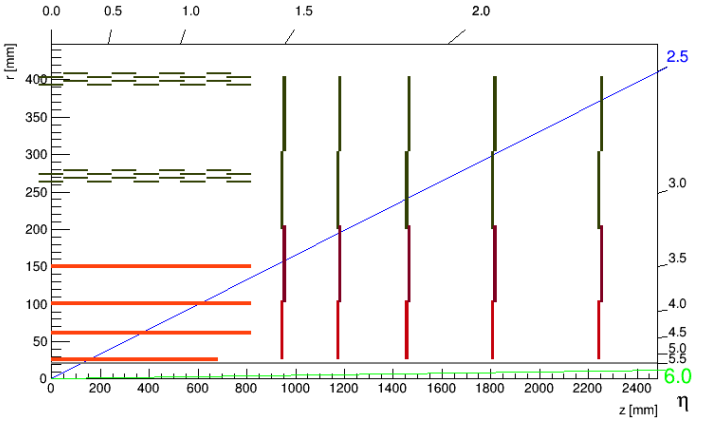
4 (3) seeding back-up



→ **Layout based on ongoing studies**

Inner Tracker (Budget): Surface & #Channels

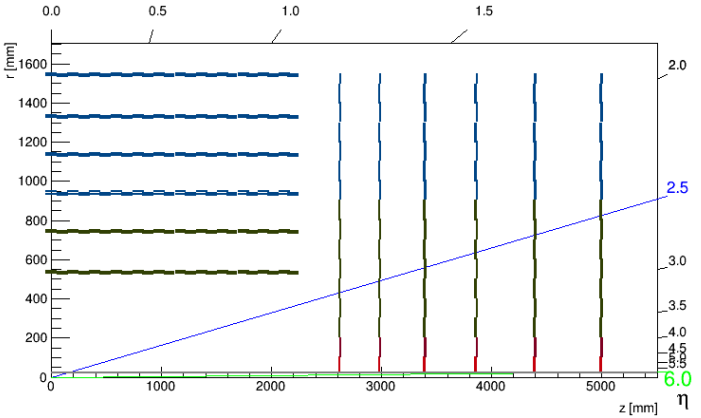
- **Inner detector:**



Module in:	Barrel	Barrel	Barrel	Endcap	Endcap	Endcap	Endcap	Total
Position:	BRL_0_L01	BRL_0_L02 BRL_0_L03 BRL_0_L04	BRL_1_L01 BRL_1_L02	ECAP_R01D1 ECAP_R01D2 ECAP_R01D3 ECAP_R01D4 ECAP_R01D5	ECAP_R04D1 ECAP_R04D2 ECAP_R04D3 ECAP_R04D4 ECAP_R04D5	ECAP_R03D1 ECAP_R03D2 ECAP_R03D3 ECAP_R03D4 ECAP_R03D5	ECAP_R02D1 ECAP_R02D2 ECAP_R02D3 ECAP_R02D4 ECAP_R02D5	
Type:	pixel	pixel	macroPixel	pixel	macroPixel	macroPixel	pixel	
Sensor area [mm^2]:	876.8	1049.6	5242.9	2571.2	5063.4	5083.2	4840.5	
Total area [m^2]:	0.2	3.4	7.5	0.3	2.2	1.6	1.0	**16.2**
Number of modules:	280	3200	1428	120	440	320	200	**5988**
Number of sensors:	280	3200	1428	120	440	320	200	
Number of channels (M):	196.40	2686.98	561.51	246.93	167.21	122.19	290.42	**4271.63**
Channels per module (R-Phi):	512	1024	1536	1352	1514	1480	1442	
Channels per module (Z):	1370	820	256	1522	251	258	1007	
Read-out chips per module:	3	4	3	9	3	3	6	

Outer Tracker (Budget): Surface & #Channels

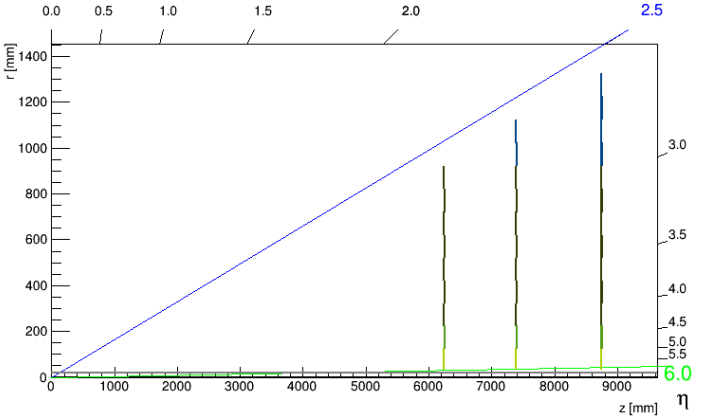
- **Outer detector:**



Module in:	Barrel	Barrel	Endcap	Endcap	Endcap	Endcap	Endcap	Endcap	Endca		
Position:	BRL_L01 BRL_L02 ECAP_R07D1 ECAP_R07D2 ECAP_R07D3 ECAP_R07D4 ECAP_R07D5 ECAP_R07D6 ECAP_R08D1 ECAP_R08D2 ECAP_R08D3 ECAP_R08D4 ECAP_R08D5 ECAP_R08D6 ECAP_R09D1 ECAP_R09D2 ECAP_R09D3 ECAP_R09D4 ECAP_R09D5 ECAP_R09D6	BRL_L03 BRL_L04 BRL_L05 BRL_L06	ECAP_R10D1 ECAP_R10D2 ECAP_R10D3 ECAP_R10D4 ECAP_R10D5 ECAP_R10D6 ECAP_R11D1 ECAP_R11D2 ECAP_R11D3 ECAP_R11D4 ECAP_R11D5 ECAP_R11D6 ECAP_R12D1 ECAP_R12D2 ECAP_R12D3 ECAP_R12D4 ECAP_R12D5 ECAP_R12D6 ECAP_R13D1 ECAP_R13D2 ECAP_R13D3 ECAP_R13D4 ECAP_R13D5 ECAP_R13D6 ECAP_R14D1 ECAP_R14D2 ECAP_R14D3 ECAP_R14D4 ECAP_R14D5 ECAP_R14D6 ECAP_R15D1 ECAP_R15D2 ECAP_R15D3 ECAP_R15D4 ECAP_R15D5 ECAP_R15D6	ECAP_R16D1 ECAP_R16D2 ECAP_R16D3 ECAP_R16D4 ECAP_R16D5 ECAP_R16D6	ECAP_R01D1 ECAP_R01D2 ECAP_R01D3 ECAP_R01D4 ECAP_R01D5 ECAP_R01D6	ECAP_R04D1 ECAP_R04D2 ECAP_R04D3 ECAP_R04D4 ECAP_R04D5 ECAP_R04D6	ECAP_R06D1 ECAP_R06D2 ECAP_R06D3 ECAP_R06D4 ECAP_R06D5 ECAP_R06D6	ECAP_R03D1 ECAP_R03D2 ECAP_R03D3 ECAP_R03D4 ECAP_R03D5 ECAP_R03D6	ECAP_R05D1 ECAP_R05D2 ECAP_R05D3 ECAP_R05D4 ECAP_R05D5 ECAP_R05D6	ECAP_R02D1 ECAP_R02D2 ECAP_R02D3 ECAP_R02D4 ECAP_R02D5 ECAP_R02D6	
Type:	macroPixel	strip	strip	strip	pixel	macroPixel	macroPixel	macroPixel	macroPixel	pixel	
Sensor area [mm^2]:	10485.8	10485.8	10485.8	5324.8	2631.3	5092.5	5457.7	5129.3	5776.2	4861.3	
Total area [m^2]:	58.6	150.8	59.9	6.1	0.4	2.7	4.2	2.0	3.6	1.2	**289.4**
Number of modules:	5584	14382	5712	1152	144	528	768	384	624	240	**29518**
Number of sensors:	5584	14382	5712	1152	144	528	768	384	624	240	
Number of channels (M):	4391.44	88.36	175.47	17.69	303.16	201.43	314.96	147.83	270.41	349.98	**6260.74**
Channels per module (R-Phi):	3072	3072	3072	3072	1397	1526	1647	1498	1654	1451	
Channels per module (Z):	256	2	10	5	1507	250	249	257	262	1005	
Read-out chips per module:	6	12	60	30	9	3	3	3	3	6	
Min-Max R-Phi resolution (μm):	9.5-9.5	9.5-9.5	9.5-9.5	9.5-9.5	7.5-7.5	9.5-9.5	9.5-9.5	9.5-9.5	9.5-9.5	9.5-9.5	
Min-Max Z(R) resolution (μm):	115.0-115.0	14434.0-14434.0	2887.0-2887.0	2887.0-2887.0	15.0-15.0	115.0-115.0	115.0-115.0	115.0-115.0	115.0-115.0	30.0-30.0	

iFWD Tracker (Budget): Surface & #Channels

- **Intermediate Forward detector:**

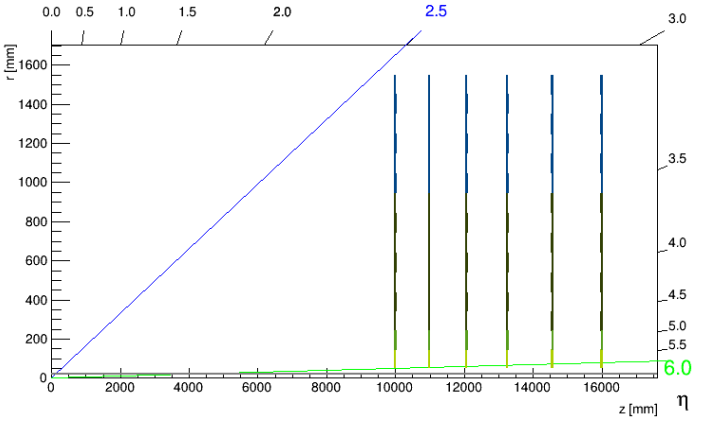


Module in:	Endcap	Endcap	Endcap	Endcap	Endcap	Endcap	Endcap	Endcap	Total
Position:	ECAP_R07D1 ECAP_R07D2 ECAP_R07D3 ECAP_R08D1 ECAP_R08D2 ECAP_R08D3 ECAP_R09D1 ECAP_R09D2 ECAP_R09D3	ECAP_R10D2 ECAP_R10D3 ECAP_R11D2 ECAP_R11D3 ECAP_R12D3 ECAP_R13D3	ECAP_R05D1 ECAP_R05D2 ECAP_R05D3	ECAP_R04D1 ECAP_R04D2 ECAP_R04D3	ECAP_R06D1 ECAP_R06D2 ECAP_R06D3	ECAP_R03D1 ECAP_R03D2 ECAP_R03D3	ECAP_R01D1 ECAP_R01D2 ECAP_R01D3	ECAP_R02D1 ECAP_R02D2 ECAP_R02D3	
Type:	macroPixel	strip	macroPixel	macroPixel	macroPixel	macroPixel	pixel	pixel	
Sensor area [mm^2]:	10485.8	10485.8	5310.2	5343.1	5624.5	5373.9	3786.1	5478.5	
Total area [m^2]:	10.1	9.1	1.8	1.4	2.2	1.0	0.3	0.7	**26.4**
Number of modules:	960	864	336	264	384	192	72	120	**3192**
Number of sensors:	960	864	336	264	384	192	72	120	
Number of channels (M):	754.97	26.54	133.81	105.73	162.14	77.38	218.11	197.16	**1675.85**
Channels per module (R-Phi):	3072	3072	1593	1602	1689	1612	1682	1643	
Channels per module (Z):	256	10	250	250	250	250	1801	1000	
Read-out chips per module:	6	60	3	3	3	6	12	6	
Min-Max R-Phi resolution (μm):	9.5-9.5	9.5-9.5	9.5-9.5	9.5-9.5	9.5-9.5	9.5-9.5	7.5-7.5	9.5-9.5	
Min-Max Z(R) resolution (μm):	115.0-115.0	2887.0-2887.0	115.0-115.0	115.0-115.0	115.0-115.0	115.0-115.0	15.0-15.0	30.0-30.0	

FWD Tracker (Budget): Surface & #Channels

- **Forward detector:**

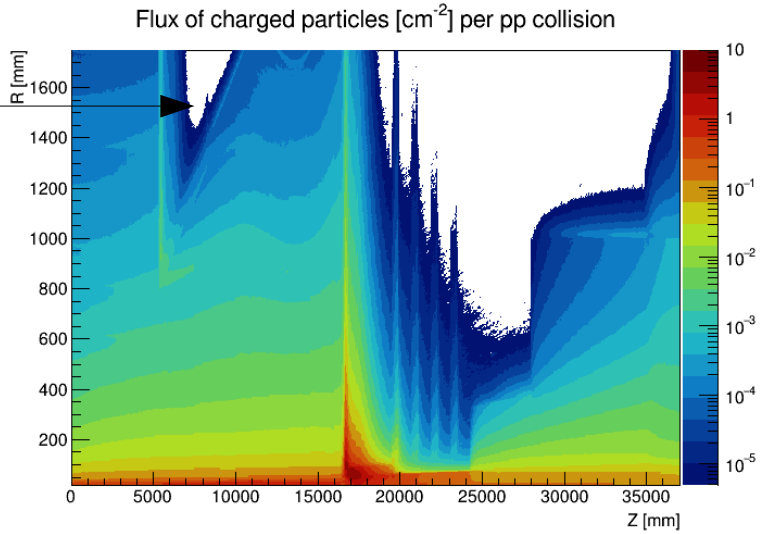
Module in:	Endcap	Endcap	Endcap	Endcap	Endcap	Endcap	Endcap	Total
Position:		ECAP_R10D1 ECAP_R10D2 ECAP_R10D3 ECAP_R10D4 ECAP_R10D5 ECAP_R10D6						
	ECAP_R06D1 ECAP_R06D2 ECAP_R06D3 ECAP_R06D4 ECAP_R06D5 ECAP_R06D6 ECAP_R07D1 ECAP_R07D2 ECAP_R07D3 ECAP_R07D4 ECAP_R07D5 ECAP_R07D6 ECAP_R08D1 ECAP_R08D2 ECAP_R08D3 ECAP_R08D4 ECAP_R08D5 ECAP_R08D6 ECAP_R09D1 ECAP_R09D2 ECAP_R09D3 ECAP_R09D4 ECAP_R09D5 ECAP_R09D6	ECAP_R11D1 ECAP_R11D2 ECAP_R11D3 ECAP_R11D4 ECAP_R11D5 ECAP_R11D6 ECAP_R12D1 ECAP_R12D2 ECAP_R12D3 ECAP_R12D4 ECAP_R12D5 ECAP_R12D6 ECAP_R13D1 ECAP_R13D2 ECAP_R13D3 ECAP_R13D4 ECAP_R13D5 ECAP_R13D6 ECAP_R14D1 ECAP_R14D2 ECAP_R14D3 ECAP_R14D4 ECAP_R14D5 ECAP_R14D6 ECAP_R15D1 ECAP_R15D2 ECAP_R15D3 ECAP_R15D4 ECAP_R15D5 ECAP_R15D6	ECAP_R04D1 ECAP_R04D2 ECAP_R04D3 ECAP_R04D4 ECAP_R04D5 ECAP_R04D6	ECAP_R03D1 ECAP_R03D2 ECAP_R03D3 ECAP_R03D4 ECAP_R03D5 ECAP_R03D6	ECAP_R05D1 ECAP_R05D2 ECAP_R05D3 ECAP_R05D4 ECAP_R05D5 ECAP_R05D6	ECAP_R02D1 ECAP_R02D2 ECAP_R02D3 ECAP_R02D4 ECAP_R02D5 ECAP_R02D6	ECAP_R01D1 ECAP_R01D2 ECAP_R01D3 ECAP_R01D4 ECAP_R01D5 ECAP_R01D6	
Type:	macroPixel	strip	macroPixel	macroPixel	macroPixel	pixel	pixel	
Sensor area [mm^2]:	10485.8	10485.8	5142.2	5103.7	5521.0	5049.9	4651.2	
Total area [m^2]:	25.2	61.9	3.0	2.2	3.7	1.5	0.7	**98.1**
Number of modules:	2400	5904	576	432	672	288	144	**10416**
Number of sensors:	2400	5904	576	432	672	288	144	
Number of channels (M):	1887.44	181.37	222.19	165.35	278.38	436.03	535.77	**3706.52**
Channels per module (R-Phi):	3072	3072	1543	1531	1657	1514	2067	
Channels per module (Z):	256	10	250	250	250	1000	1800	
Read-out chips per module:	6	60	3	3	3	6	16	
Min-Max R-Phi resolution (μm):	9.5-9.5	9.5-9.5	9.5-9.5	9.5-9.5	9.5-9.5	9.5-9.5	7.5-7.5	
Min-Max Z(R) resolution (μm):	115.0-115.0	2887.0-2887.0	115.0-115.0	115.0-115.0	115.0-115.0	30.0-30.0	15.0-15.0	



Fluka Fluence Map & Hit Rates

- **A cookbook "recipe":**
  - Use Fluka simulated fluence of charged particles per pp collision [cm^{-2}] scaled by **1000 pile-ups**

ECAL



  - Scan tracker module by module → find max/avg fluence
  - Calculate occupancy & hit rates (@ 2 scenarios):
    → Non-triggered data @ f = 40MHz
    → Triggered data @ f ~ 1MHz (~ given by hardware limits, e.g. FPGA)
  - **Comment:** Fluence data shared **@ CERNBox** common FCC-hh Tracker workspace:
    → Subscribe to: cernbox-project-fcc-hh-readers & download from: https://cernbox.cern.ch → DataDir

Definition: Data Bandwidth & Data Rates

- **2 options of data addressing:**

1) Sparsified data:

→ address each channel: **nBits** = $\log_2$(nRows) + $\log_2$(nColumns)

→ add data block for cluster-width: assuming avg cluster-size ~3 → **2bits**

→ add data block for pulse-height: **0bits** (binary read-out) or 4-8bits (analog read-out)

2) Unsparsified data:

→ address tho whole matrix: **nBits** = 1bit/channel x nRows x nColumns (x 4-8bits for analog)

Inner BRL: Occupancy & Data Rates

Layer no :	1	2	3	4	5	6	Total [TB/s]
Radius [mm] :	25.0	60.0	100.0	150.0	270.0	400.0	
Module max occupancy (max[sen1,sen2])[%] :	0.45	0.11	0.05	0.02	0.08	0.04	
#Hit-channels per module per BX :	2694	741	333	166	314	150	
Module avg occupancy (max[sen1,sen2])[%] :	0.38	0.09	0.04	0.02	0.08	0.04	
Module bandwidth/(addr+clsWidth=2b[b] :	22	22	22	22	21	21	
Mod. bandwidth(#chnls*(addr+clsWidth)[kb] :	57.88	15.93	7.16	3.57	6.44	3.08	
Mod. bandwidth (matrix*1b/channel) [kb] :	685.00	820.00	820.00	820.00	384.00	384.00	
Data rate per layer - 40MHz,spars [Tb/s] :	603.7	379.9	277.3	202.2	138.7	97.5	212.4
Data rate per layer - 1MHz,spars [Tb/s] :	15.1	9.5	6.9	5.1	3.5	2.4	5.3
Data rate per ladder - 40Mhz,spars [Gb/s] :	44159.7	24313.2	10920.7	5449.3	4177.1	1996.5	
Data rate per ladder - 1Mhz,spars [Gb/s] :	1104.0	607.8	273.0	136.2	104.4	49.9	
Data rate per module - 40Mhz,spars [Gb/s] :	2207.99	607.83	273.02	136.23	245.71	117.44	
Data rate per module - 1Mhz,spars [Gb/s] :	55.20	15.20	6.83	3.41	6.14	2.94	
Data rate per cm^2 - 40Mhz,spars [Gb/s/cm^2]:	251.82	57.91	26.01	12.98	4.69	2.24	
Data rate per cm^2 - 1Mhz,spars [Gb/s/cm^2]:	6.30	1.45	0.65	0.32	0.12	0.06	

→ Module maximum occupancy [%]

Inner BRL: Occupancy & Data Rates

Layer no :	1	2	3	4	5	6	Total [TB/s]
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Module bandwidth/(addr+clsWidth=2b[b] :	22	22	22	22	21	21	
Mod. bandwidth(#chnls*(addr+clsWidth)[kb] :	57.88	15.93	7.16	3.57	6.44	3.08	
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Data rate per cm^2 - 40Mhz,spars [Gb/s/cm^2]:	251.82	57.91	26.01	12.98	4.69	2.24	
Data rate per cm^2 - 1Mhz,spars [Gb/s/cm^2]:	6.30	1.45	0.65	0.32	0.12	0.06	

→ Hit-rate/collision/module @pile-up

Inner BRL: Occupancy & Data Rates

Layer no :	1	2	3	4	5	6	Total [TB/s]
Radius [mm] :	25.0	60.0	100.0	150.0	270.0	400.0	
Module max occupancy (max[sen1,sen2])[%] :	0.45	0.11	0.05	0.02	0.08	0.04	
#Hit-channels per module per BX :	2694	741	333	166	314	150	
Module avg occupancy (max[sen1,sen2])[%] :	0.38	0.09	0.04	0.02	0.08	0.04	
Module bandwidth/(addr+clsWidth=2b[b] :	22	22	22	22	21	21	
Mod. bandwidth(#chnls*(addr+clsWidth)[kb] :	57.88	15.93	7.16	3.57	6.44	3.08	
Mod. bandwidth (matrix*1b/channel) [kb] :	685.00	820.00	820.00	820.00	384.00	384.00	
Data rate per layer - 40MHz,spars [Tb/s] :	603.7	379.9	277.3	202.2	138.7	97.5	212.4
Data rate per layer - 1MHz,spars [Tb/s] :	15.1	9.5	6.9	5.1	3.5	2.4	5.3
Data rate per ladder - 40Mhz,spars [Gb/s] :	44159.7	24313.2	10920.7	5449.3	4177.1	1996.5	
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Data rate per module - 1Mhz,spars [Gb/s] :	55.20	15.20	6.83	3.41	6.14	2.94	
Data rate per cm^2 - 40Mhz,spars [Gb/s/cm^2]:	251.82	57.91	26.01	12.98	4.69	2.24	
Data rate per cm^2 - 1Mhz,spars [Gb/s/cm^2]:	6.30	1.45	0.65	0.32	0.12	0.06	

→ #bits per module to address data
→ Mod bandwidth (sparsified, binary)
→ Mod bandwidth (unsparsified, bin.)

Inner BRL: Occupancy & Data Rates

Layer no :	1	2	3	4	5	6	Total [TB/s]
Radius [mm] :	25.0	60.0	100.0	150.0	270.0	400.0	
Module max occupancy (max[sen1,sen2])[%] :	0.45	0.11	0.05	0.02	0.08	0.04	
#Hit-channels per module per BX :	2694	741	333	166	314	150	
Module avg occupancy (max[sen1,sen2])[%] :	0.38	0.09	0.04	0.02	0.08	0.04	
Module bandwidth/(addr+clsWidth=2b[b] :	22	22	22	22	21	21	
Mod. bandwidth(#chnls*(addr+clsWidth)[kb] :	57.88	15.93	7.16	3.57	6.44	3.08	
Mod. bandwidth (matrix*1b/channel) [kb] :	685.00	820.00	820.00	820.00	384.00	384.00	
Data rate per layer - 40MHz,spars [Tb/s] :	603.7	379.9	277.3	202.2	138.7	97.5	212.4
Data rate per layer - 1MHz,spars [Tb/s] :	15.1	9.5	6.9	5.1	3.5	2.4	5.3
Data rate per ladder - 40Mhz,spars [Gb/s] :	44159.7	24313.2	10920.7	5449.3	4177.1	1996.5	
Data rate per ladder - 1Mhz,spars [Gb/s] :	1104.0	607.8	273.0	136.2	104.4	49.9	
Data rate per module - 40Mhz,spars [Gb/s] :	2207.99	607.83	273.02	136.23	245.71	117.44	
Data rate per module - 1Mhz,spars [Gb/s] :	55.20	15.20	6.83	3.41	6.14	2.94	
Data rate per cm^2 - 40Mhz,spars [Gb/s/cm^2]:	251.82	57.91	26.01	12.98	4.69	2.24	
Data rate per cm^2 - 1Mhz,spars [Gb/s/cm^2]:	6.30	1.45	0.65	0.32	0.12	0.06	

→ Layer data rate (40MHz)
→ Layer data rate (1MHz, trigger)

→ Data rate per cm^2 (40MHz)
→ Data rate per cm^2 (1MHz, trigger)

Challenge: 6.3 Gb/s/cm^2

Inner Endcap: Occupancy & Data Rates

Ring no :	1	2	3	4	Total [TB/s]
Average radius [mm] :	64.8	153.0	251.1	353.3	
Module max occupancy (max[sen1,sen2])[%]:	0.46	0.13	0.18	0.08	
#Hit-channels per module per BX :	1853	885	410	221	
Module avg occupancy (max[sen1,sen2]) [%] :	0.09	0.06	0.11	0.06	
Module bandwidth/(addr+clsWidth=2b[b] :	24	23	22	21	
Mod. bandwidth(#chnls*(addr+clsWidth)[kb] :	43.43	19.88	8.82	4.53	
Mod. bandwidth (matrix*1b/channel) [kb] :	2009.52	1418.06	372.89	371.11	
Data rate per ringLayer-40MHz,spars [Tb/s]:	194.2	148.2	105.1	74.3	65.2
Data rate per ringLayer- 1MHz,spars [Tb/s]:	4.9	3.7	2.6	1.9	1.6
Data rate per ring - 40Mhz,spars [Gb/s] :	19882.7	15170.8	10765.8	7610.6	
Data rate per ring - 1Mhz,spars [Gb/s] :	497.1	379.3	269.1	190.3	
Data rate per module - 40Mhz,spars [Gb/s]:	1656.89	758.54	336.43	172.97	
Data rate per module - 1Mhz,spars [Gb/s]:	41.42	18.96	8.41	4.32	
Data rate per cm^2 - 40Mhz,spars [Gb/s/cm^2]:	64.44	15.67	6.62	3.42	
Data rate per cm^2 - 1Mhz,spars [Gb/s/cm^2]:	1.61	0.39	0.17	0.09	

Challenge: 1.6 Gb/s/cm^2

Outer Barrel: Occupancy & Data Rates

Layer no :	1	2	3	4	5	6	Total [TB/s]
Radius [mm] :	530.0	742.4	937.2	1132.0	1326.7	1541.5	
Module max occupancy (max[sen1,sen2])[%] :	0.02	0.01	0.75	0.43	0.27	0.21	
#Hit-channels per module per BX :	176	77	42	24	15	11	
Module avg occupancy (max[sen1,sen2])[%] :	0.02	0.01	0.70	0.40	0.25	0.19	
Module bandwidth/(addr+clsWidth=2b[b] :	22	22	15	15	15	15	
Mod. bandwidth(#chnls*(addr+clsWidth)[kb] :	3.80	1.67	0.63	0.36	0.22	0.17	
Mod. bandwidth (matrix*1b/channel) [kb] :	768.00	768.00	6.00	6.00	6.00	6.00	
Data rate per layer - 40MHz,spars [Tb/s] :	226.0	134.5	63.6	43.9	31.7	28.1	66.0
Data rate per layer - 1MHz,spars [Tb/s] :	5.6	3.4	1.6	1.1	0.8	0.7	1.6
Data rate per ladder - 40Mhz,spars [Gb/s] :	6806.5	2993.9	1123.2	642.1	395.3	300.1	
Data rate per ladder - 1Mhz,spars [Gb/s] :	170.2	74.8	28.1	16.1	9.9	7.5	
Data rate per module - 40Mhz,spars [Gb/s] :	144.82	63.70	23.90	13.66	8.41	6.38	
Data rate per module - 1Mhz,spars [Gb/s] :	3.62	1.59	0.60	0.34	0.21	0.16	
Data rate per cm^2 - 40Mhz,spars [Gb/s/cm^2]:	1.38	0.61	0.23	0.13	0.08	0.06	
Data rate per cm^2 - 1Mhz,spars [Gb/s/cm^2]:	0.03	0.02	0.01	0.00	0.00	0.00	

Outer Endcap: Occupancy & Data Rates

Ring no :	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Total [TB/s]
Average radius [mm] :	64.6	151.5	251.0	352.0	451.6	553.6	651.1	753.6	850.8	953.5	1049.7	1152.6	1247.6	1350.8	1444.7	1522.8	
Module max occupancy (max[sen1,sen2])[%]:	0.58	0.15	0.21	0.10	0.06	0.04	0.02	0.02	0.01	0.23	0.20	0.13	0.12	0.08	0.08	0.05	
#Hit-channels per module per BX :	2098	1062	499	272	186	107	151	99	79	56	40	32	23	19	15	6	
Module avg occupancy (max[sen1,sen2]) [%] :	0.10	0.07	0.13	0.07	0.04	0.03	0.02	0.01	0.01	0.18	0.13	0.10	0.08	0.06	0.05	0.04	
Module bandwidth/(addr+clsWidth=2b[b] :	24	23	22	21	22	21	22	22	22	18	18	18	18	18	18	17	
Mod. bandwidth(#chnls*(addr+clsWidth)[kb] :	49.18	23.86	10.72	5.58	4.01	2.20	3.25	2.15	1.70	1.00	0.72	0.57	0.42	0.35	0.27	0.11	
Mod. bandwidth (matrix*1b/channel) [kb] :	2055.94	1424.08	375.96	372.56	423.19	400.49	768.00	768.00	768.00	30.00	30.00	30.00	30.00	30.00	30.00	15.00	
Data rate per ringLayer-40MHz,spars [Tb/s]:	263.8	213.3	153.4	109.8	93.2	63.1	63.8	49.9	42.5	28.5	21.9	19.2	15.7	13.8	11.4	4.6	146.0
Data rate per ringLayer- 1MHz,spars [Tb/s]:	6.6	5.3	3.8	2.7	2.3	1.6	1.6	1.2	1.1	0.7	0.5	0.5	0.4	0.3	0.3	0.1	3.6
Data rate per ring - 40Mhz,spars [Gb/s] :	22513.6	18201.6	13091.2	9368.4	7955.2	5382.3	5448.2	4258.2	3625.8	2431.9	1865.7	1639.3	1342.4	1175.3	976.3	390.1	
Data rate per ring - 1Mhz,spars [Gb/s] :	562.8	455.0	327.3	234.2	198.9	134.6	136.2	106.5	90.6	60.8	46.6	41.0	33.6	29.4	24.4	9.8	
Data rate per module - 40Mhz,spars [Gb/s]:	1876.13	910.08	409.10	212.92	152.99	84.10	123.82	81.89	64.75	38.00	27.44	21.57	15.98	13.36	10.17	4.06	
Data rate per module - 1Mhz,spars [Gb/s]:	46.90	22.75	10.23	5.32	3.82	2.10	3.10	2.05	1.62	0.95	0.69	0.54	0.40	0.33	0.25	0.10	
Data rate per cm^2 - 40Mhz,spars [Gb/s/cm^2]:	71.30	18.72	7.98	4.18	2.65	1.54	1.18	0.78	0.62	0.36	0.26	0.21	0.15	0.13	0.10	0.08	
Data rate per cm^2 - 1Mhz,spars [Gb/s/cm^2]:	1.78	0.47	0.20	0.10	0.07	0.04	0.03	0.02	0.02	0.01	0.01	0.01	0.00	0.00	0.00	0.00	

Challenge: 1.8 Gb/s/cm^2

iFWD: Occupancy & Data Rates

Ring no :	1	2	3	4	5	6	7	8	9	10	11	12	13	Total [TB/s]
Average radius [mm] :	78.3	172.0	270.4	369.9	468.2	567.9	667.6	769.8	869.7	972.0	1071.4	1173.9	1272.8	
Module max occupancy (max[sen1,sen2])[%]:	0.51	0.13	0.20	0.11	0.07	0.04	0.03	0.02	0.02	0.48	0.24	0.12	0.07	
#Hit-channels per module per BX :	2477	1120	548	317	195	132	181	118	150	97	40	28	17	
Module avg occupancy (max[sen1,sen2]) [%] :	0.08	0.07	0.14	0.08	0.05	0.03	0.02	0.02	0.02	0.32	0.13	0.09	0.06	
Module bandwidth/(addr+clsWidth=2b[b] :	24	23	21	21	21	21	22	22	22	18	18	18	18	
Mod. bandwidth(#chnls*(addr+clsWidth)[kb] :	58.07	25.17	11.25	6.51	4.01	2.72	3.90	2.55	3.22	1.72	0.71	0.49	0.30	
Mod. bandwidth (matrix*1b/channel) [kb] :	2958.28	1604.49	393.55	391.11	388.92	412.35	768.00	768.00	768.00	30.00	30.00	30.00	30.00	
Data rate per ringLayer-40MHz,spars [Tb/s]:	155.8	112.5	80.4	64.0	50.1	39.0	41.8	29.6	43.2	16.4	7.6	2.8	1.9	80.6
Data rate per ringLayer- 1MHz,spars [Tb/s]:	3.9	2.8	2.0	1.6	1.3	1.0	1.0	0.7	1.1	0.4	0.2	0.1	0.0	2.0
Data rate per ring - 40Mhz,spars [Gb/s] :	26584.3	19207.0	13726.9	10923.1	8557.4	6650.7	7133.5	5057.3	7376.1	2796.6	1303.6	475.6	319.2	
Data rate per ring - 1Mhz,spars [Gb/s] :	664.6	480.2	343.2	273.1	213.9	166.3	178.3	126.4	184.4	69.9	32.6	11.9	8.0	
Data rate per module - 40Mhz,spars [Gb/s]:	2215.36	960.35	428.97	248.25	152.81	103.92	148.61	97.25	122.93	65.55	27.16	18.78	11.40	
Data rate per module - 1Mhz,spars [Gb/s]:	55.38	24.01	10.72	6.21	3.82	2.60	3.72	2.43	3.07	1.64	0.68	0.47	0.28	
Data rate per cm^2 - 40Mhz,spars [Gb/s/cm^2]:	58.51	17.53	7.98	4.65	2.88	1.85	1.42	0.93	1.17	0.63	0.26	0.18	0.11	
Data rate per cm^2 - 1Mhz,spars [Gb/s/cm^2]:	1.46	0.44	0.20	0.12	0.07	0.05	0.04	0.02	0.03	0.02	0.01	0.00	0.00	

Challenge: 1.5 Gb/s/cm^2

FWD: Occupancy & Data Rates

Ring no :	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	Total [TB/s]
Average radius [mm] :	97.1	190.1	288.9	388.3	487.1	588.6	689.4	791.4	891.9	994.1	1094.4	1196.6	1296.6	1398.8	1498.5	
Module max occupancy (max[sen1,sen2])[%]:	0.28	0.11	0.20	0.12	0.08	0.05	0.04	0.03	0.02	0.46	0.34	0.25	0.16	0.11	0.09	
#Hit-channels per module per BX :	2430	1013	545	340	236	303	219	154	133	102	62	40	29	21	14	
Module avg occupancy (max[sen1,sen2]) [%] :	0.07	0.07	0.14	0.09	0.06	0.04	0.03	0.02	0.02	0.33	0.20	0.13	0.10	0.07	0.05	
Module bandwidth/(addr+clsWidth=2b[b] :	25	23	21	21	21	22	22	22	22	18	18	18	18	18	18	
Mod. bandwidth(#chnls*(addr+clsWidth)[kb] :	59.34	22.77	11.20	6.97	4.85	6.51	4.71	3.32	2.86	1.80	1.10	0.72	0.52	0.37	0.26	
Mod. bandwidth (matrix*1b/channel) [kb] :	3633.40	1478.52	373.78	376.71	404.54	768.00	768.00	768.00	768.00	30.00	30.00	30.00	30.00	30.00	30.00	
Data rate per ringLayer-40MHz,spars [Tb/s]:	318.3	244.3	180.2	149.6	121.5	116.4	101.0	77.1	76.7	54.9	35.5	25.6	19.5	15.2	11.0	193.4
Data rate per ringLayer- 1MHz,spars [Tb/s]:	8.0	6.1	4.5	3.7	3.0	2.9	2.5	1.9	1.9	1.4	0.9	0.6	0.5	0.4	0.3	4.8
Data rate per ring - 40Mhz,spars [Gb/s] :	27165.7	20849.8	15374.8	12767.3	10364.6	9933.1	8618.5	6577.3	6548.3	4681.3	3033.6	2186.0	1666.3	1295.5	938.8	
Data rate per ring - 1Mhz,spars [Gb/s] :	679.1	521.2	384.4	319.2	259.1	248.3	215.5	164.4	163.7	117.0	75.8	54.7	41.7	32.4	23.5	
Data rate per module - 40Mhz,spars [Gb/s]:	2263.81	868.74	427.08	265.99	185.08	248.33	179.55	126.49	109.14	68.84	42.13	27.33	19.84	14.08	9.78	
Data rate per module - 1Mhz,spars [Gb/s]:	56.60	21.72	10.68	6.65	4.63	6.21	4.49	3.16	2.73	1.72	1.05	0.68	0.50	0.35	0.24	
Data rate per cm^2 - 40Mhz,spars [Gb/s/cm^2]:	48.67	17.20	8.37	5.17	3.35	2.37	1.71	1.21	1.04	0.66	0.40	0.26	0.19	0.13	0.09	
Data rate per cm^2 - 1Mhz,spars [Gb/s/cm^2]:	1.22	0.43	0.21	0.13	0.08	0.06	0.04	0.03	0.03	0.02	0.01	0.01	0.00	0.00	0.00	

Challenge: 1.2 Gb/s/cm^2

Summary & Outlook

- **Geometry layouts:**
  - **Option3_v02:** Macro-pixels need to be extended up-to 900mm → **change resol.** for R=600-900mm
    → no effect on geometry layout, negligible effect on parametric sim., effect on pattern-reco (full sim.)
  - **Option3_v03 (NEW):** optimized mainly by pattern-reco performance
    → Non-tilted design finished, tilted design ongoing ...
    → **Expected tracker surface:** 9.7m^2 (pixels), 133m^2 (macro-pixels), 287.7m^2 (strips)
    → **Expected number of channels:** 5460.9M (pixels), 9966.4M (macro-pixels), 489.4M (strips)

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- **Data rates:**
  - Estimated data rates for 2 scenarios: 40MHz (untriggered) & ~1MHz (triggered)
    → Expected total data rates: 764 TB/s (untriggered), 19 TB/s (triggered)
  - **Even triggered (1MHz) first 2 layers in the inner barrel region and the first 3 "ring-layers" in the end-cap with data flows >> 10Gb/s per module**
    → 1st (2nd) layer in inner barrel: 6.3 (1.5) Gb/s/cm^2
    → 1st (2nd) ring-layer in inner end-cap: 1.8 (0.5) Gb/s/cm^2
    → "out of scale" for the current technology → need for trigger & special technology!