The CMS Phase1 Pixel Detector Upgrade

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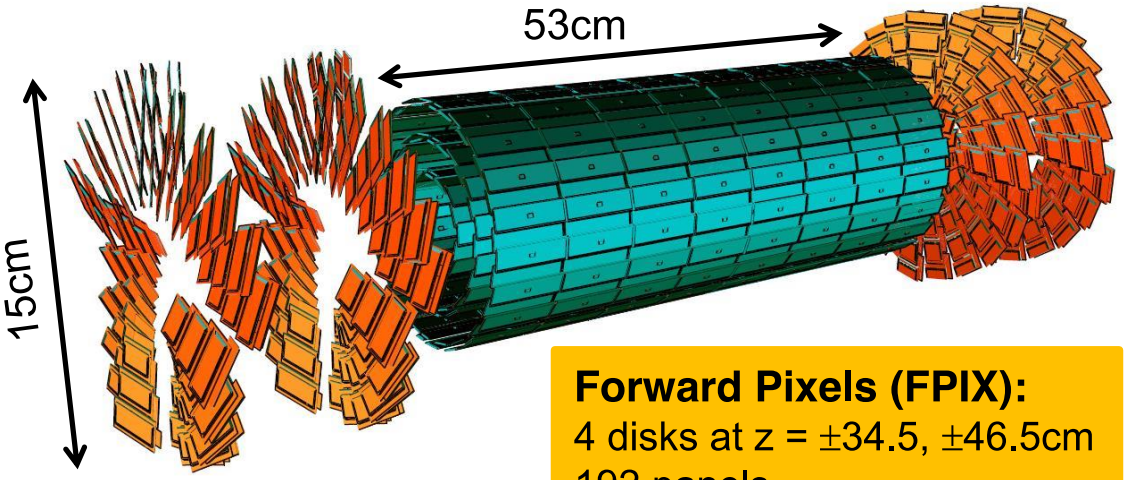
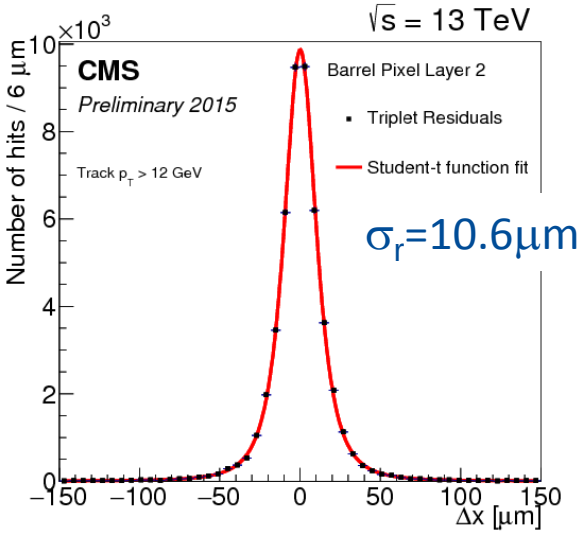
Reminder: the current CMS pixel detector

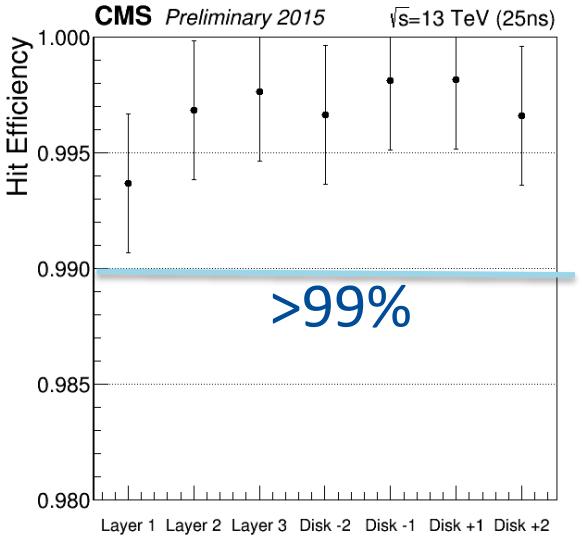
Barrel Pixels (BPIX):
3 barrel layers at 4.4, 7.3, 10.2cm
768 modules

Present detector designed for $10^{34}cm^{-2}s^{-1}$ and 25ns bunch spacing



Forward Pixels (FPIX):
4 disks at z = ±34.5, ±46.5cm
192 panels

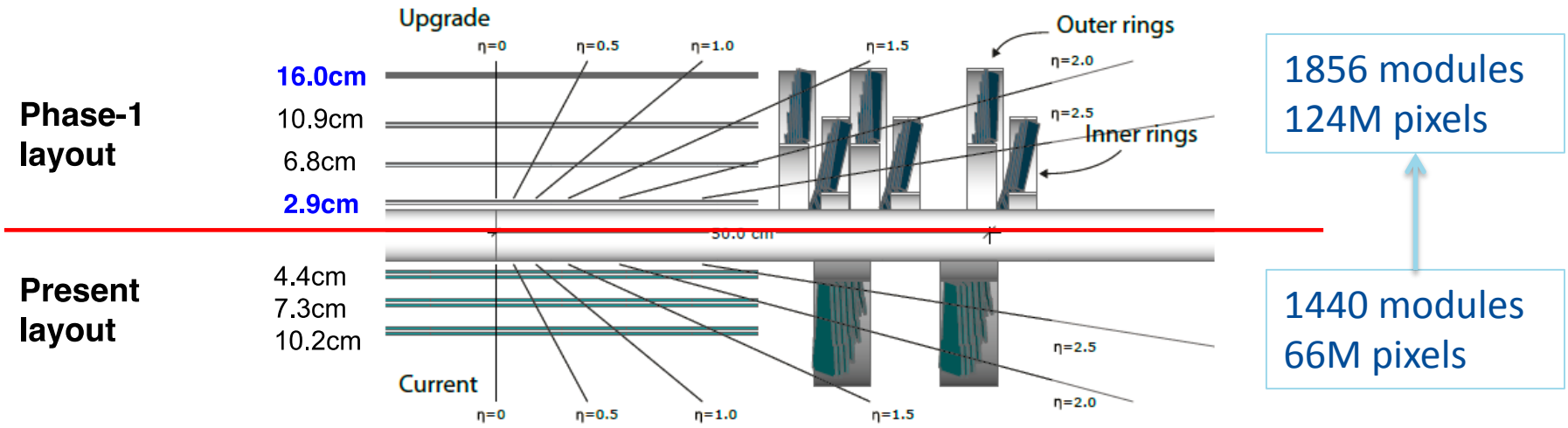




- $1m^2$ of n^+-in-n silicon sensors
- Excellent resolution and efficiency
- Excellent good-channel fraction and uptime in Run1 and Run2 so far

Phase1 pixel detector design

- Installation during extended year-end technical stop 2016/17 in February'17
- Smooth transition needed from installation to physics data taking; not much time for in-situ calibrations
  - Sensor technology, pixel size and module concept very similar; need to fit into existing infrastructure
  - Move from analog to digital readout chip (ROC) → reduced buffer overflow and inefficiency
  - Move from 3- to 4-hit coverage → increase redundancy and track finding efficiency
  - Move closer to the beam → improve vertexing and b-tagging
  - Move from single-phase fluorocarbon (C6F14) to evaporative, bi-phase CO_2 cooling



Phase1 upgrade improvements

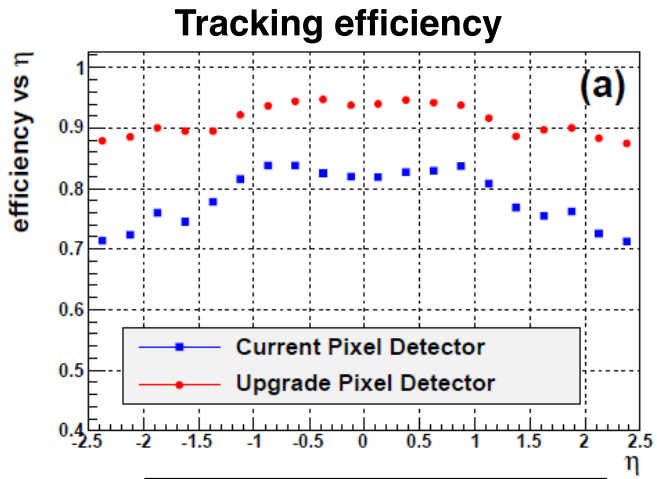
- Present detector designed for $10^{34}cm^{-2}s^{-1}$ and 25ns bunch spacing
- Expect twice as much before LS3 (2024)
  - 50 pileup events, hit rates of ~600MHz/cm^2

➢ **Improve redundancy:** from 3 to 4 layers (BPIX), from 2 to 3 disks on each end (FPIX); impacting tracking efficiency and purity

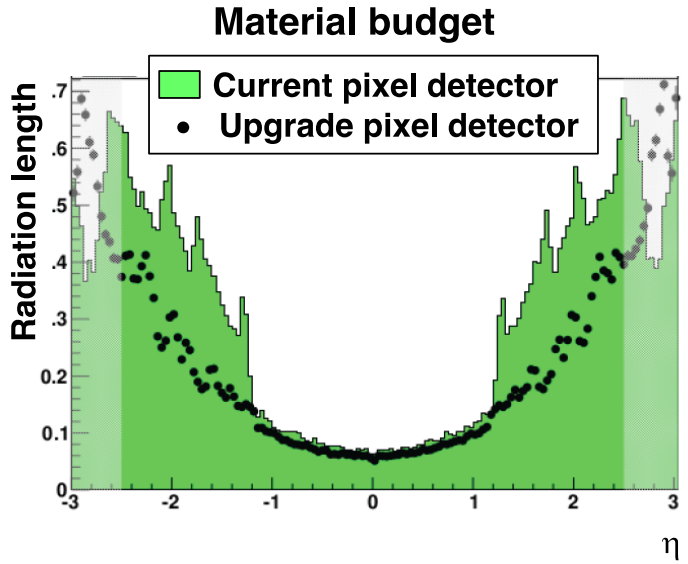
➢ **Move closer to beam:** improve vertexing and b-tagging

➢ **Avoid hit inefficiency** of up to 16% due to buffer overflow in readout chip (ROC) with new digital ROC

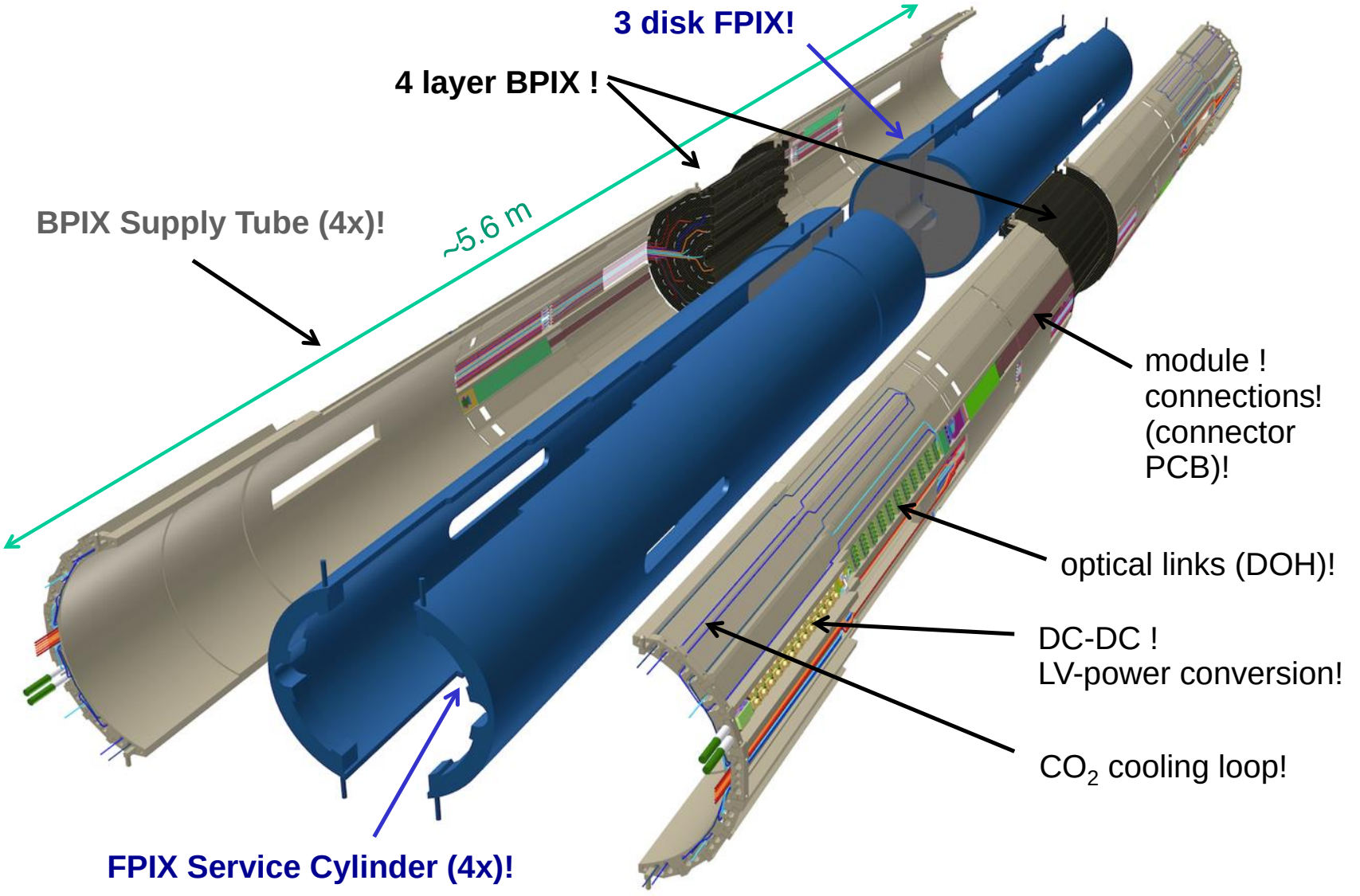
➢ **Reduce mass:** use CO_2 cooling instead of water-glycol



ttbar sample, 50 pileup events

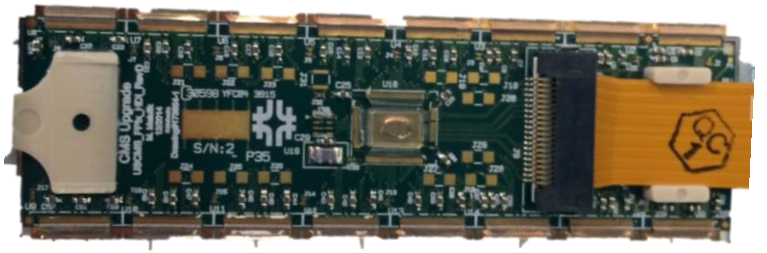


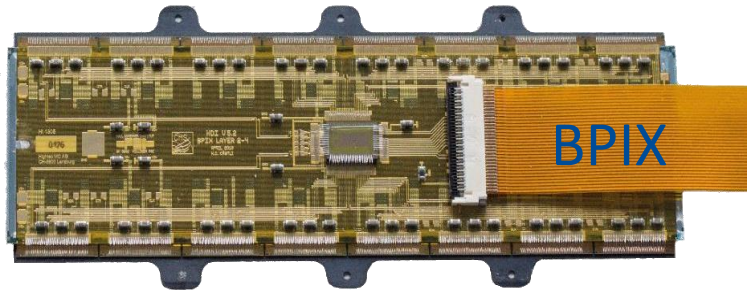
BPIX & FPIX exploded view

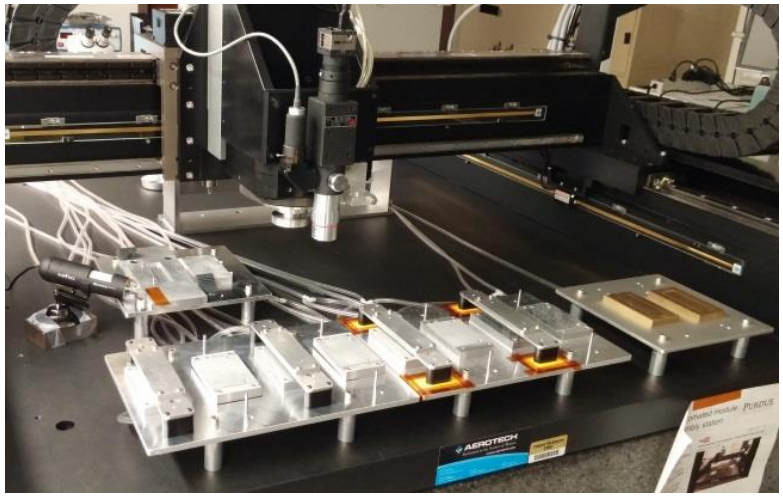


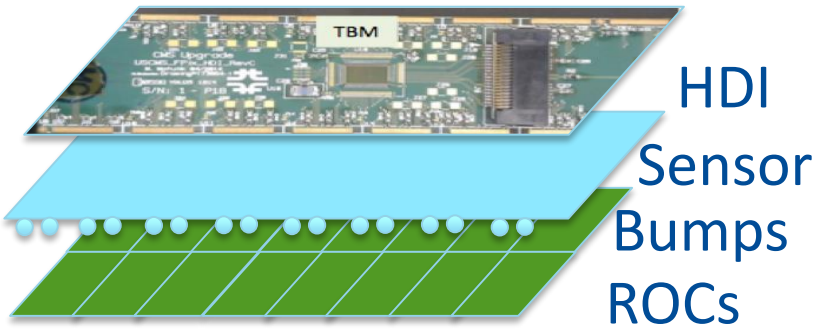
Pixel Modules

- FPIX:
  - Bump bonding done at vendor (RTI)
  - Module assembly done in house at two institutions
- BPIX:
  - Bump bonding and module assembly done at vendors and in-house at several institutions
- Module = Sandwich{ROCs+SiSensor+HDI}
  - 16 ROCs = >66k pixels



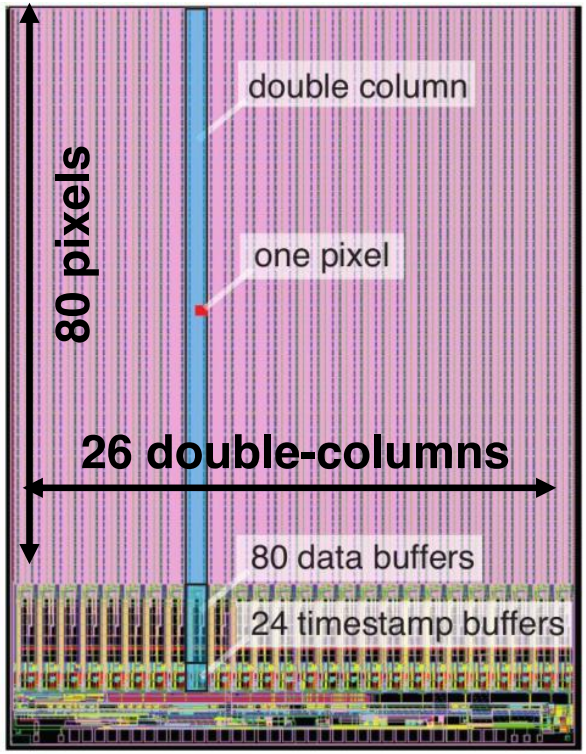


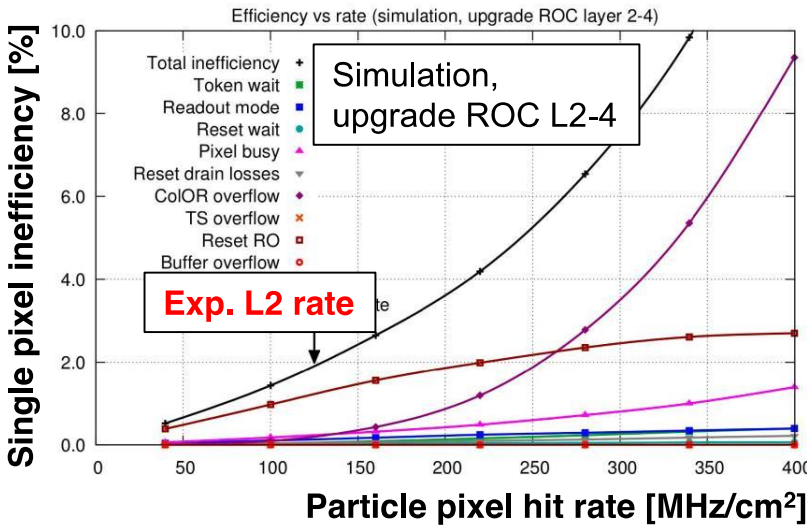




Readout Chip

- New, digital readout chip based on present analog PSI46
- Same technology (0.25μm CMOS) and column drain architecture
  - 40MHz analog → 160 Mbits/s digital (8 bit ADC)
  - Increase of hit (32 → 80) and time stamp (12 → 24) buffer depth
  - Additional readout buffer
  - Smaller cross talk + improved comparator → threshold reduced from 3200e$^-$ to ~2000e$^-$ → better efficiency, resolution and longevity
- Final version for BPIX L2,3,4 and FPIX performing very well
- Special version for L1 (580 MHz/cm^2) with cluster readout

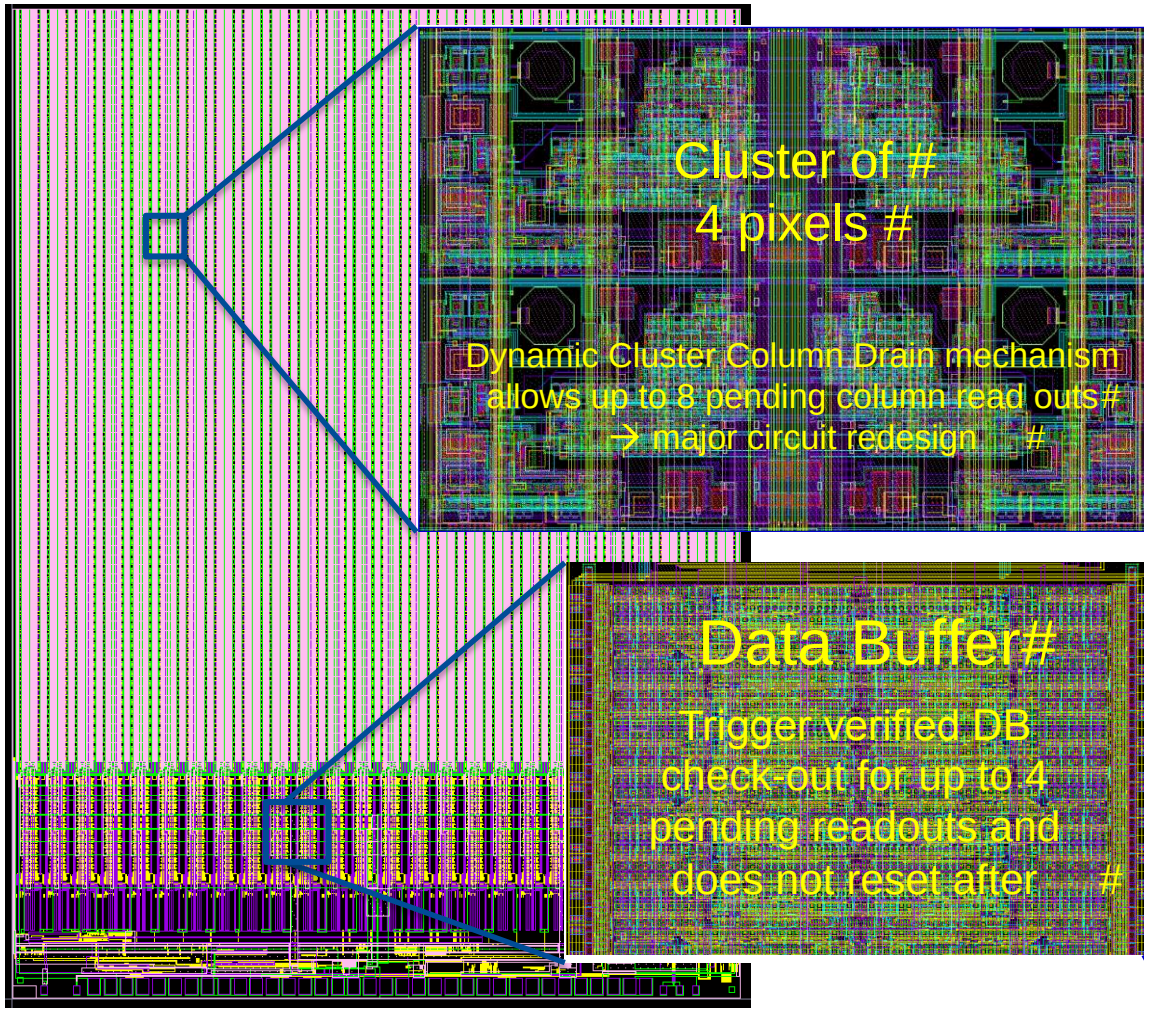




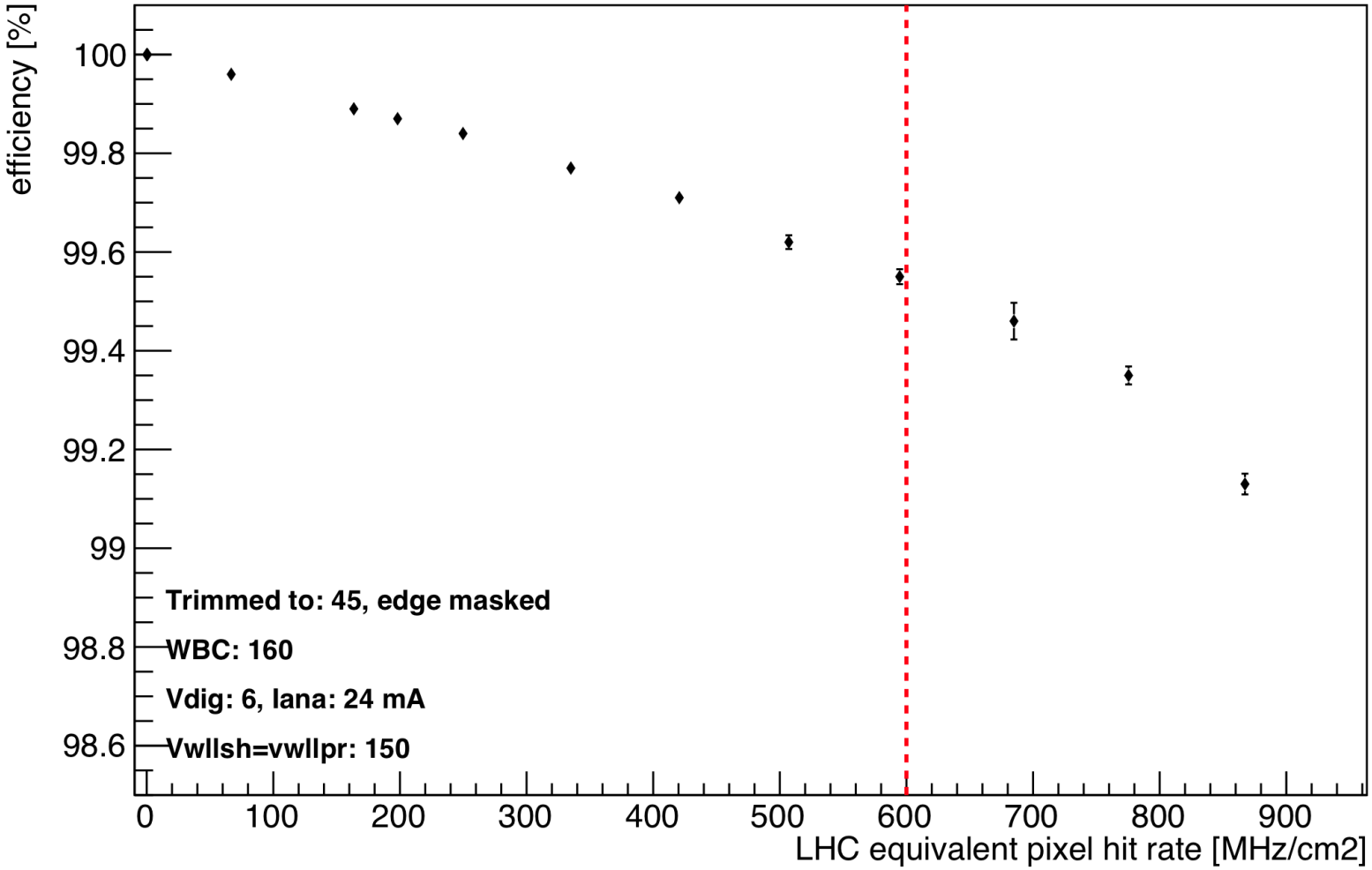
Layer 1 PROC600 Innovations

Design parameters:!

- chip size 7860 m x 10'550 m
- pixel size 100 m x 150 m #
- 339 transistors / pixel (268 L24 ROC)#
- pixel array 52 x 80#
- DCCD transfer in DC at 40MHz#
- Data Buffer Cluster Cells (4x) 56#
- Timestamp Buffer 40#
- ROC Read-out Buffer 64#
- Total transistor count : 2.2 M#
- analog pulse height : 8 bit ADC#
- pixel rate ~600MHz/cm^2 *~FEI4!*
- expect rad. hardness ~500Mrad#
- power consumption#
  - analog power identical to L24 ROC#
  - digital power probably less than L24 #



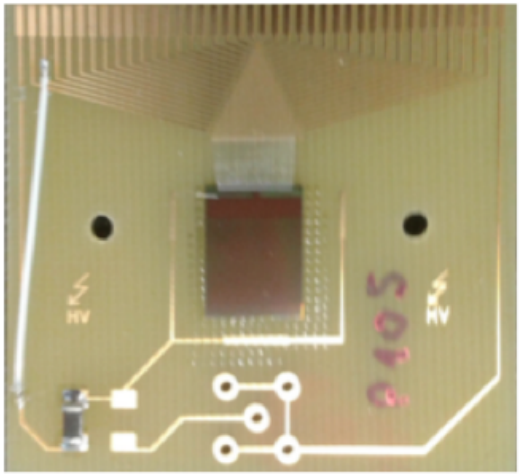
High rate x-ray test of PROC600v2

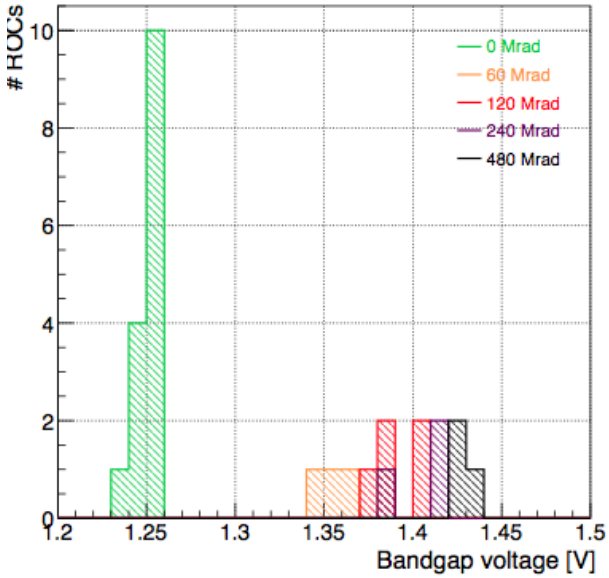


High rate x-ray tests confirm excellent behavior of v2 chip

PROC600 irradiation studies

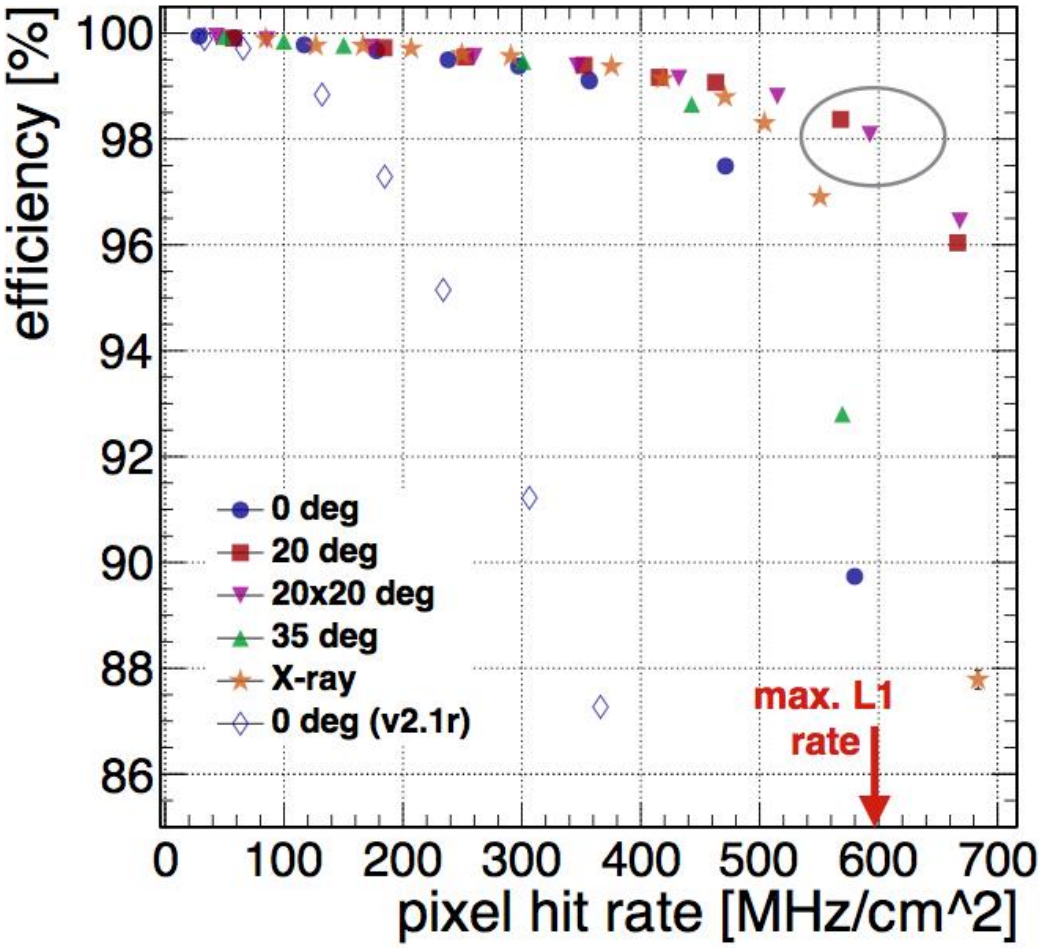
Irradiation dose [Mrad]	Fluence [1MeV Neq/cm^2]	# samples	Equivalence
0	0	15	/
66	$0.44 \cdot 10^{15}$	4	Layer 2
137	$0.91 \cdot 10^{15}$	5	Layer 1
265	$1.77 \cdot 10^{15}$	3	/
495	$3.3 \cdot 10^{15}$	3	/





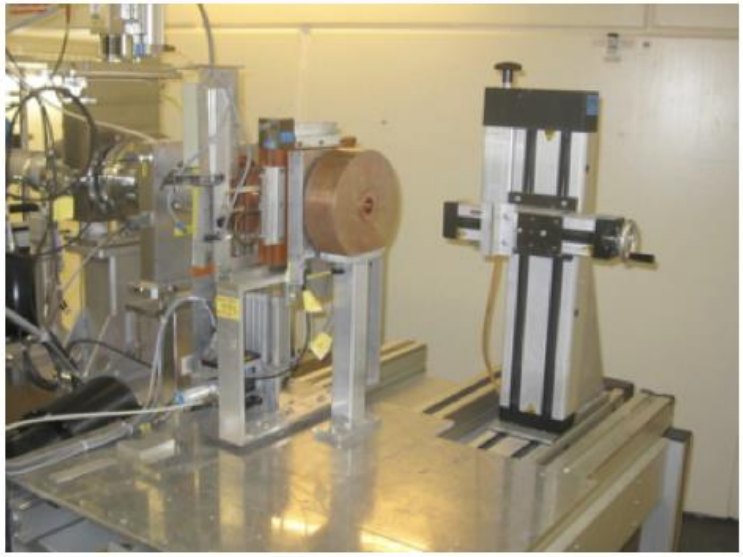
- irradiation study of PROC600(v1) samples, some with sensor
- irradiated with 23 MeV protons up to 480 Mrad
- dynamic range of DACs studied after irradiation
- electrically operational up to 480 Mrad
- HR efficiency checked for 60 and 120 Mrad samples

High rate test beam with protons

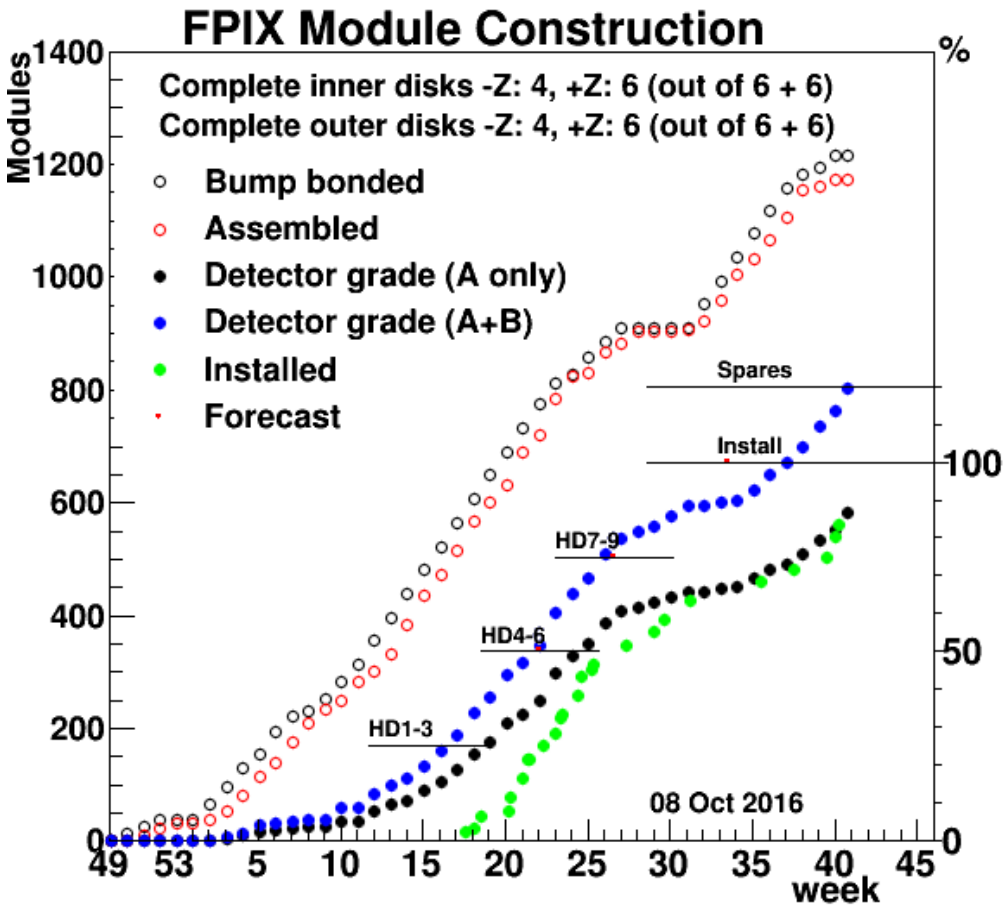


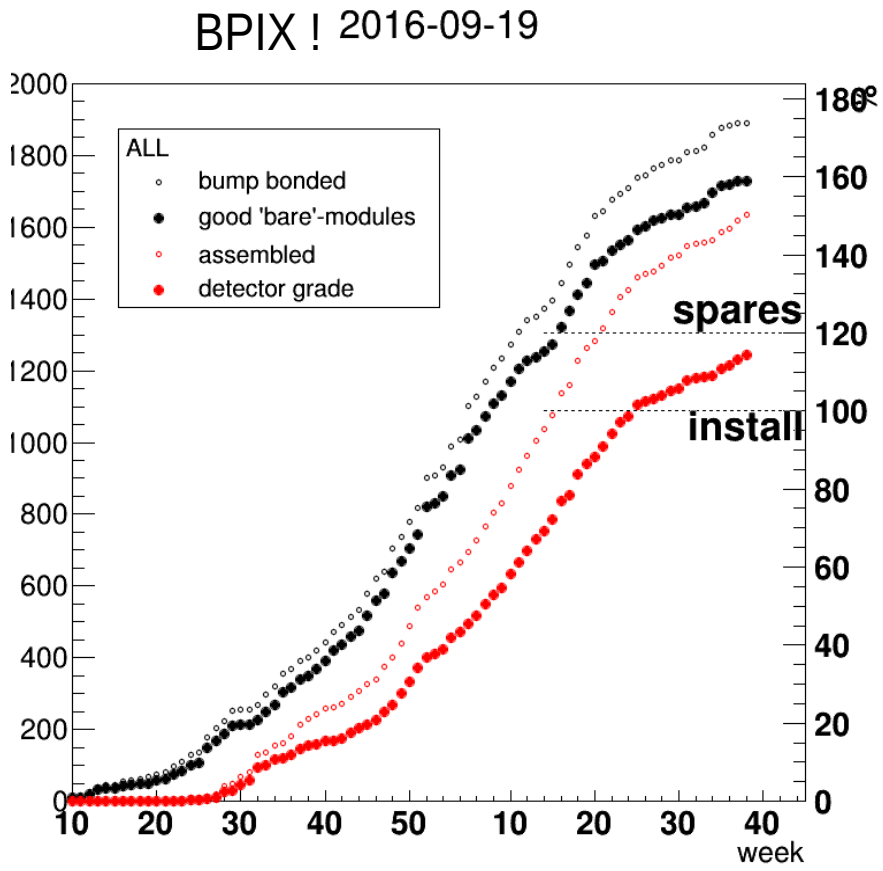
PIF = PSI proton Irradiation Facility

- high rate (up to 1.2 GHz/cm2) beam test with PROC600v2 chip with protons
- efficiency of ~97.5-98% at 600 MHz/cm2 for cluster sizes of ~2 pixels measured



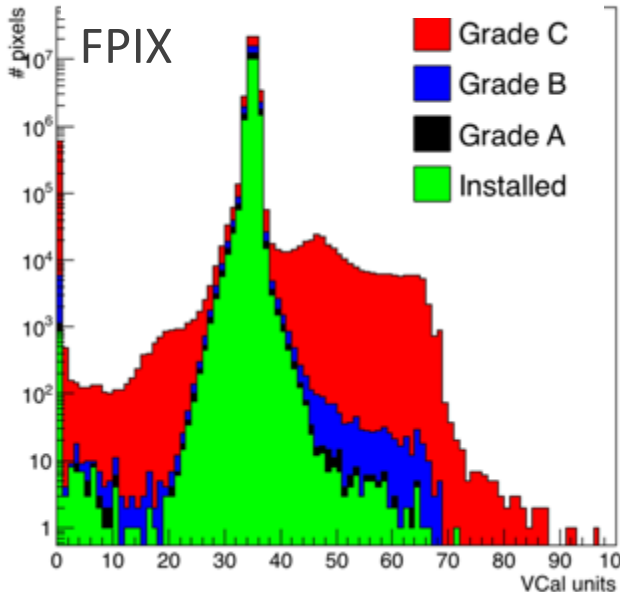
Module production



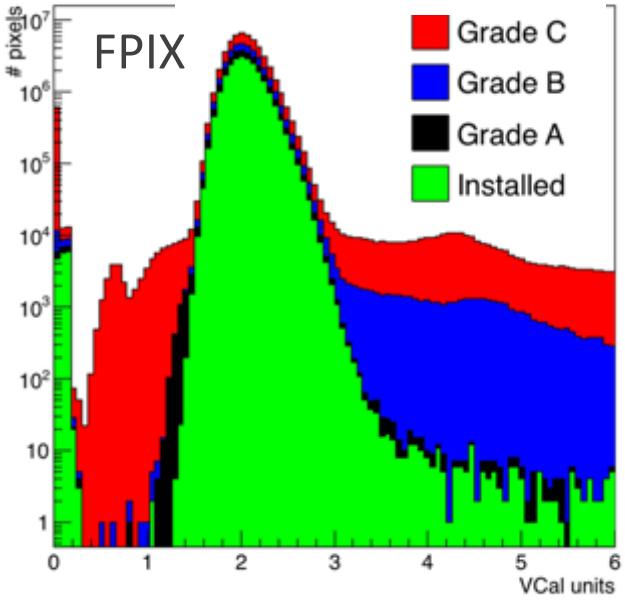


Module Production and Quality

Pixel turn-on threshold

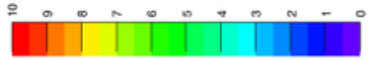


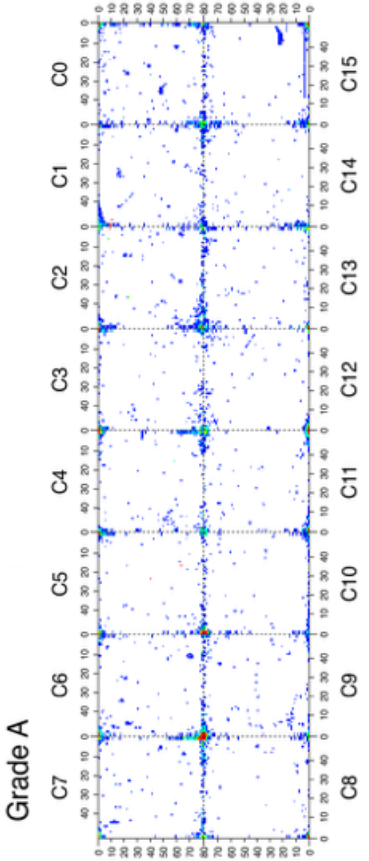
Pixel noise

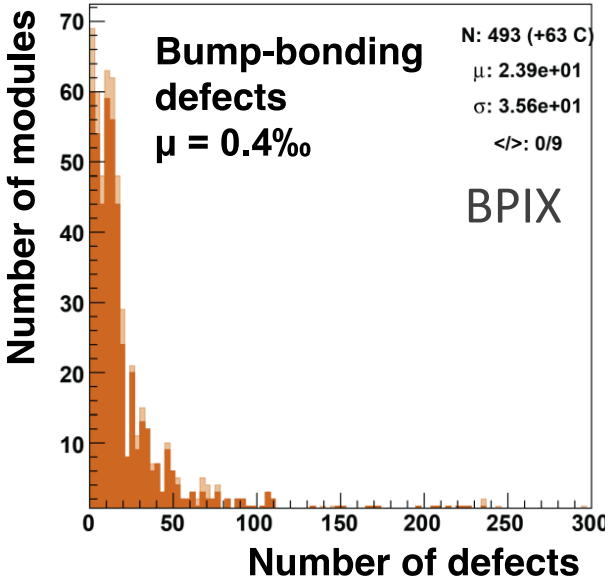


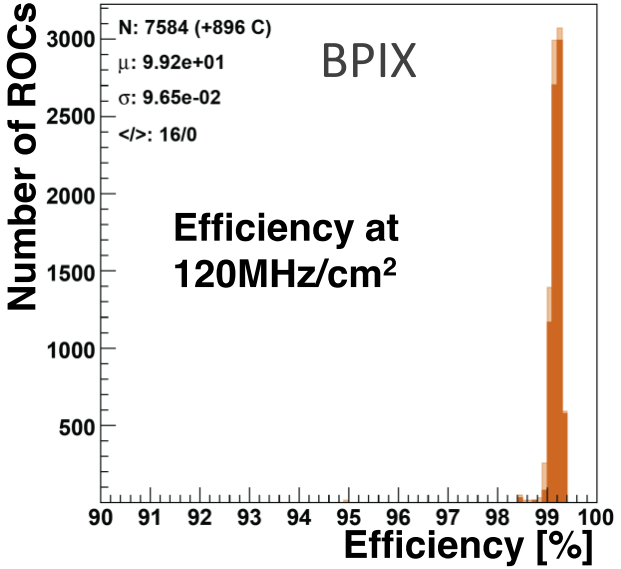
FPIX

bad bumps [O(1/1000)]
(sum of all modules)



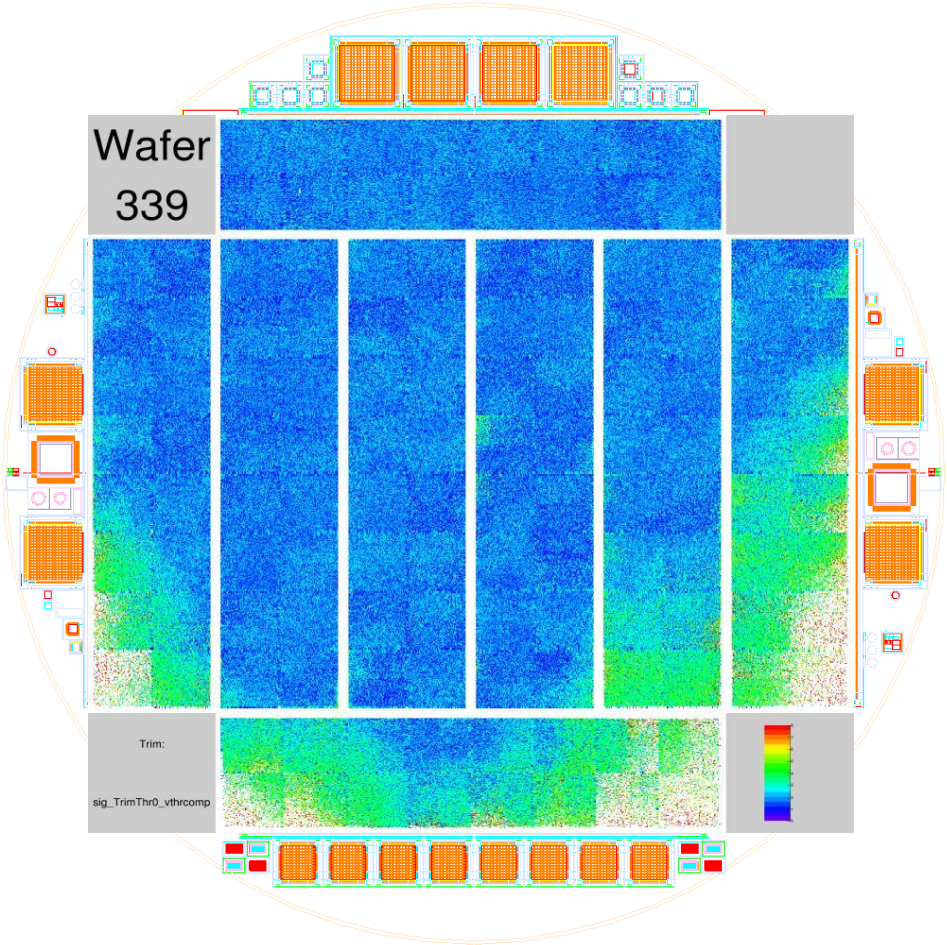






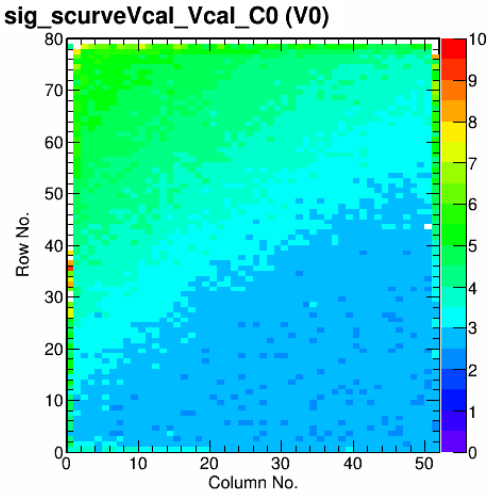
FPIX modules @ 300V (instead of 150V)

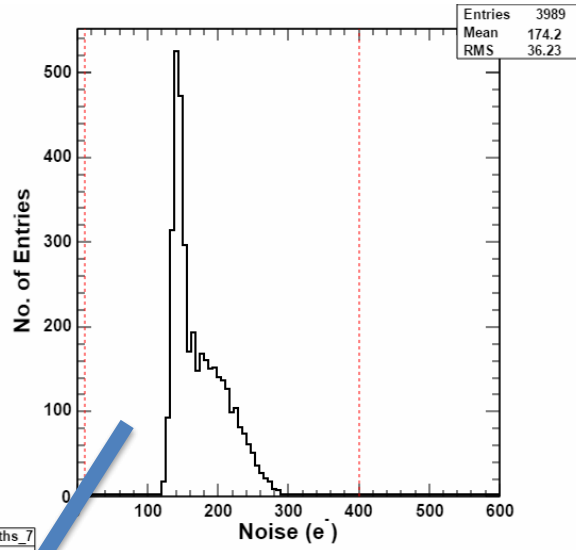
- Half of last batch of sensor wafers shows effects of surface traps that limit charge collection efficiency
- We have not found a cure for these modules
- Some installed in FPIX, operate 1 disk at 300 V
- What happens with irradiation ?

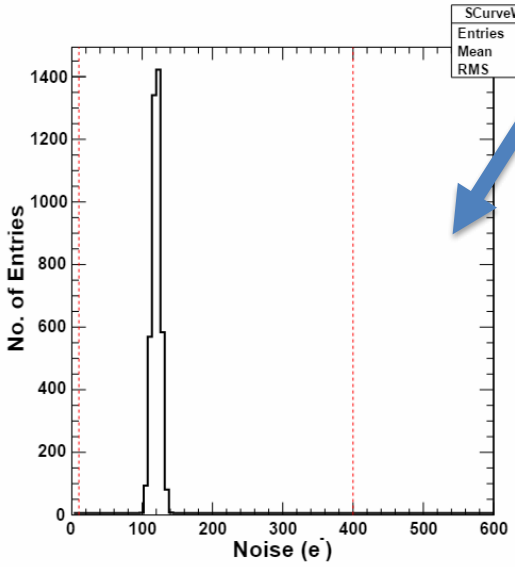


Irradiation helps!

- Have irradiated single chip assemblies (and control samples) to doses corresponding to 10 fb^{-1}, 70fb^{-1} and 300 fb^{-1}
  - Many thanks to the Karlsruhe group for the irradiation and for letting us use their facilities for the measurements

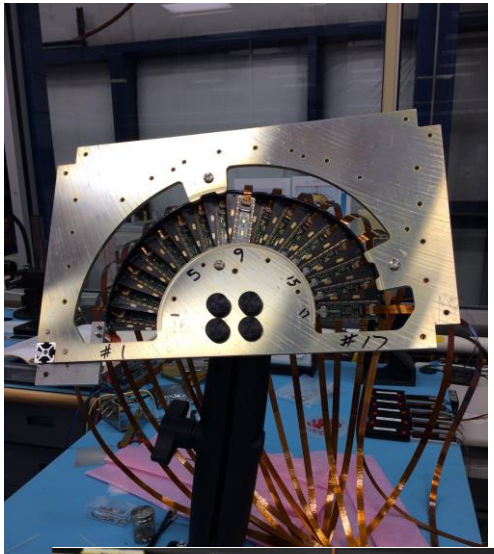


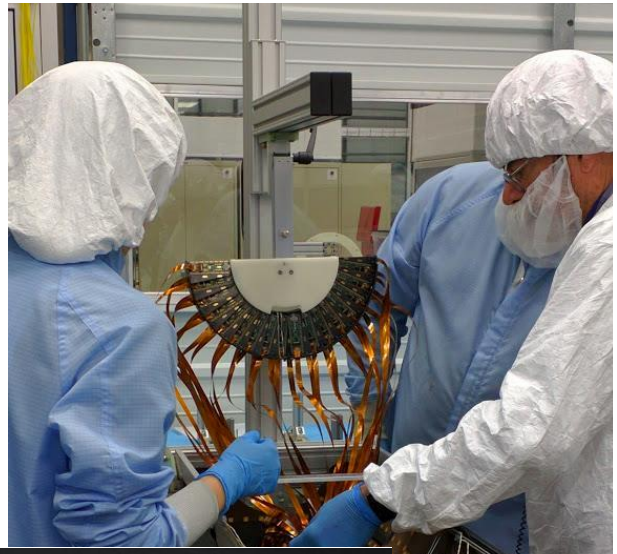


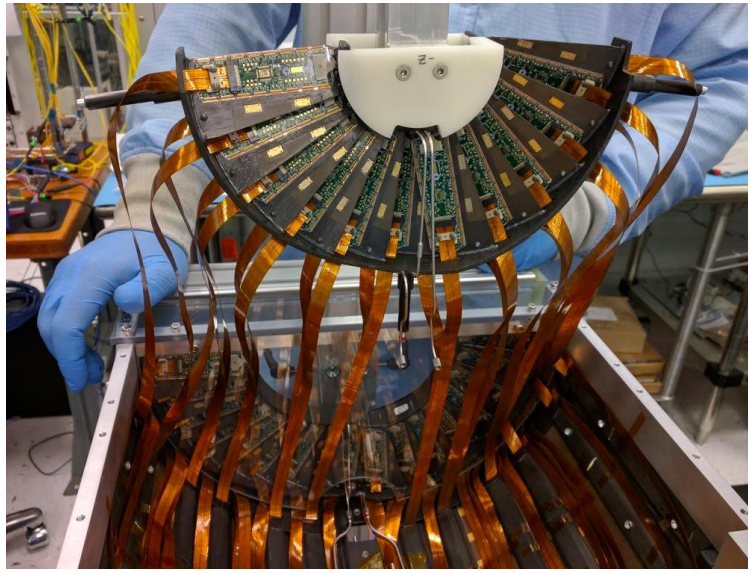


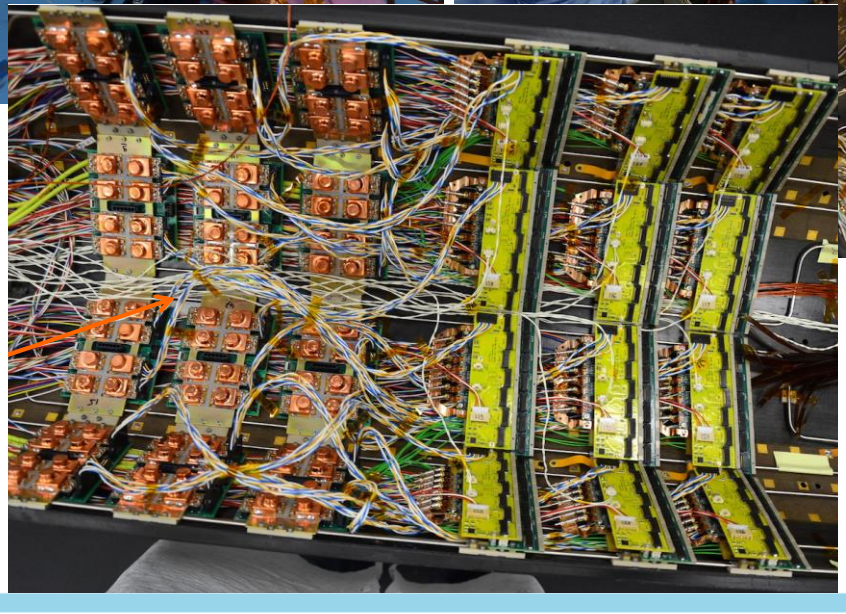
- After type inversion inefficiency / noise are gone
  - This sample irradiated to 10 fb^{-1}

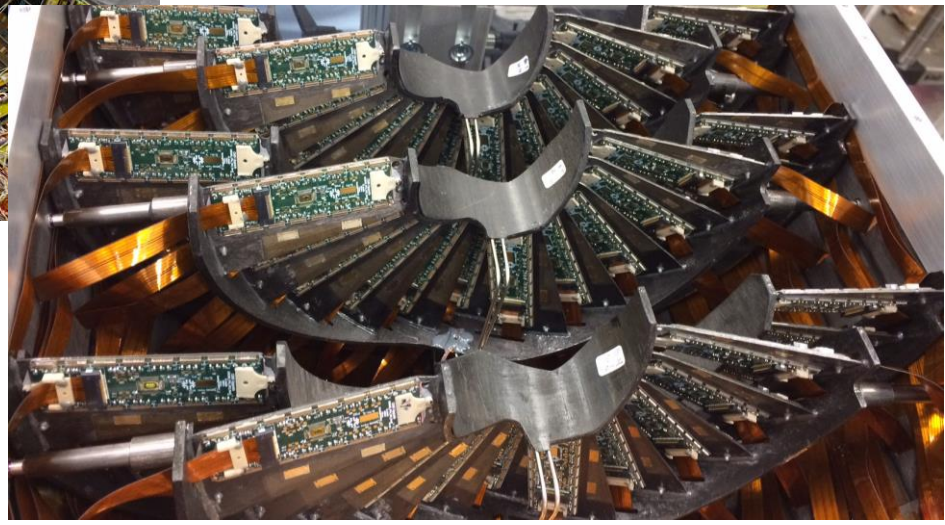
FPIX Detector Assembly at Fermilab







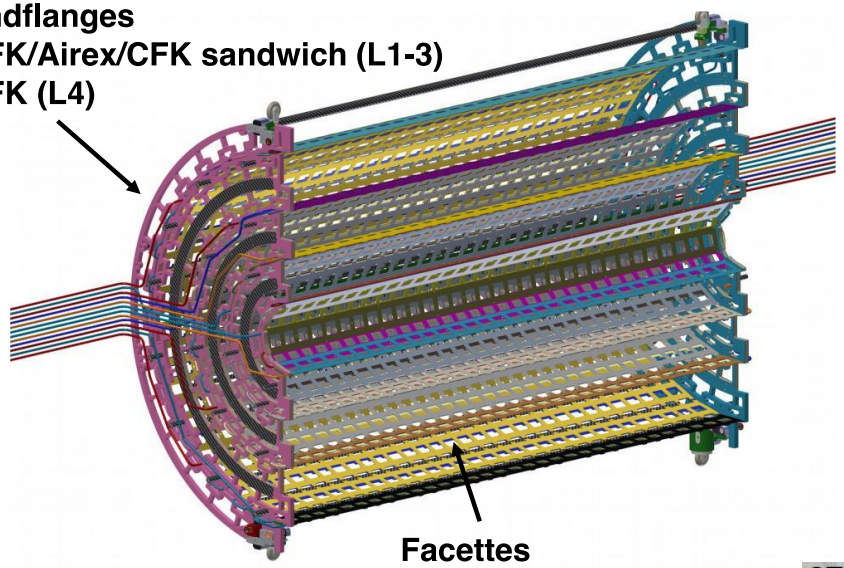


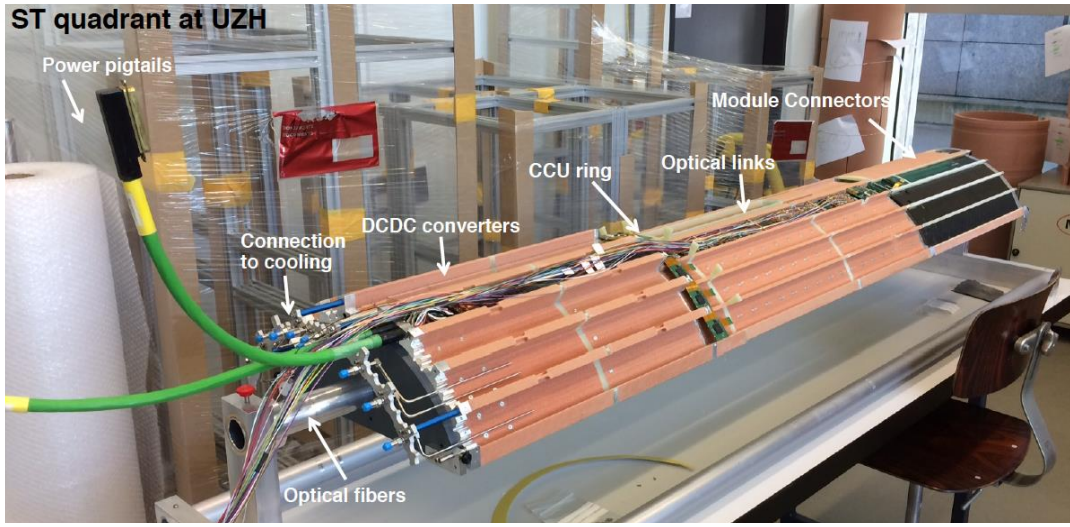


FPIX shipping and reassembly at CERN

- 1st and 2nd half cylinder at CERN, reassembled and tested
- 3rd half cylinder will be shipped this week, its disks on 11/2
- 4th half cylinder plus disks will be shipped week of 11/9

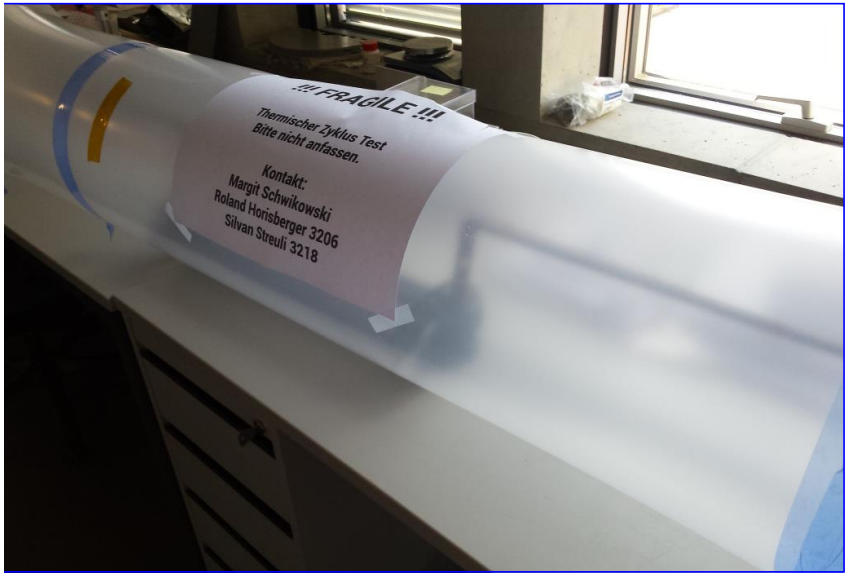
BPIX Detector Assembly at PSI

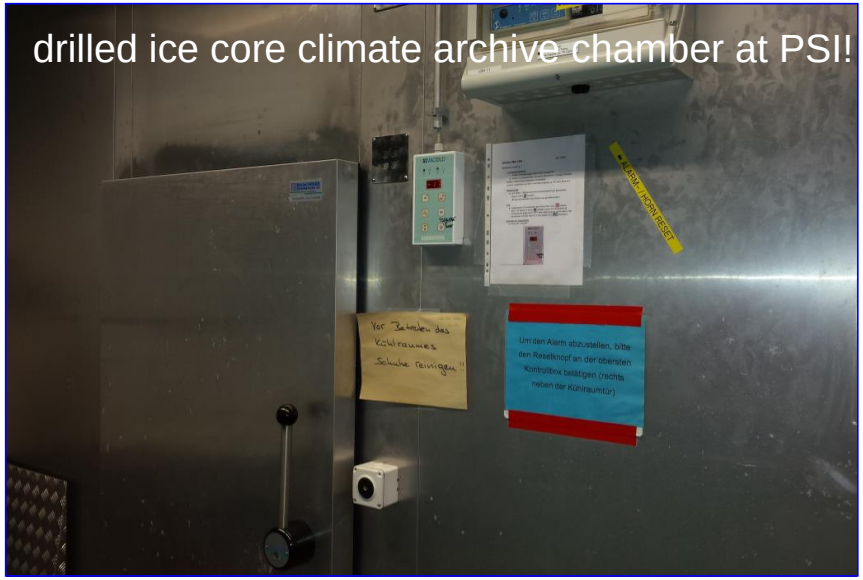




- Modules are screwed via base strips (L2-4) or clamped (L1) to CF facettes
- Cooling pipes running in groove below CF

Thermal cycling of mechanical structures





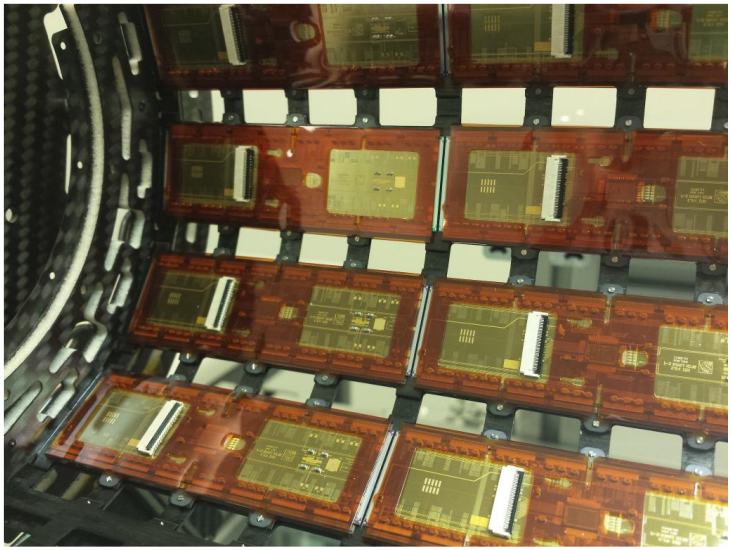
thermal cycling of BPIX mechanics design!

- check for delamination due do CTE missmatch!
- L1 half shell cycled 5 times [+25^{0}C, -18^{0}C] → ok!!

→ consider basic CTE design as sound !

- L2 half shell cycled 3 times [+25^{0}C, -18^{0}C] → ok!!
- continue thermal cycling of all half shells as QC ! !

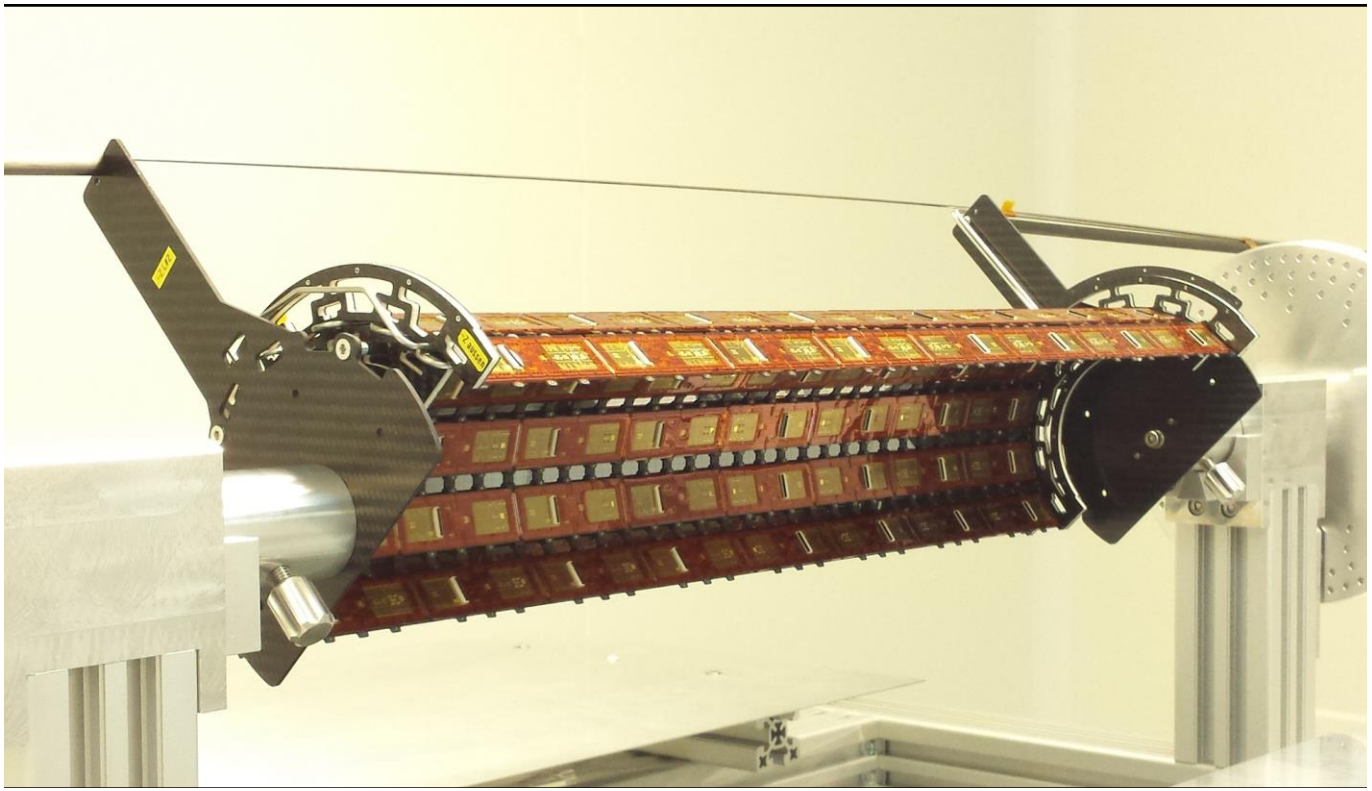
L2 module mounting

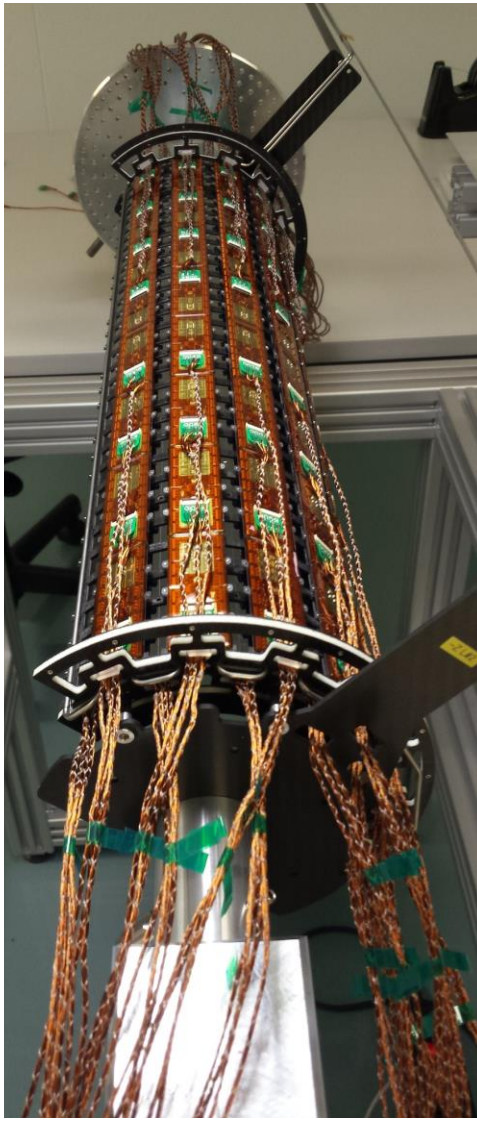


module mounting rate ~ 80 modules/day!

(based on L2 and L3 module mounting)!

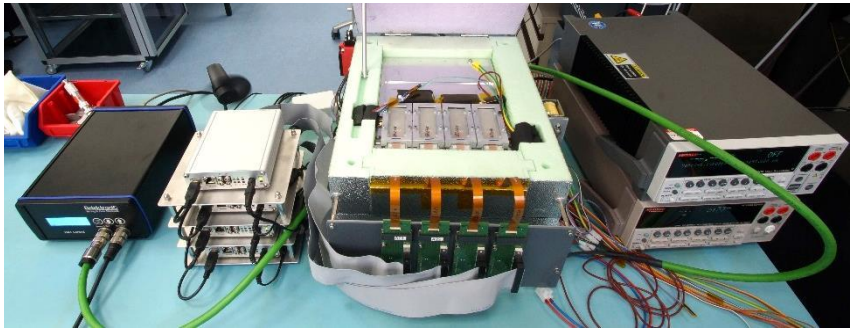
Completed L2

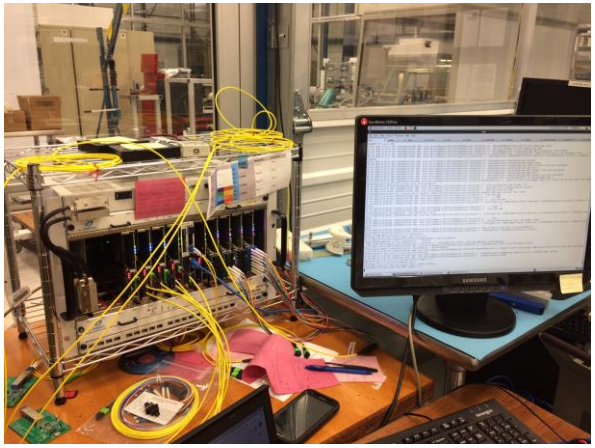


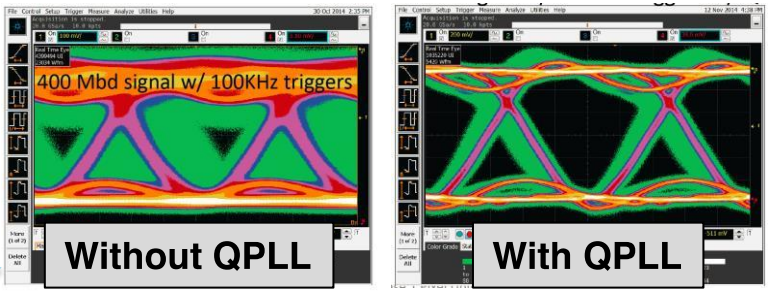


Commissioning and μTCA DAQ

- All modules are fully qualified and calibrated at -20ºC on the bench
- Full readout chain tested with final components in situ after assembly
- New DAQ system (μTCA instead of VME)
- Time for calibration inside CMS very short/non-existent before LHC turns on
- Close to final calibrations performed in cleanroom at CERN before installation
- Might include one quarter of FPIX into CMS cDAQ (from surface) to exercise whole chain
- Already gained invaluable experience with pilot system (a few FPIX modules installed in 3rd disk position of current detector (since LS1)







Summary

- CMS will replace its pixel detector in early 2017
- This will maintain high quality physics data taking until HL-LHC upgrades
- Newly designed readout chip, CO_2 cooling, almost double the number of pixels, new DAQ technology; all within the framework of the existing infrastructure and power supplies
- Module production almost finished
- Detector assembly progressing well, scheduled to finish next month