Institut des Nanotechnologies de Lyon UMR 5270

Novel 3D SPAD architecture in an advanced FDSOI technology

*Francis Calmon, Matteo Vignetti **

October 21, 2016

(WP2 ESR PhD student)*

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Content

- **Short introduction on SPAD**
- **Concept : SPAD integration in CMOS FDSOI technology**
- **TCAD study**
  - Breakdown Voltage and Premature Edge Breakdown
  - Noise - Dark Count Rate
  - Photon Detection Probability
- **Towards matrix implementation**
- **Conclusion and perspectives**

SPAD: Single Photon Avalanche Diode
FDSOI: Fully Depleted Silicon On Insulator
CMOS: Complementary Metal Oxide Semiconductor
TCAD : Technology Computer Aided Design

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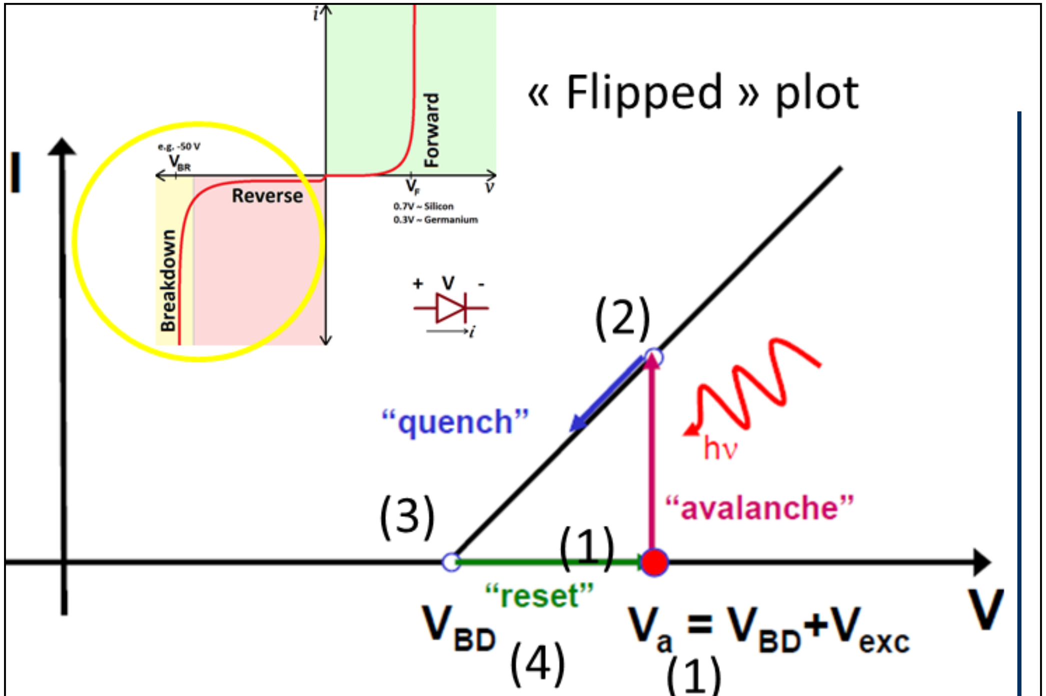
Introduction on SPAD (also called Geiger-mode avalanche diode)

Working principle

- p-n junction reverse biased above the breakdown voltage :
  $V_{BD} + V_{exc}$ (1)
- an electron-hole pair generated by a photon/particle in the space charge region can trigger an avalanche (due to multiplication process by impact ionization)



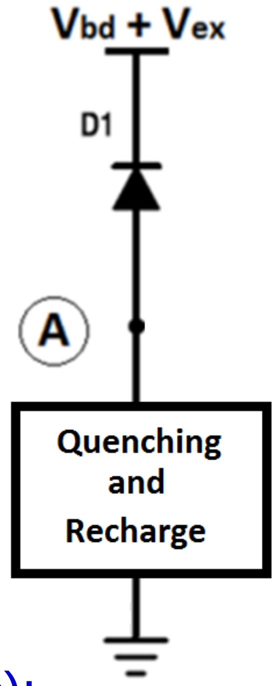
Cova et al. http://home.deib.polimi.it/cova/elet/Articoli%20e%20presentazioni/2013SPADlab_SSN.pdf

- a macroscopic electrical current is produced in the diode which can be easily detected by a read-out electronics (2)
- a dedicated electronics is needed to quench the breakdown process right after the avalanche by promptly lowering the voltage across the diode below the breakdown voltage (3)
- the device is restored to the initial biasing and is ready to detect another photon (4)

Introduction on SPAD (also called Geiger-mode avalanche diode)

SPAD key-parameters and figures of merit:

- V_{BD} : breakdown voltage
- Noise / DCR : dark count rate
- *PDP* : photon detection probability (visible light to infrared)
- Jitter : time variation
- Fill factor : sensing area over occupied area
- …



Applications (high-timing resolution and high-dynamic):

- Consumer devices: Time of Flight (TOF), telemetry, 3D vision systems …
- Medical application: fluorescence lifetime imaging microscopy (FLIM), … medical physics (e.g. proton therapy: dosimetry, beam control, pCT)
- Physics: Light Detection and Ranging (LIDAR), time-correlated single-photon counting (TCSPC) … high energy physics (particle tracking) …

Introduction on SPAD (also called Geiger-mode avalanche diode)

SPAD implementation :

- in dedicated technologies : silicon or III-V material for infrared
- but also in standard silicon CMOS technology for consumer application ex. telemetry (near infrared 940nm),

With the need to increase the fill factor, the pitch, the photon detection efficiency … => towards 3D implementation => 2 tiers stacked

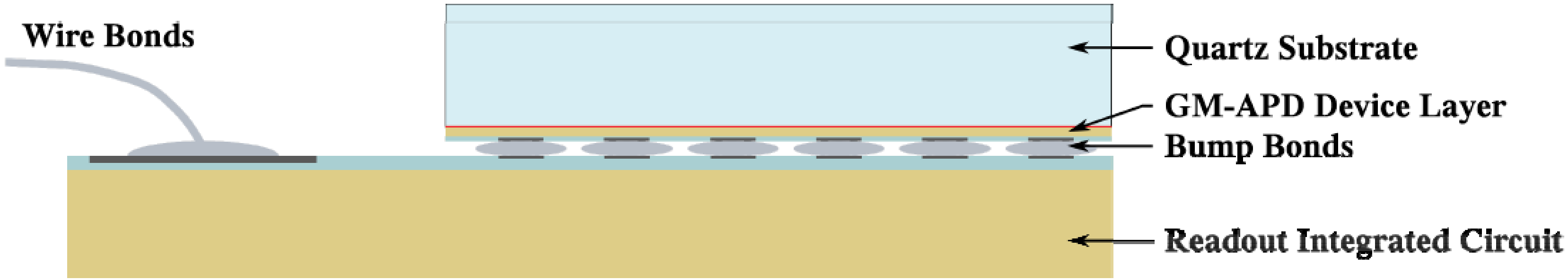


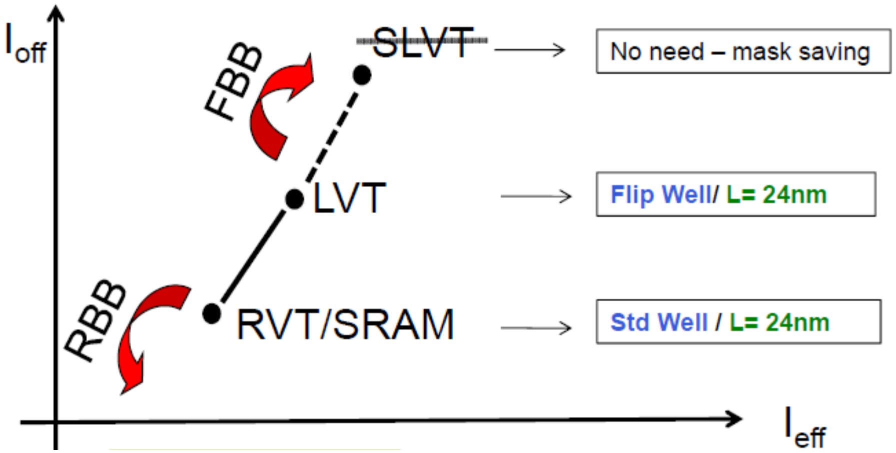
Figure 1: Cross section of the hybrid GM-APD detector assembly illustrating the relative locations of the quartz substrate, the thin GM-APD device layer, the CMOS ROIC and the wirebonds for the control and readout of the device.

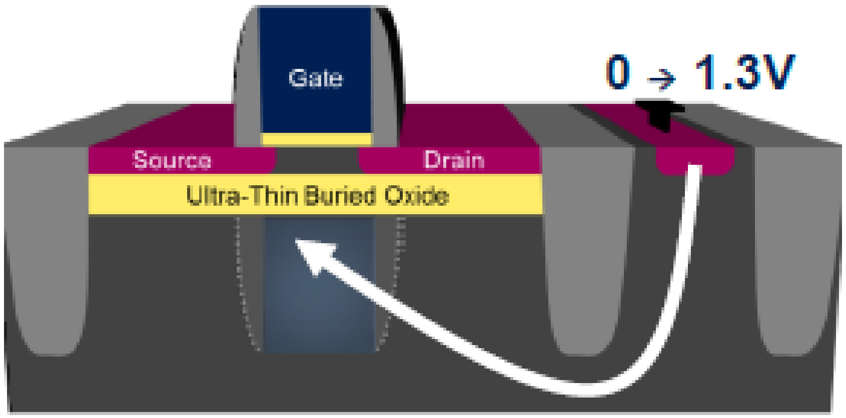
[D.R Schuette et al. "Hybridization process for back-illuminated silicon Geiger-mode avalanche photodiode arrays" 2016]

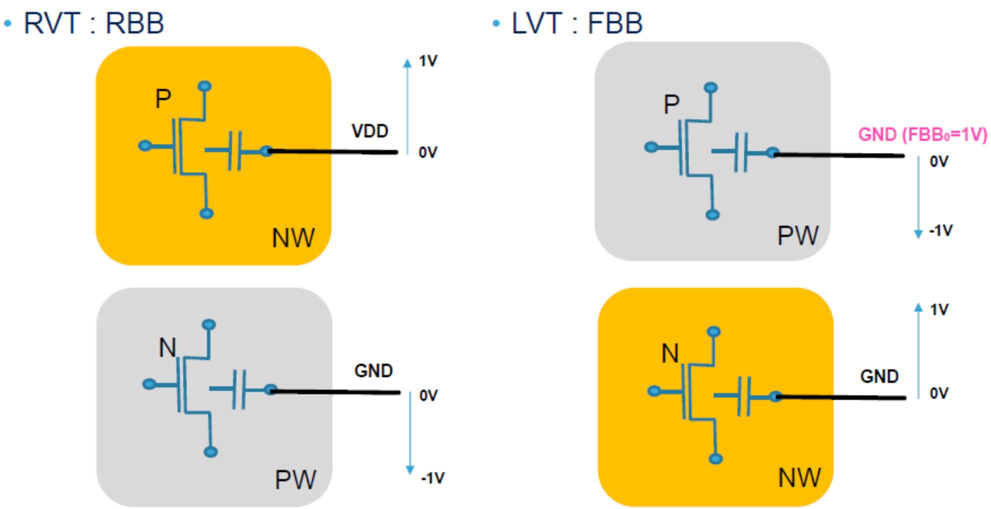
Content

Concept : SPAD integrated in FDSOI

STMicroelectronics has introduced : CMOS 28nm FDSOI technology with ultra thin buried box - UTBB featuring transistor back biasing and different transistor families: RVT as Regular V_T, LVT as Low V_T (and associated libraries)





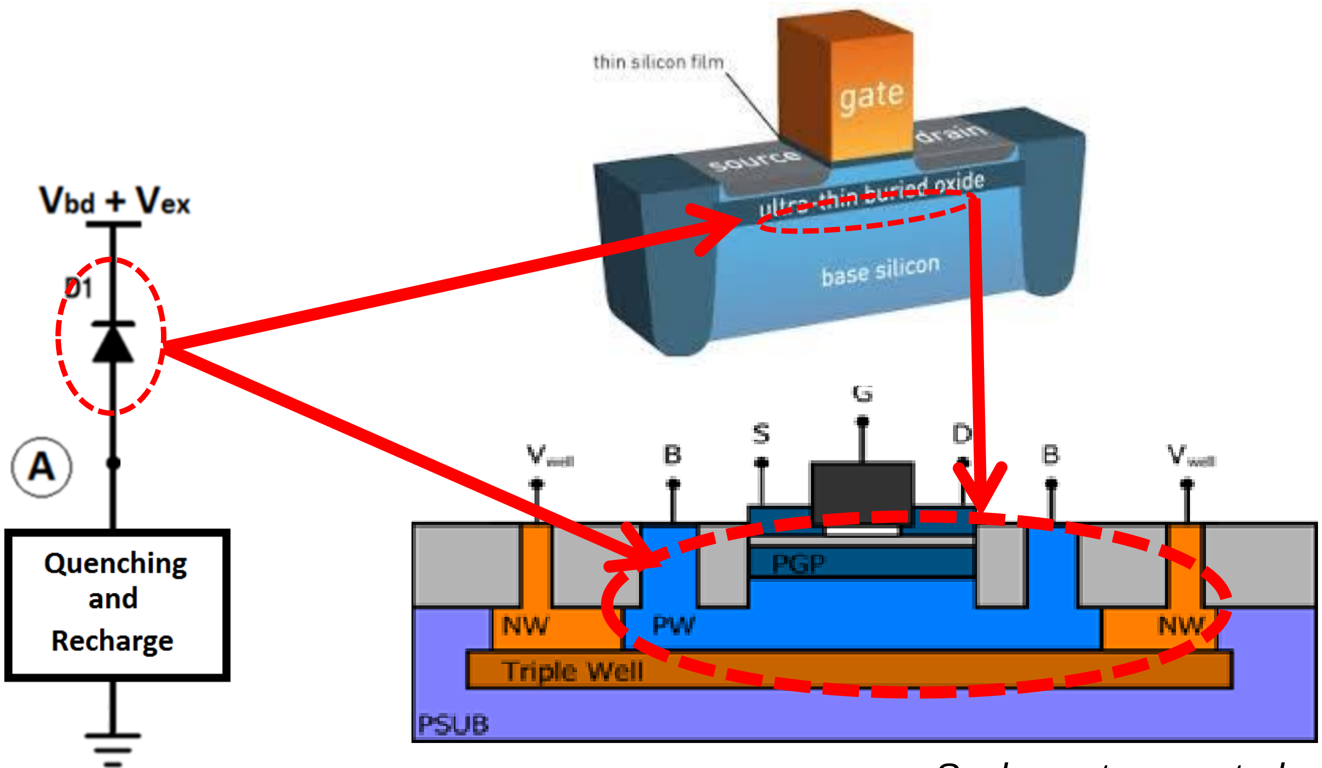


High performance / speed

and ultra low power

in the same CMOS platform

Concept : SPAD integrated in FDSOI

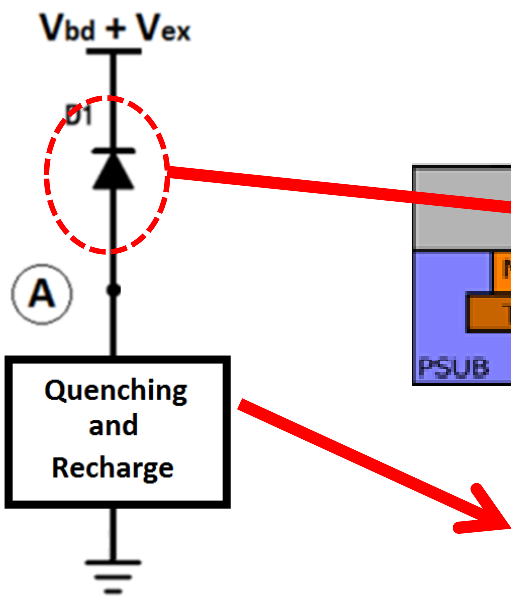


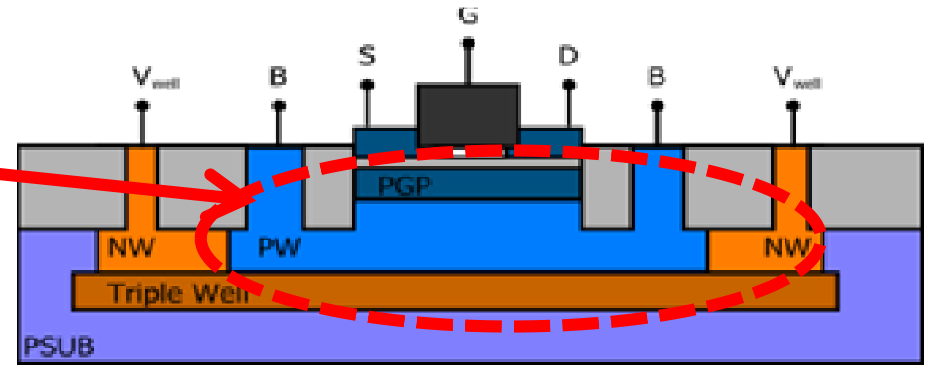
Scales not respected

our proposal :

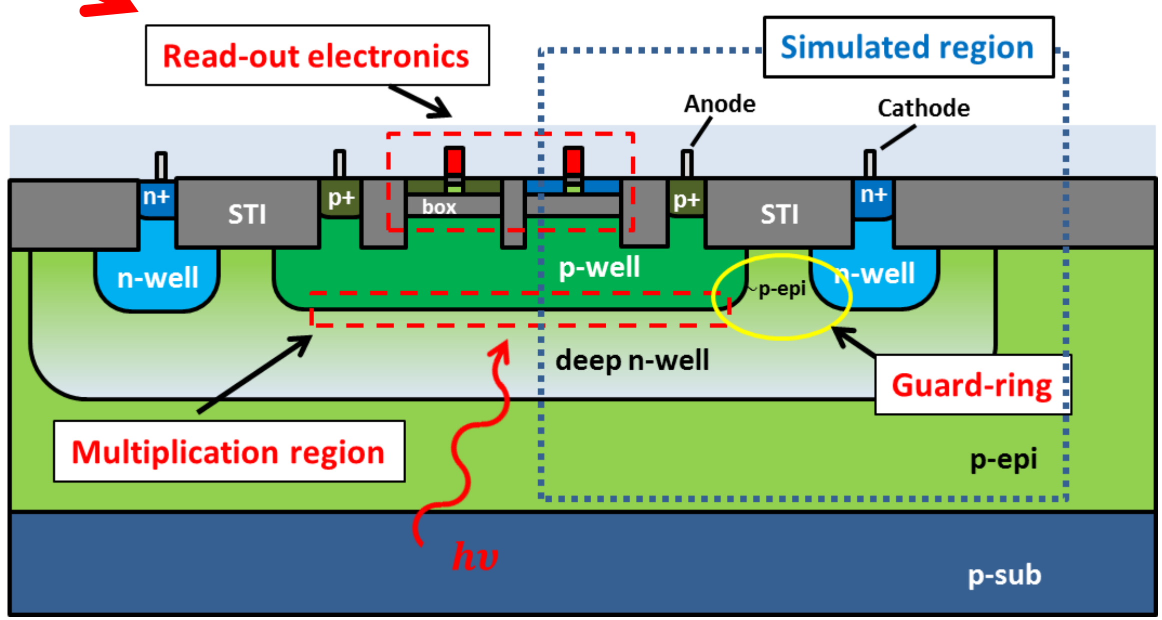
why not integrating the diode below the buried box using the different layers initially dedicated to the transistor back biasing to realize a 3D pixel (sensing area below the box + readout electronics on top)

Concept SPAD integrated in FDSOI





Scales not respected



TCAD study ←

Rk. back side illumination

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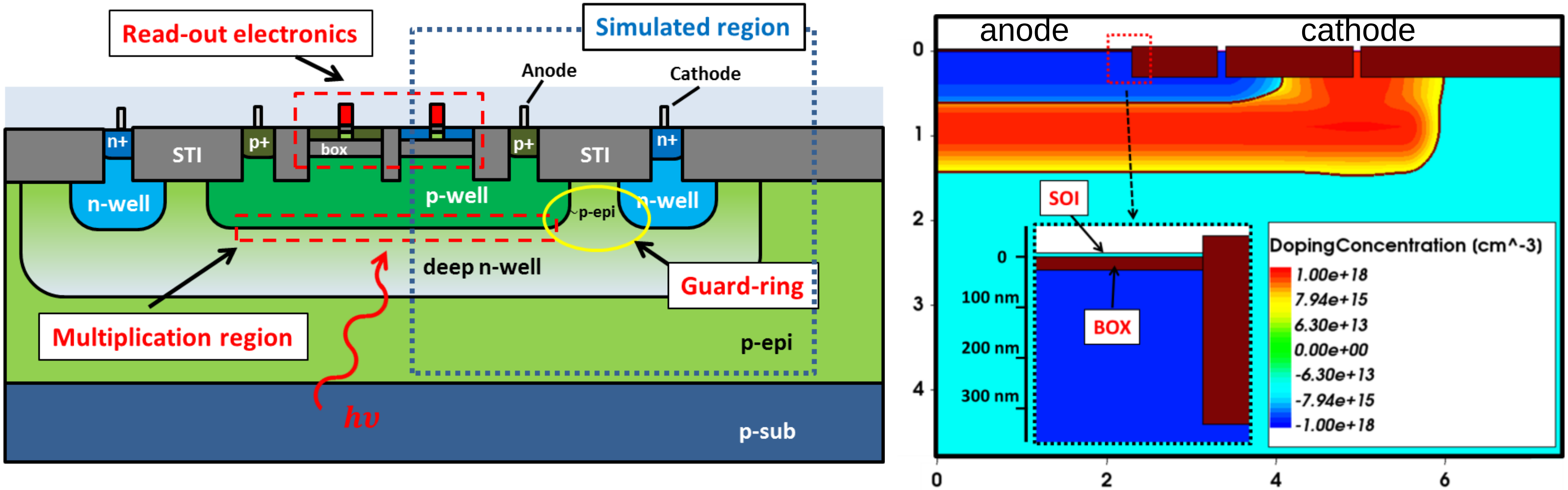
TCAD study : Electrical field, breakdown voltage (V_{BD})

½ diode (cylindrical symmetry) described in TCAD environment : doping profiles …

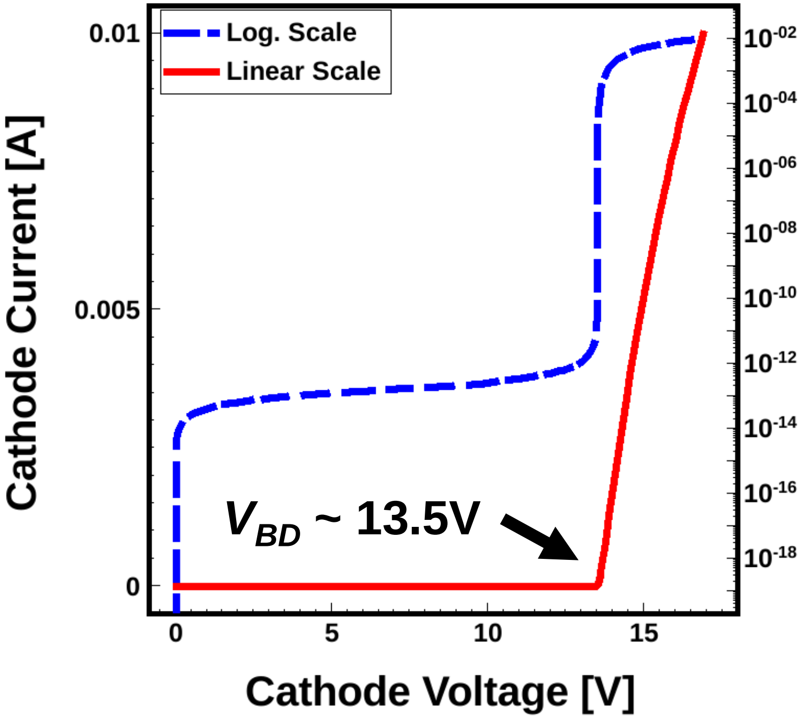


a) b)

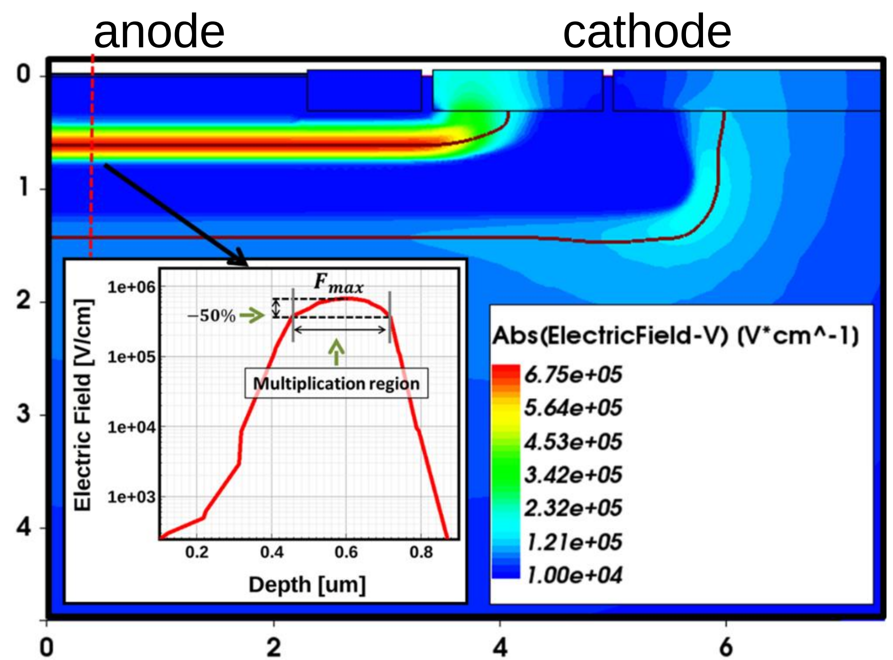
Schematic representation of (a) the proposed 3D SOI pixel and (b) its associated TCAD model. (positive values refer to n-type doping. Spatial scales are in μm)

[M.M. Vignetti et al. Conf. eurosoi-ulis 2016]

TCAD study : Electrical field, breakdown voltage (V_{BD})



TCAD Simulation: Reverse bias I-V curve of the avalanche diode.
(Sensitive area diameter $D = 7\mu m$)



TCAD Simulation: Electric field color map of the pixel, when the avalanche diode is reverse biased at $V_{rev} = 16.5\ V$ (Spatial scales are in μm)

V_{BD} ~ 13.5V

Geometry is optimized to avoid Premature Edge Breakdown – PEB, i.e. uniform E-field in the sensing region – no hot spot ☑

[M.M. Vignetti et al. Conf. eurosoi-ulis 2016]

TCAD study and post-processing

Post-processing will allow to extract :

- **Avalanche triggering probability**
- **Noise - Dark Count Rate**
- **PDP - Photon Detection Probability - Efficiency**

TCAD simulation

- Electrostatics Analysis (Electric Field distribution)
- Diode reverse bias I-V curve (breakdown voltage extraction)

- ionization coefficients for electrons and holes(α_e, α_h)
- Electron – Hole pair generation rates (G_{SRH}, G_{B2B})

↓

Post-processing

- Avalanche Triggering Probability (P_{tr})
- Dark Count Rate (DCR)
- Photon Detection Probability (PDP)

$$P_{tr}(x) = P_e + P_h - P_e P_h$$

[R. J. McIntyre IEEE TED, 1973]

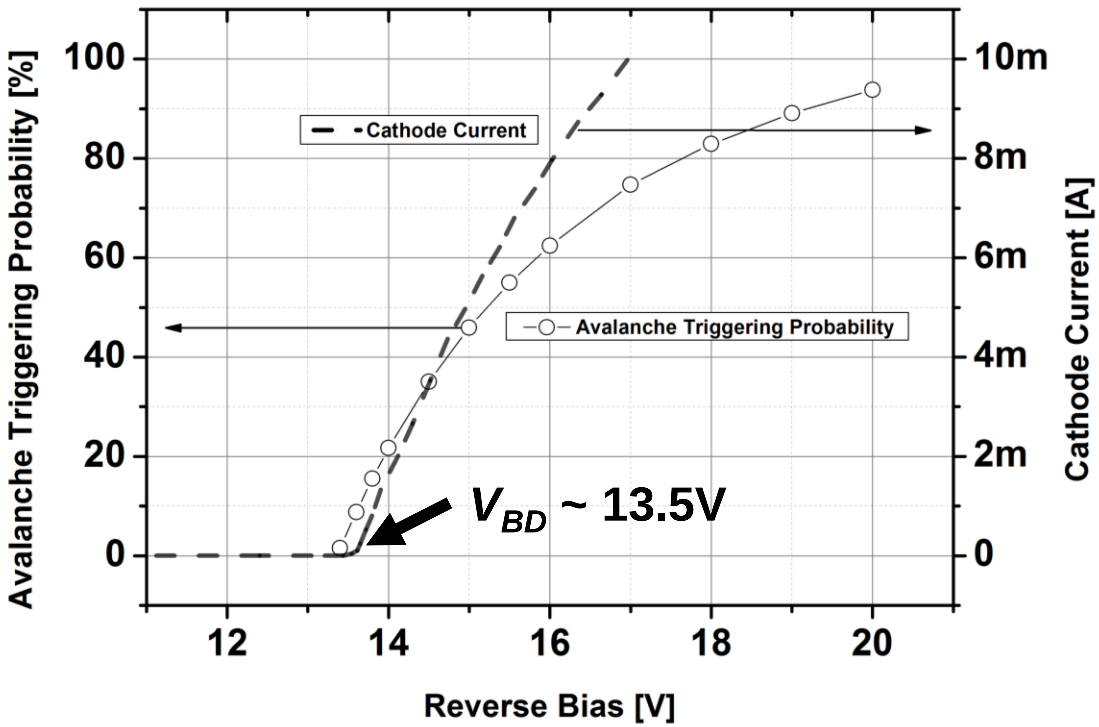
$$\overline{P_{tr}} = \frac{1}{x_n - x_p} \int_{x_p}^{x_n} P_{tr}(x)\, dx$$

$$DCR = \int_{x_p}^{x_n} P_{tr}(x) G_{EHP}(x)\, dx$$

$$PDP(\lambda) = \int P_{tr}(x) p_{abs}(x, \lambda) dx$$

[M.M. Vignetti et al. to be published Solid State Electronics]

TCAD study : avalanche triggering probability P_{tr}



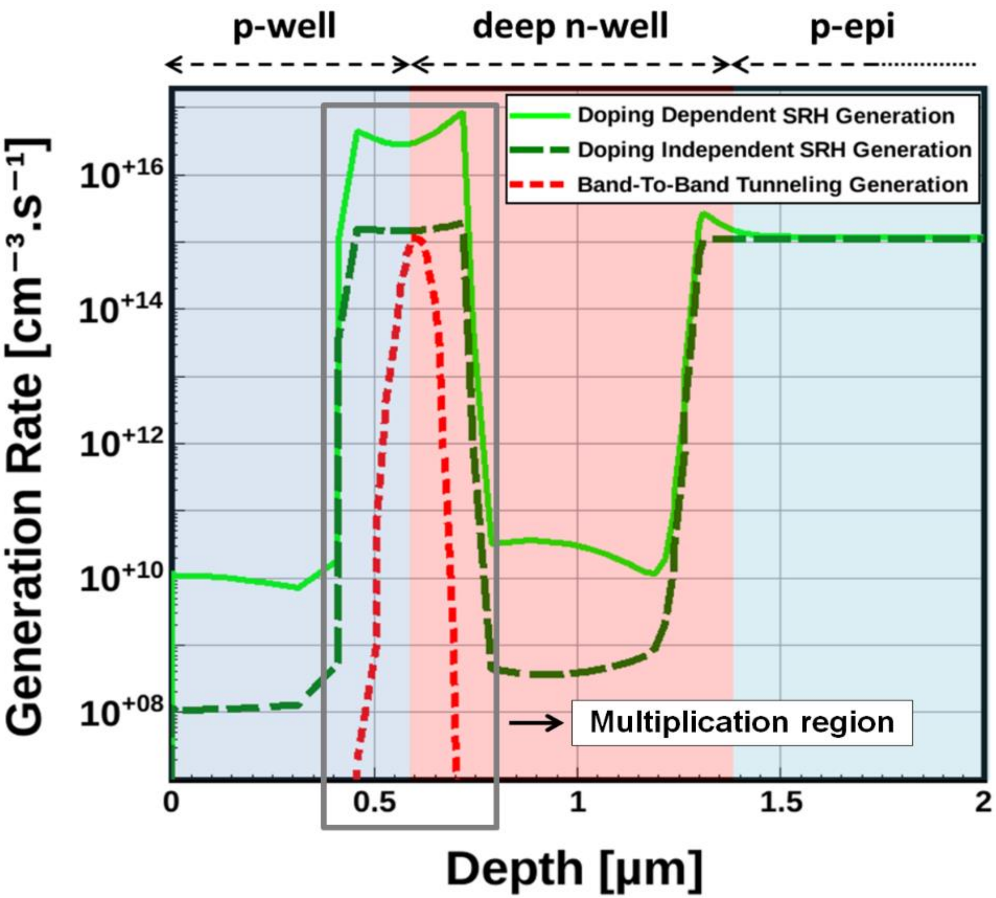
*Left : average avalanche triggering probability calculated according to the method proposed by [*R. J. McIntyre 1973*]. Right: reverse bias I-V curve of the avalanche diode*

[M.M. Vignetti et al. to be published Solid State Electronics]

Avalanche triggering probability is extracted in accordance to the reverse *I-V* curve

TCAD study : dark count rate - *DCR*

$$DCR = \int_{x_p}^{x_n} P_{tr}(x) G_{EHP}(x)\, dx$$

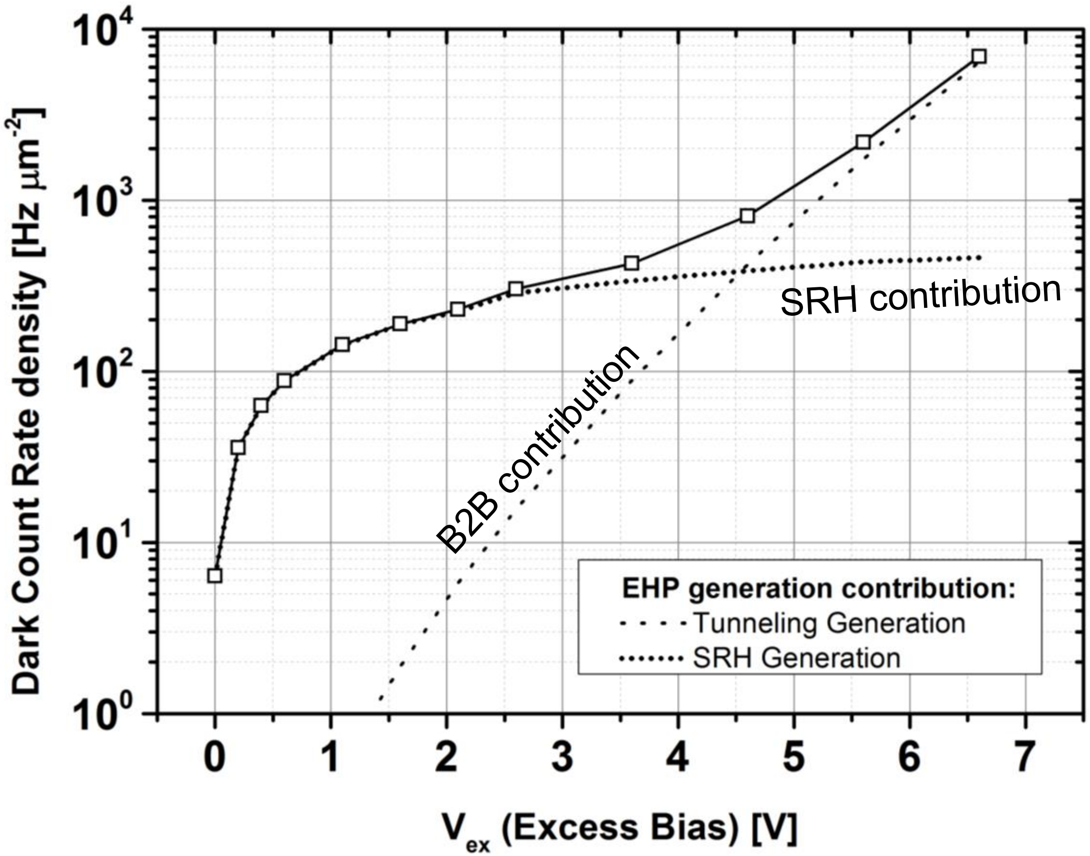


TCAD Simulation: e/h pair generation rates (for different mechanisms) in the multiplication region of the diode at $V_{rev} = 16.5V$

[M.M. Vignetti et al. to be published Solid State Electronics]

TCAD study: dark count rate - *DCR*

$$DCR = \int_{x_p}^{x_n} P_{tr}(x) G_{EHP}(x)\, dx$$

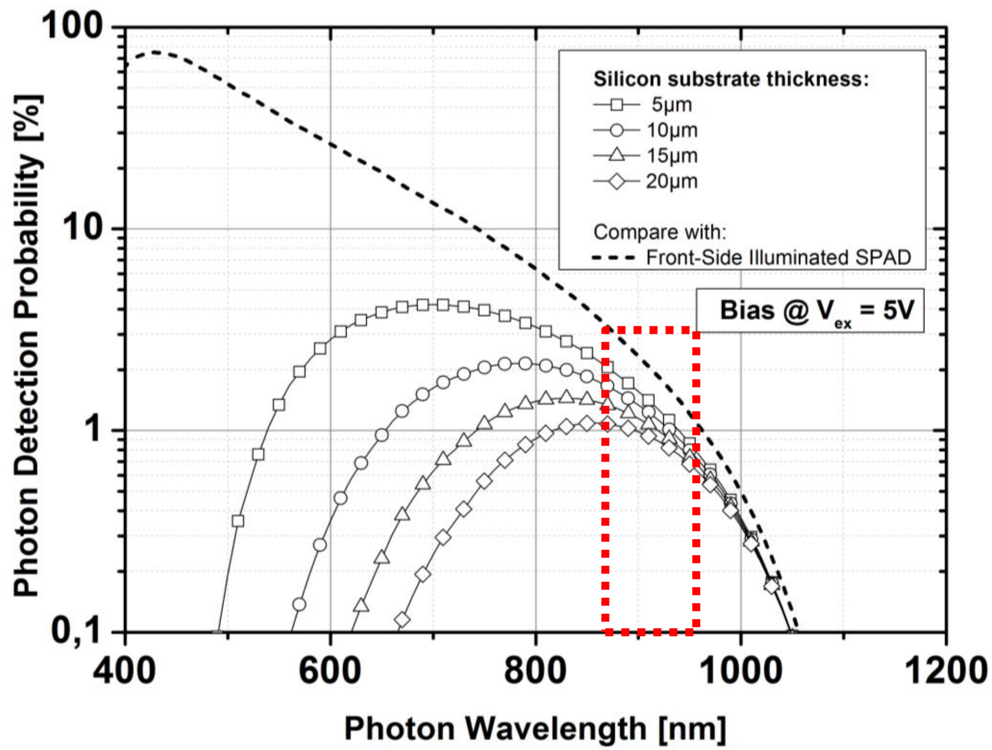


Total DCR per unit surface for the simulated avalanche diode (and contributions of SRH and band-to-band generation mechanisms)

[M.M. Vignetti et al. to be published Solid State Electronics]

TCAD study: photon detection probability (efficiency)

$$PDP(\lambda) = \int P_{tr}(x) p_{abs}(x,\lambda) dx$$



Photon detection probability for different substrate thicknesses with back-side illumination (and comparison with front-side illumination)

[M.M. Vignetti et al. to be published Solid State Electronics]

BSI FDSOI SPAD suitable for IR application (e.g. @ 940nm)

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TCAD : Technology Computer Aided Design
SPAD: Single Photon Avalanche Diode
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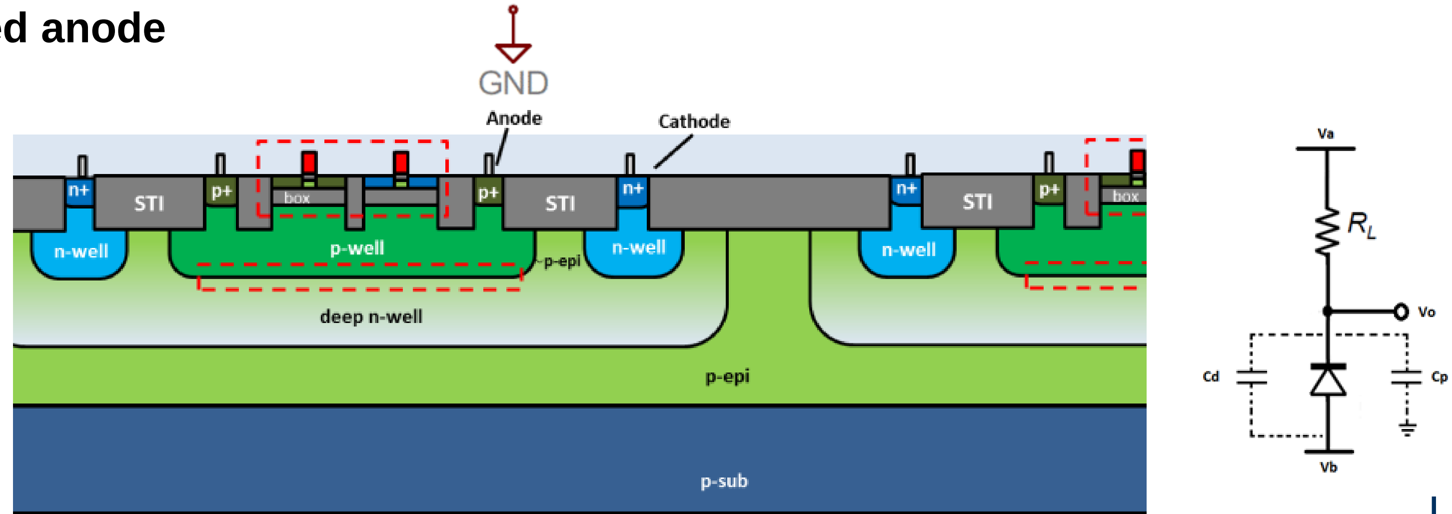
Towards matrix implementation

Solution (a): grounded anode

☺ **back-biasing insensitive solution**

☹ **fill-factor**



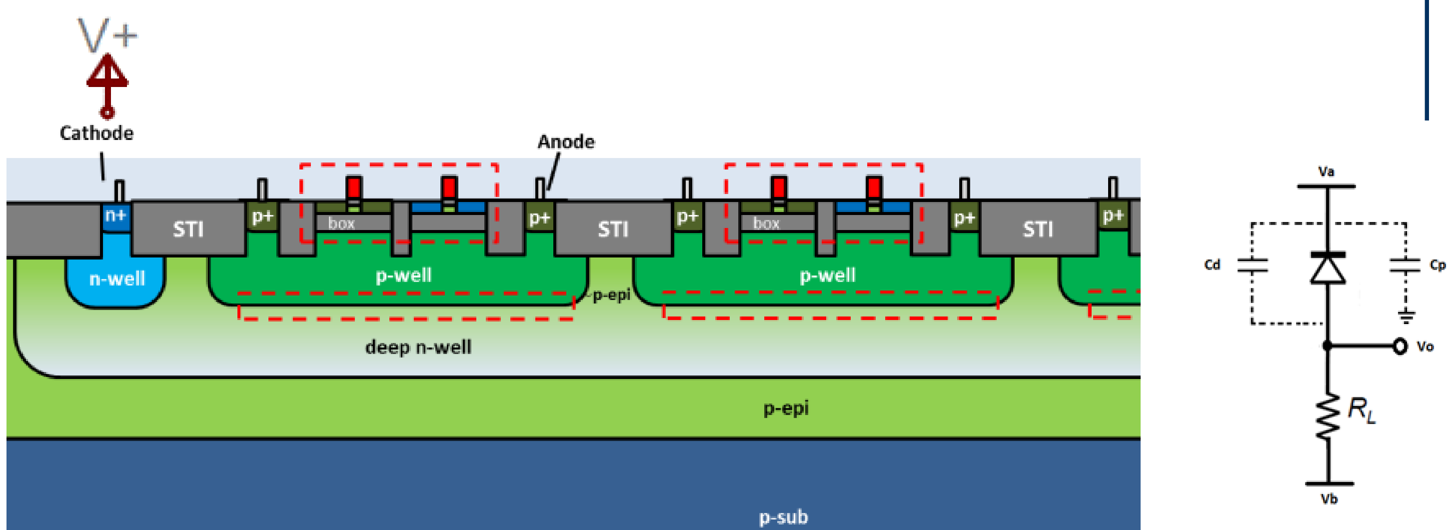
Solution (b):

common deep n-well (common cathode)

☺ **fill-factor**

☹ **anode is the moving node**

⇒ **back biasing but…**



[M.M. Vignetti et al. Conf. eurosoi-ulis 2016]

Towards matrix implementation

Solution (b):

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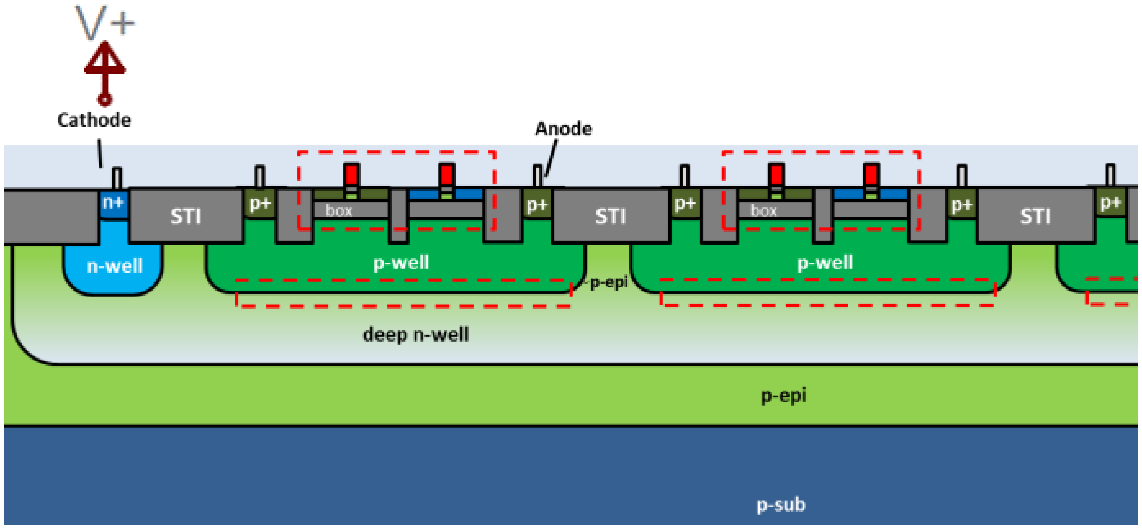

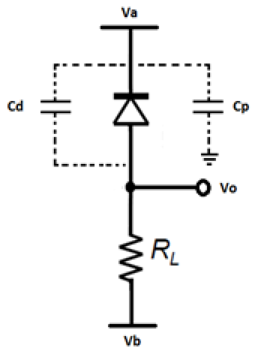

When event occurs : anode is moving

⇒ detection with TMOS as a sensor (current overshoot or …) ☺

⇒ isolated read-out (no need to interface the anode node) ☺

Conclusion and perspectives

- **Original concept of SPAD integration in CMOS FDSOI technology**
  - **due to intrinsic 3D architecture : very high fill factors are expected**
- **Preliminary TCAD results are promising e.g. IR detection**
- **Silicon test chip will be necessary to validate the concept**

… study to be continued …

Thank you for your attention

We would like to thanks the students involved in the TCAD study :
Teodoro Graziosi, Florian Dubois, Paul Lesieur, Clement Lauseker