JESD204B
High Speed ADC Interface Standard

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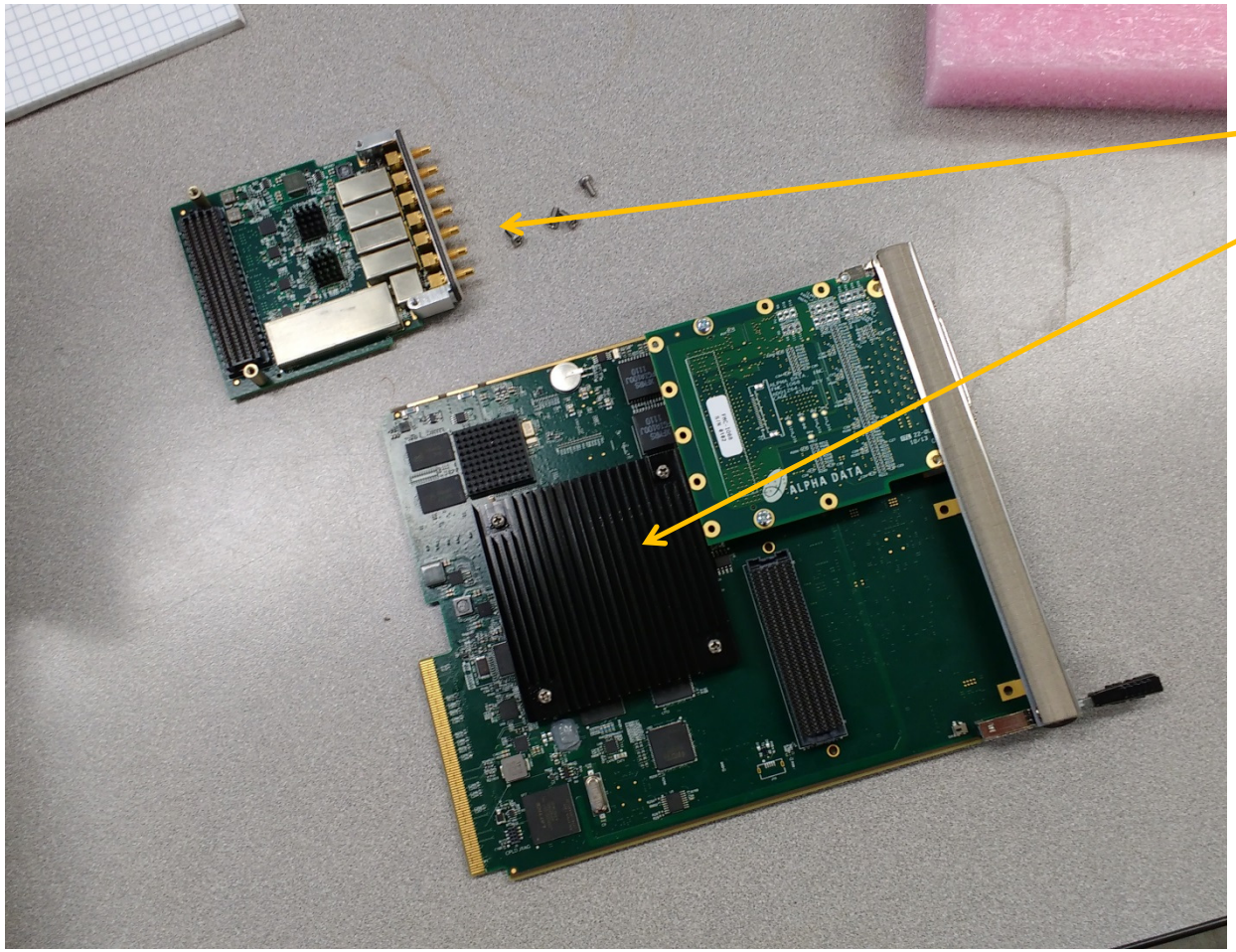
Introduction

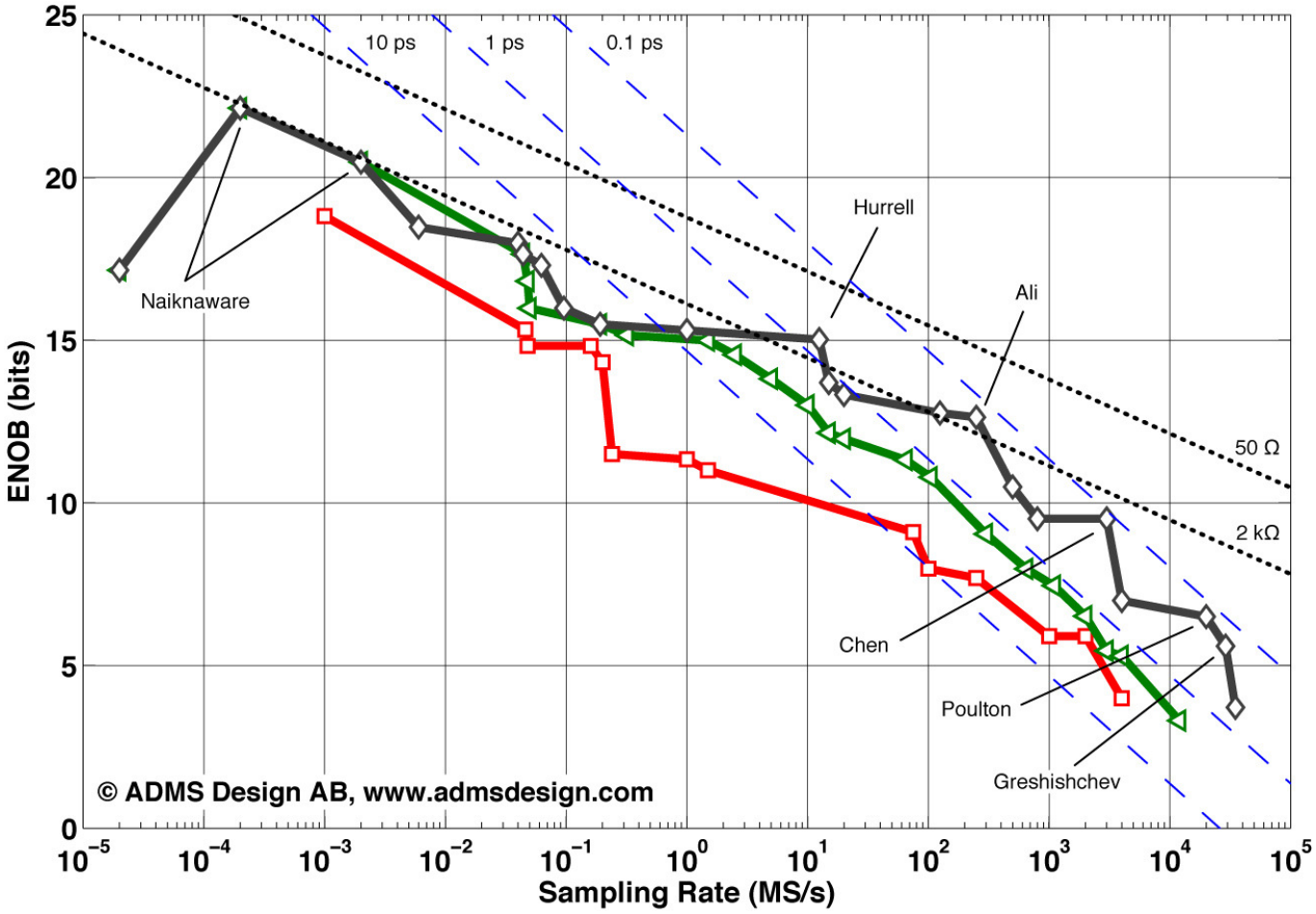
- Applications:
  - Medical imaging: ultrasound
  - **Digital oscilloscopes: PMT waveform digitization**
  - Software defined radio
  - Synthetic aperture radar
- Wide range of applications benefit from high speed (> 200 MSPS) analog-to-digital converters
  - Commercially available components
  - Commercially available modules
- Application development benefits from well-defined standards followed by multiple vendors

Introduction



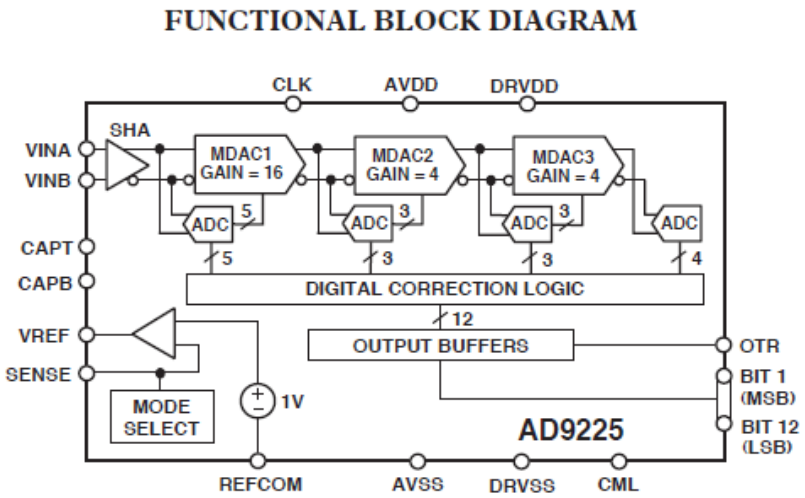
Vadatech
FMC228
AMC502

Analog to Digital Conversion



Data Interfaces

- Example: AD9225 (circa 1998)
  - One channel, 12-bits, 25 MSPS, 5V CMOS



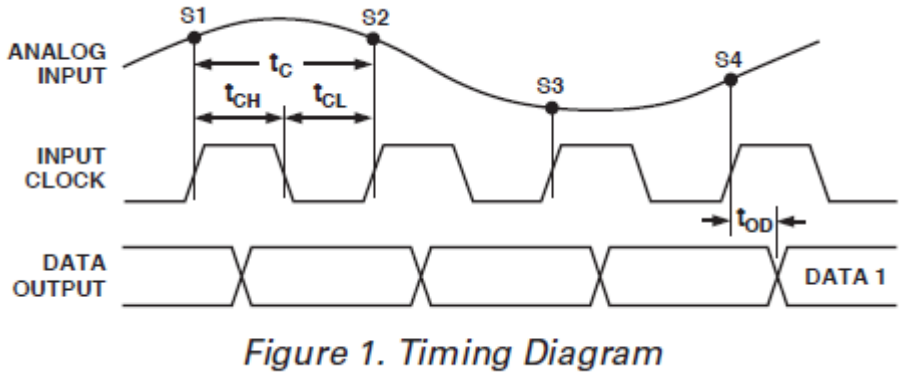
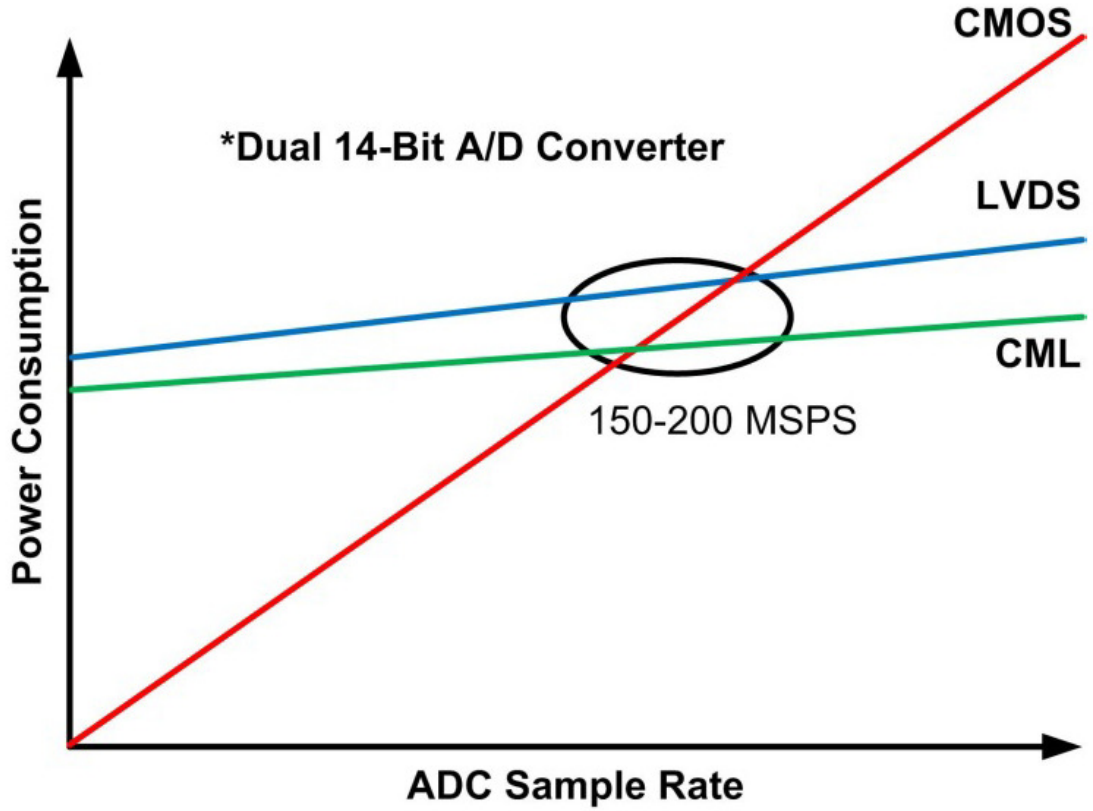


Figure 1. Timing Diagram

- Parallel interfaces become challenging above 100 MSPS due to noise, signal skew.

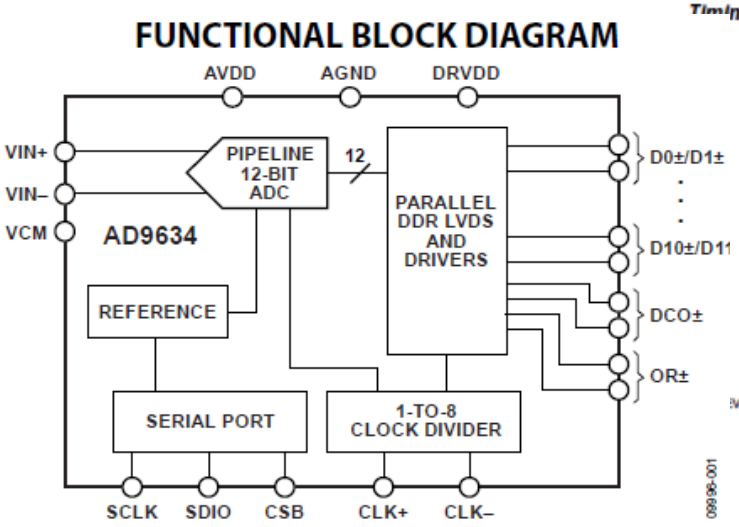
Data Interfaces

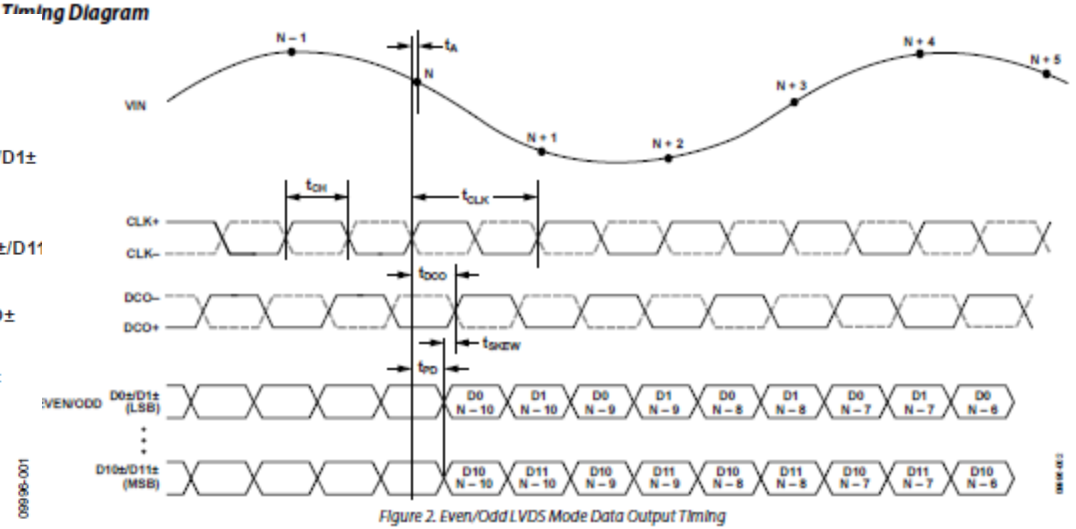
- Power dissipation is also a factor:



Data Interfaces

- Example: AD9634 (circa 2011)
  - One channel, 12-bits, 250 MSPS, 1.8V CMOS

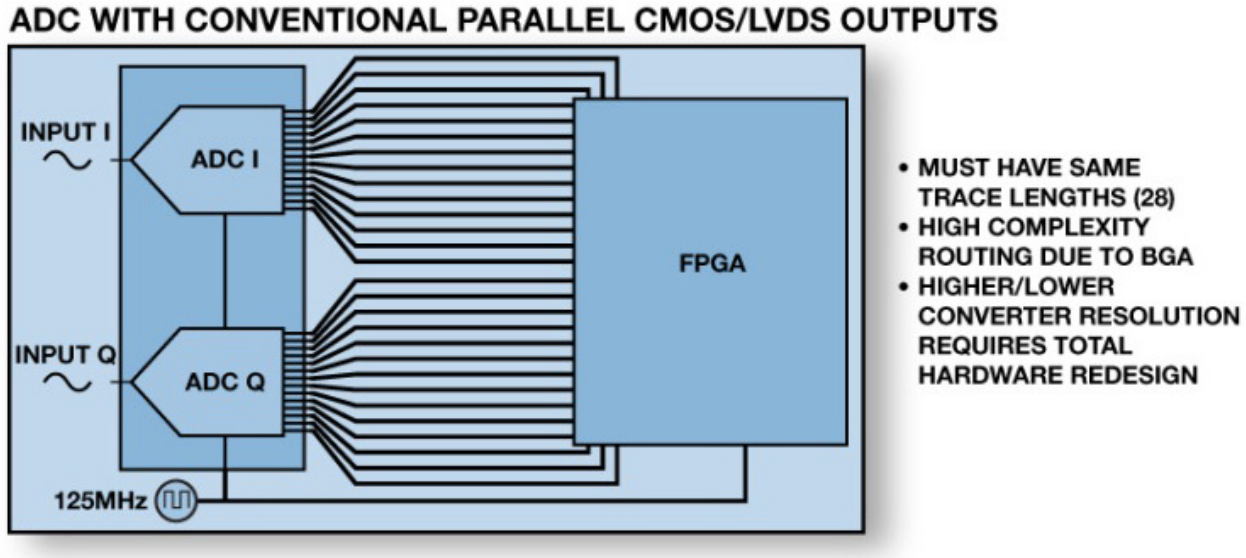




- Lower voltage, differential signals, forwarded clock output but signal skew still a potential problem.

Data Interfaces

- PCB design complications:



- Most of these problems can be mitigated by means of a high-speed, reconfigurable serial interface (JESD204)

Data Interfaces

Table 1. Pin Count Comparison—200 MSPS ADC

Number of Channels	Resolution	CMOS Pin Count	LVDS Pin Count (DDR)	CML Pin Count (JESD204B)
1	12	13	14	2
2	12	26	28	4
4	12	52	56	8
8	12	104	112	16
1	14	15	16	2
2	14	30	32	4
4	14	60	64	8
8	14	120	128	16
1	16	17	18	2
2	16	34	36	4
4	16	68	72	8
8	16	136	144	16

Complexity of the interface is moved from PCB routing into FPGA logic.

Serial Data Communications

- Differential signals (LVDS or CML)
- Clock recovery:

- 8b10b encoding: replace 8 bits with 10 bit code
- Ensures DC balance and a sufficient number of transitions for clock recovery.

8b10b Encoding

- 256 data bytes encoded using 512 10-bit words, selected to maintain DC balance.

Data Byte Name	Converter Sample Data	Current Running Disparity --	Current Running Disparity +
D0.0	00000000	1001110100	0110001011
D1.0	00000001	0111010100	1000101011
D2.0	00000010	1011010100	0100101011
D3.0	00000011	1100011011	0011100100
D4.0	00000100	1101010100	0010101011
D5.0	00000101	1010011011	0101100100
D6.0	00000110	0110011011	1001100100

- Not all the remaining 512 words are useful
  - Too many long sequences of 1's or 0's
- The ones that are useful are control characters

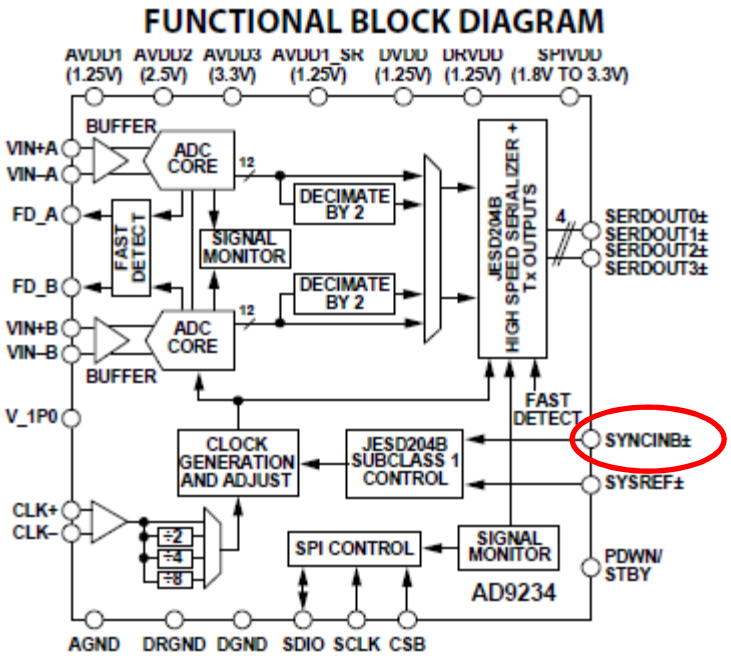
8b10b Control Codes

JESD204B Control characters

	Input – Special Symbols		RD = -1	RD = +1
	K-Codes	HGF EDCBA	abcdei fghj	abcdei fghj
/R/	K.28.0	000 11100	001111 0100	110000 1011
	K.28.1	001 11100	001111 1001	110000 0110
	K.28.2	010 11100	001111 0101	110000 1010
/A/	K.28.3	011 11100	001111 0011	110000 1100
/Q/	K.28.4	100 11100	001111 0010	110000 1101
/K/	K.28.5	101 11100	001111 1010	110000 0101
	K.28.6	110 11100	001111 0110	110000 1001
/F/	K.28.7	111 11100	001111 1000	110000 0111
	K.23.7	111 10111	111010 1000	000101 0111

- Used to transmit “non-data” status and control information on the serial link
- Decoded data provided as 8-bits plus one bit to indicate D- or K-code.

Multi-Lane Data Interface



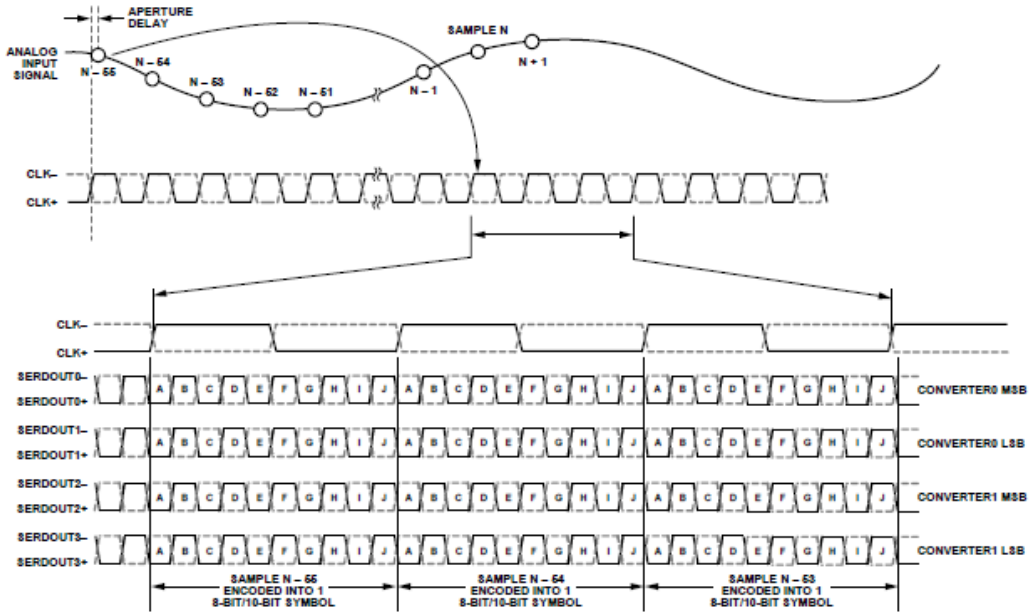


Figure 4. Data Output Timing (Full Bandwidth Mode; L = 4; M = 2; F = 1)

- Clock recovery determines relative phase of data bits.
- Additional information is required to align to frame boundaries.
- JESD204B introduces the SYNC~ signal…

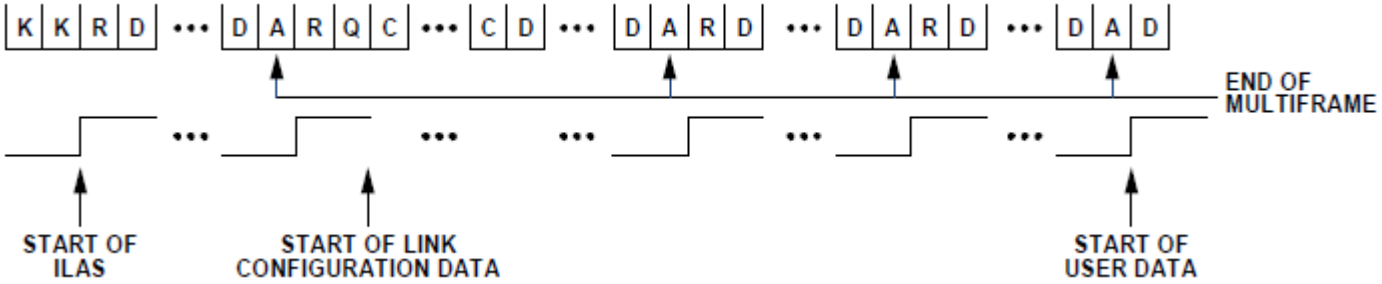
Link Bandwidth

- L = number of lanes/device (eg, 4)
- M = number of converters/device (eg, 2)
- F = octets per frame (eg, 1)
- N = converter resolution (eg, 12)
- CS = number of control bits/sample (eg, 4)
- N’ = number of bits per sample (N’=N+CS)
- S = samples rate/converter/frame (eg, 1 GSPS)

$$Lane\ rate = \frac{M\ \times N' \times \left(\frac{10}{8}\right) \times \mathrm{S} \times F}{L} = 10\ Gbps$$

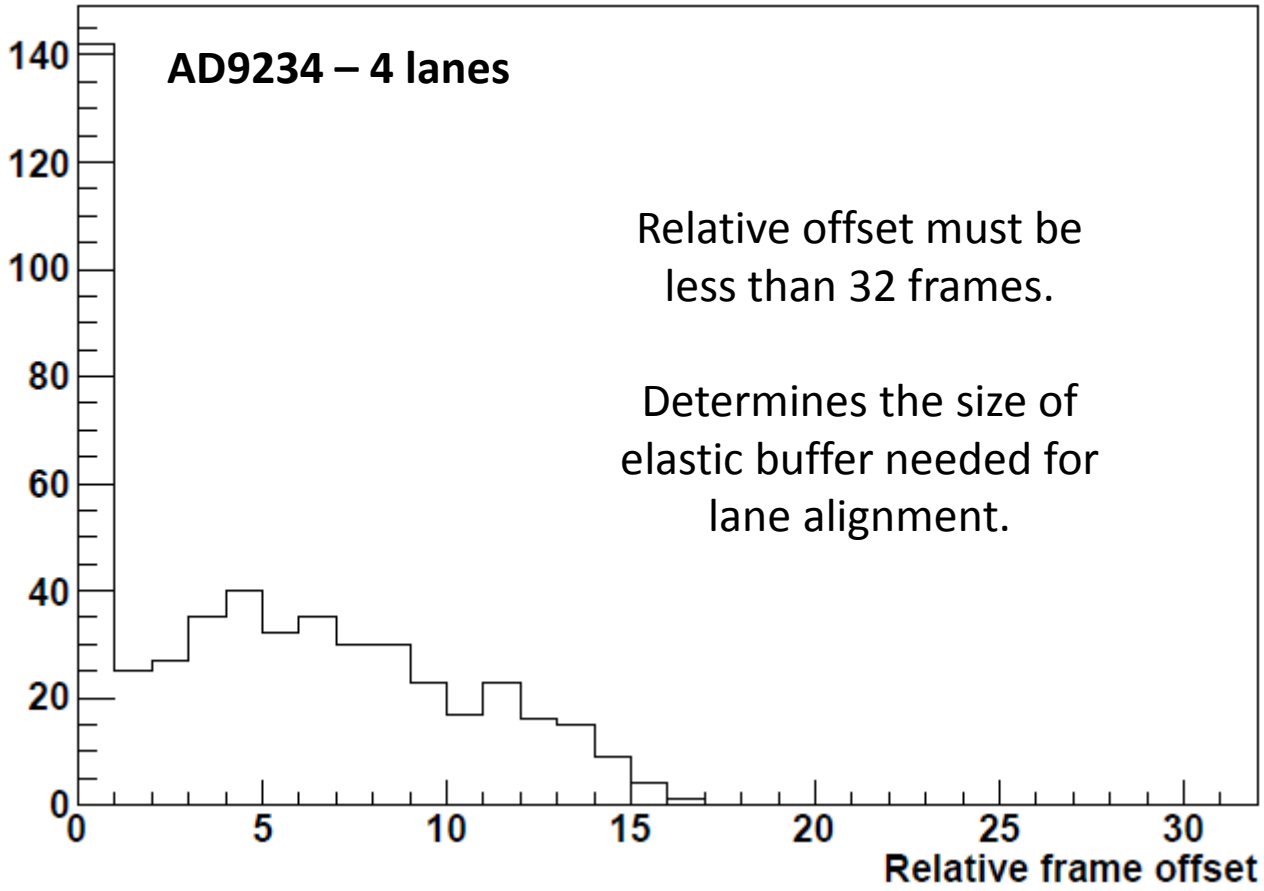
Aligning Multiple Lanes

- Asserting SYNC~ initiates Code Group Synchronization (CGS): transmits **/K/**
- After aligning to **/K/** characters, SYNC~ is deasserted and the device transmits the Initial Lane Alignment Sequence (ILAS):



- Second multi-frame transmits data link parameters
  - Self-describing data link configuration
- User data starts after fourth multiframe.

Aligning Multiple Lanes



Relative offset must be less than 32 frames.

Determines the size of elastic buffer needed for lane alignment.

Scrambling/Descrambling

Output bits defined by linear feedback shift register:

$$1+x^{14}+x^{15}$$

Avoids spectral artifacts due to repetitive data.

Descrambling is efficient to implement in FPGA logic.

```
function descramble(
  din : std_logic_vector(15 downto 0);
  scram : std_logic_vector(15 downto 0)
) return std_logic_vector is
  variable dout : std_logic_vector(15 downto 0);
begin
  dout(0) := din(0) xor cin(14) xor din(15);
  dout(1) := din(1) xor scram(0) xor din(15);
  dout(2) := din(2) xor scram(1) xor scram(0);
  dout(3) := din(3) xor scram(2) xor scram(1);
  dout(4) := din(4) xor scram(3) xor scram(2);
  dout(5) := din(5) xor scram(4) xor scram(3);
  dout(6) := din(6) xor scram(5) xor scram(4);
  dout(7) := din(7) xor scram(6) xor scram(5);
  dout(8) := din(8) xor scram(7) xor scram(6);
  dout(9) := din(9) xor scram(8) xor scram(7);
  dout(10) := din(10) xor scram(9) xor scram(8);
  dout(11) := din(11) xor scram(10) xor scram(9);
  dout(12) := din(12) xor scram(11) xor scram(10);
  dout(13) := din(13) xor scram(12) xor scram(11);
  dout(14) := din(14) xor scram(13) xor scram(12);
  dout(15) := din(15) xor scram(14) xor scram(13);
  return dout;
end;
```

Complete Data Path

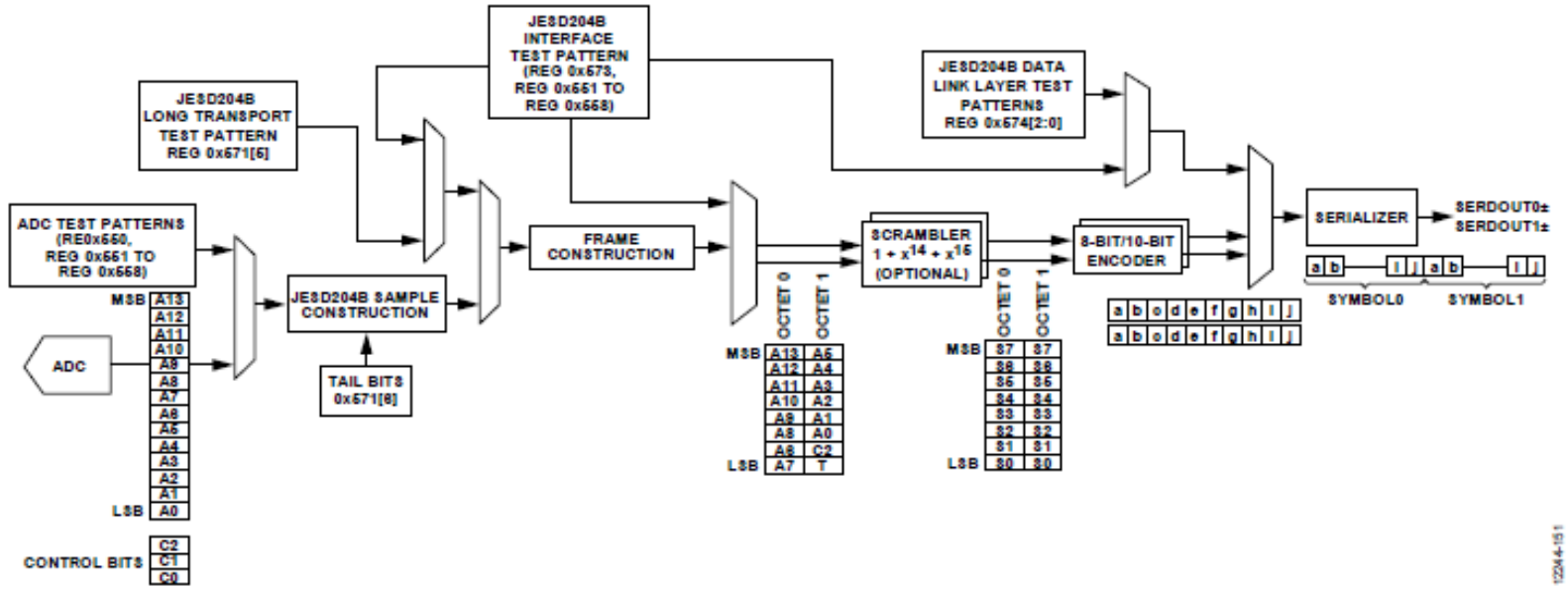
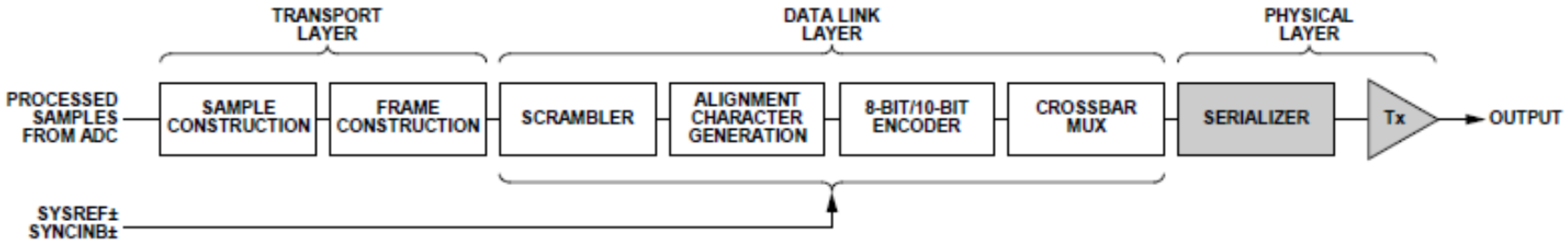
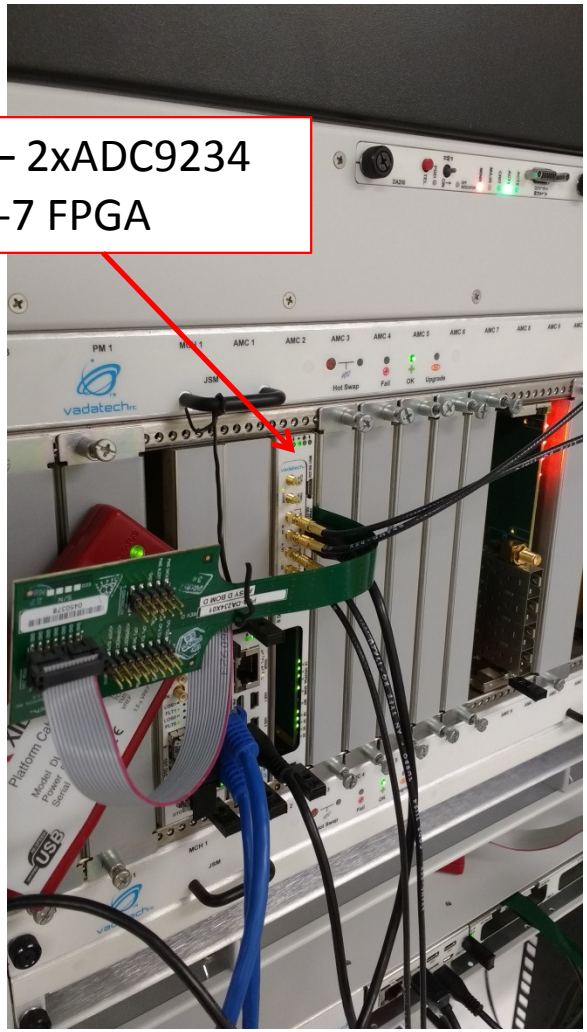


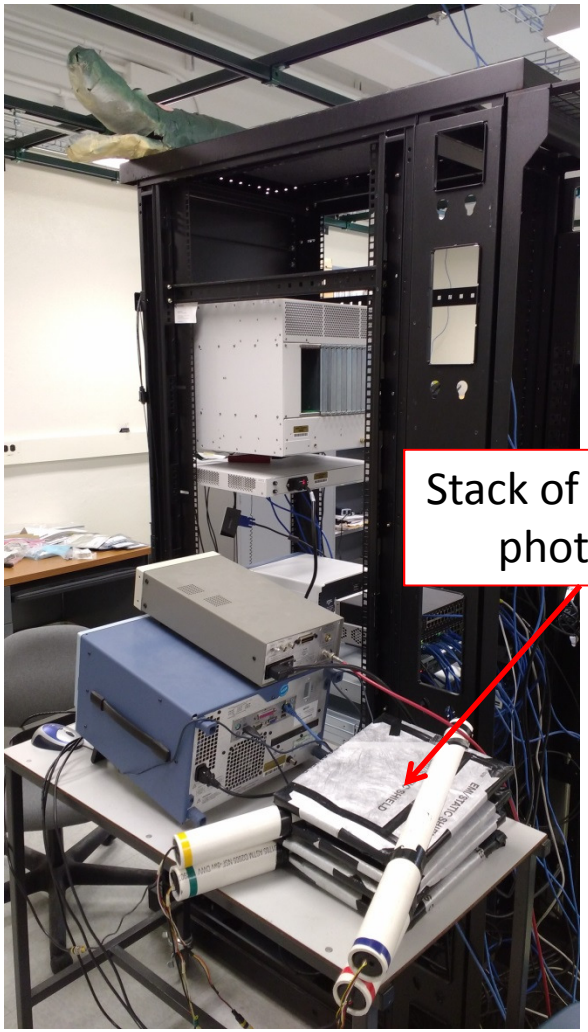
Figure 91. ADC Output Datapath Showing Data Framing



Example Application

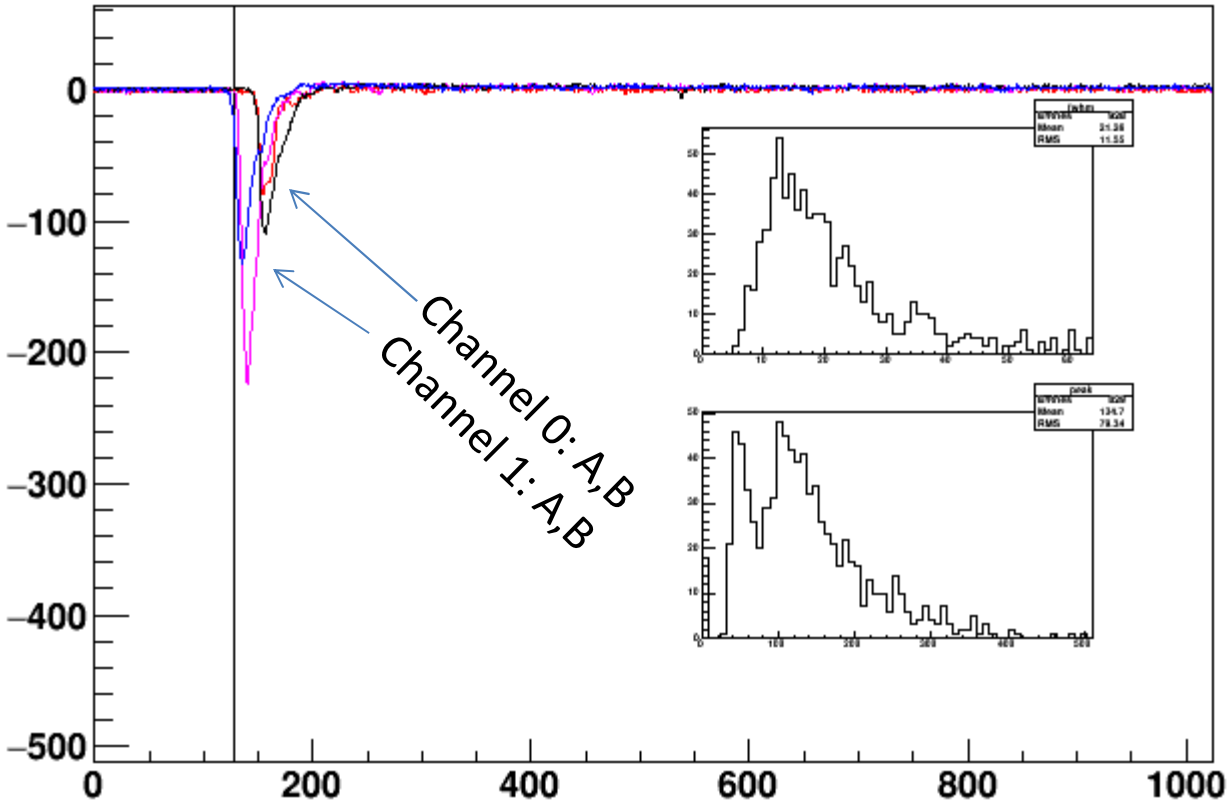
FMC228 – 2xADC9234
→ Kintex-7 FPGA





Stack of 4 scintillators + photomultipliers

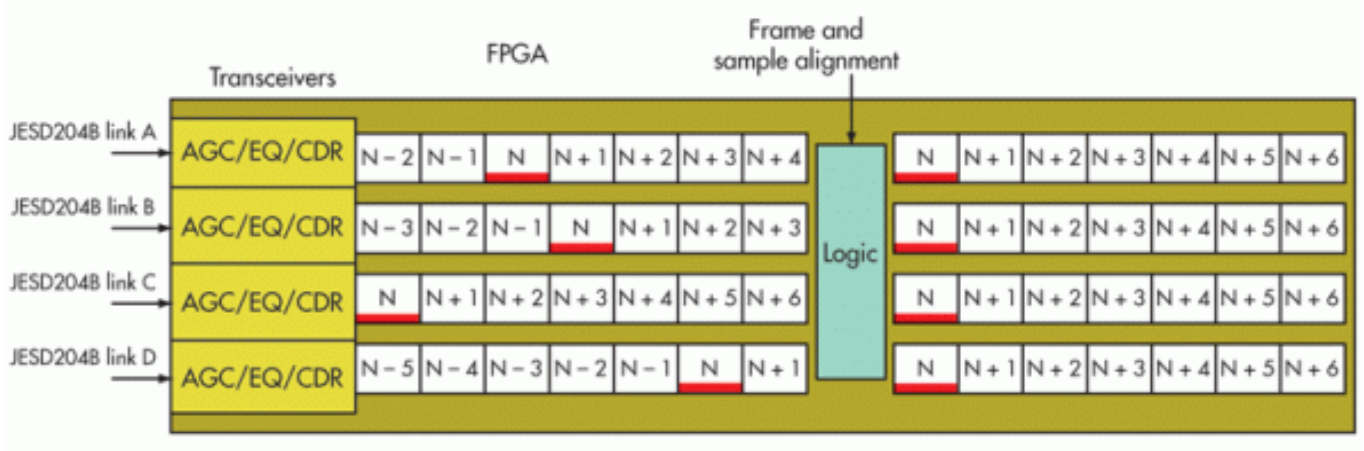
Decoded Waveforms



Firmware trigger on 3 out of 4 pulses above threshold.

Alignment of Multiple Devices

- Deterministic Latency refers to the ability to determine the absolute latency of the decoded data.
- Each ADC maintains a Local Multi-Frame Clock (LMFC)
  - Eg, 1/16 of the input clock frequency
  - ILAS sequence starts on a LMFC boundary
- JESD204B introduces the SYSREF~ signal.
  - All LMFC clocks are synchronized to the SYSREF~ signal edge.

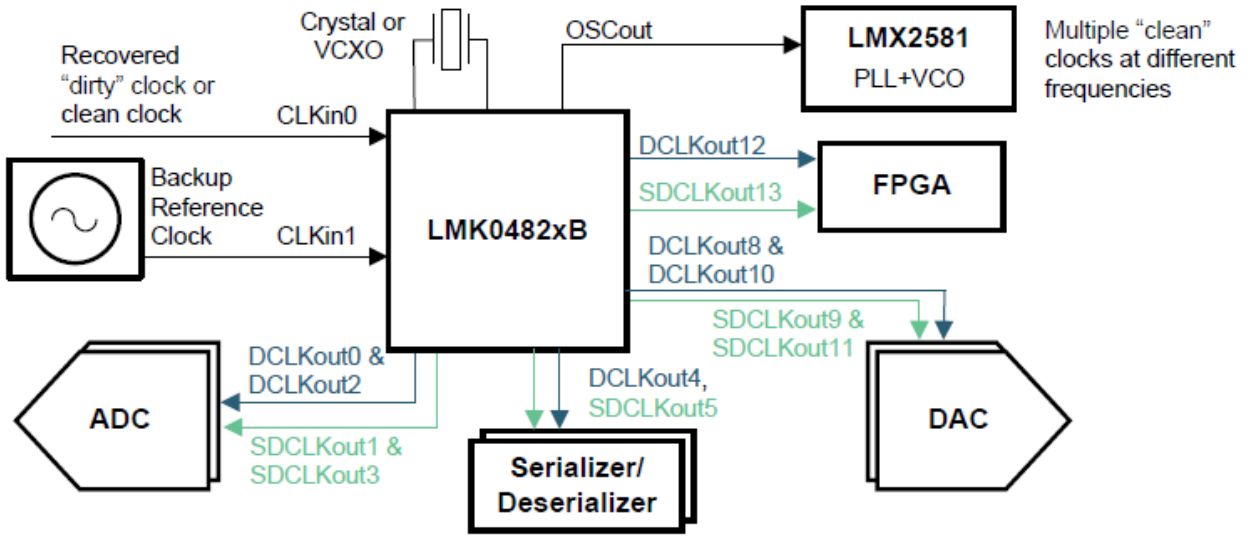


Support for Clock Synthesis

- The standard allows interoperability of different vendor's chip sets.
  - Eg. Texas Instruments

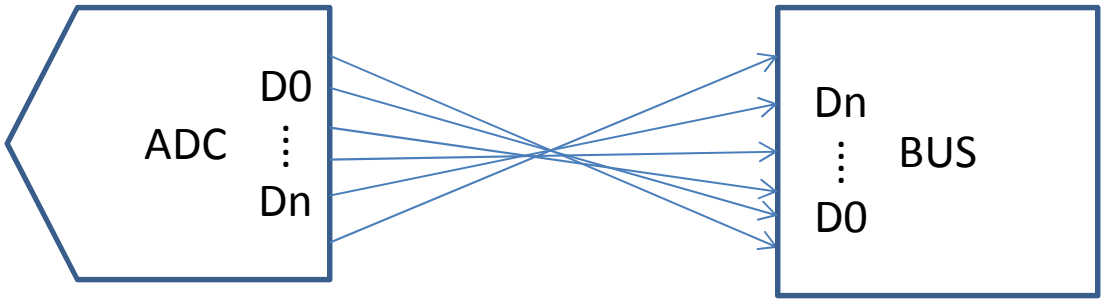
LMK0482x Ultra Low-Noise JESD204B Compliant Clock Jitter Cleaner with Dual Loop PLLs

Simplified Schematic



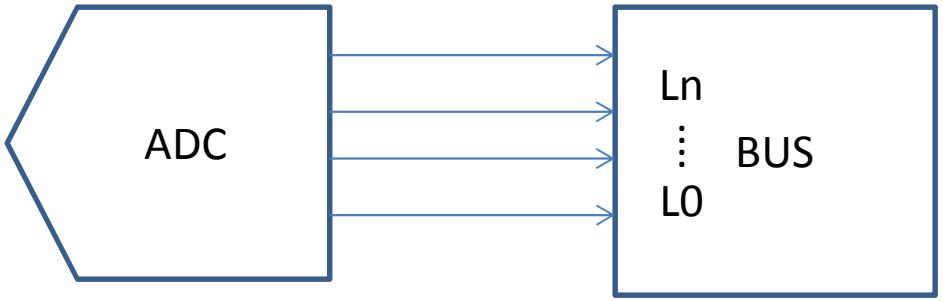
Other Advantages

- Reconfigurable through software
  - Change sample resolution
  - Pin-compatible devices with different resolution/sample rate
  - Re-mapping of physical channels



Routing complexity on PCB due to opposite bit order

JESD204B lane order remapped by internal crossbar switch



Comments

- Deterministic latency is not the same as low latency
  - LVDS may still be more appropriate in cases where low latency is of primary concern
- Same issues apply to high speed DAC's driven by an FPGA
- Potentially interesting for high-speed serial interfaces exchanging trigger data
  - No need to transmit bunch crossing counter with each data frame

Hardware/Firmware Support

- Hardware:
  - Analog Devices
  - Texas Instruments
  - Intersil
  - Linear Technology
  - Others…
- Firmware vendors:
  - Xilinx:
    - JESD204 PHY v3.2 (free): physical interface
    - JESD204 core (licensed): bus interface
  - Altera:
    - JESD204B IP Core (licensed)

Summary

- The JESD204B standard is widely applicable to high-speed ADC and DAC applications
- Widely accepted by industry
- Solves several problems common to similar DAQ models
  - High speed, low noise, low power
  - Deterministic latency
  - Versatile, reconfigurable links
- Applicable beyond ADC/DAC interfaces
- Implementation is not all that difficult but working examples can be quite helpful