HVCMOS sensor technology R&D

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INFIERI WORKSHOP

FERMILAB, 18/10/2016

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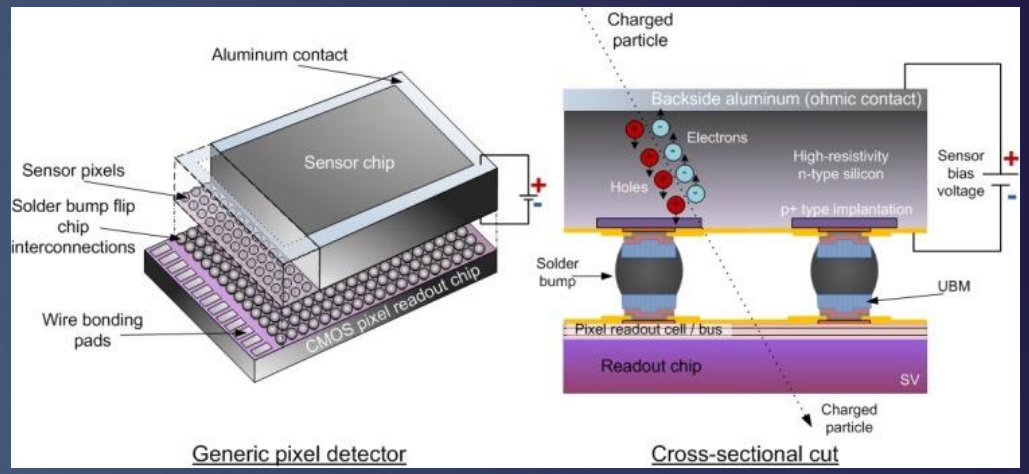
Current status of LHC pixel detectors

Standard Planar Silicon Detectors

- √ Complex signal processing
- √ 25 ns in-time efficiency
- √ Radiation hard (≈ $5x10^{15}$ n_{eq} /cm^2)
- √ High rate capability (≈MHz/mm^2)
- √ Good spatial resolution (≈10÷15 μm)
- √ High efficiency (>99%)
- x Large material budget
- x Complex and laborious module production
  - x bump-bonding / flip-chip
  - x Many production steps



Expensive

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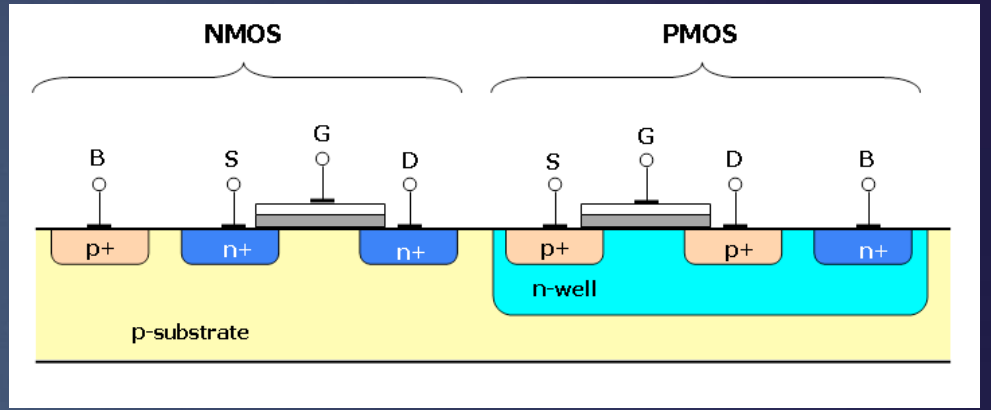
CMOS technology: an alternative

- Commercial process
  - Mature
  - Cheap
- Allows for Monolithic Pixels
  - No hybridization
  - Wafer scale processes
- Can achieve very small sizes
  - O(25x25 μm^2)
- CMOS Standard: low voltage, low resistivity
  - No depletion region -> Charge collection only by diffusion (no drift)
  - Small signal
  - Slow



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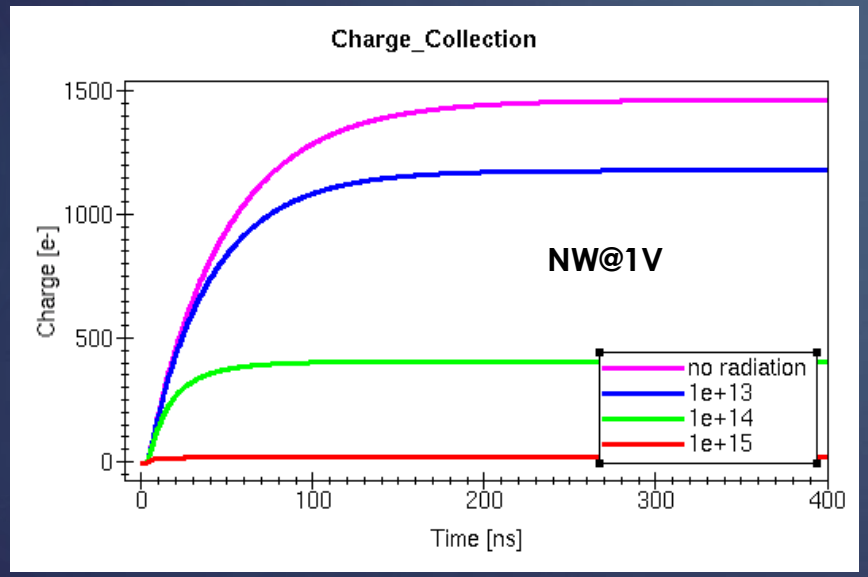
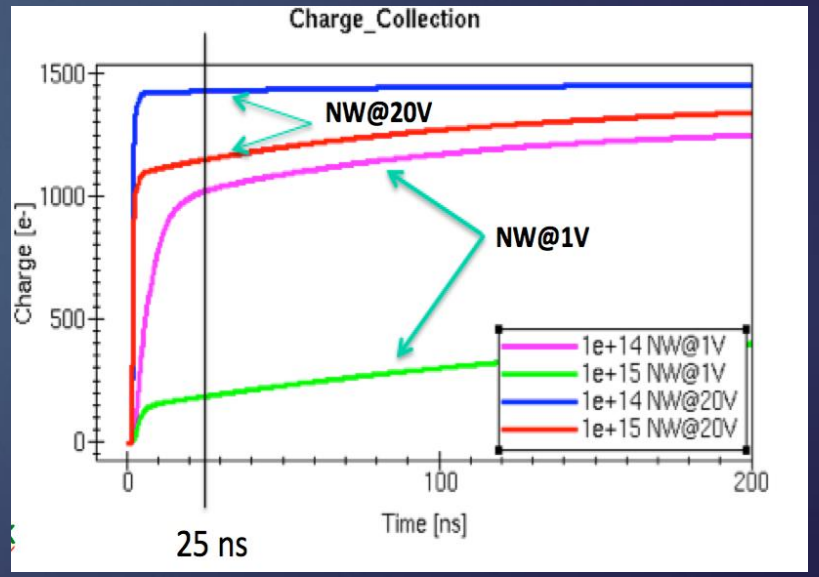
CMOS technology: LHC requirements

- Fast charge collection (< 25ns "in-time" efficient)
- Reasonably large signal (~4000 e-)
- Short collection distance to avoid trapping (rad hardness)

Low resistivity (10 Ωcm), low voltage



High resistivity (2 kΩcm), high voltage



Simulations by Tomasz Hemperek (Bonn)

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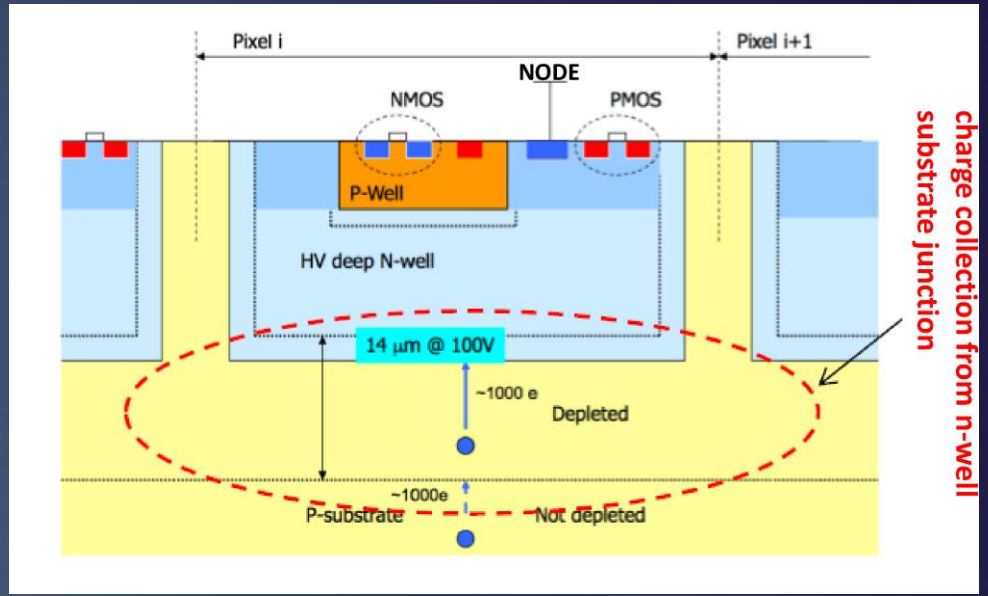
CMOS technology: add-ons

- CMOS component inserted inside deep N-well
  - Isolation from high voltage
  - Depletion region created between deep N-well and backside of p-substrate
- High resistivity wafers
- Multiple nested wells
- Backside processing



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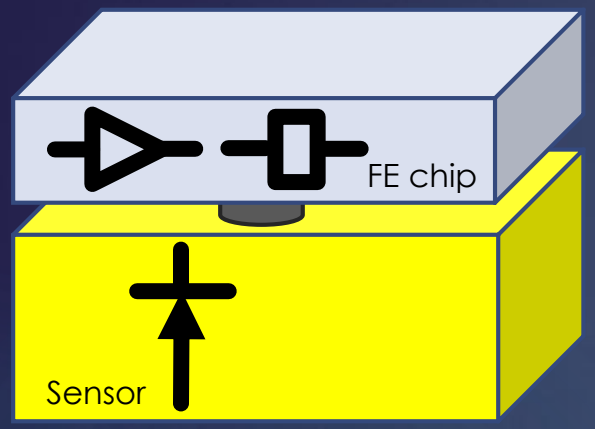
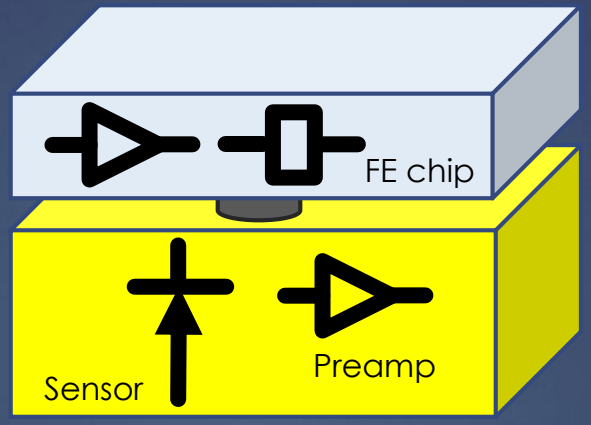
CMOS technology: configurations



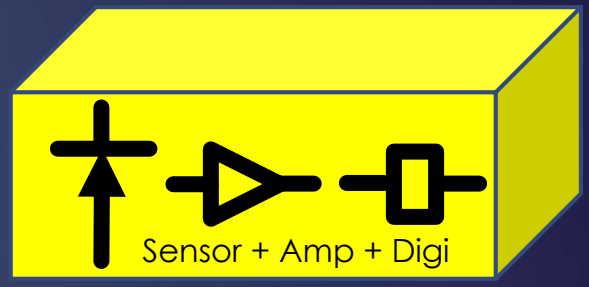
Standard Hybrid
CMOS passive sensor

CMOS Passive Pixels



CMOS active Hybrid
Bump-bonded or glued

CMOS Strip Project (Chess)



Fully monolithic

CCPD Detectors

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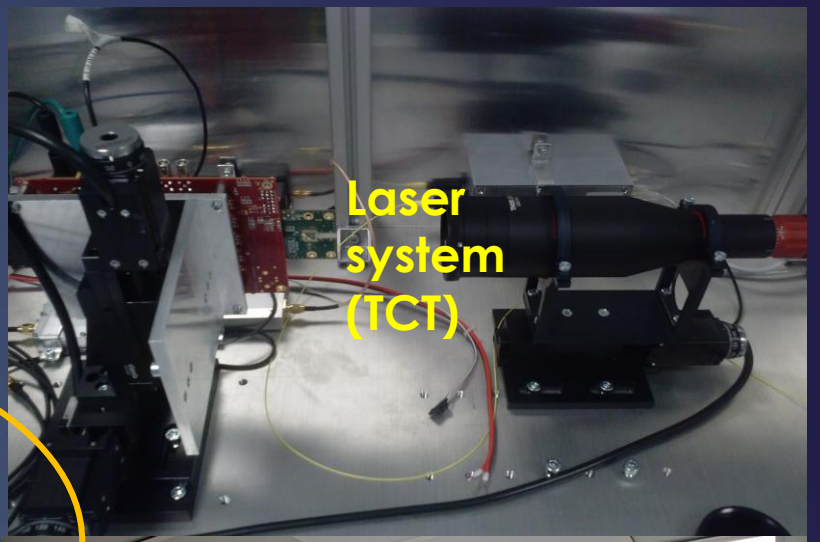
CMOS technology: development

RD50

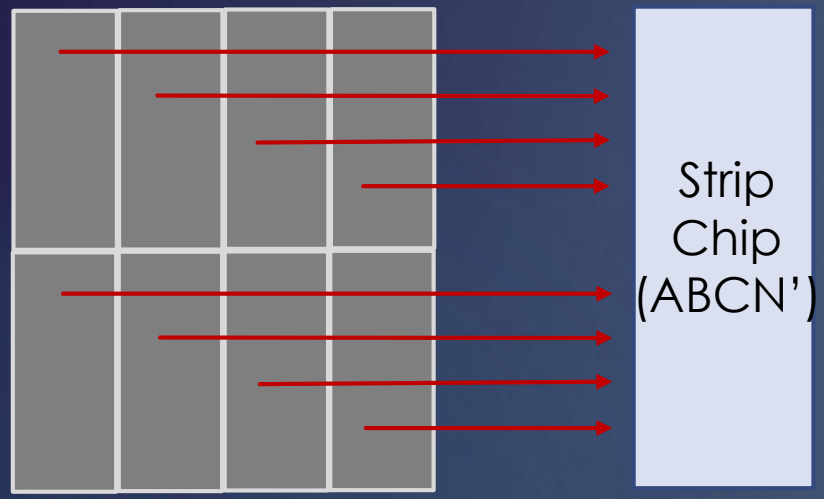
Oxford Physics Microstructure Detector facility

Two clean rooms:
- Class 10k (ISO7) 120 m^2
- class 100 (ISO5) 40 m^2



CMOS Strip

"Strixels" Concept



Column information given by active pixel components

Row information given by read-out chip

Goal: minimal modifications on the current chip design

- Pixel-like resolution
- Easy read-out
- Less material

Status:

- ✓ Basic prototypes produced and tested
  - ✓ HVStripV1
  - ✓ Chess1

  } Test structures
- ✓ Complete prototype just produced
  - ✓ Chess2 — Full digitalized matrix + test structures

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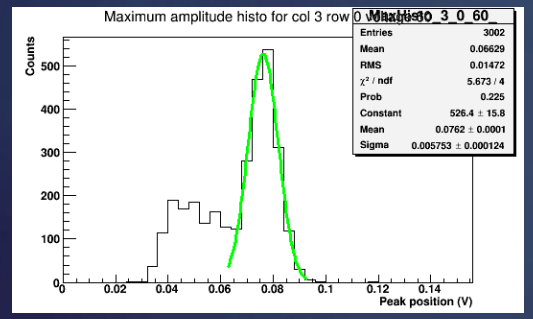
CMOS Strip: HVStripV1

- AMS35 Technology
- 22x2 channels, 40x400 μm² each
- 750 μm total thickness
- 5 Ω cm resistivity
- Up to 80 V bias

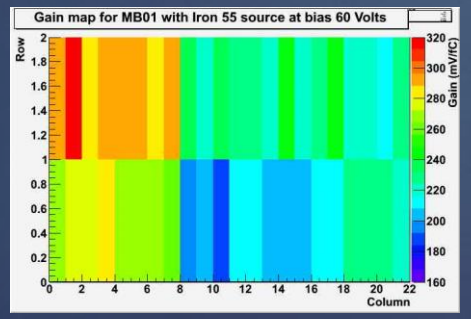
I. Peric

Only analogue output investigated (one channel at a time)

Fe⁵⁵ characterization



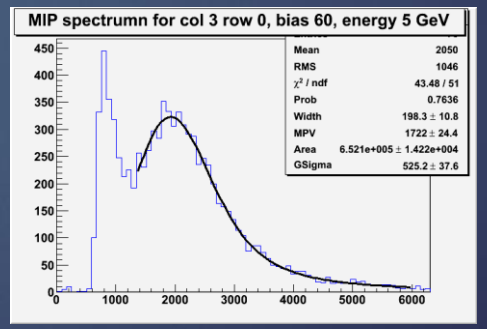
Single spectrum



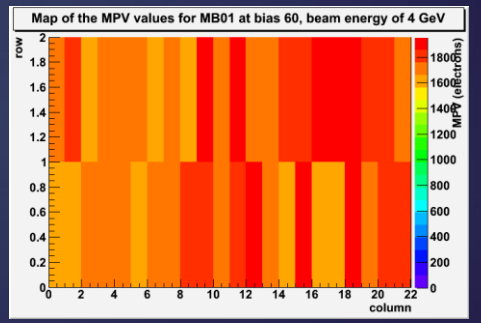
Gain map

(Bias 60 V)
(Noise ≈70e-)

Test Beam at DESY (3 GeV electrons)



Single spectrum



MPV map

Charge Most Probable Value compatible with 20 μm depletion

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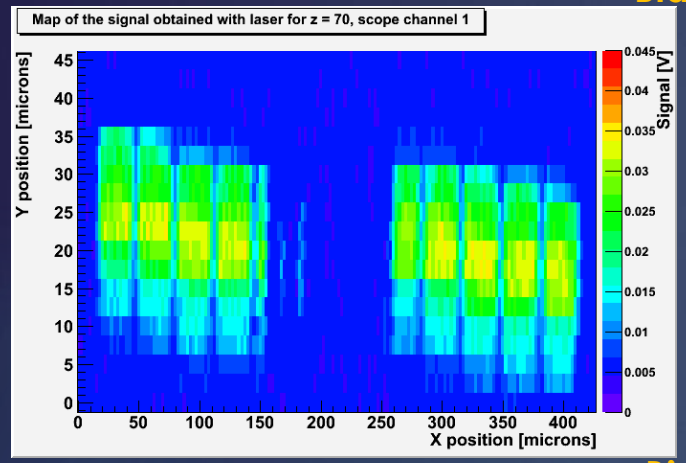
CMOS Strip: HVStripV1

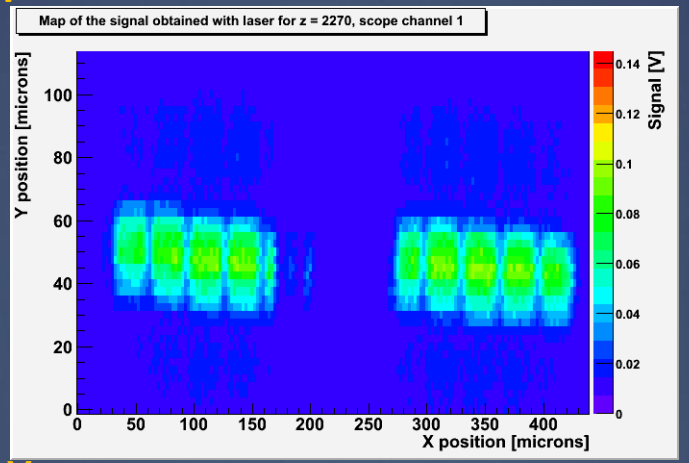
Laser characterization

Red Laser (640nm)

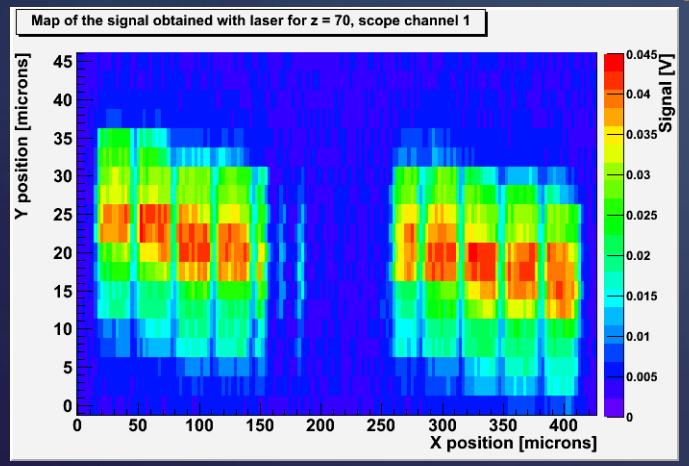
Infrared Laser (1060nm)

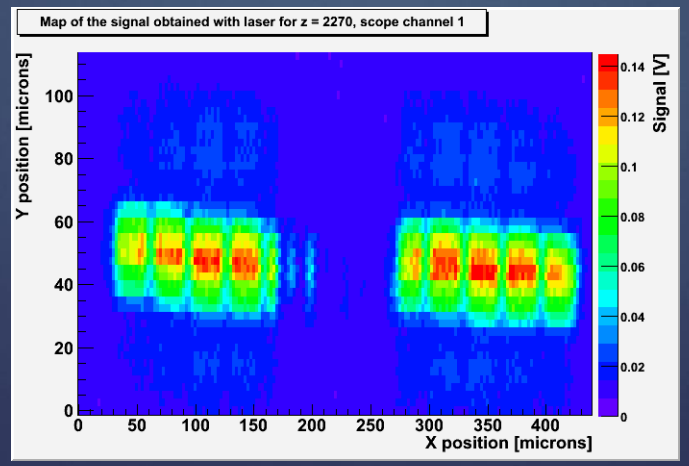
Bias 10 V



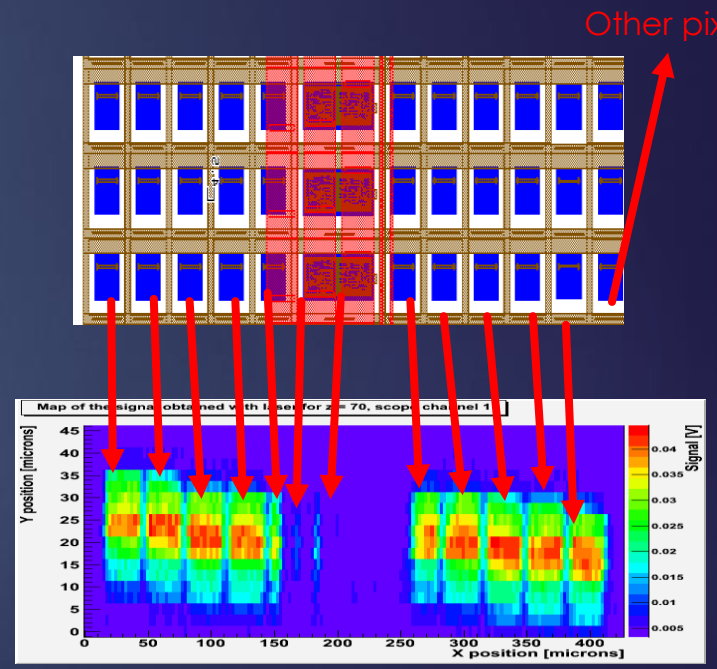


Bias 80 V





Matching with design



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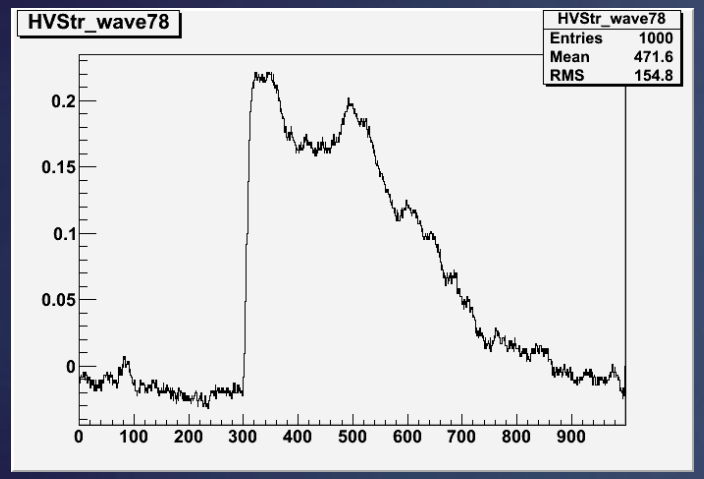
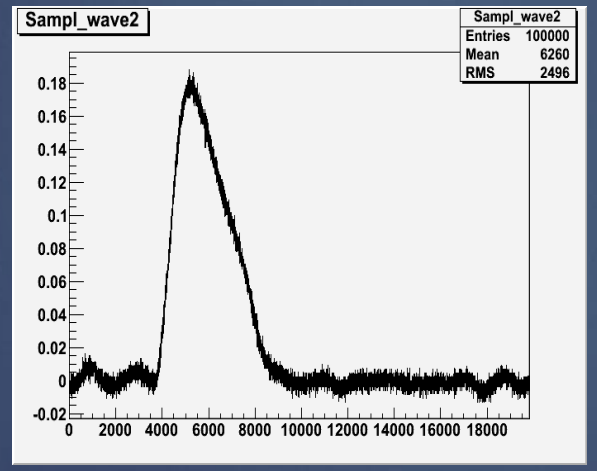
CMOS Strip: HVStripV1

Irradiation

- Birmingham: 27 MeV protons from the cyclotron
- Fluence of about 8×10^{14} n_{eq}/cm^2

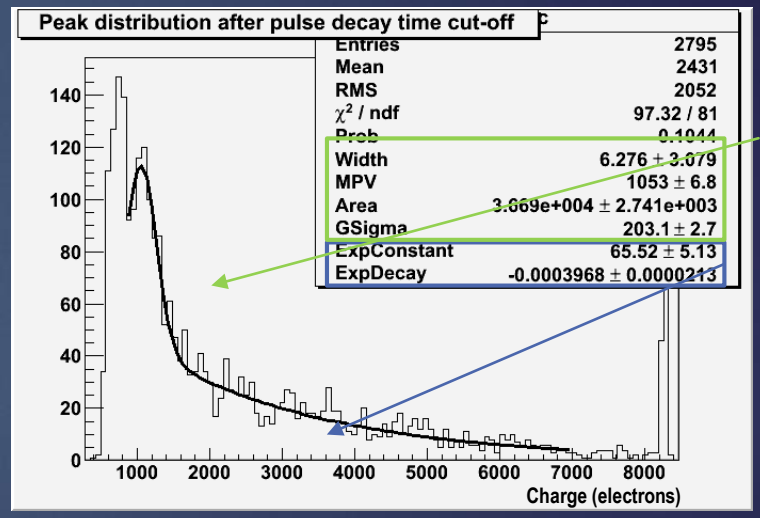




Signal significantly degraded after irradiation

Recovered after annealing and changing of DACs

Despite noise, Landau peak observed with Sr^{90} (Cambridge)



Landau-Gauss convolution

+

Exponential

Bias 60 V

- Exponential function to parameterize the observed background
- MIP peak observed, lower MPV than unirradiated (~60%)

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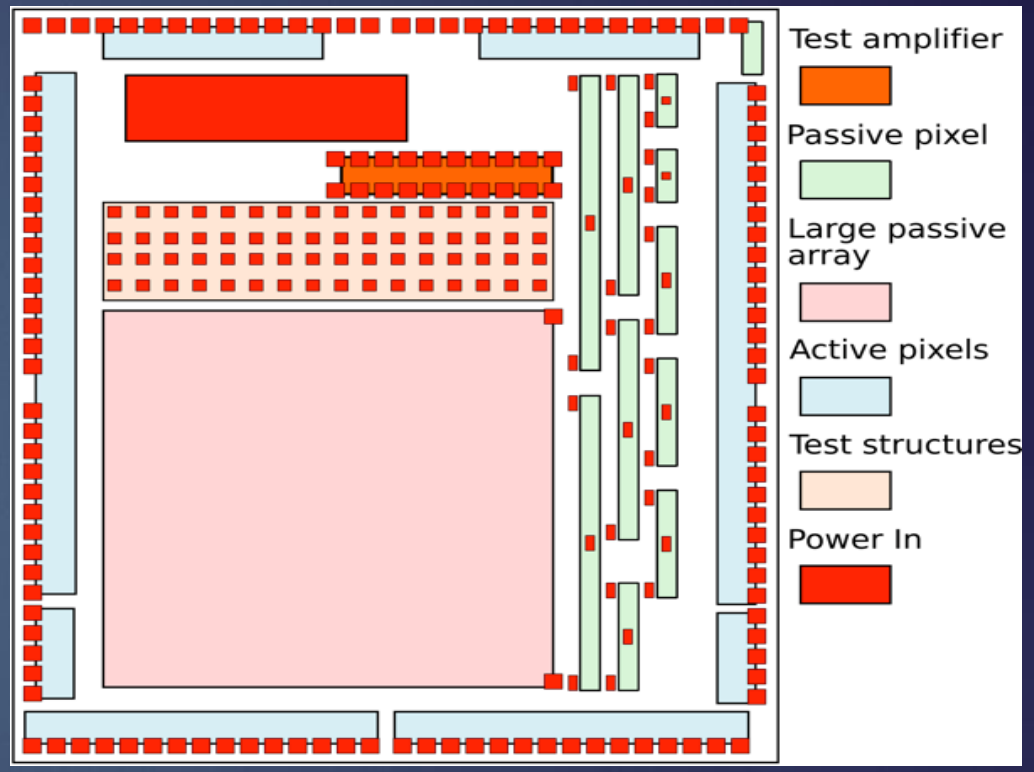
CMOS Strip: Chess1

- Complex device with many different structures
  - We focus on Active Pixel Arrays (APA)
  - 72 channels in total, divided in 8 types (APA1,…,APA8)

APA #	Pixel size	Fill Factor
APA01	45x100μm^2	30%
APA02	45x100μm^2	50.4%
APA03	45x200μm^2	30%
APA04	45x200μm^2	50.4%
APA05	45x400μm^2	30%
APA06	45x400μm^2	50.4%
APA07	45x800μm^2	30%
APA08	45x800μm^2	50.4%



Global layout

- ams fabrication
- 5 Ohm cm resistivity
- Bias up to 80V

V. Fadeyev,
H. Grabas (Santa Cruz)

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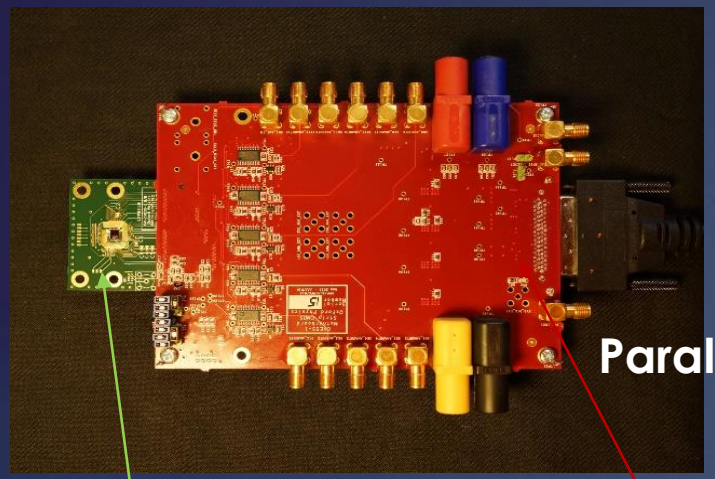
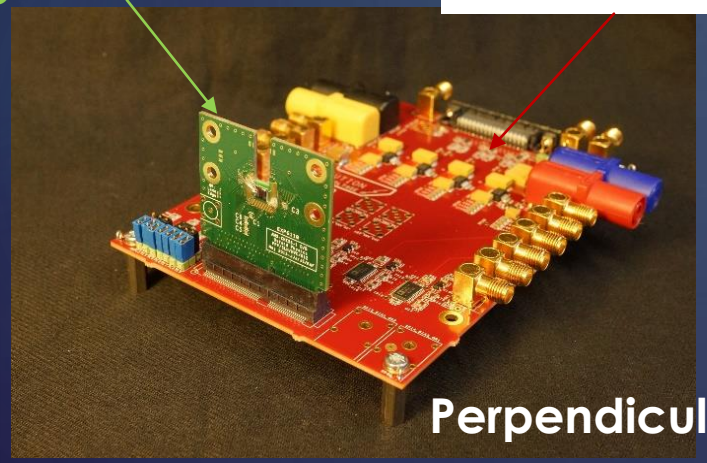
CMOS Strip: Chess1

Laser characterization



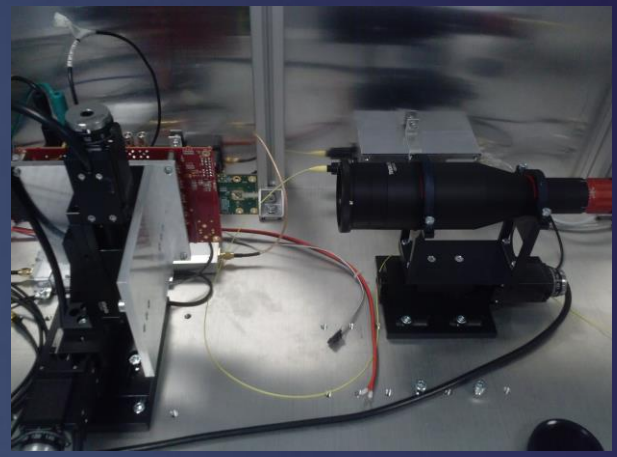


J. John, T. Huffmann (Oxford)

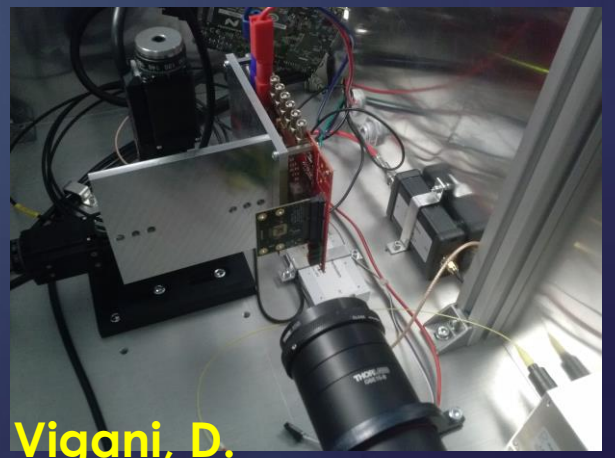
Read out system:

- Motherboard + Daughterboard
- 10 channels readable at the same time
- 6 DACs to regulate

Two configurations of mother-daughterboard connection for 2 different laser scans



Edge TCT



Front TCT

L. Vigani, D. Bortoletto

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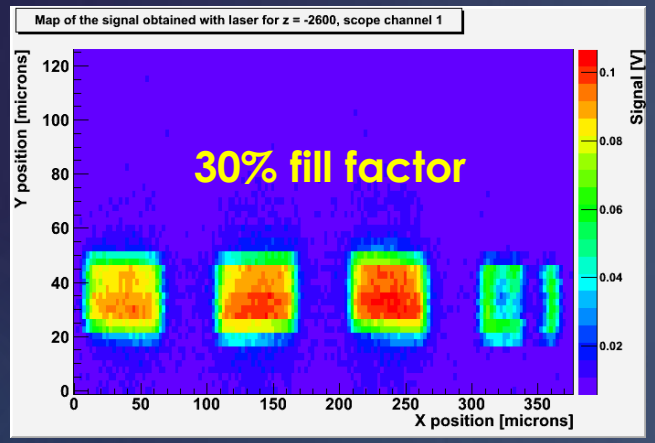
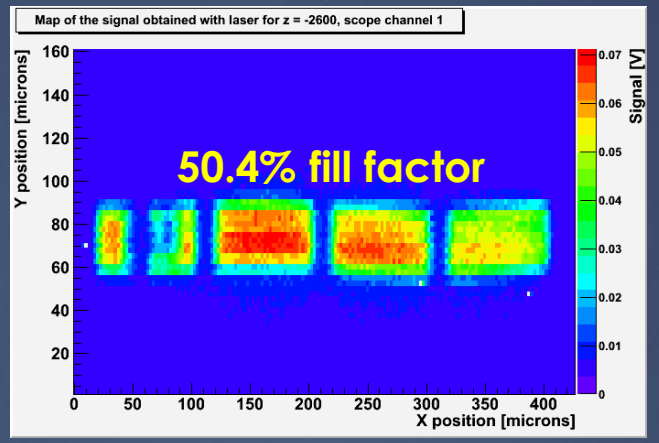
CMOS Strip: Chess1

Front TCT

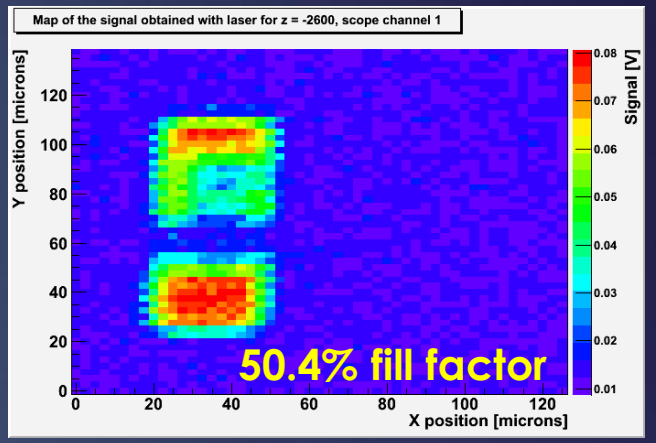
APA5



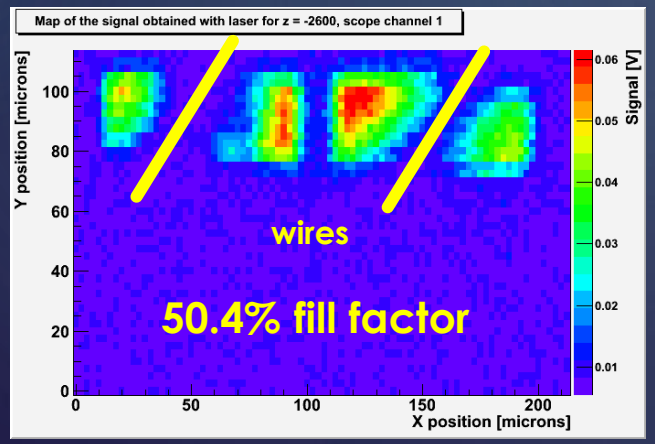
APA6



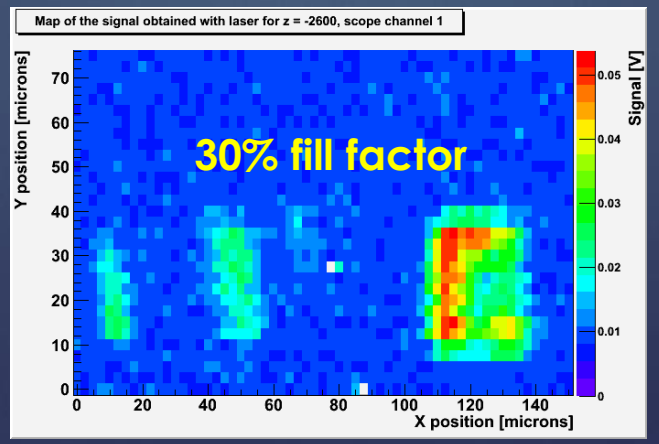
APA2



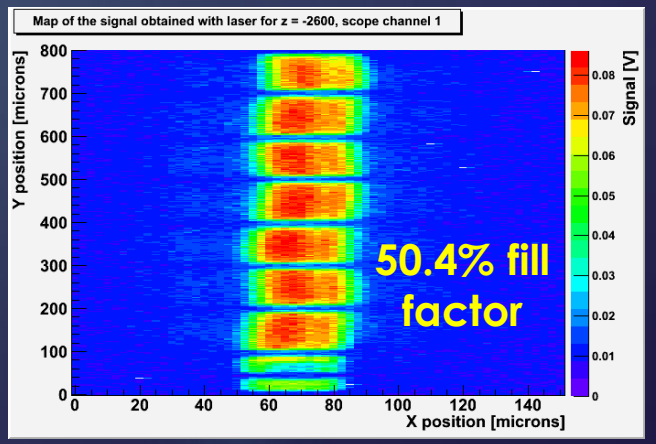
APA4



APA3



APA8



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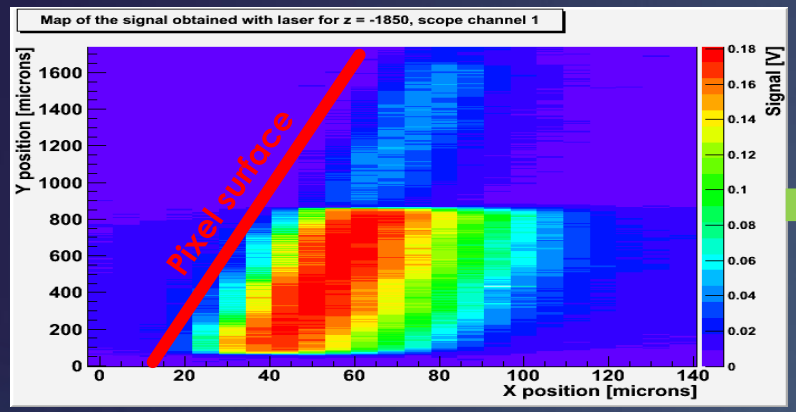
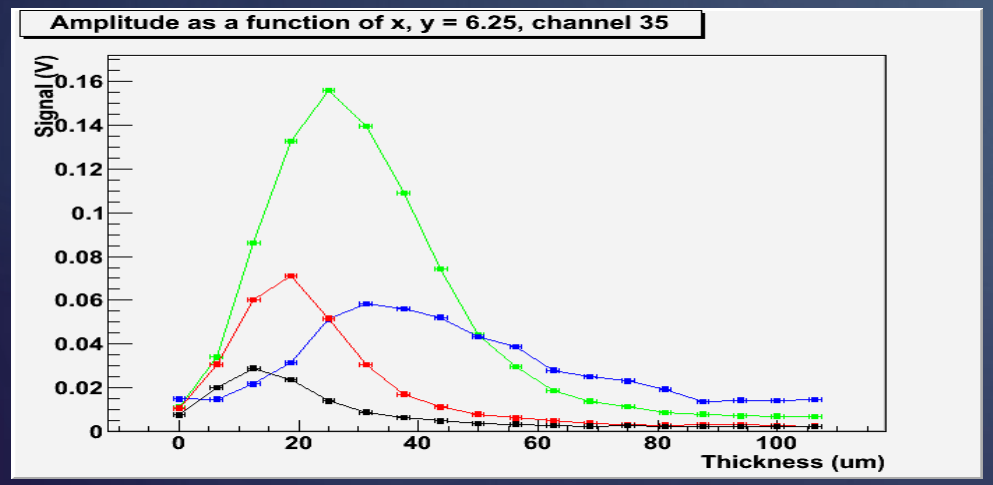
CMOS Strip: Chess1



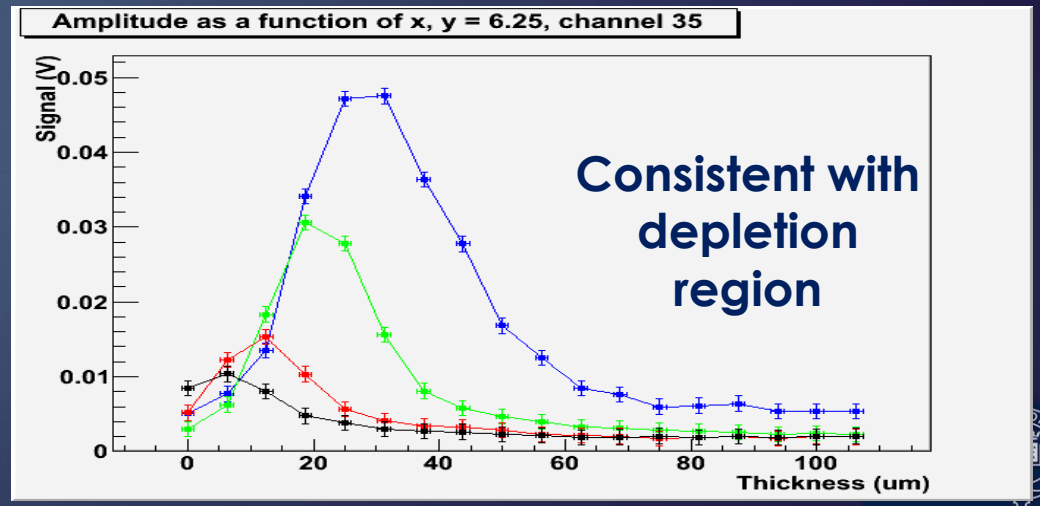
Edge TCT

- APA8 (800 µm pitch on that side)
- Slightly tilted about laser axis (less than 2 degrees)
- Slow DAC configuration: mainly diffusion
  - Sharing with nearby pixel

Signal as a function of depth, bias dependence:



- Black: 20V
- Red: 40V
- Green: 60V
- Blue: 80V



Slow signal DAC configuration

Fast signal DAC configuration

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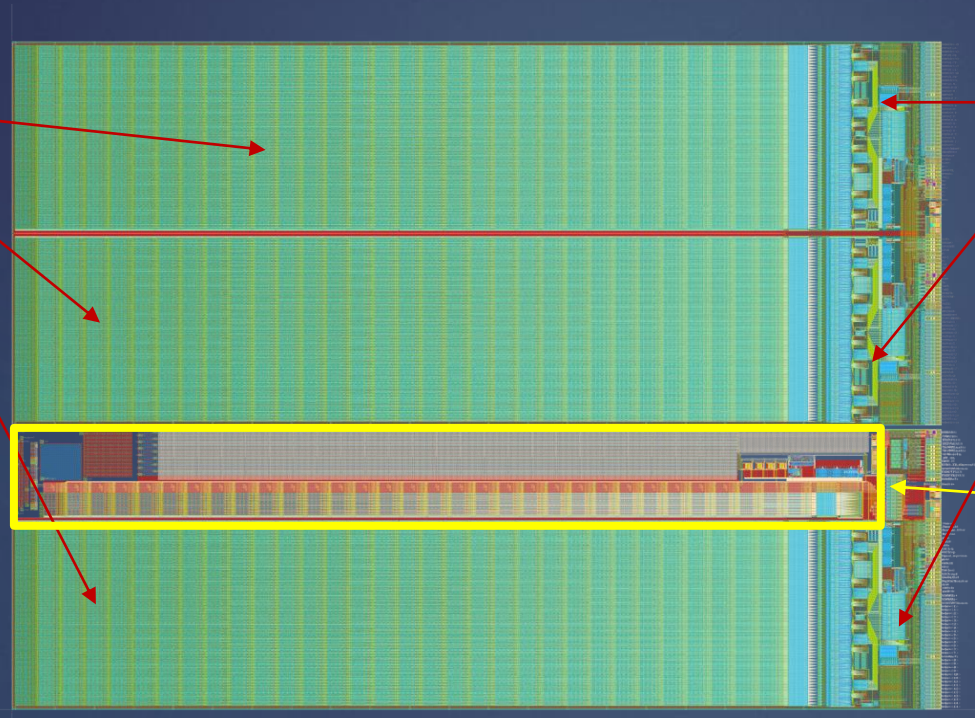
CMOS Strip: Chess2

First example of monolithic CMOS sensor for a strip detector

3 strip-like pixel arrays

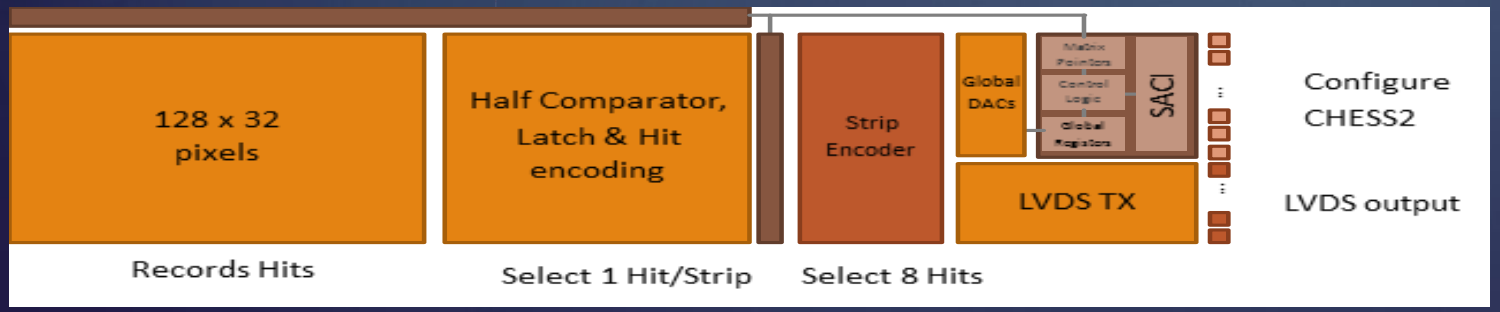


Chip periphery with additional electronics

Test structures

- 128 strips divided by 32 pixels each (40x630 μm^2)
- 250 μm thick
- Different resistivities from 20 to 2000 Ω cm)

- Passive and active CMOS diodes
- Board to read them out Chess1-like

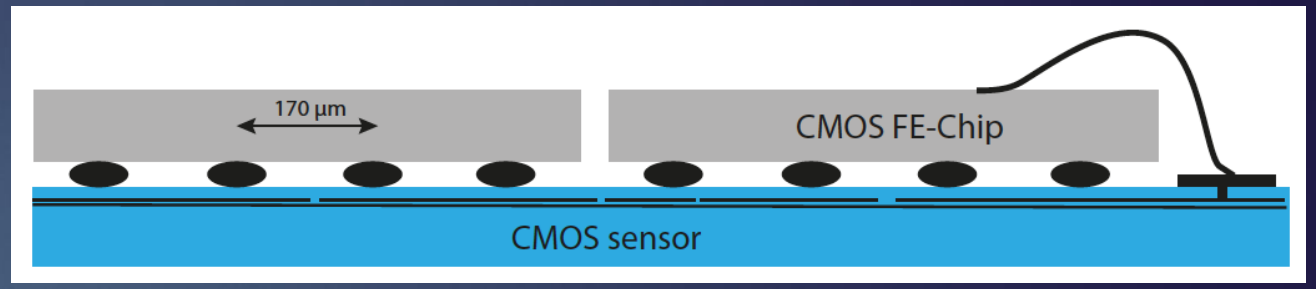


Chips just produced! Some tests currently performed. Chess1-like boards in production

CMOS Pixels: passive

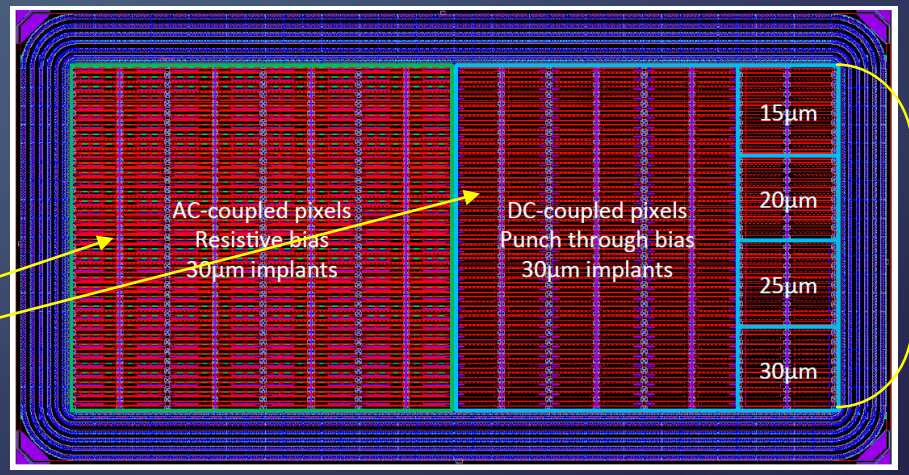
C4 bumps: come with chip fabrication at low cost

- No fine-pitch bumping
- Flip-chipping in-house (large pitch)
- Cheap large feature size technology
- Large sensors
- Wafer based flip-chipping
- Can have in-pixel AC coupling and voltage redistribution layers



- LFoundry 150 nm CMOS technology
- 2 kΩ cm p-type bulk
- ATLAS FE-I4 pixel pitch (50x250 µm^2)

- 16x36 pixels
- 300 µm thick
- Backside processed



Prototype with 2 areas to test 2 coupling alternatives

Different n-well widths: Different fill factors

T. Hemperek, F. Hugging, H. Kruger, J. Janssen, D. Pohl (UBonn), A. Macchiolo (MPI M), L. Gonella (Birmingham)

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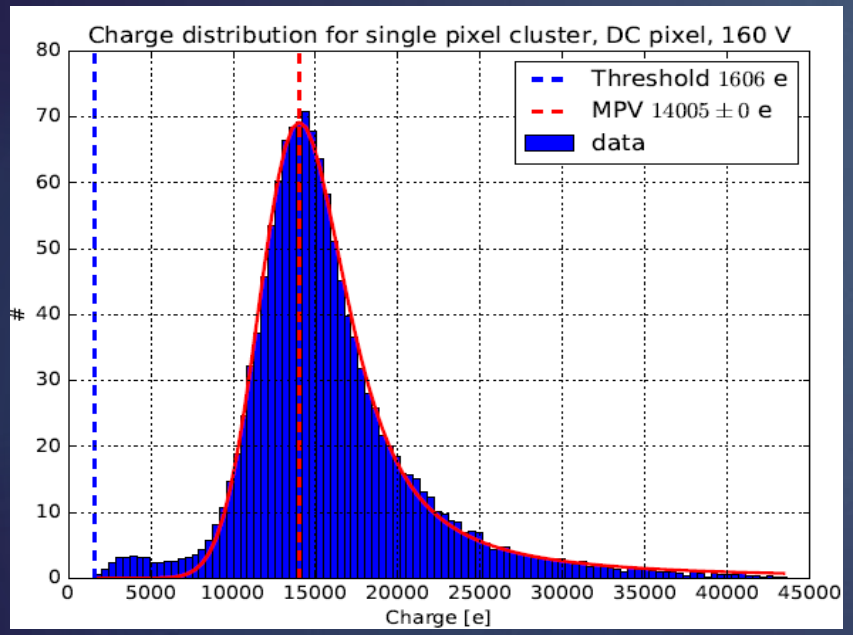
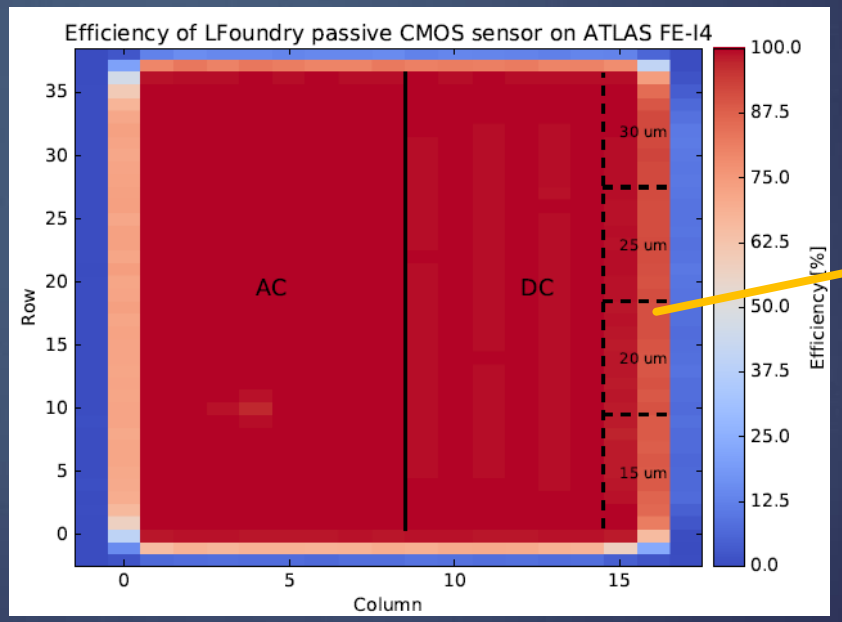
CMOS Pixels: passive

Test Beam at ELSA (Bonn)

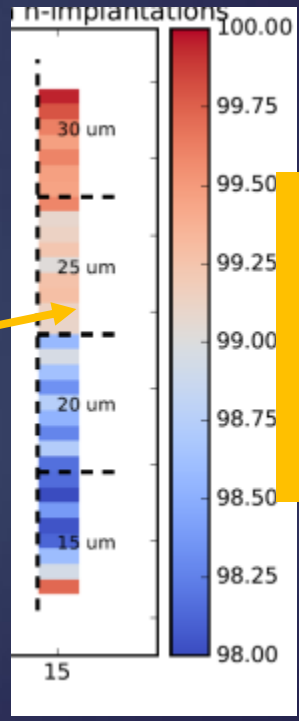
- 3 GeV electrons, -160V bias
- Only 2 FE-I4 planes telescope → No in-pixel resolution.



Charge collected
Depletion depth about 200 µm



Efficiency
DC area seems to have less effective columns



Smaller fill factor = smaller efficiency?

D. Pohl, J. Janssen (Bonn)

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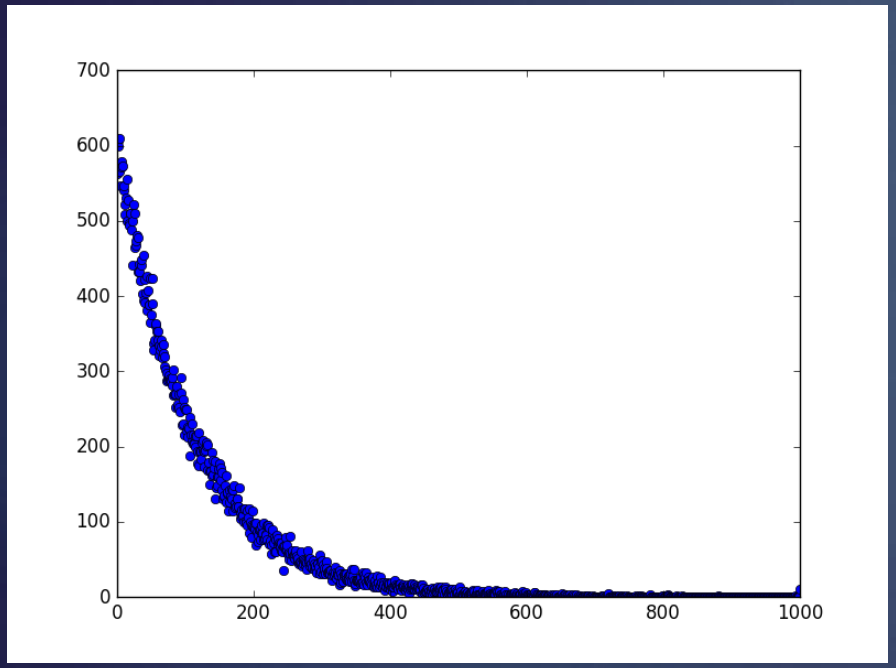
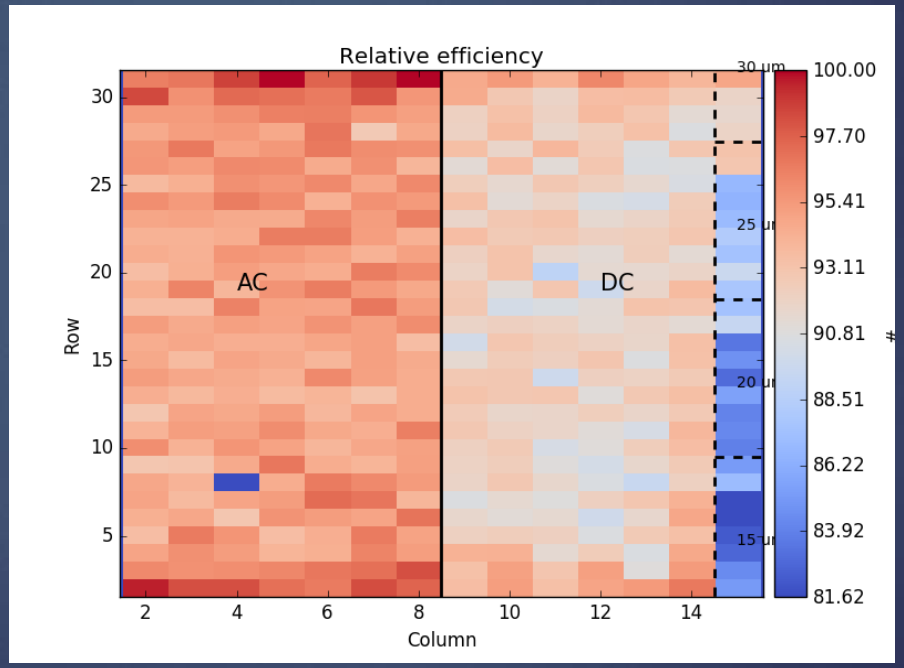
CMOS Pixels: passive

Source scan

- Americium
- Full-coverage source



Single pixel time difference distribution for source decay. From exponential: rate.



Differences in pixel rate due to difference in efficiency: Relative efficiency map

Efficiency behavior confirmed

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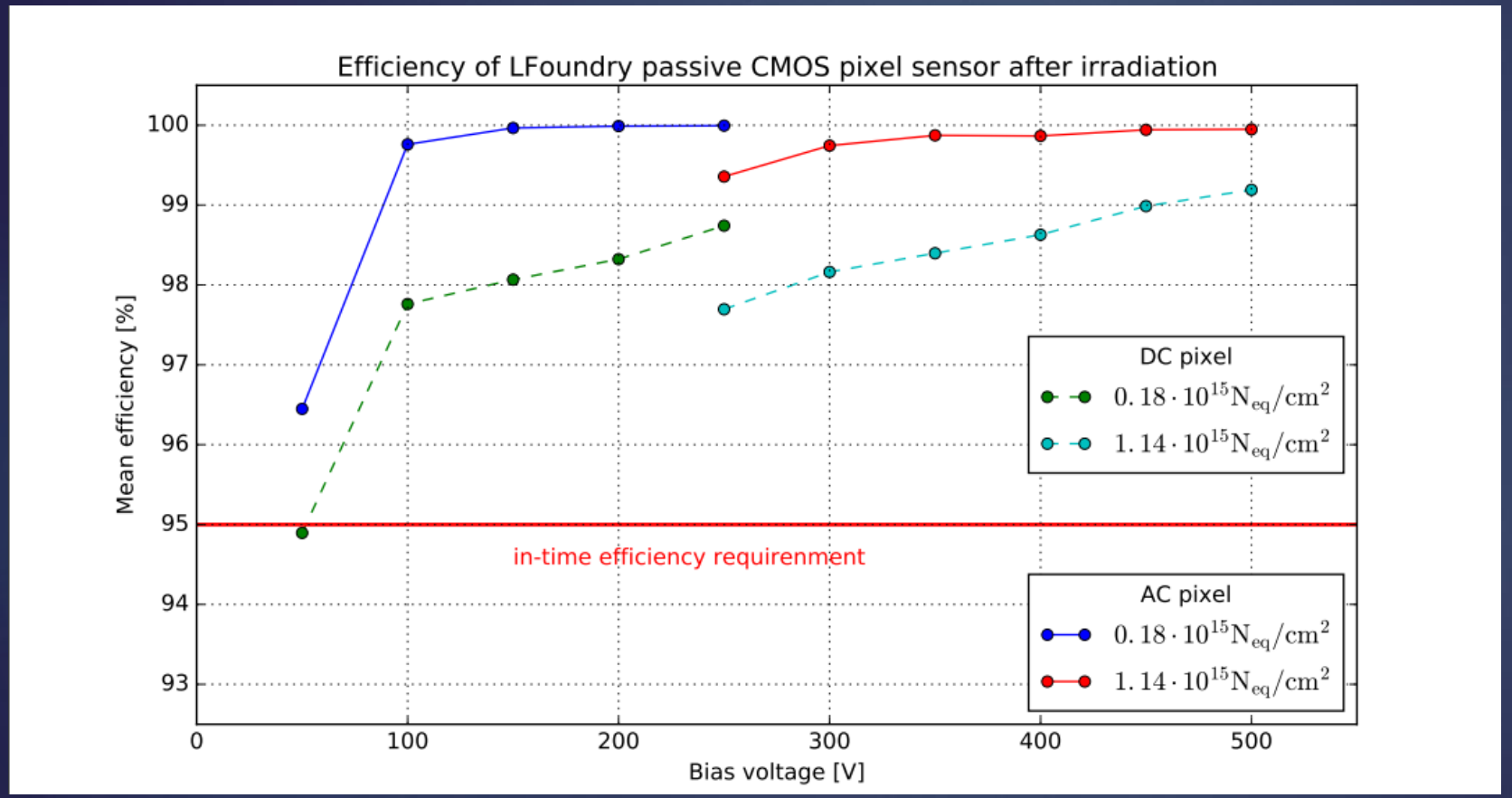
CMOS Pixels: passive

Test beam after Irradiation



Good radiation hardness!

Efficiency

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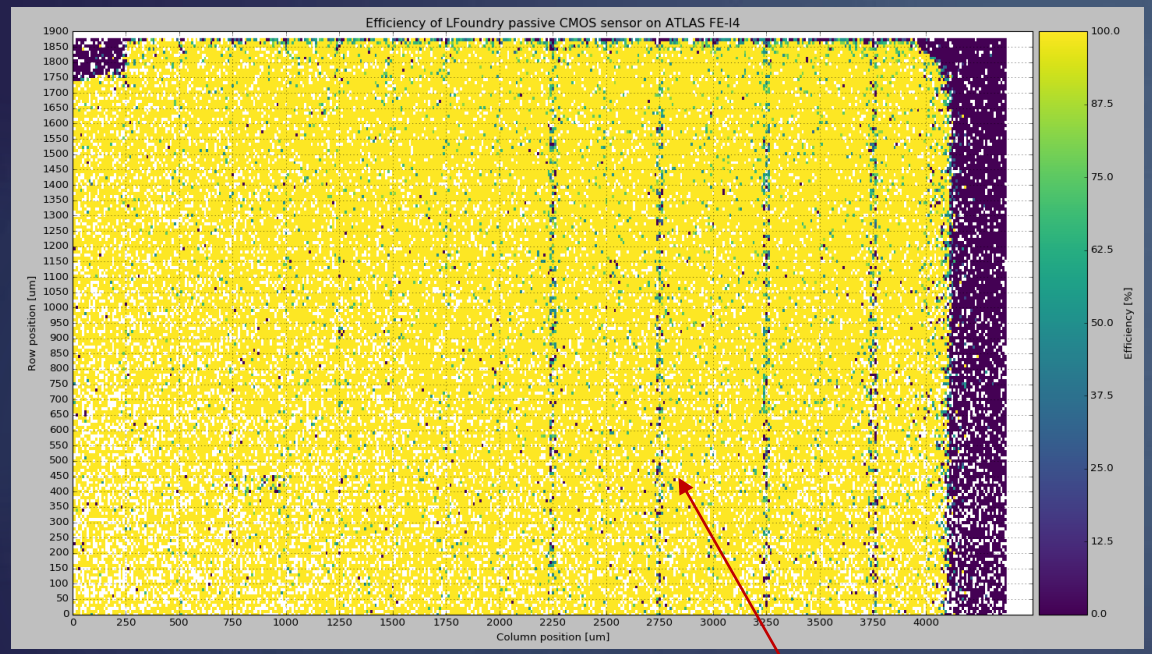
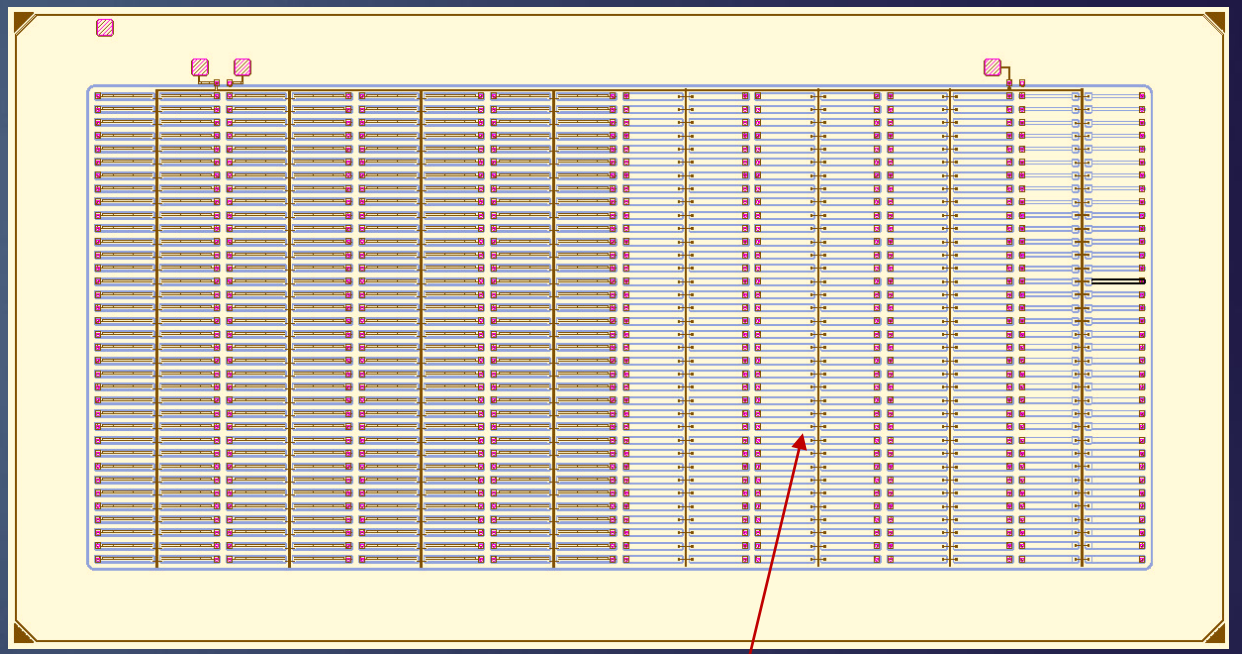
CMOS Pixel: passive

Test Beam at SPS (CERN)

- Mimosa telescope
- Fine resolution

D. Pohl, J. Janssen (Bonn)





Efficiency map

Design

Good match!

Efficiency drop in DC part related to contacts in voltage distribution.

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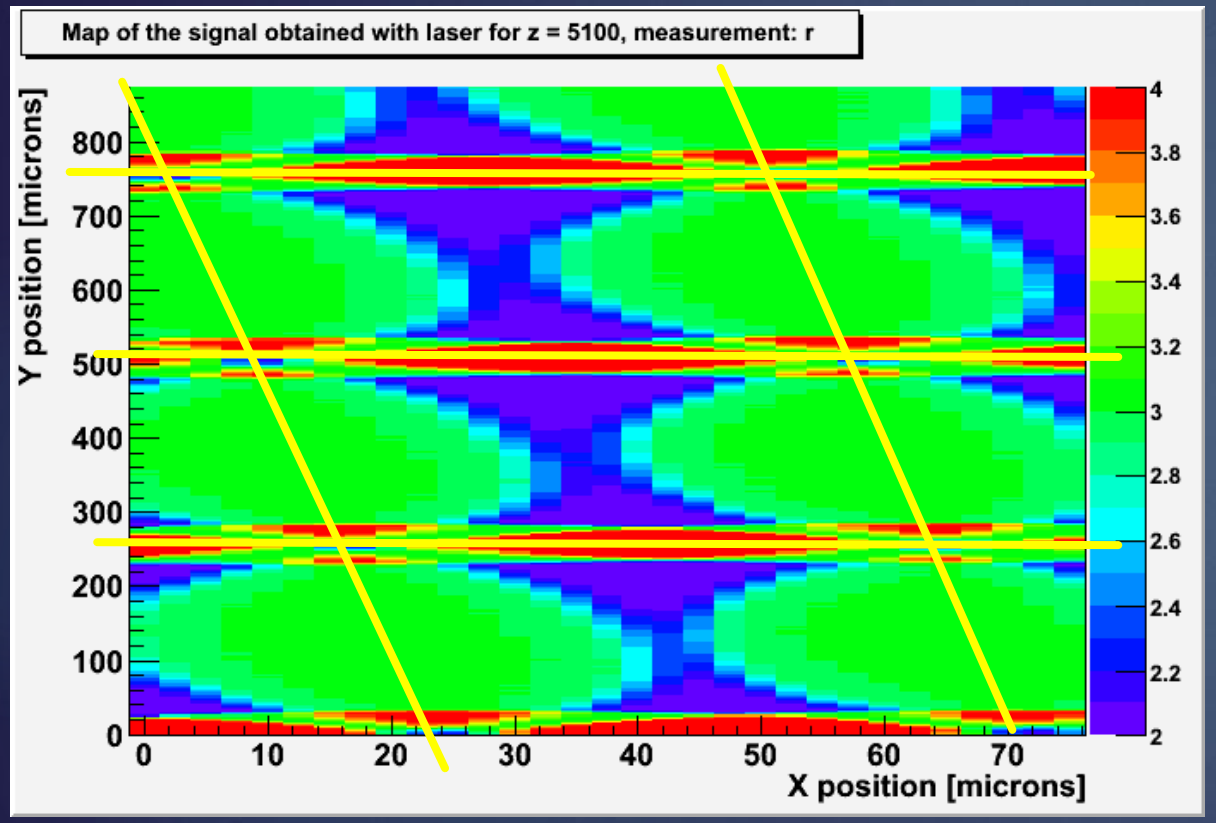
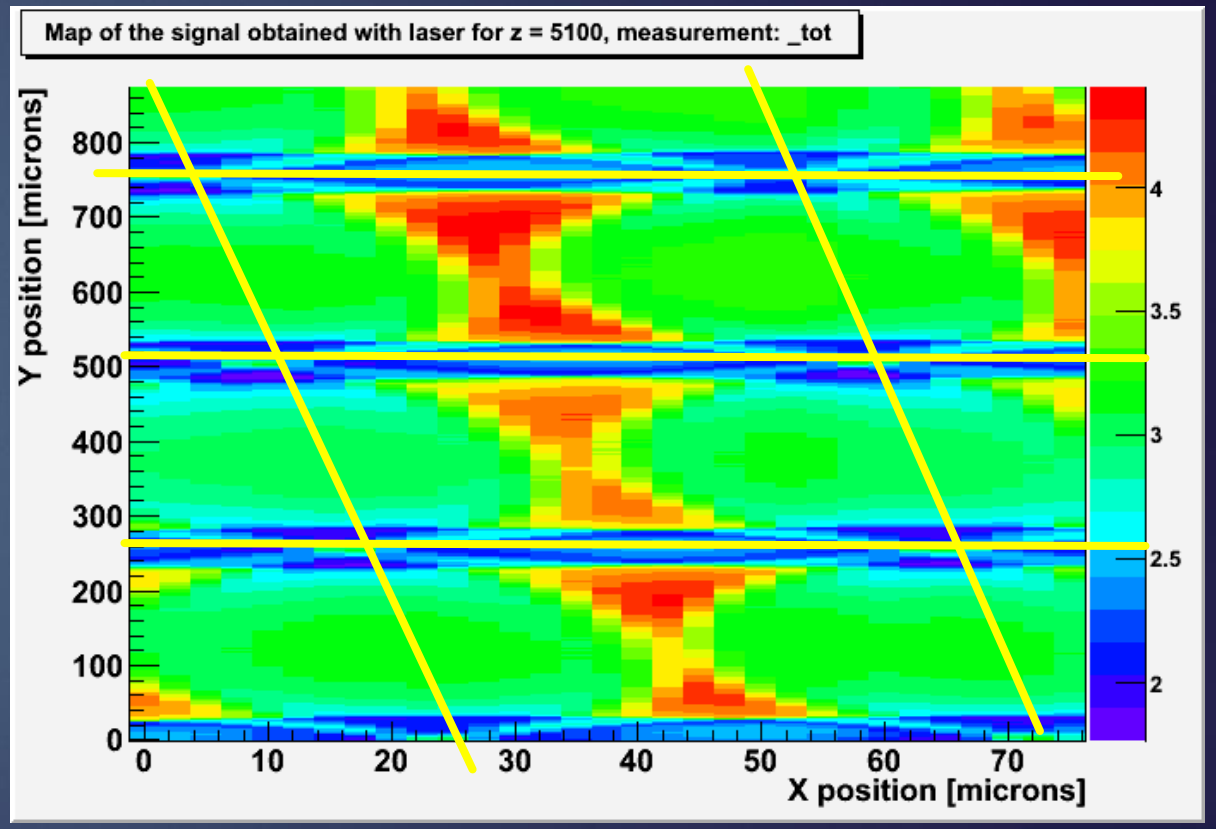
CMOS Pixels: Passive

Laser scan



Average cluster size



Average TOT (charge collected)

50x250 μm^2 reticule, slightly tilted

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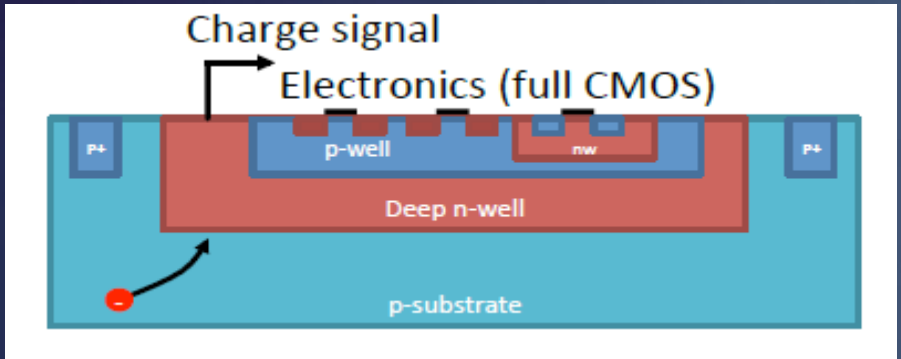
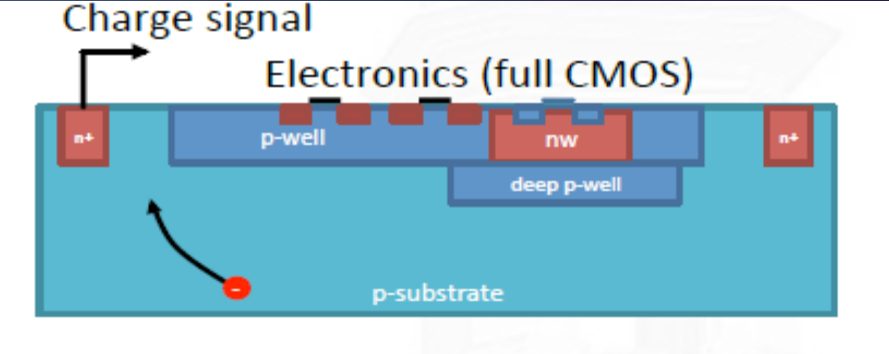
CMOS Pixels: active to monolithic

- **CCPD_LF**
  - Amplifier and discriminator inside the sensor
  - Analogue signal
  - Two possible read-outs:
    - Custom board (analogue only)
    - Capacitive glued to FE-I4
  - LFoundry 150 nm

T. Hemperek, F. Hugging, H. Kruger, T. Hirono, N. Wermes (Bonn)



2 versions:



Electronics inside the collection well

- Large fill factor for high Charge Collection Efficiency and rad-hardness
- Larger capacitance (larger noise)
- Full CMOS, isolation via deep p-well (PSUB)

Electronics outside the collection well

- Small fill factor, no competing wells
- Lower capacitance (lower noise)
- Full CMOS, isolation via deep n- and p-well

- **Next goal: fully monolithic sensor** → **LF monopix**

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Conclusions

- Good prospects for CMOS technology in High Energy Particle Physics
- Great interest from many institutions
- ATLAS has many projects under development
  - Both Pixels and Strips
  - All types of CMOS (passive, active and monolithic)
- Many issues must be fully addressed yet
  - Radiation hardness
  - Effective cost
  - In-time efficiency
  - Eventual displacement inside the tracker

NEXT

- Fully monolithic devices
- Full functional modules

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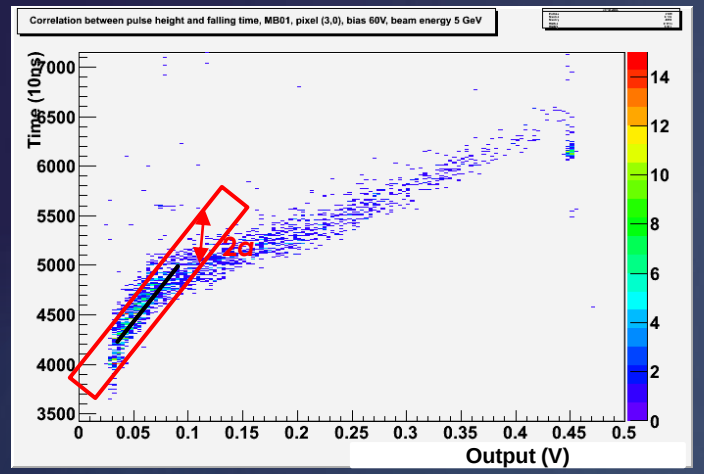
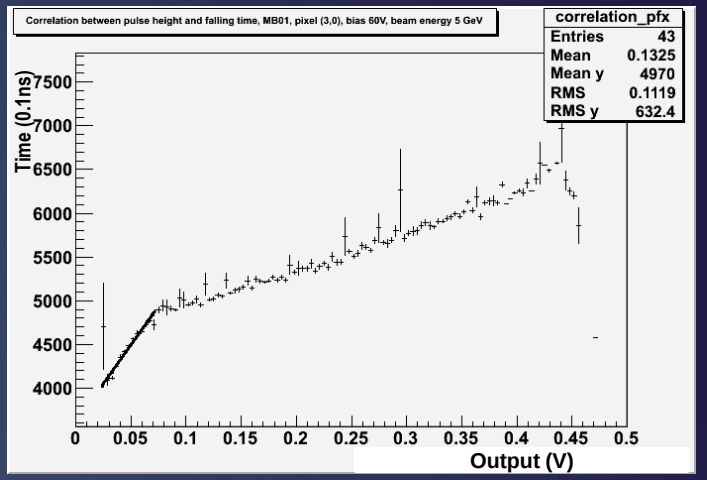
Backup: HVStripV1 irradiated Sr^{90} spectrum

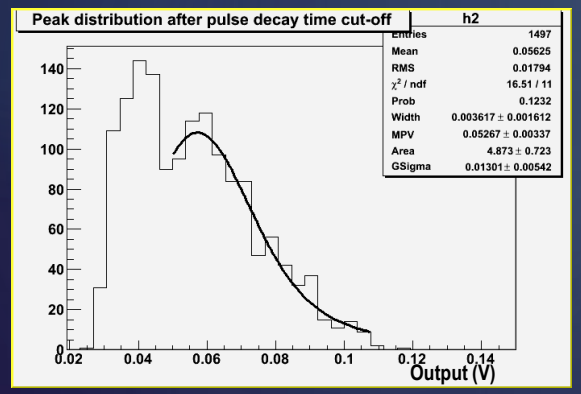


Signal-peaking time correlation:
the higher the signal, the longer it takes to reach the peak.
Two different slopes are observed, one for low and one for high charge region.

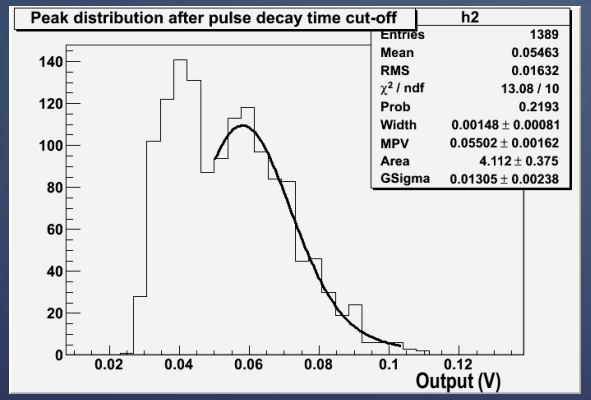
X profile

Cut close to the slope for the signal region

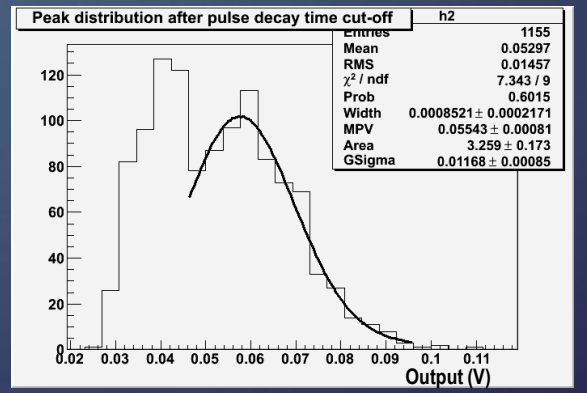




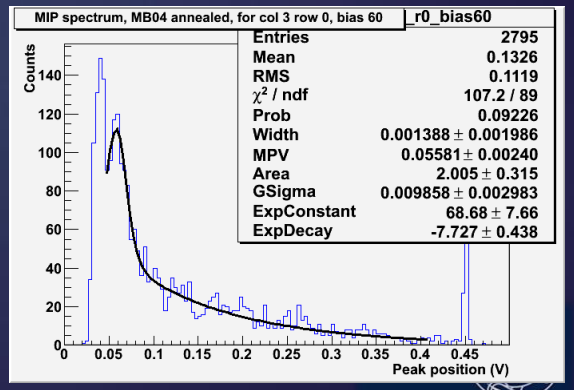
a = 400 ns



a = 300 ns



a = 200 ns



No cuts

No High charge background! MPV similar to previous fit (here no calibration is applied).

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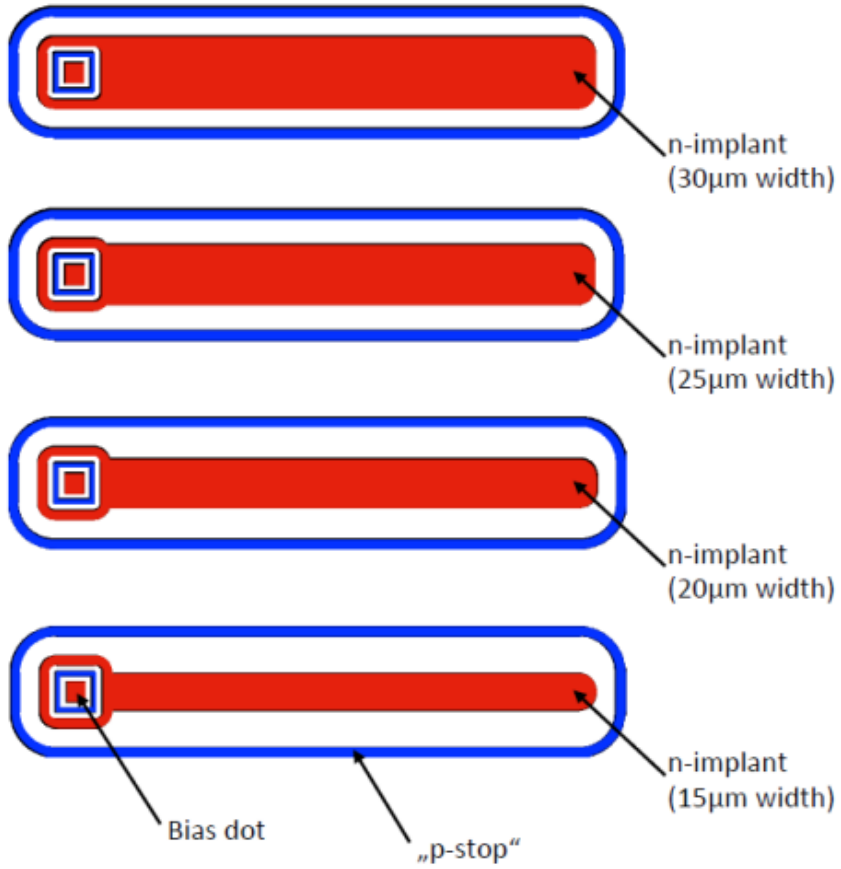
Backup: passive CMOS pixels

Pixel Layout Variants

universitätbonn

Implant width	Gap width
30µm	20µm
25µm	25µm
20µm	30µm
15µm	35µm

- Bias dot (punch-though) layout not changed
- Implant length not changed
- Implant width variation covers ~200µm of the implant length



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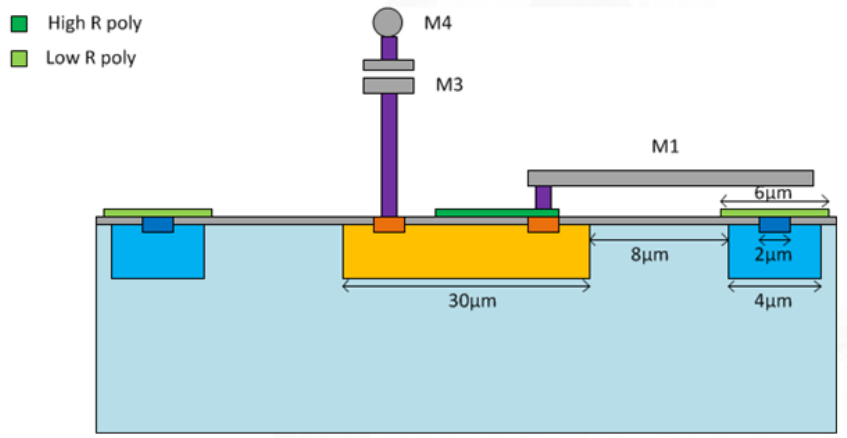
Backup: passive CMOS pixels

AC coupling

- MIM cap between M3 and M4 used for the AC coupling
  - implemented a up to 10pF capacitor into each pixel
- high resistive poly-silicon layer used for bias resistor
  - 15 MΩ resistor in each pixel
  - contributes to the input capacitance → relevant for noise
- low resistive poly-silicon layer used for field plate on top of p-stop
  - improvement of breakdown behavior
  - p-stop consists a contact to apply an external voltage



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Backup: passive CMOS pixels

More details:

- For the outer ITk pixel layers:
  - AC coupled passive CMOS sensors on 8“ CZ wafers
  - No fine pitch bump bonding necessary
    - Simplified module production, Flip-chip can be done in-house
    - Cost reduction to 1 / 3
  - Stripped down FE-65 from inner layer:
    - No leakage current compensation circutry necessary
    - Larger pixel pitch and less pixels → Lower power
    - Wafers can be ordered already equipped with C4 bumps

- For the module concept:
  - Module without larger gap pixel

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