# Development of HV-CMOS sensors at University of Liverpool

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2012-FP7-ITN-317446 INFIERI

# Outline

- Introduction to the HV-CMOS sensor technology
- Status of HV-CMOS developments and its application fields
- Previous work at Uni. Liverpool and the new submission in LFoundry 150 nm
- My work — the biasing block
- Conclusion and future plans

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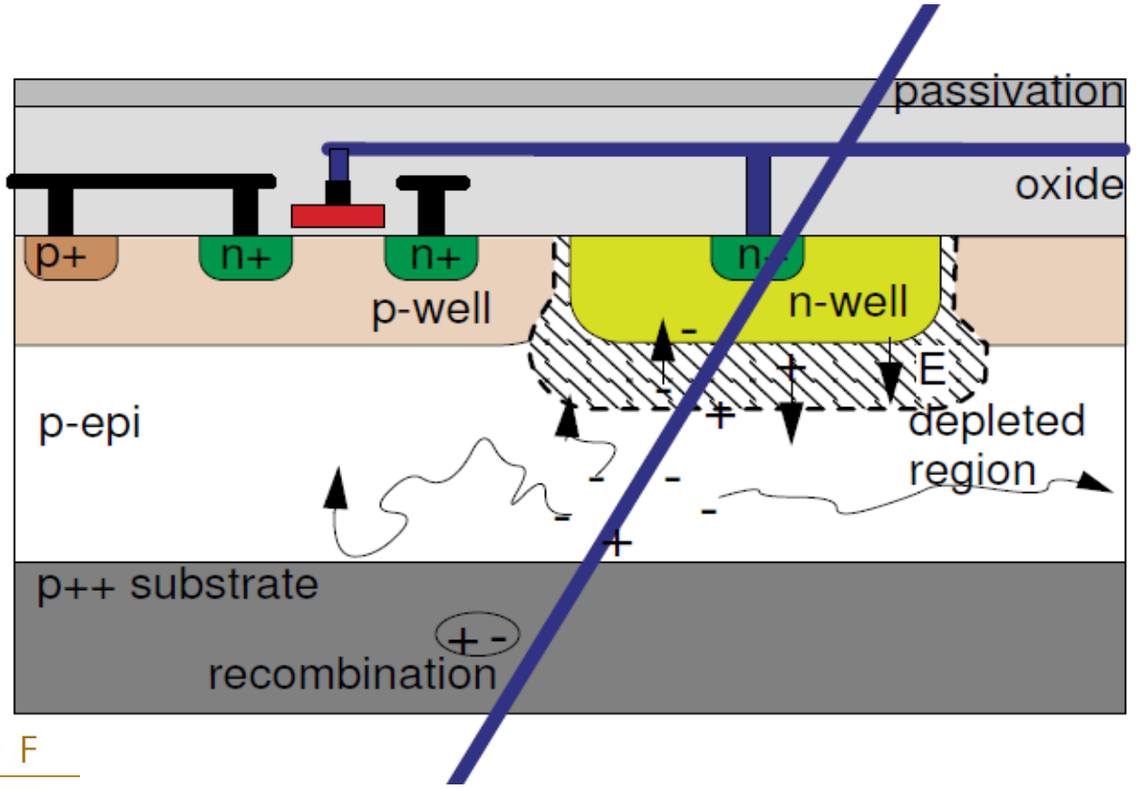
# from CMOS to HV-CMOS

Pros:
- Fabricated in commercial CMOS technologies —> high performance and low cost
- In-pixel processing electronics is possible

Cons:
- The lightly doped p-type epitaxial layer in CMOS sensors is not fully depleted as only low-voltage is supported
- Charge collection is mainly by **diffusion** (< 100 ns)
- Limited radiation tolerance (< 1 Mrad)

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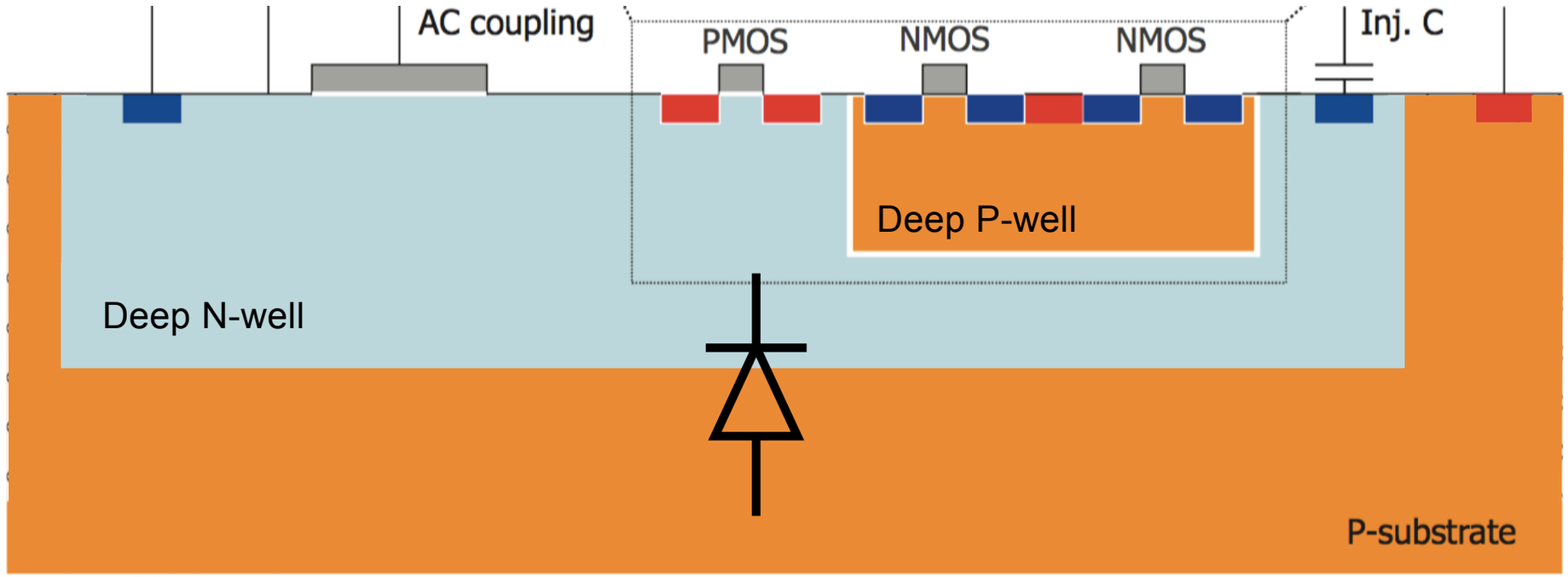
# from CMOS to HV-CMOS

- Future HEP experiments (ATLAS ITk upgrade, CLIC, Mu3e) demand **higher data rates, finer granularity, better radiation tolerance**
- HV-CMOS supports ***high negative voltages*** (<120V) to form a ***wide depletion region*** as a deep N-well / P-substrate diode that result in **higher speed** and **better radiation tolerance**
- HV-CMOS is also a Mature industry-standard technology and commercially available



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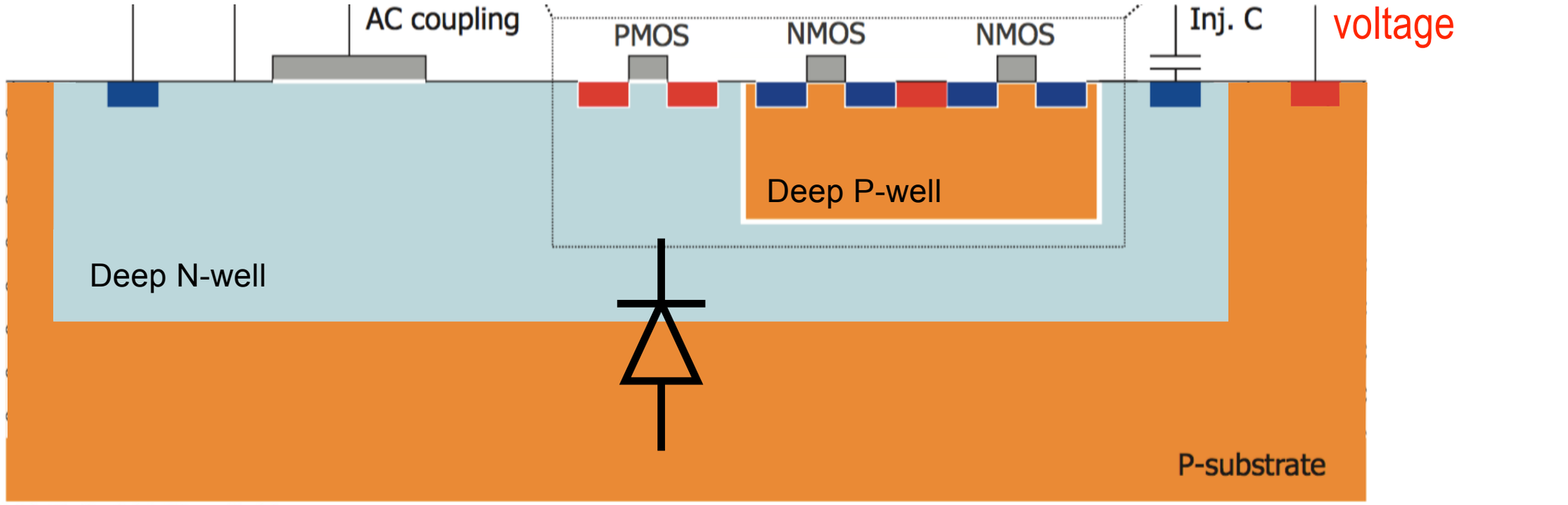

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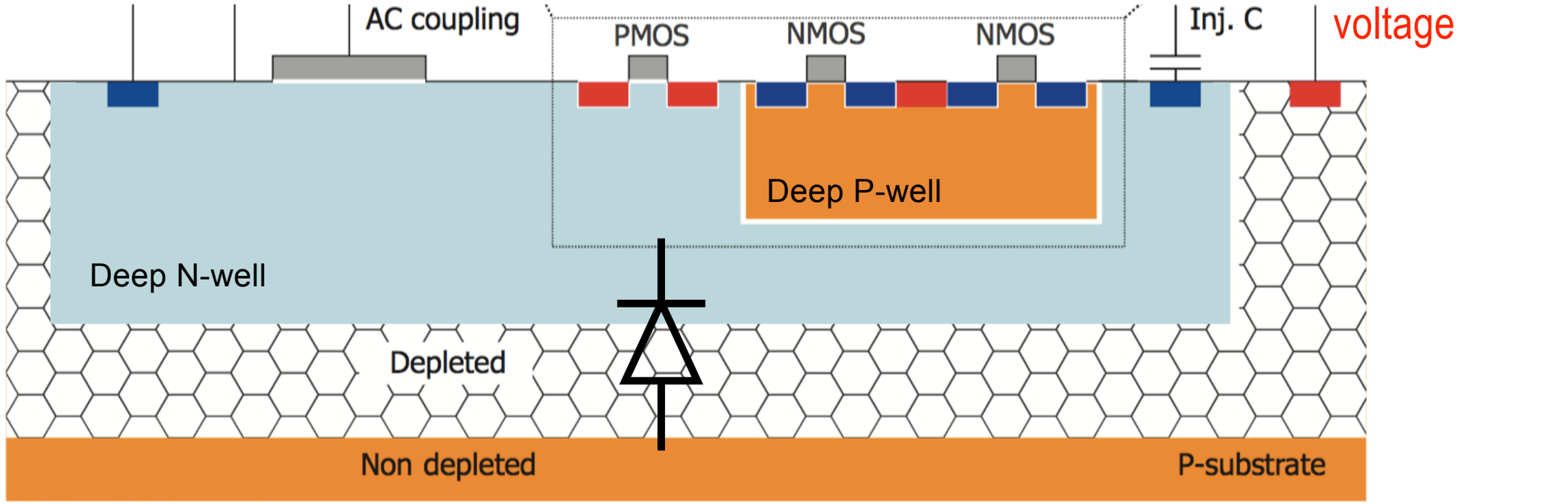

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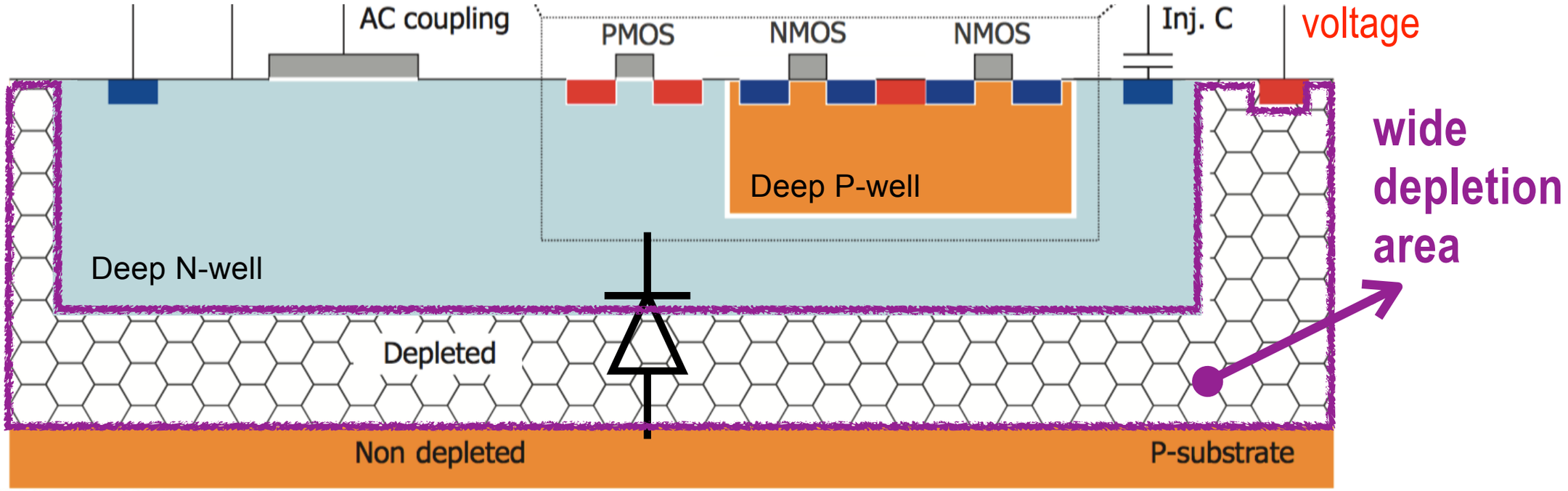

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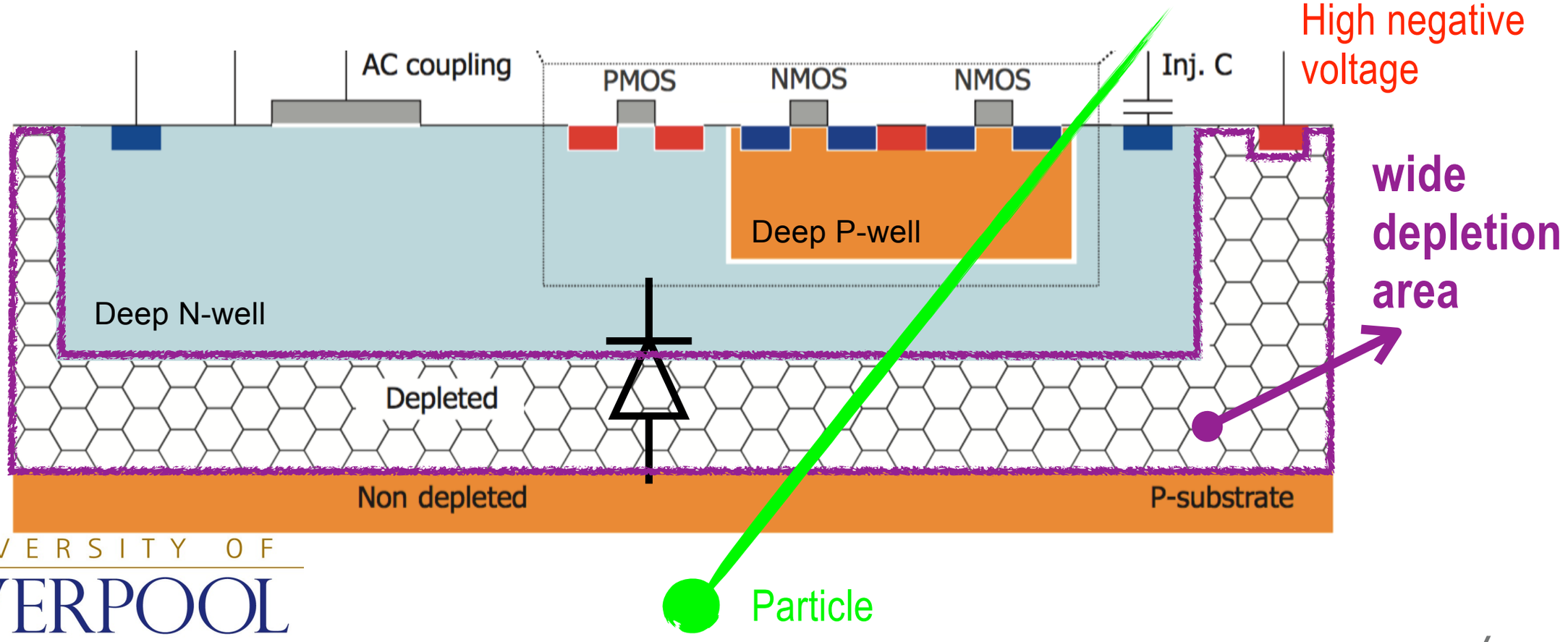

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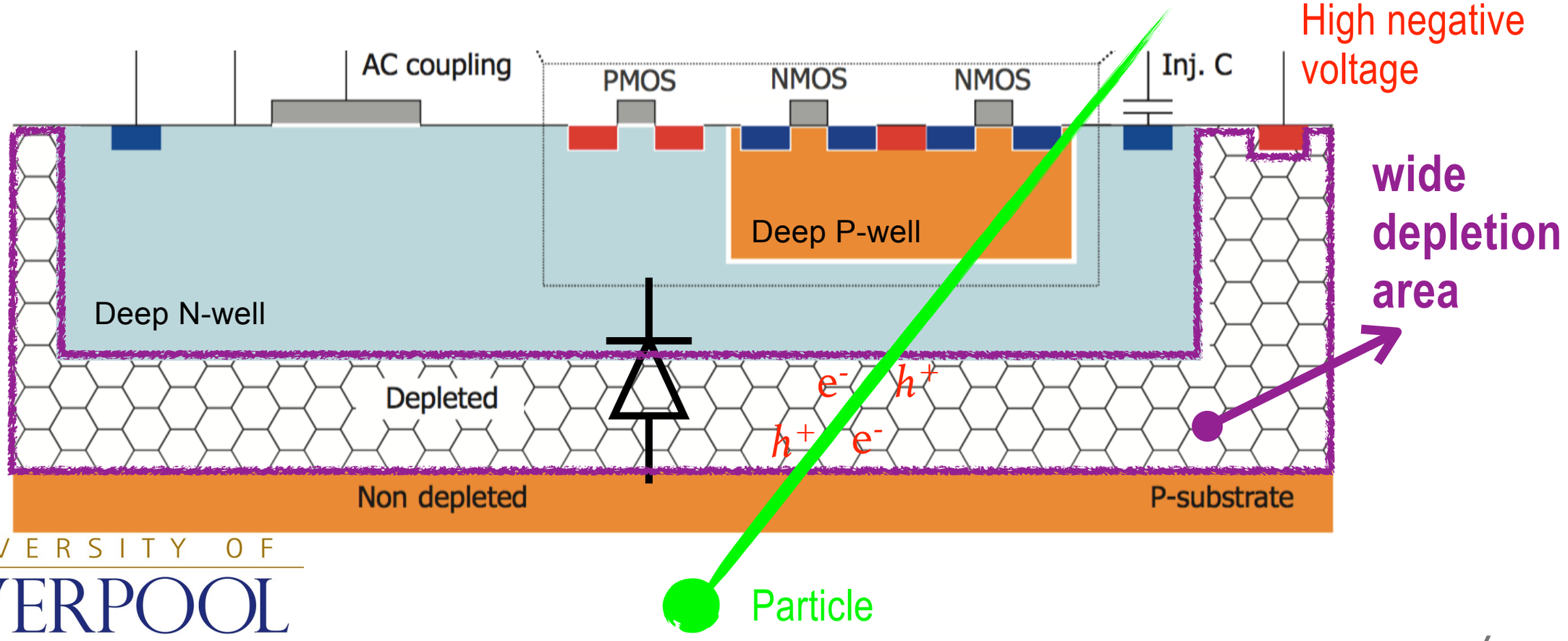
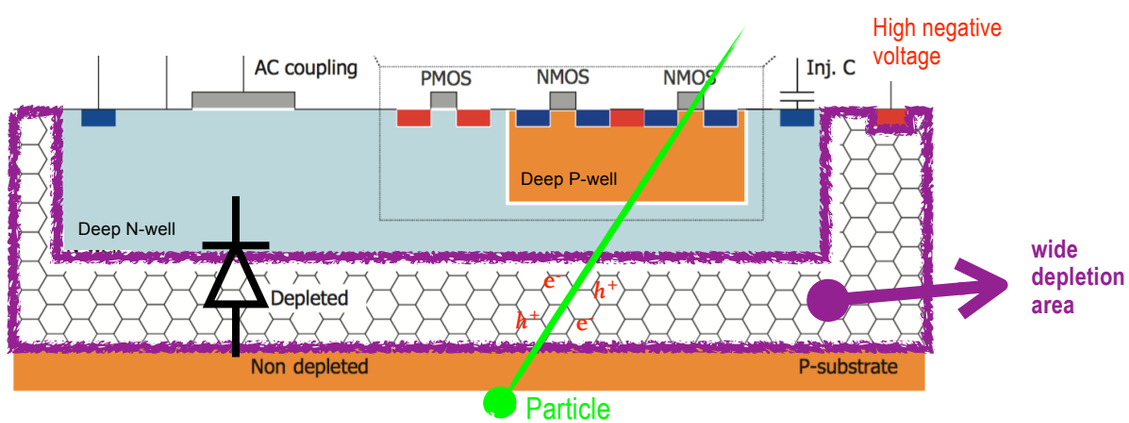


# HV-CMOS sensor technology

1. **Wide depletion** helps to improve both position and time resolution
    - High negative bias voltage (~ 120 V) generates a **high electric field** in the depletion area -> Fast charge collection via **drift** (~ 200 ps) -> **good time resolution** (< 20 ns)
    - Small sensor capacitance -> excellent noise performance -> high SNR
    - More charges generated in wider depletion area (wider with higher substrate resistivity) -> large charge signal amplitude -> high SNR
    - Lower leakage current in high radiation -> Better **radiation tolerance**

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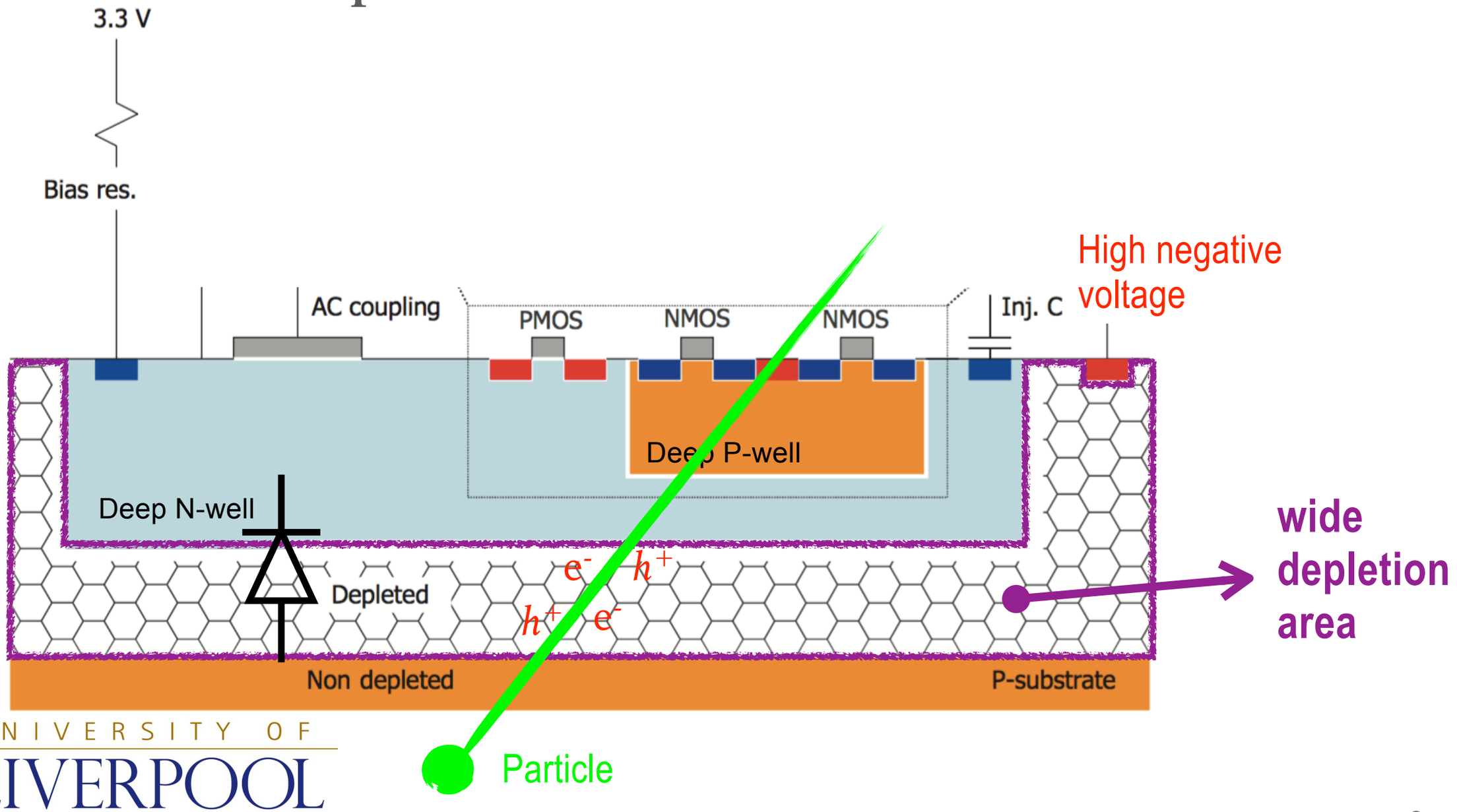
# HV-CMOS sensor technology

2. Embedded CMOS electronics within the sensing area

-> **monolithic pixel**



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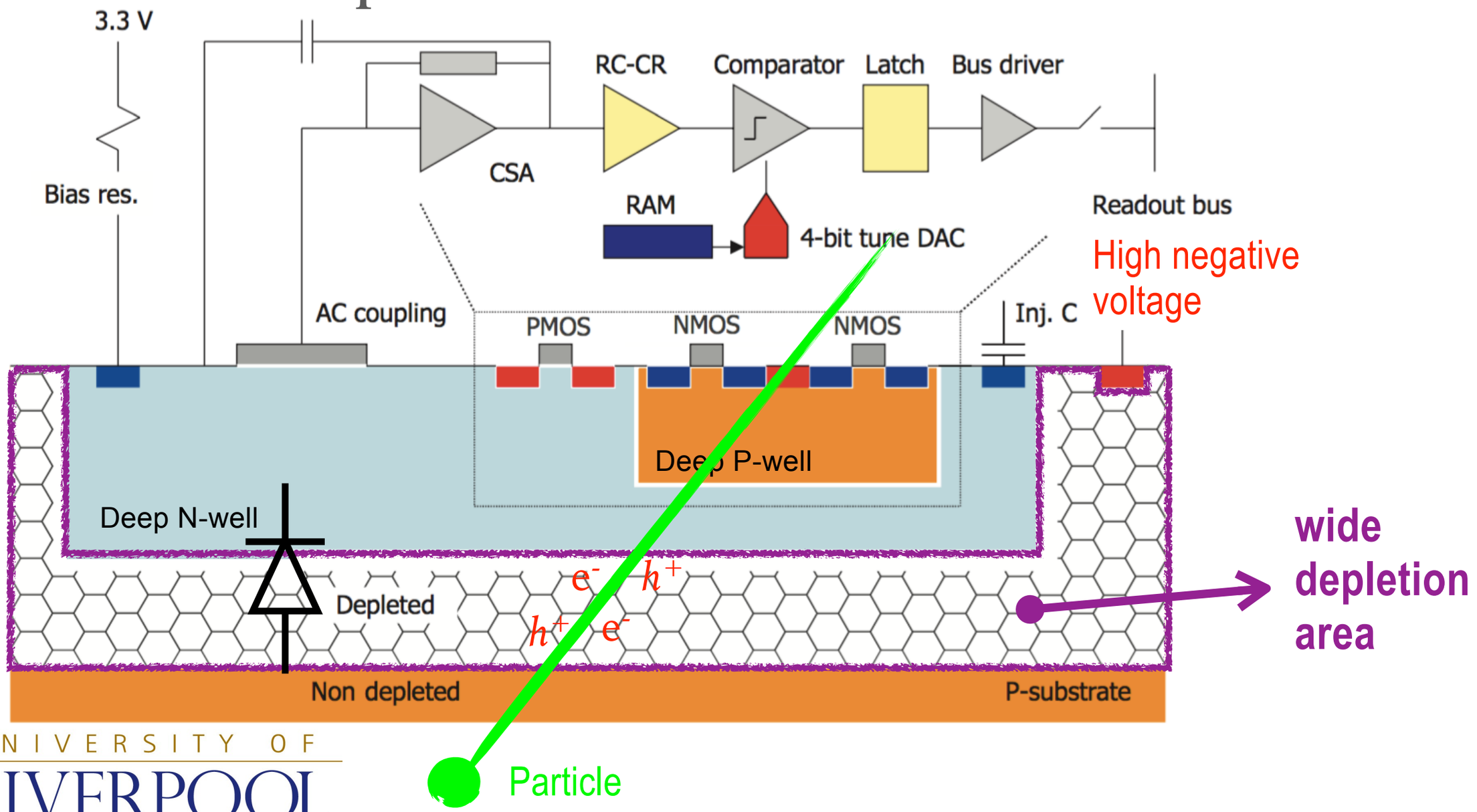
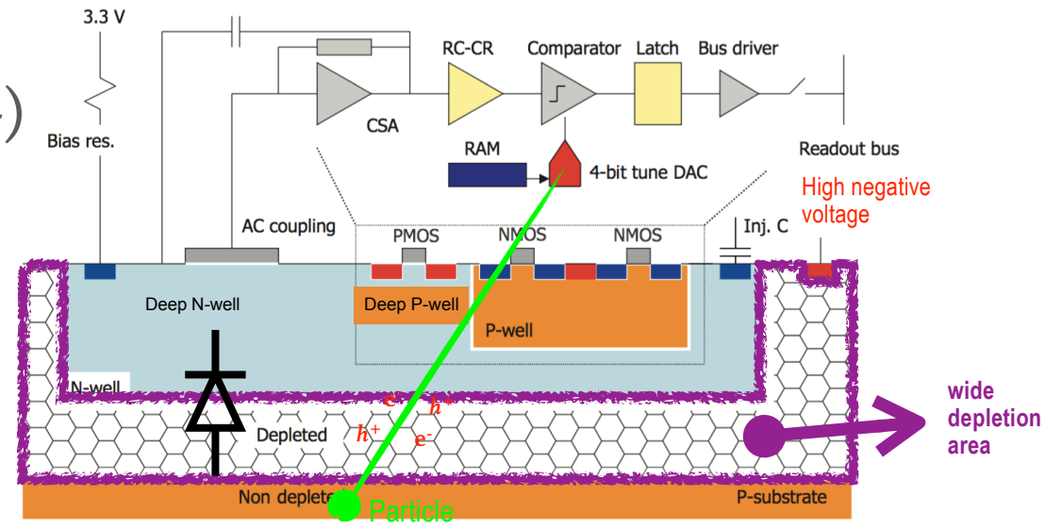


# HV-CMOS sensor technology

2. Embedded CMOS electronics within the collecting electrode -> **monolithic pixel**
   - ➤ Possible to embed complex electronics in the sensor layer (biasing circuit, CSA, shaper, comparator and even digital readout electronics) -> higher integration density of silicon
   - ➤ CMOS electronics can be isolated from the high-voltage-biased sensing junction when enough layers are available in the technology -> small crosstalk noise
3. Small individual pixels (~ 50 μm × 50 μm) -> **good granularity**
4. **Thin sensors** (≥ 50 μm) -> reduce particle multi-scattering and good position resolution
5. Compatibility with existing readout chips (FE-I4)

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# HV-CMOS sensors – Available foundries

| | AMS | LFoundry | ESPROS | XFAB | TowerJazz |
|---|---|---|---|---|---|
| Feature node | 0.35µm/180nm | 150nm | 150nm | 180nm | 180nm |
| HV | ≤100V/≤150V | ≤60V | ≤15V | ≤200V | ≤5V |
| HR | 2016/Yes | Yes | Yes | Yes | Yes |
| Quadruple-well | No (triple) | Yes | Yes | No (BOX) | Yes |
| Metal layers | 6/4 | 6 | 6 | 6 | 6 |
| Backside processing | No | Yes | Yes | No | Yes |
| Stitching | No | Yes | No | No | Yes |
| TSV | Yes | No | No | No | No |

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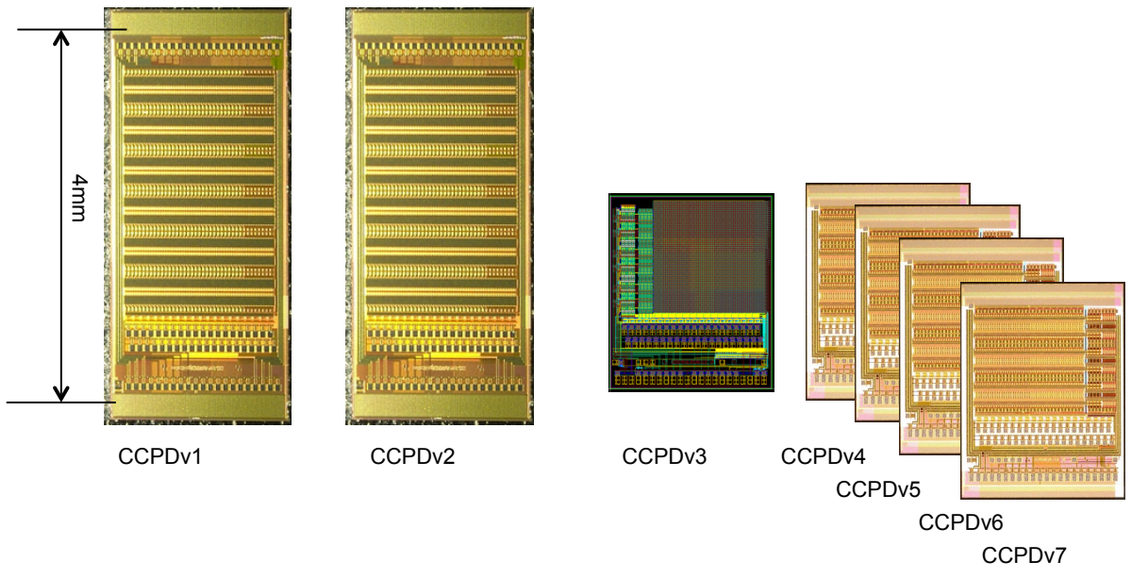
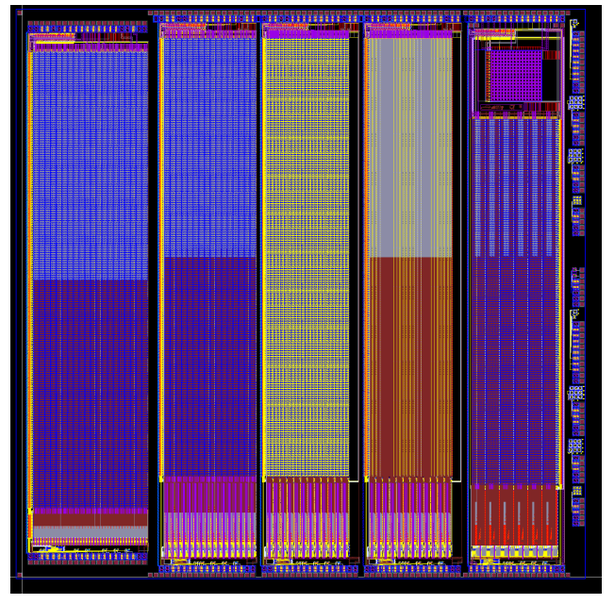
# Status of HV-CMOS developments

- First HV-CMOS chip was submitted in HV-AMS 0.35 μm by Ivan Peric in 2006, which proved the concept of HV-CMOS sensors having complex CMOS electronics implemented inside the charge-collecting DNWELL
- Many developments have been under way since then:
  - in different technologies: mostly in HV-AMS 0.35 μm / 180 nm and LFoundry 150 nm, also in ESPROS 150 nm, XFAB 180 nm, TJ 180 nm  and etc.
  - targeting at various applications: Particle Physics (ATLAS upgrade, ILC / CLIC and Mu3e (the first real application of HV-CMOS sensors)), Astro-Physics, Medical imaging
  - by several groups: CERN, IFAE, KIT, SLAC, Uni. Bonn, Uni. Liverpool, Uni. Geneva and etc.




Evolvement of CCPD in AMS H18 HVCMOS



Monolithic Sensors in LFA15 Process
1 cm × 1 cm, August 2016

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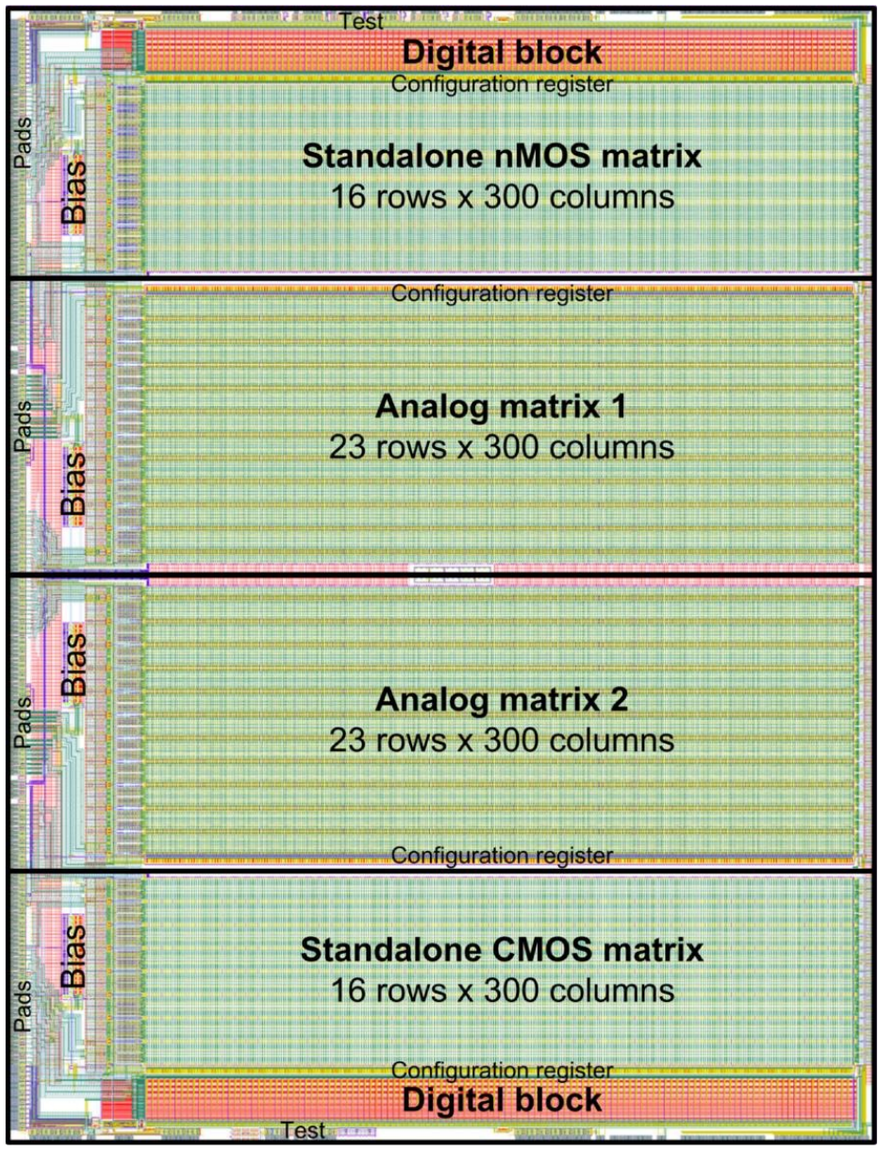
# Previous work in Liverpool – H35DEMO




- The **University of Liverpool** started developing HV-CMOS sensors in 2014
- First submission: **H35DEMO** in AMS 0.35 µm High-Voltage CMOS technology
  - submission in October 2015 and wafer delivered in December 2015
  - different substrate resistivity to test its impact on SNR - 20 Ω·cm (standard), 80 Ω·cm, 200 Ω·cm, 1 KΩ·cm
- Four arrays with different features:
  1. standalone nMOS matrix

     - digital pixels with in-pixel nMOS comparators

     - standalone digital readout
  2. two analog matrices

     - 2 identical arrays with different gain and speed
  3. standalone CMOS matrix

     - analog pixels with off-pixels CMOS comparators in the Periphery

     - standalone digital readout

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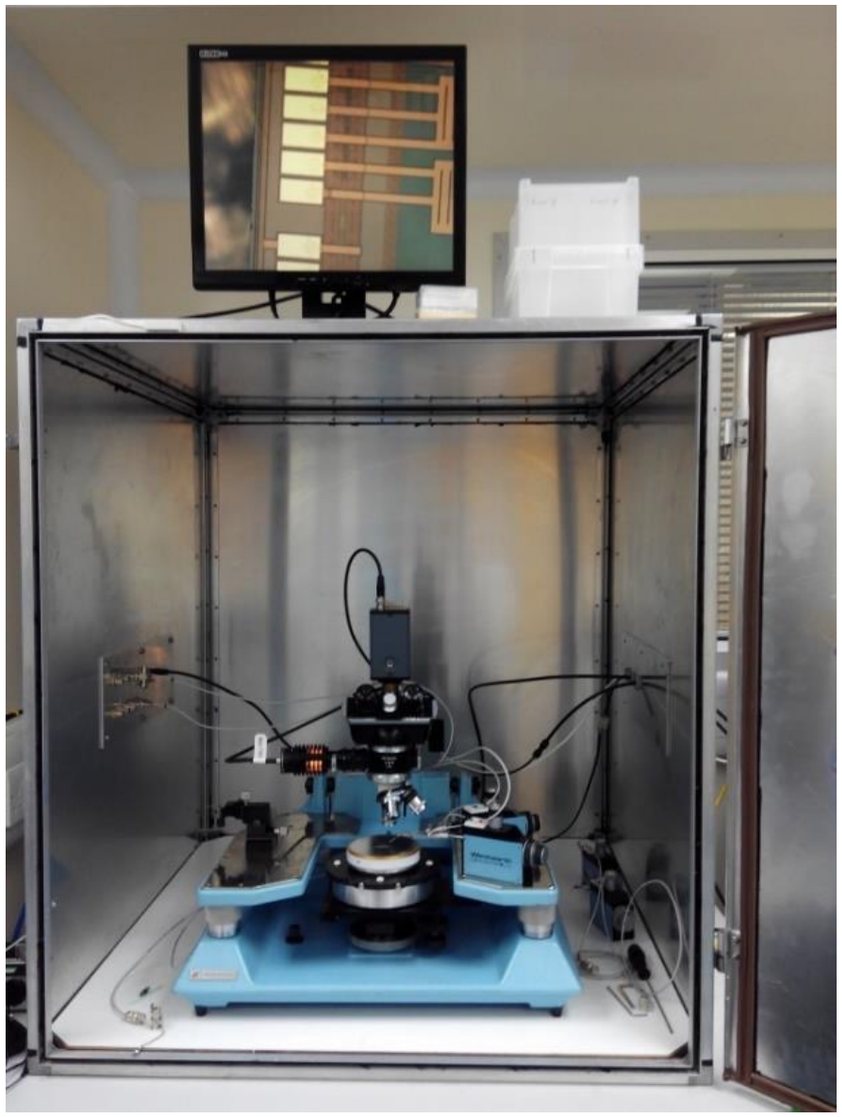
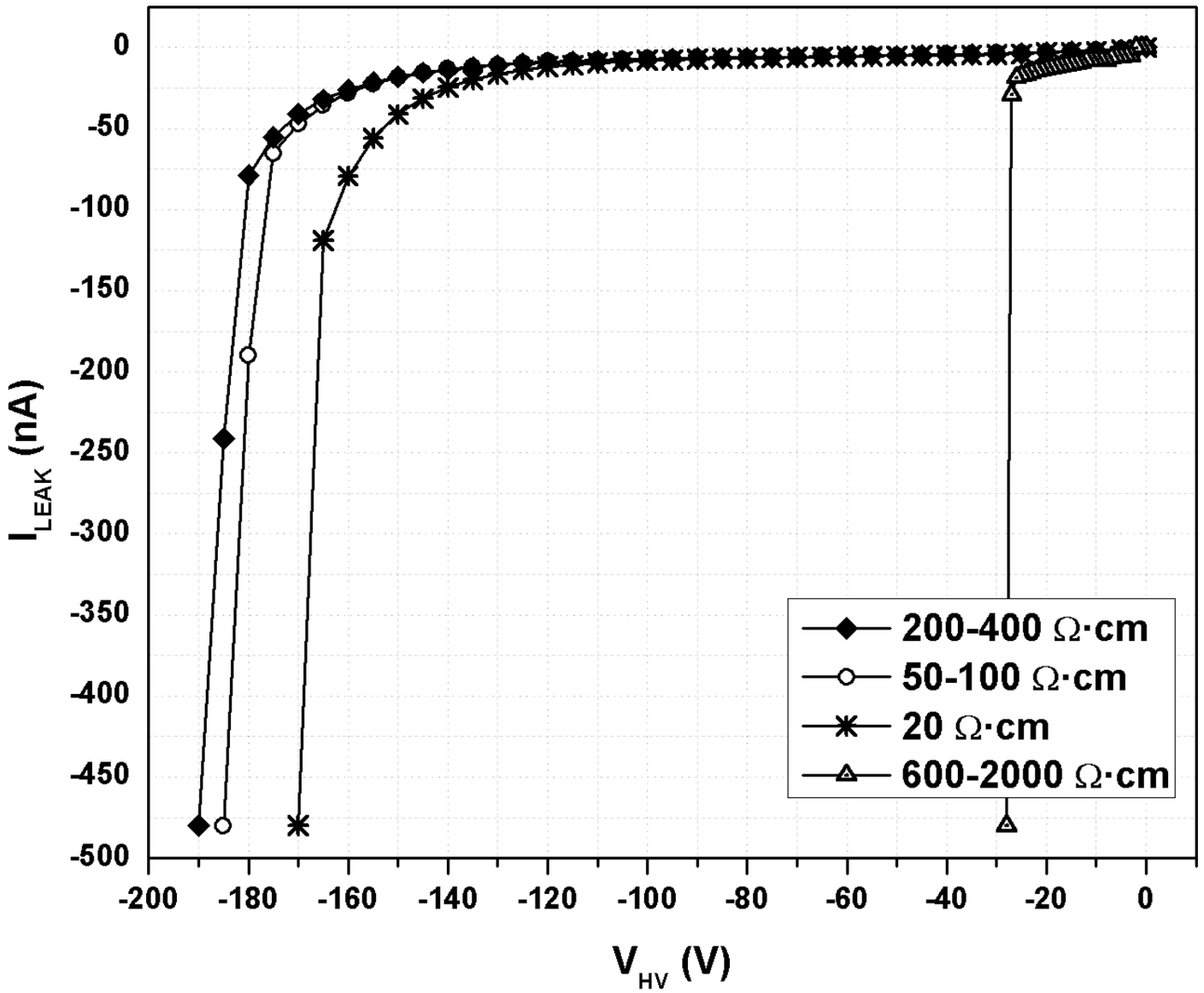
# Previous work at Liverpool – H35DEMO



Probe station in University of Liverpool clean room

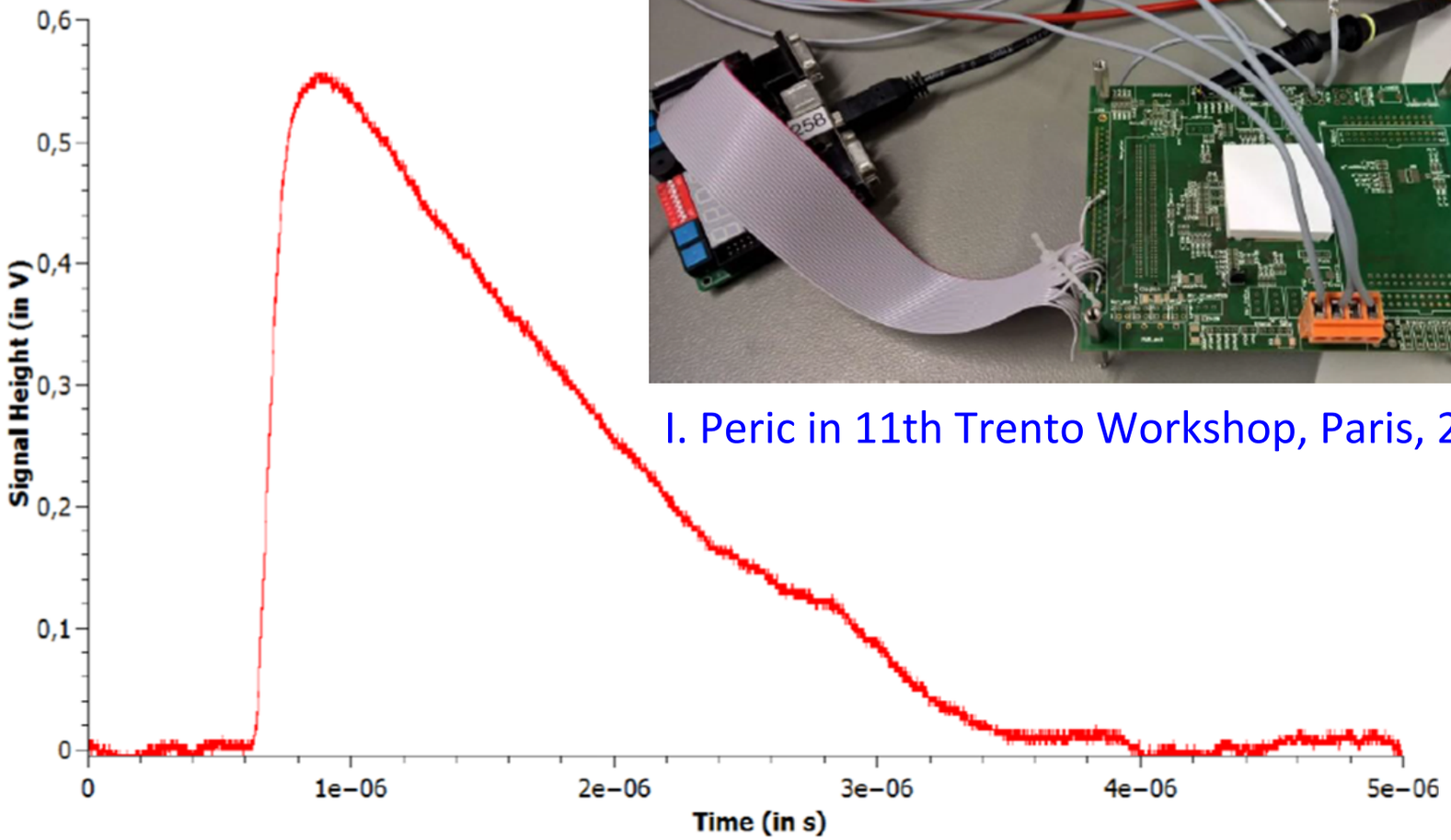



$I_{LEAK} < 10$ nA

$I_{LEAK} < 2.2$ nA / cm$^2$

# Previous work at Liverpool – H35DEMO

- On-going measurements are taking place in parallel in different institues






I. Peric in 11th Trento Workshop, Paris, 2016

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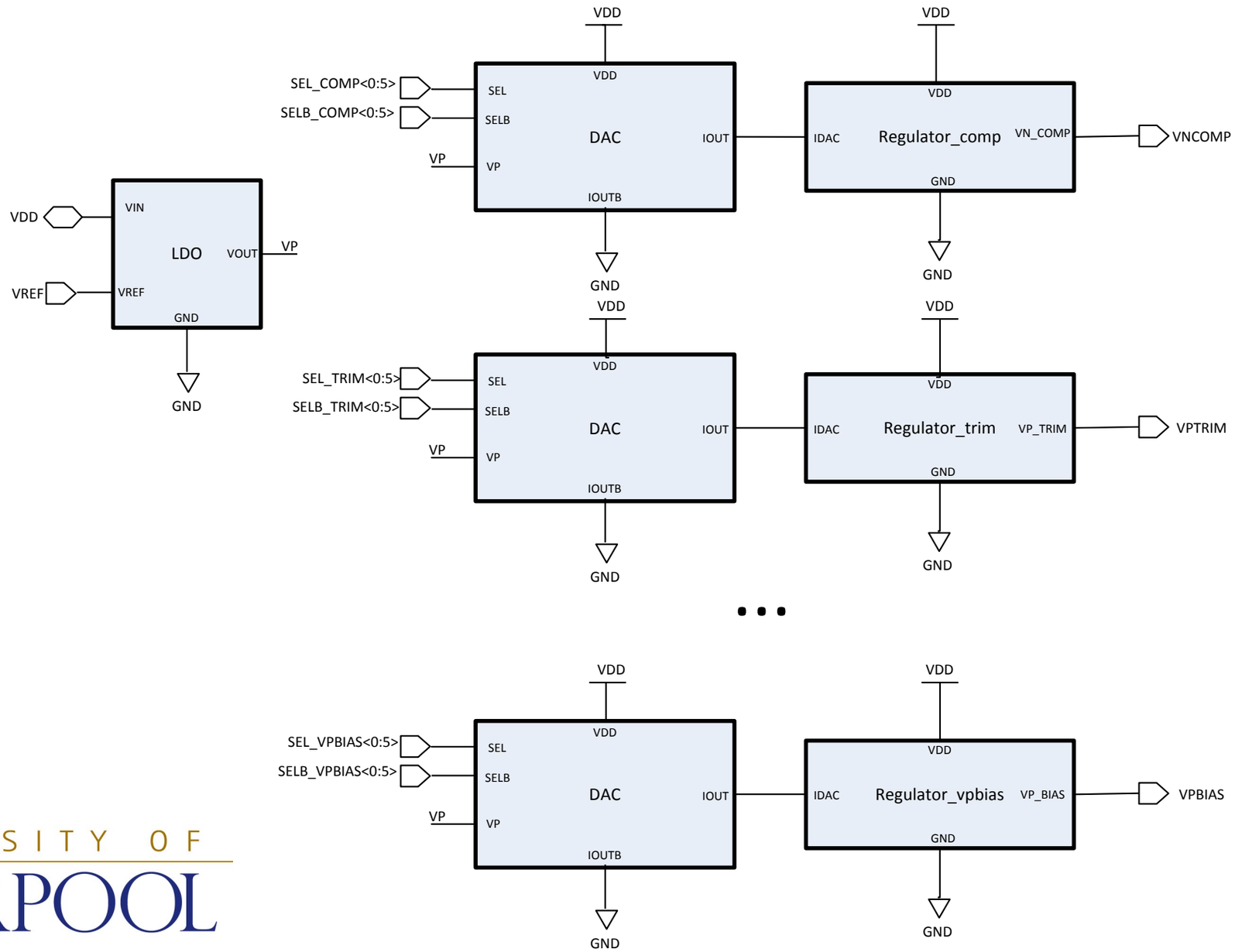
# New submission in LFoundry 150 nm

- Design of an HV-CMOS sensor prototype in LFoundry 150 nm is now ready for submission and will be submitted by the end of October 2016
- The prototype includes 2 matrices of different features:
  - **Matrix 1**: 50 µm × 50 µm pixels with FE-I3 readout circuit inside the pixel area
  - **Matrix 2**: 75 µm × 75 µm pixels with counters for photon counting
- Fabrication in different substrate resistivity (HR) are foreseen
- Prototype area will be 5 mm×5 mm (MPW)

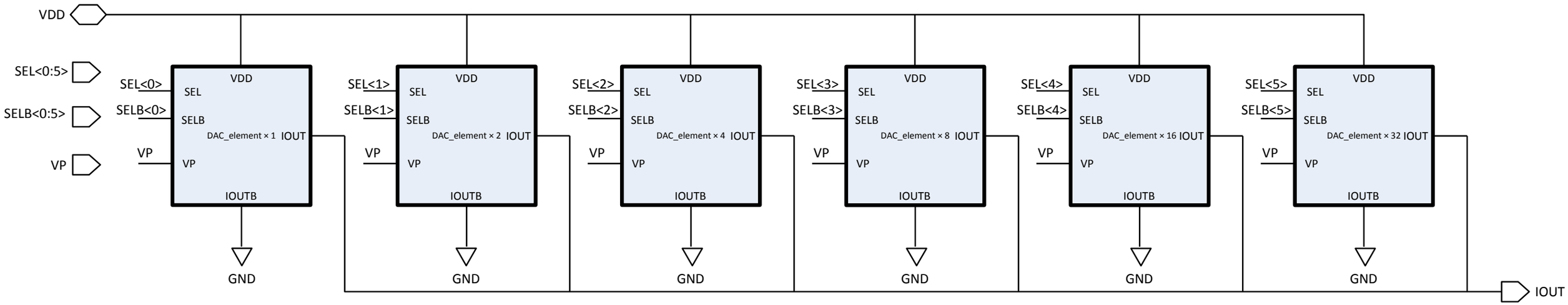
# My work – Design of the biasing block

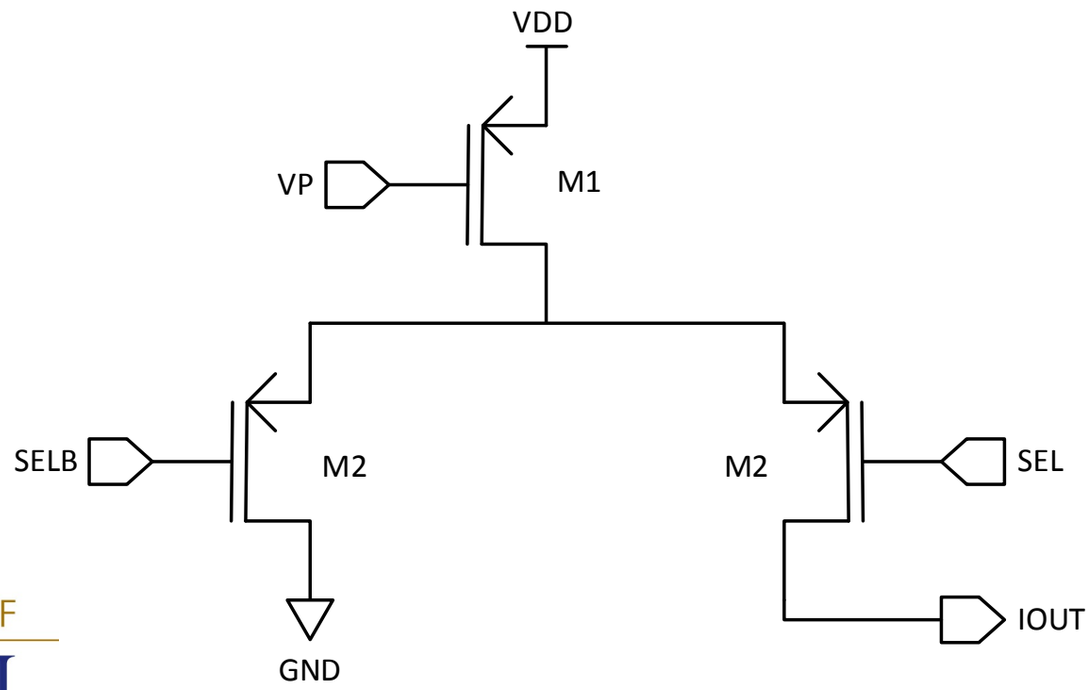
- A biasing block in general produces the biasing voltages and currents for the whole sensor to keep it in the proper working condition
- It is made up of 3 parts: **DACs**, **Current Regulators**, and the **LDO**



# The biasing block – DAC

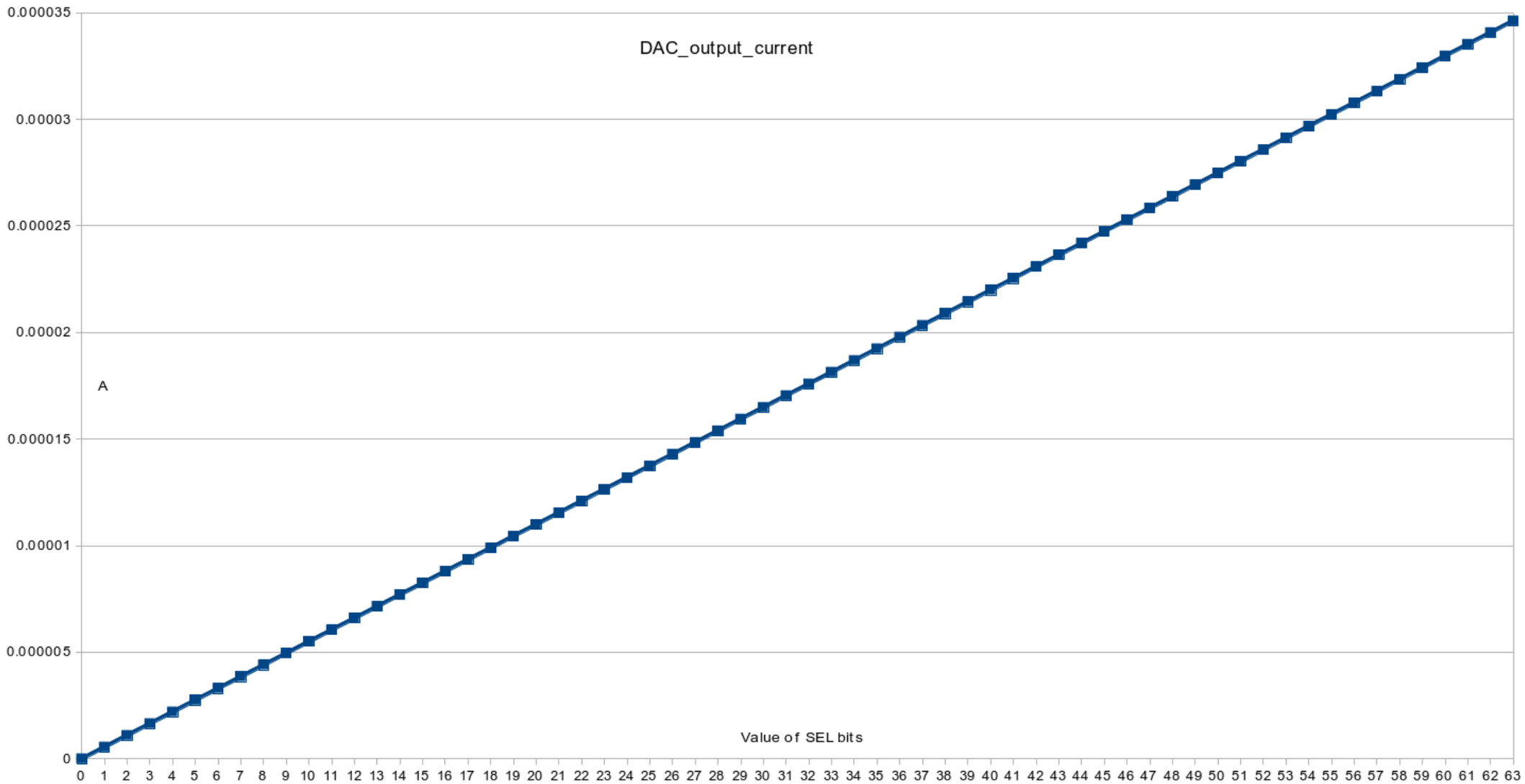
- Its output changes according to the digital input control bits SEL<5:0>
- It takes the reference voltage from LDO



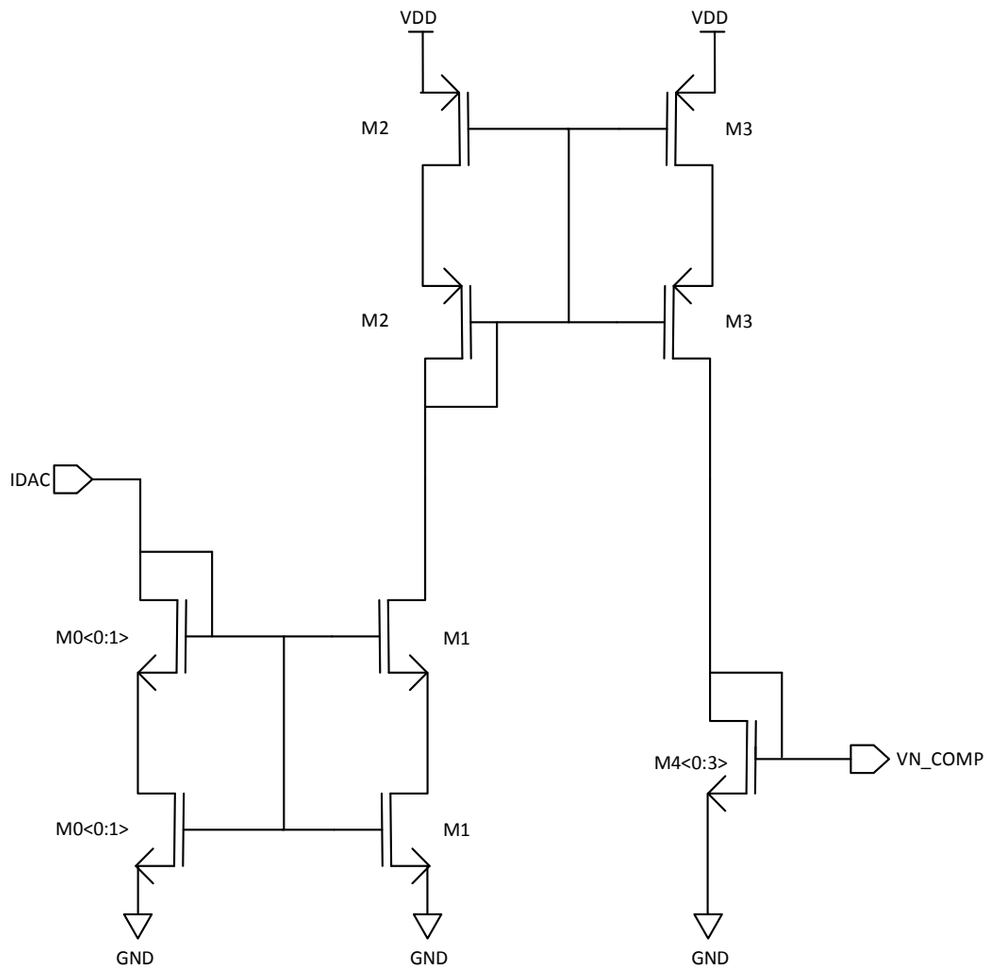
# The biasing block – DAC

- With VP = 1.123 V, its output current range is 0 ~ 34.5 µA



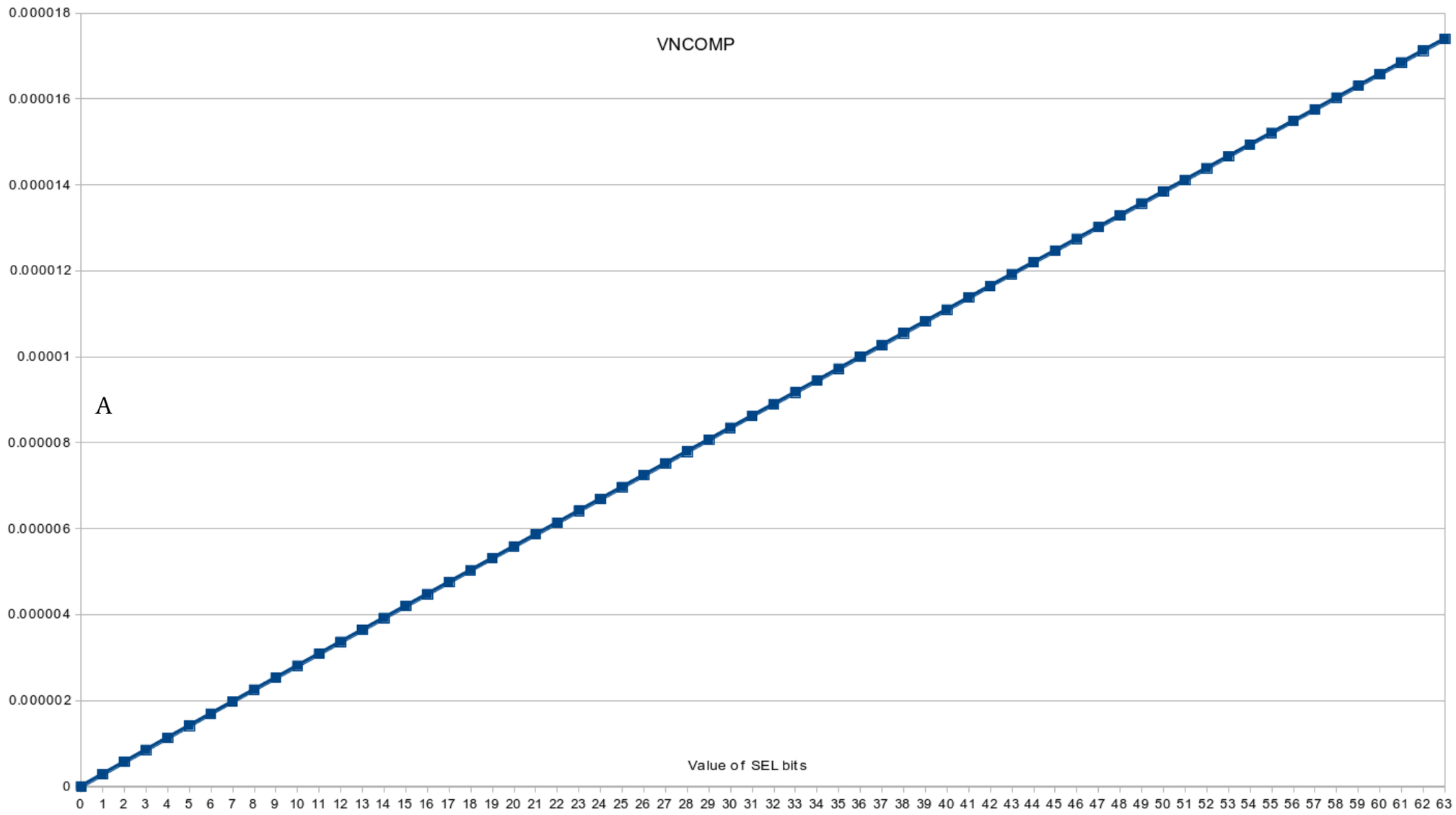
# The biasing block – Current Regulator

- Current Regulators are basically combinations of current mirrors that regulate the currents generated by DACs to the desired range of each bias channel.
- The regulating ratio can be adjusted by changing the sizes and numbers of transistors in the current mirrors
- Each channel has its own current regulator of different ratios.



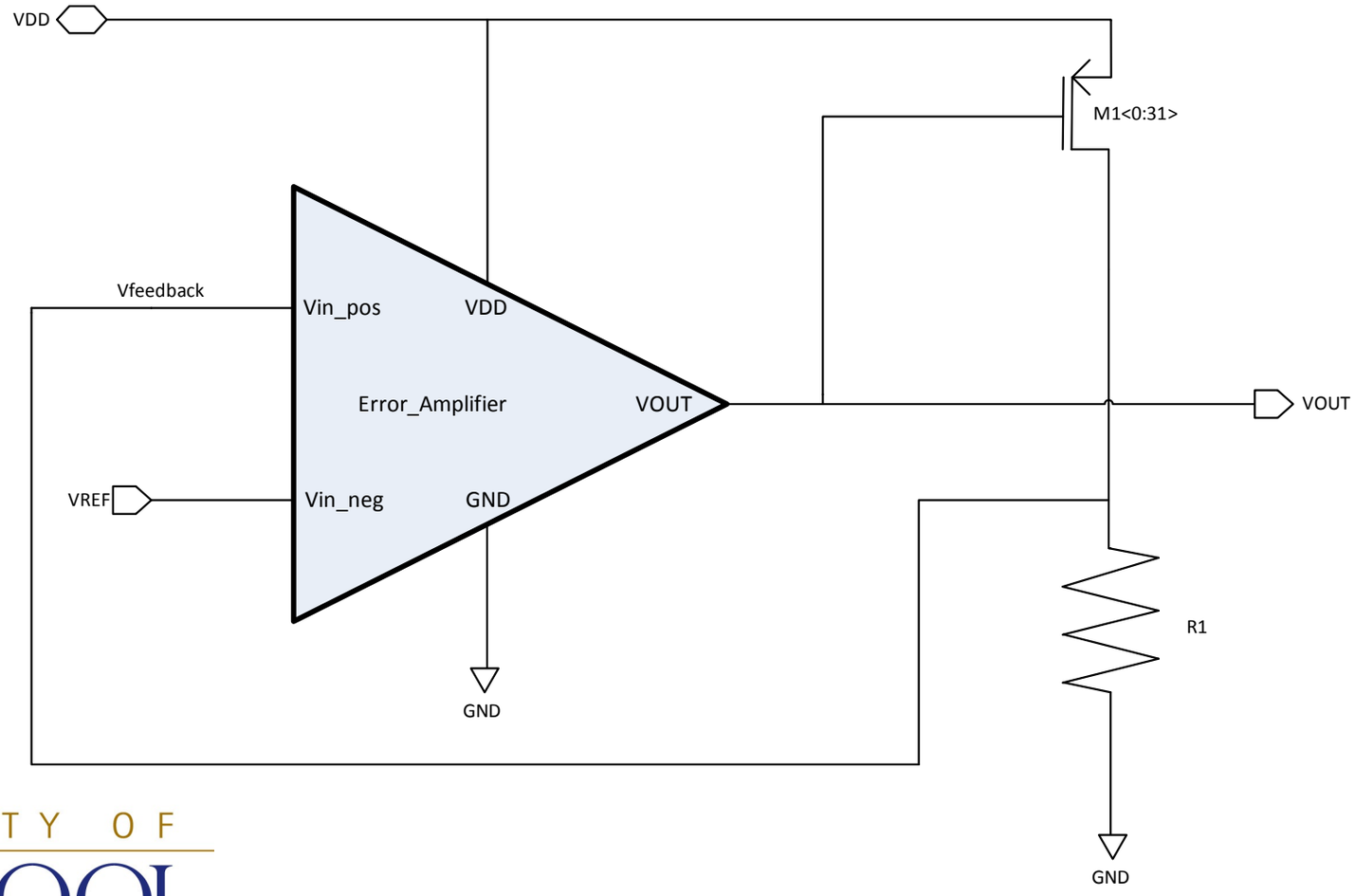
# The biasing block – Current Regulator

- The relationship between the current biased by VNCOMP and its  input SEL value as an example is shown below (0 ~ 17.5 μA):



# The biasing block – LDO

- To improve performance of bias circuits, introduce a Low-Dropout (**LDO**) voltage regulator, its output biasing voltage VOUT keeps the output currents from DACs stable despite changes in the power supply voltage
- If there is variation in VDD, VOUT can change correspondingly to keep the current through M1 transistor constant



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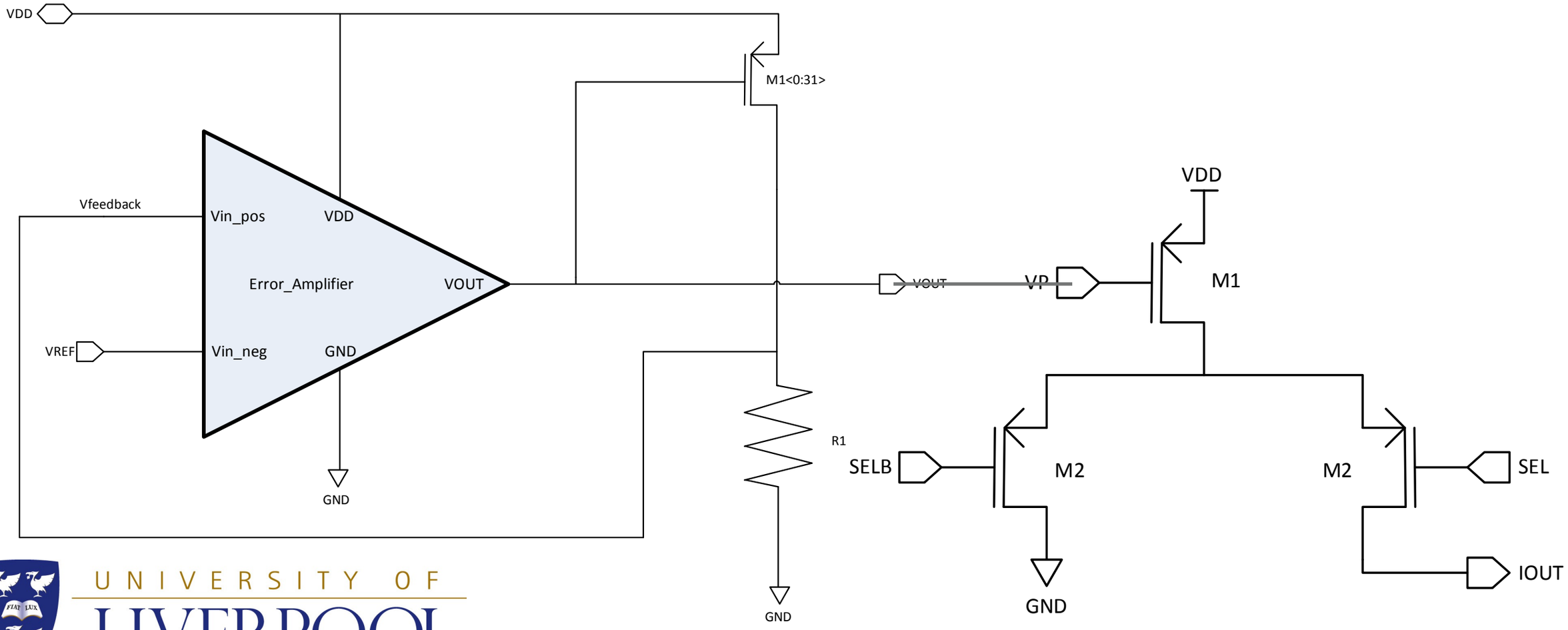
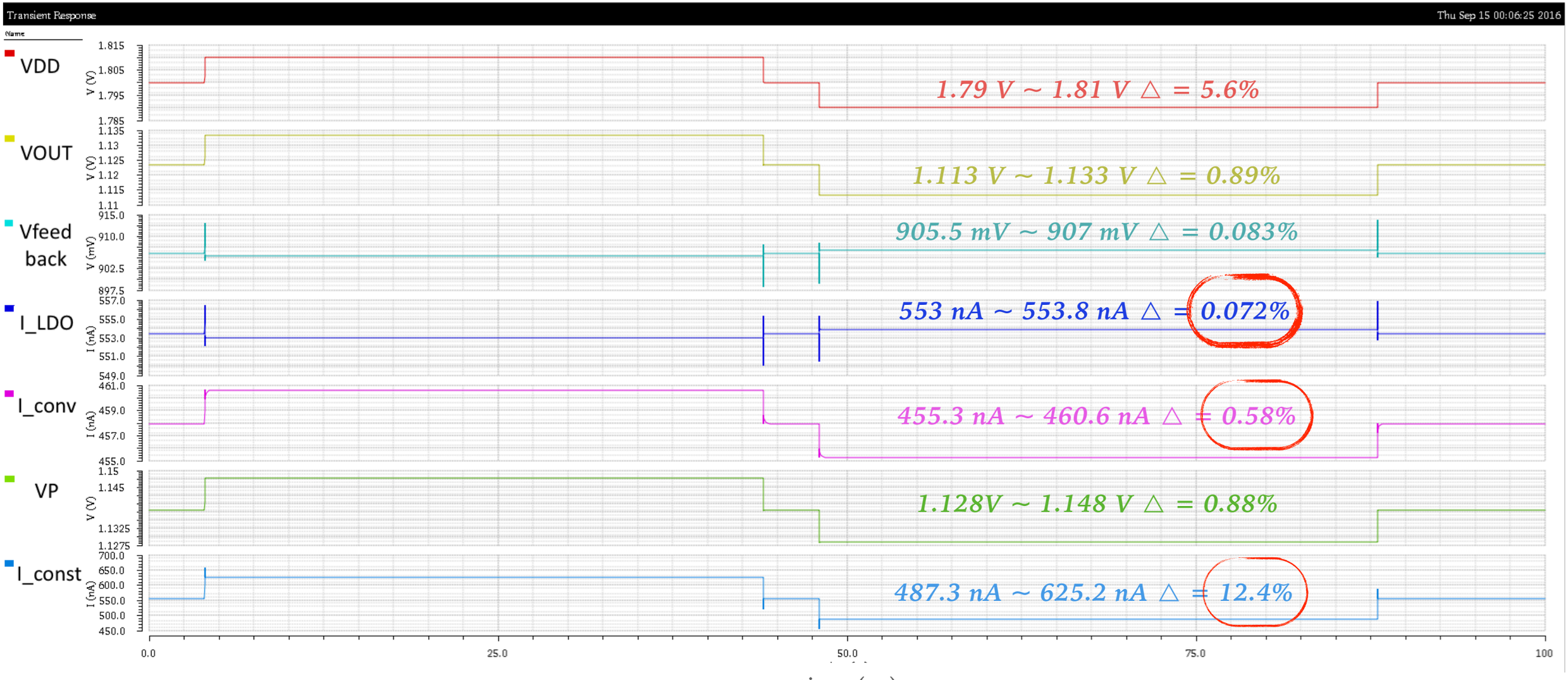


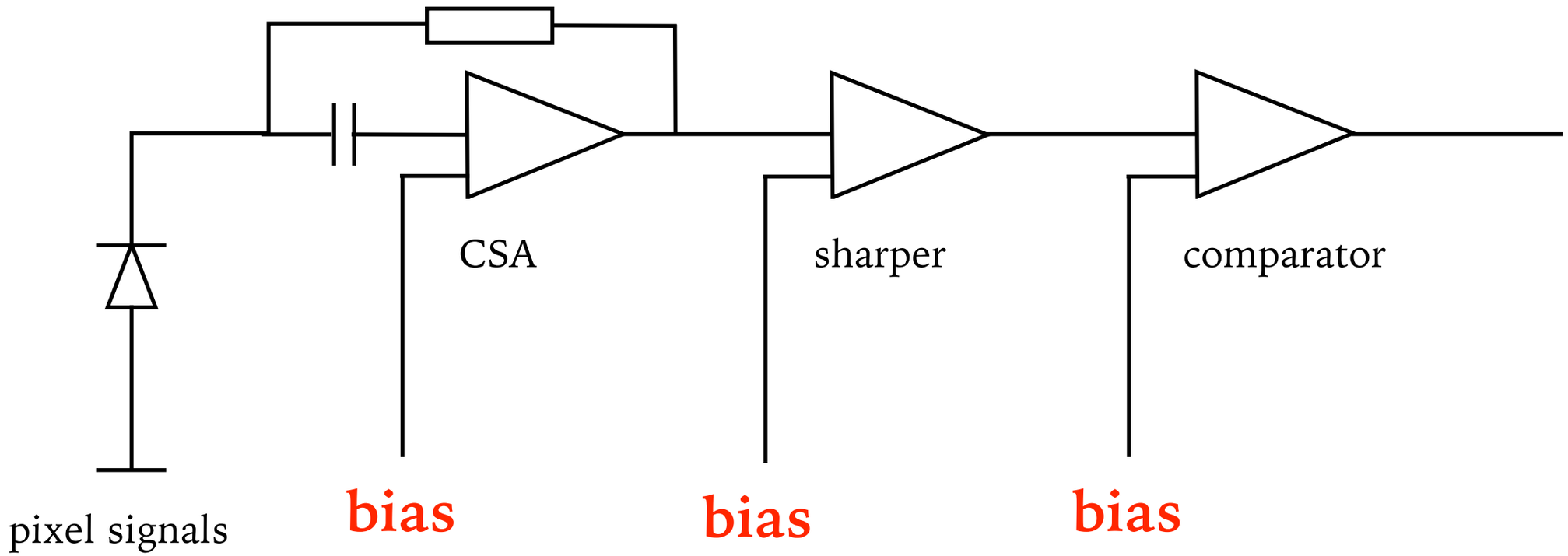
# The biasing block

## The biasing block transient simulation result



# My work – Design of the biasing block

- The bias block will be assembled into the particle sensor together with other parts designed by my colleagues
- The bias block takes the job of biasing other blocks with appropriate voltages to help them achieve the desired gain or shaping time



# Conclusion

- HV-CMOS sensor technology is a very feasible and advantageous option for particle physics experiments and other related applications in the future
- Liverpool has started an R&D program to develop HV-CMOS sensors for HEP experiments:
  - design of a pixel demonstrator in 0.35µm HV-AMS technology (H35DEMO)
  - New submission in LFoundry 150 nm will be in October 2016

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# Future plans

- Submission of the prototype in LFoundry will be in October 2016
- Chip (MPW) delivery will be in less than 3 months after submission
- PCB and FPGA (HW / SW) will be designed in the meantime to verify the fabricated chips

# Thank you for your attention!

# Questions?

The research leading to these results has received funding from the People Programme (Marie Curie Actions) of the European Union's Seventh Framework Programme FP7/2007-2013/ under REA grant agreement n [317446] INFIERI "INtelligent Fast Interconnected and Efficient Devices for Frontier Exploitation in Research and Industry"

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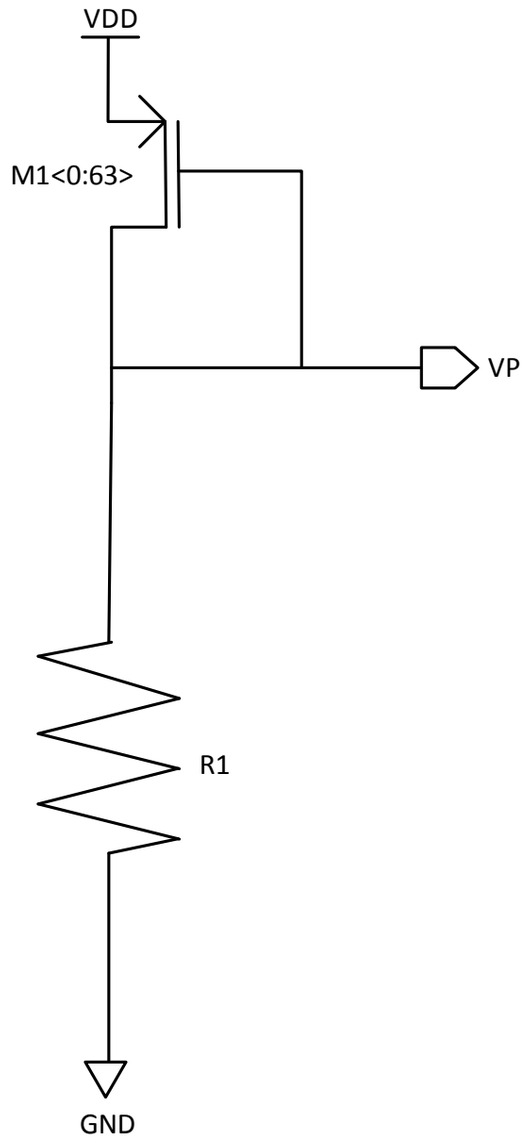
# The biasing block – LDO (backup)




conventional VP generating structure

# Application fields of HV-CMOS sensors (backup)

## ➤ Astro-physics

HV-CMOS sensors provide the measurement of mixed particles in the high-radiation space environment with advantages of being low-sized, low-weighted and low-power-consuming

## ➤ Medical imaging

HV-CMOS sensors can be used for positron emission tomography (PET) scans

## ➤ Particle physics

HV-CMOS sensors can be used to track high-energy particles with *high-position-resolution*, *high-time-resolution*, *high-radiation-tolerance* and *high Signal-to-Noise Ratio* (SNR)

# Previous work at Liverpool (backup)

TCAD simulation

- Back-side biasing versus top-side biasing:
  - back-side biasing forms a more uniform E-field
  - AMS does not support back-side biasing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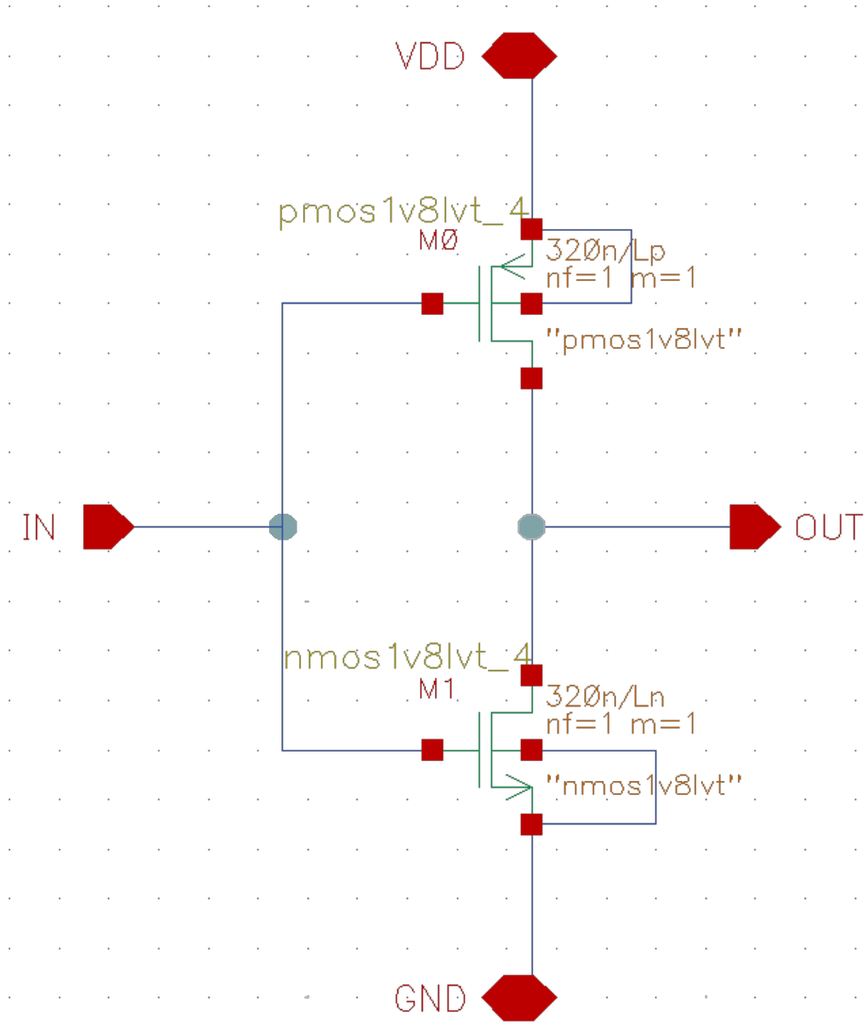
# New submission in LFoundry – design flow

Take the inverter as an example:

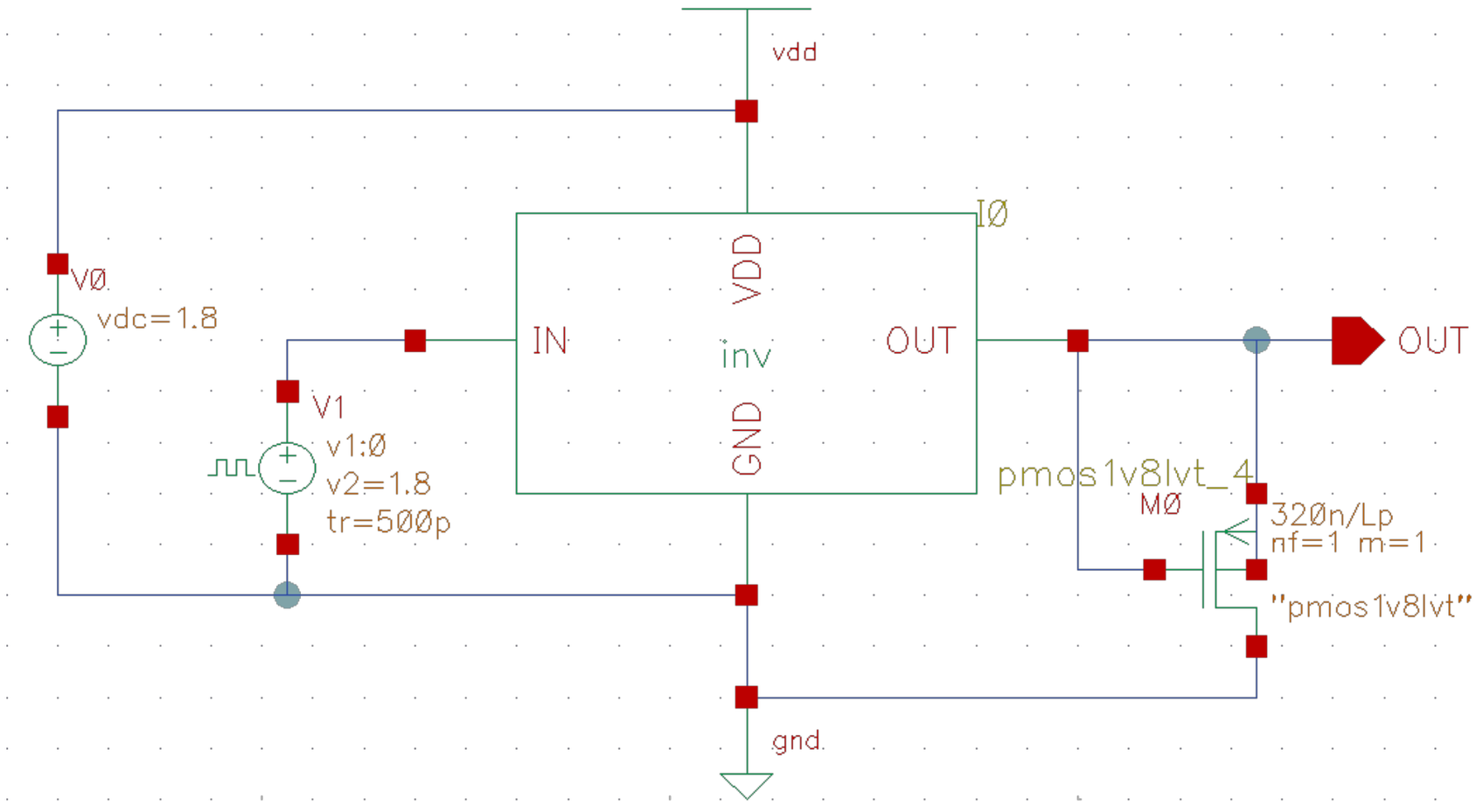
1. **schematic** (sizing and connection of devices)



# New submission in LFoundry – design flow

Take the inverter as an example:

2. **simulation** (create a testbench to test the performance of the circuit by simulation, DC, AC, transient, etc.)



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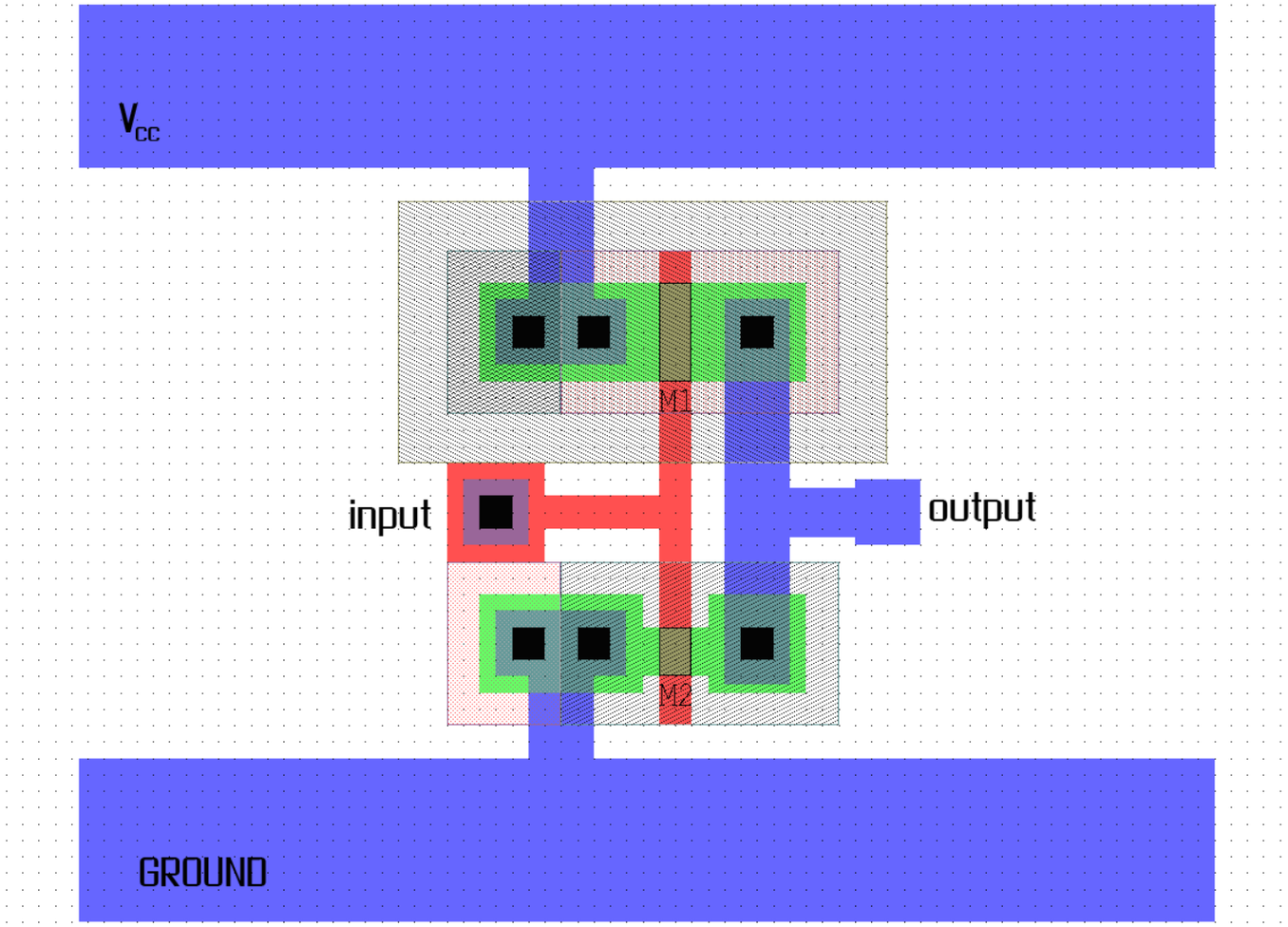
Take the inverter as an example:

3. **layout** (schematic driven)



# New submission in LFoundry – design flow

Take the inverter as an example:

4. **physical verification on the layout** (DRC, LVS, Parasitic extraction)

5. **post-layout simulation**

6. **Stream out** (translate graphical layout to standard exchangeable formate, like GDSII, OASIS etc, which is sent to the foundry for fabrication)