

New developments on Avalanche Pixels and R&D results

*Matteo VIGNETTI ^{*a}*
(WP2 ESR PhD Student)

INFIERI 8th International Workshop – FermiLAB

F. Calmon ^a(Supervisor), P. Pittet ^a, G. Pares ^b, R. Cellier ^a, L. Quiquerez ^a, A. Savoy-Navarro ^c

^a Institut des Nanotechnologies de Lyon, Lyon (France)

^b CEA-LETI, Grenoble (France)

^c Laboratoire d'AstroParticule et Cosmologie, Université Paris-Diderot, Paris (France)



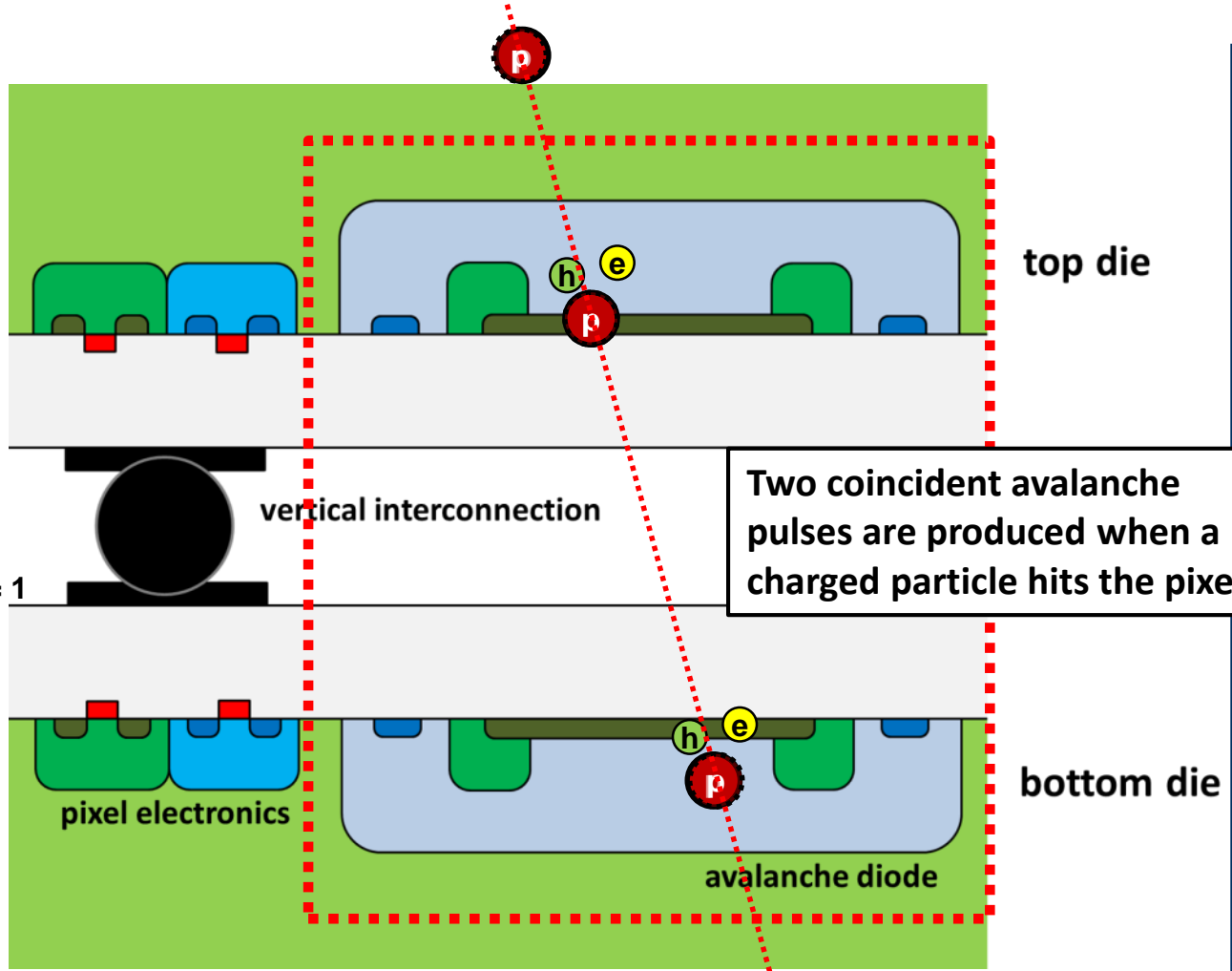
- Avalanche Pixel concept
- Development
- Characterization
- Ongoing work

➤ **Avalanche Pixel concept**

- Development
- Characterization
- Ongoing work

A novel 3D pixelated detector suitable for particle tracking and imaging

Two vertically aligned avalanche diodes operated in Geiger-mode



Two coincident avalanche pulses are produced when a charged particle hits the pixel

The coincidence is verified thanks to dedicated electronics

- ✓ Avalanche Pixel concept

- Development

- Characterization

- Ongoing work

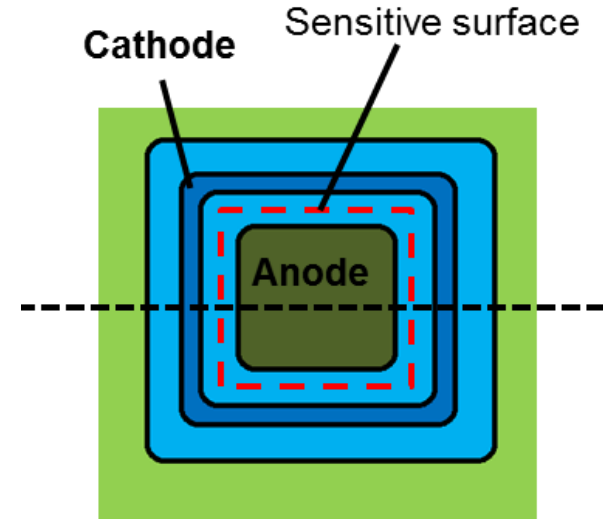
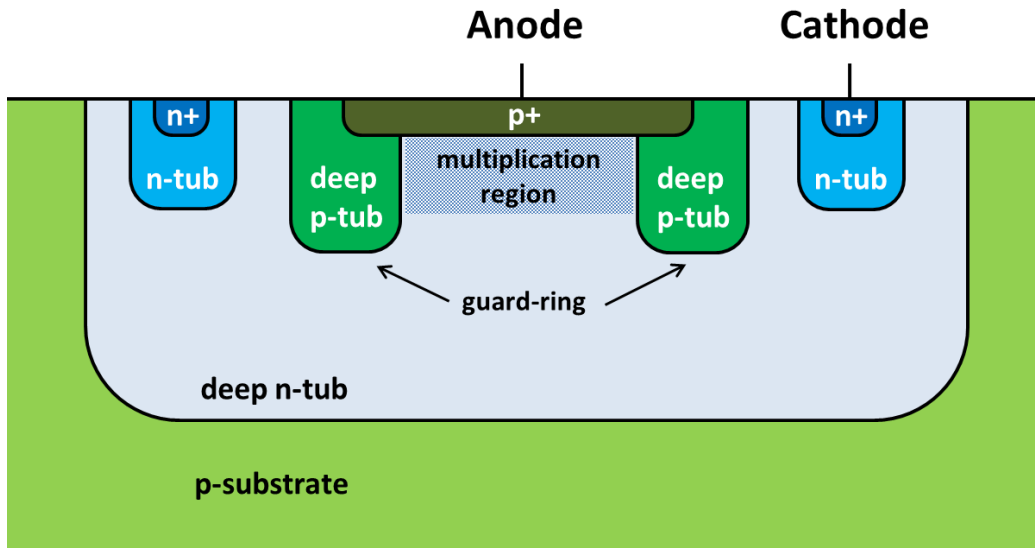
✓ Avalanche Pixel concept

➤ **Development**

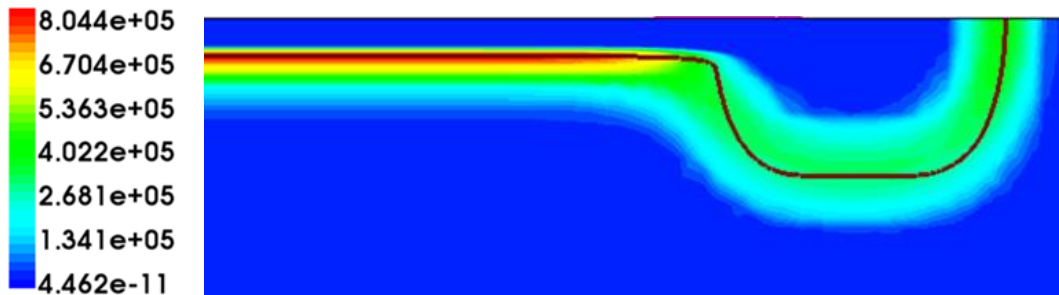
- Characterization
- Ongoing work

Design of the avalanche diode

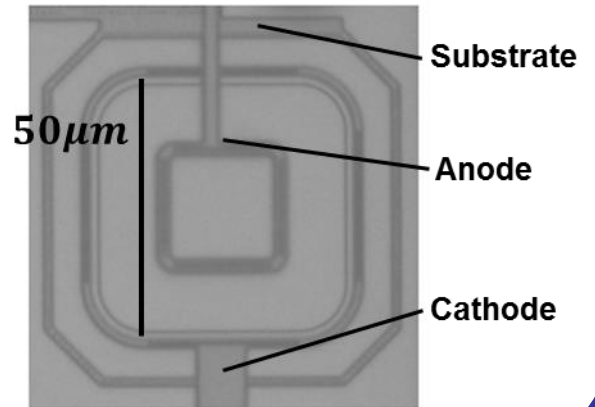
AMS HV-CMOS 0,35 μ m technology



Abs(ElectricField-V) ($V \cdot cm^{-1}$)

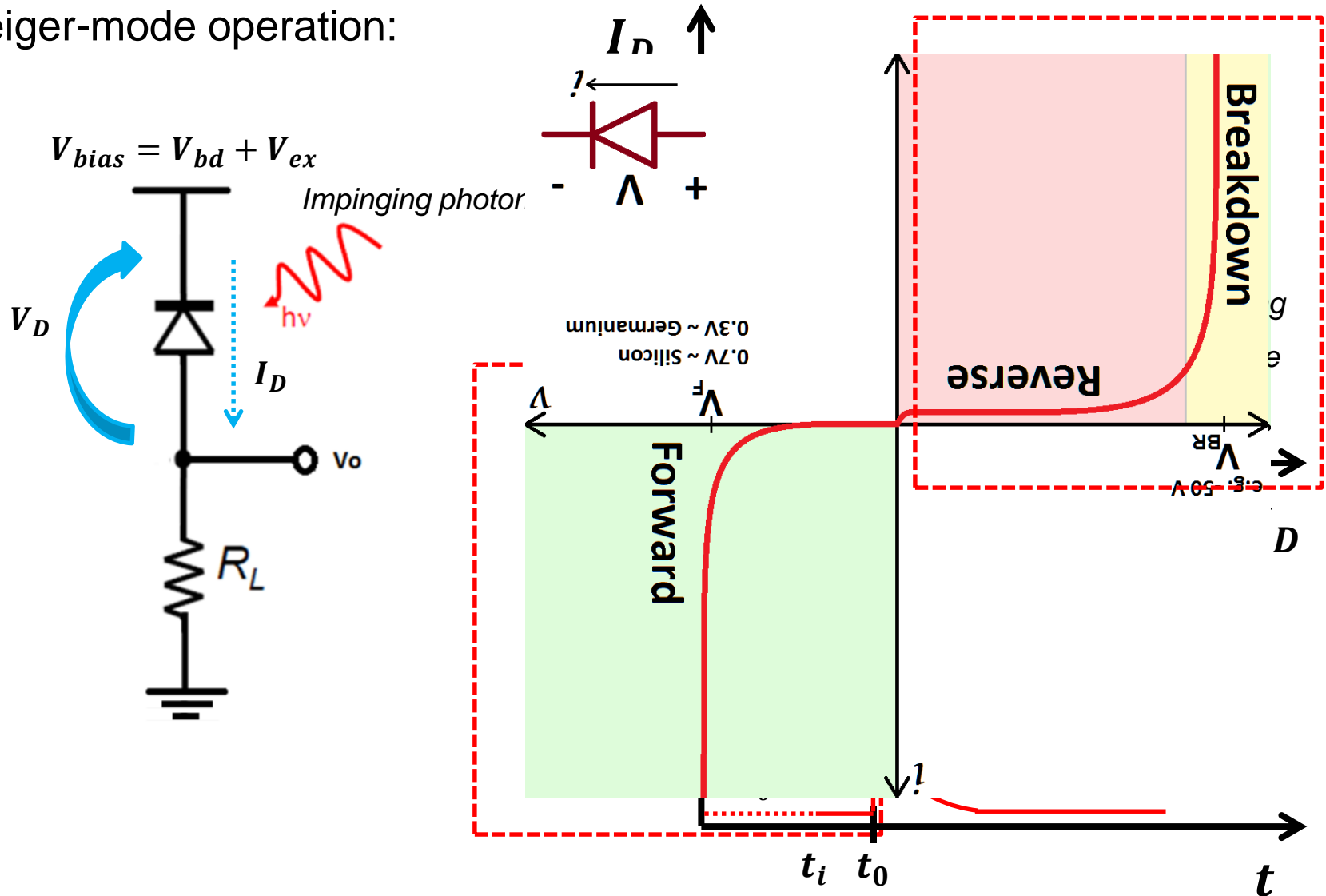


Premature edge breakdown (PEB) prevention



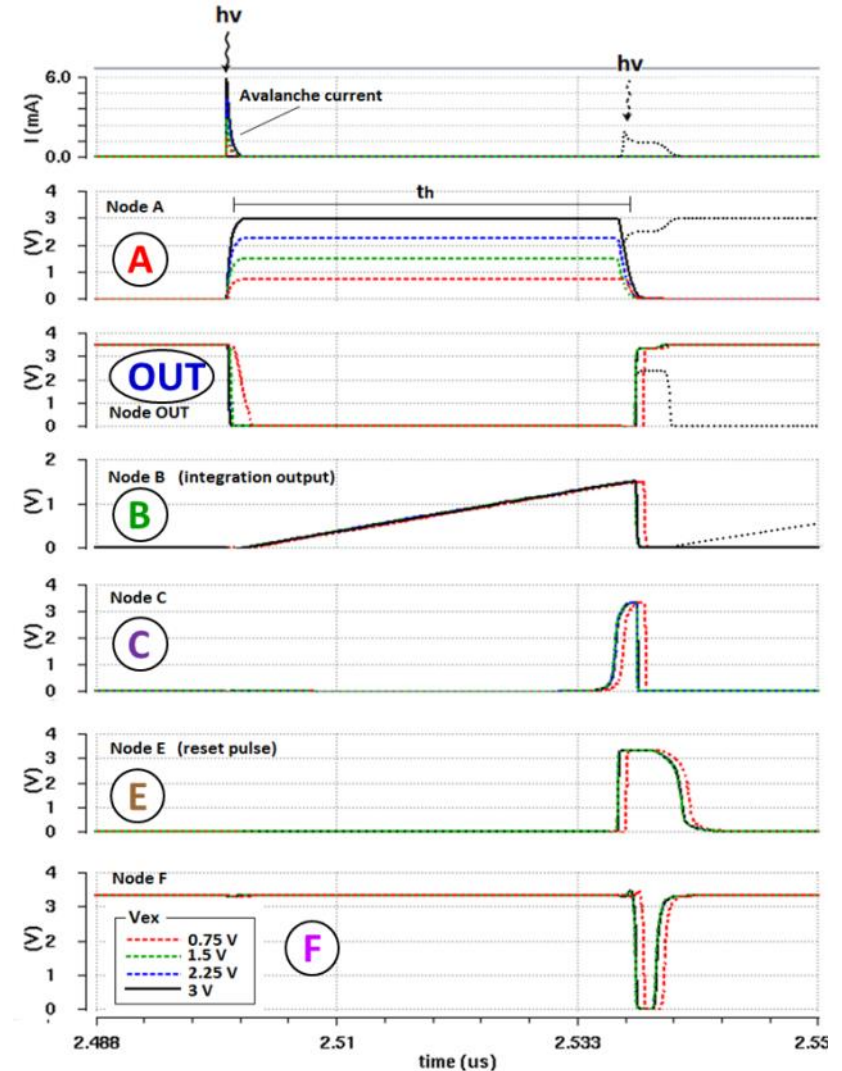
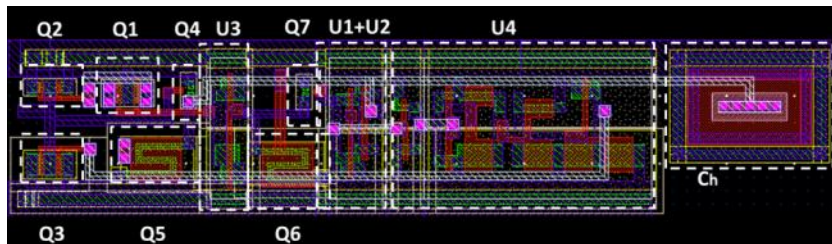
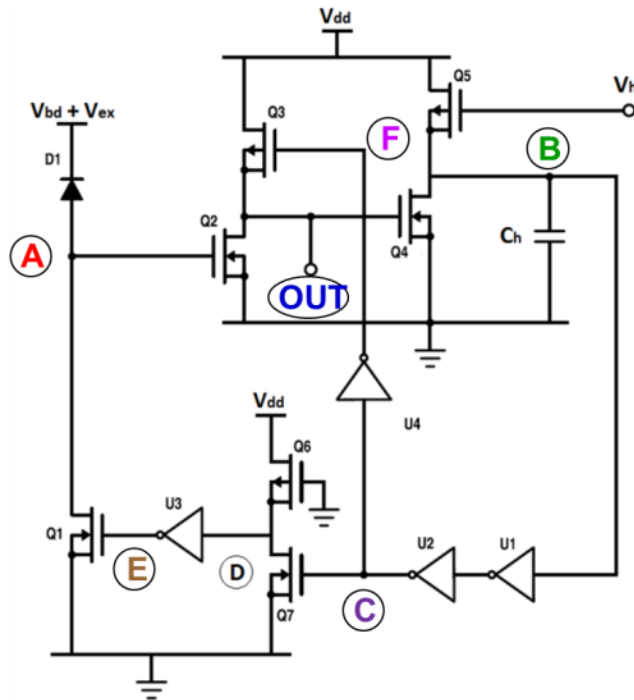
Design of the pixel electronics for Geiger-mode

Geiger-mode operation:



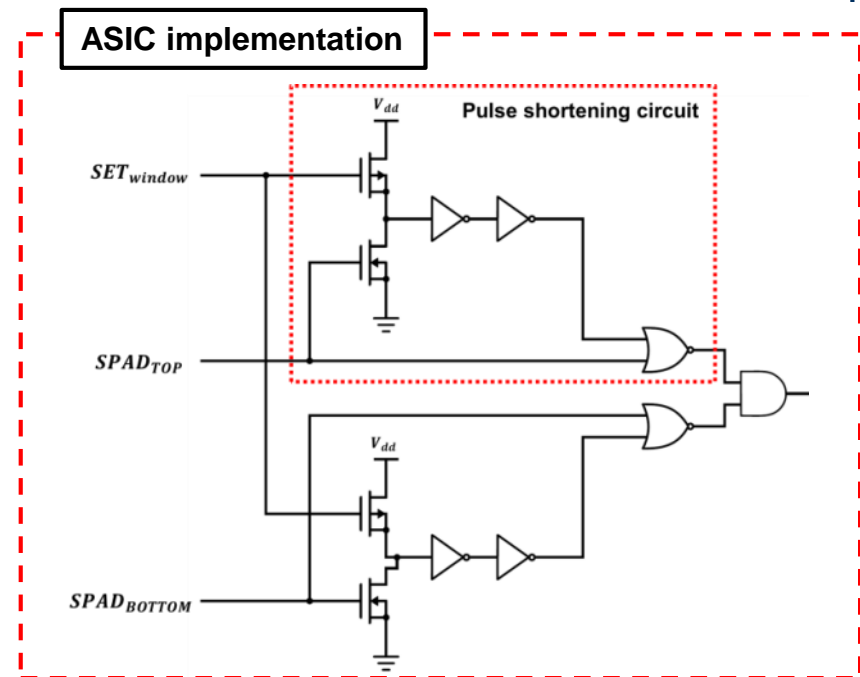
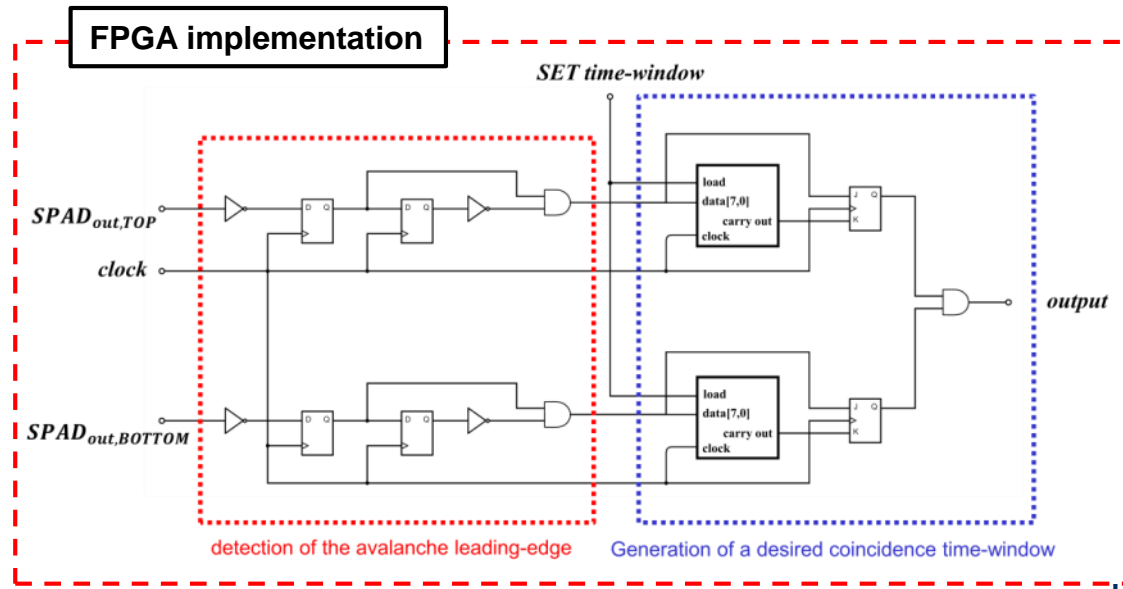
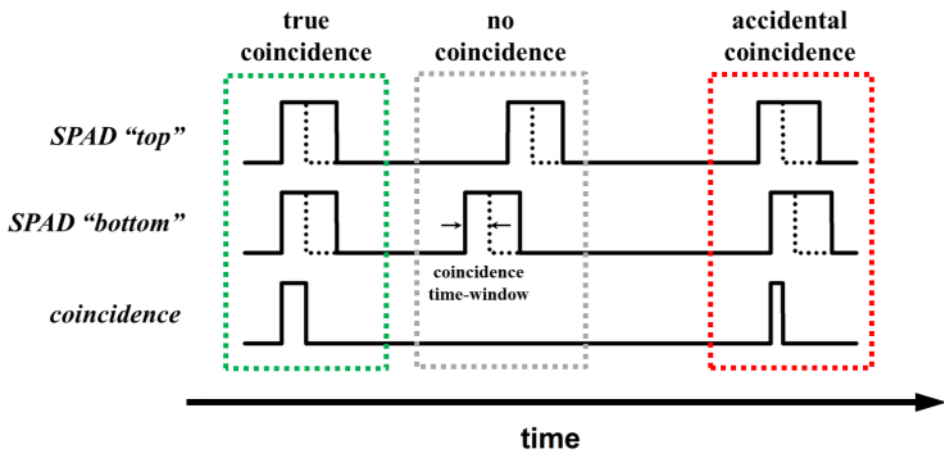
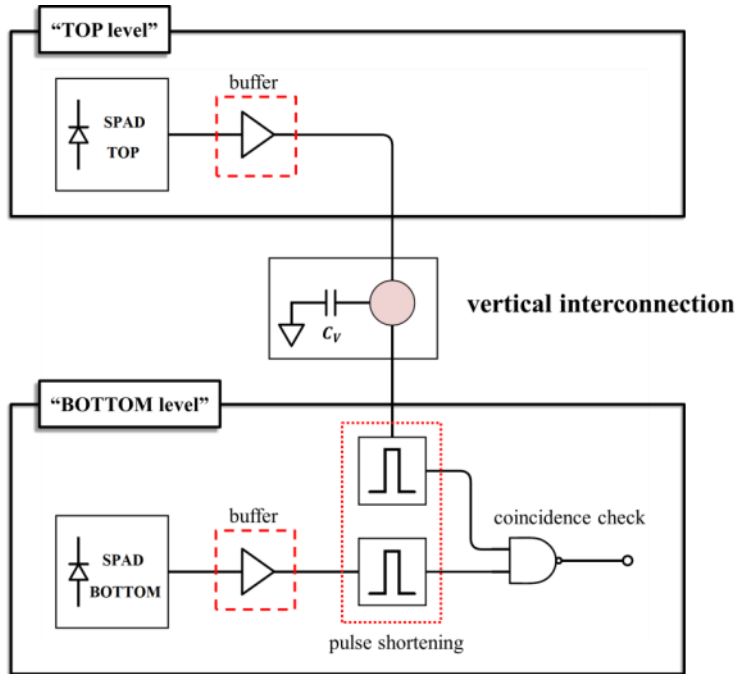
Design of the pixel electronics – 2D level

A time integration-based passive quench - active recharge circuit

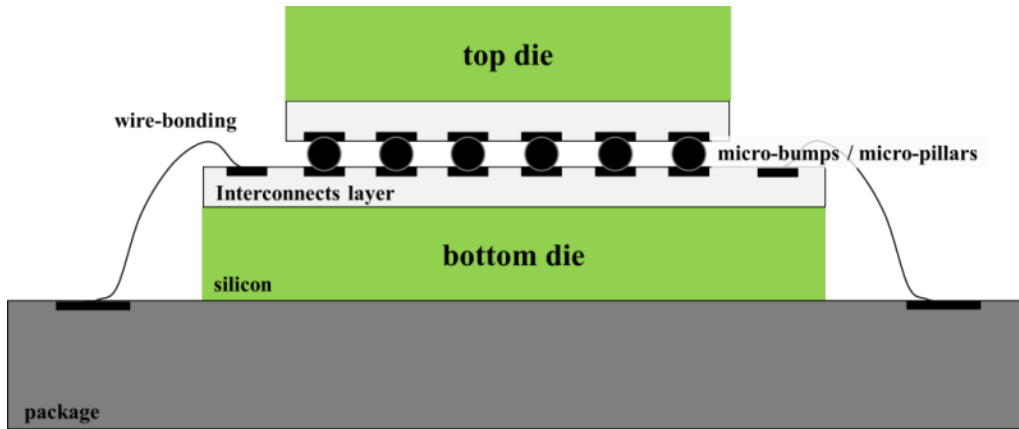


Vignetti M. et al "A time-integration based quenching circuit for Geiger-mode avalanche diodes" 13th IEEE International New Circuits and Systems Conference (NEWCAS 2015) June 7-10, 2015 Grenoble, France (2015)

Design of the pixel electronics – 3D level



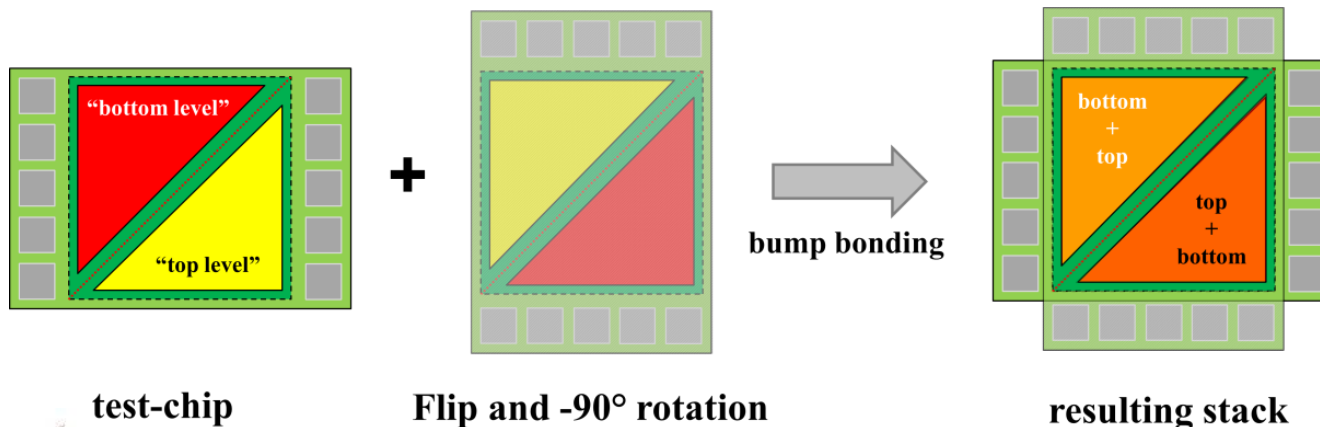
3D vertical stacking: flip-chip assembly



Gold stud bump based assembly

- 😊 Die-to-die assembly: not costly
- 😊 Gold bumps deposition “by hand”
- 😞 Large bump diameter (70 μm)
- 😞 Parasitics and low-degree of integration

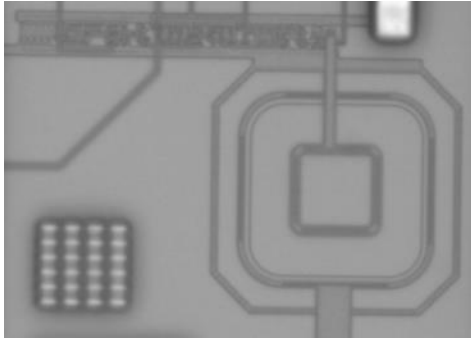
Assembling strategy: **TOP level and BOTTOM level on the same test-chip**



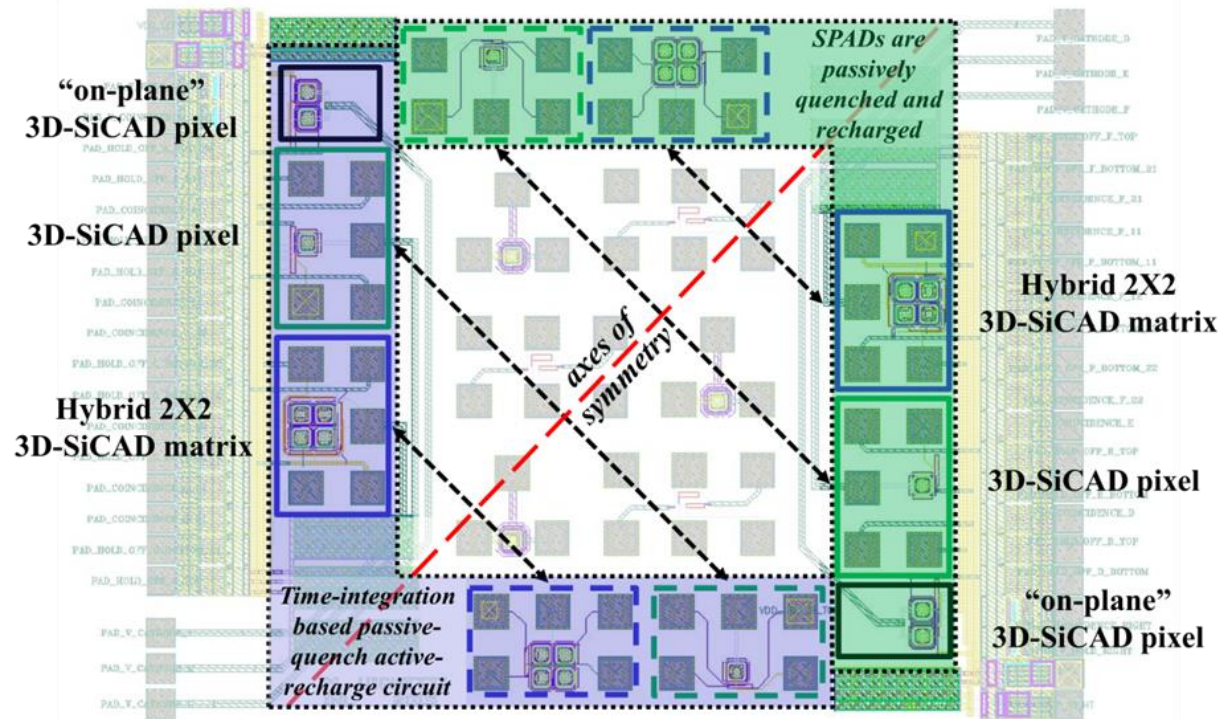
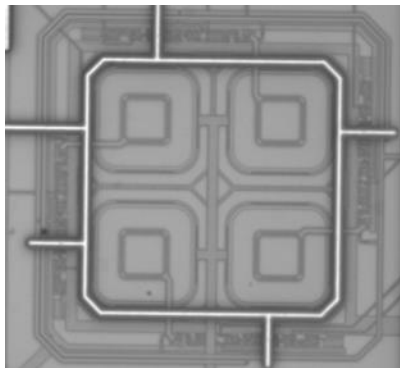
Only external PADS on BOTTOM die will be wire-bonded

Tape-out: CMP run – AMS HV-CMOS 0,35um

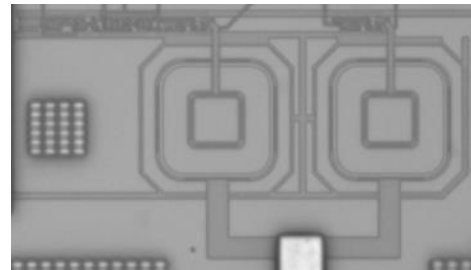
3D pixels cells



2x2 hybrid matrix cells



Test structures



- ✓ Avalanche Pixel concept

- ✓ Development
 - Characterization

 - Ongoing work

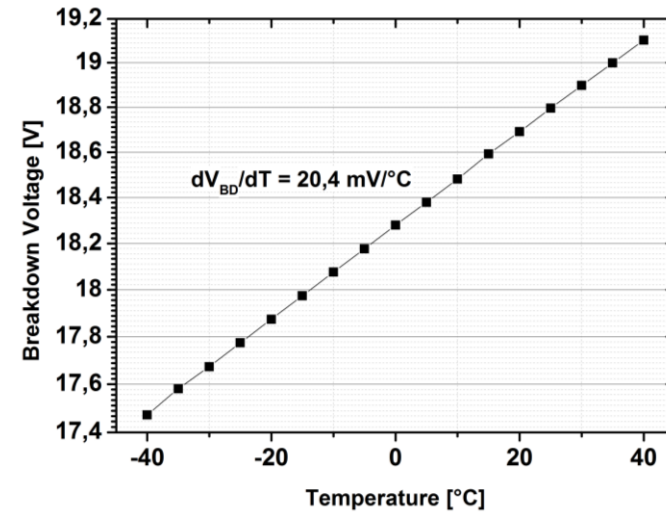
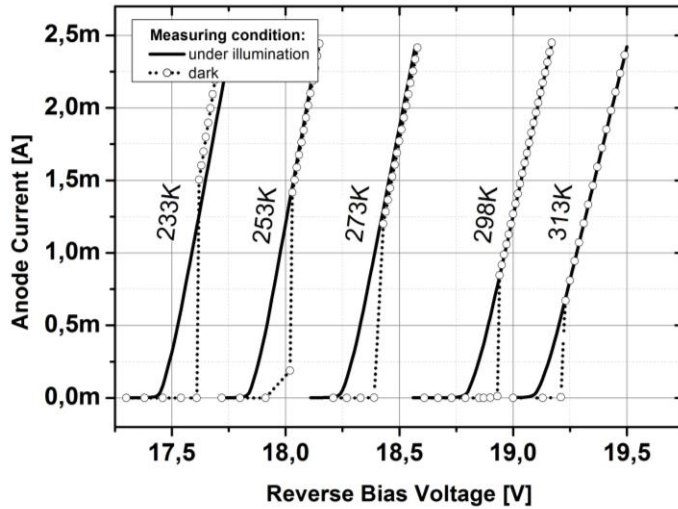
✓ Avalanche Pixel concept

✓ Development

➤ **Characterization**

• Ongoing work

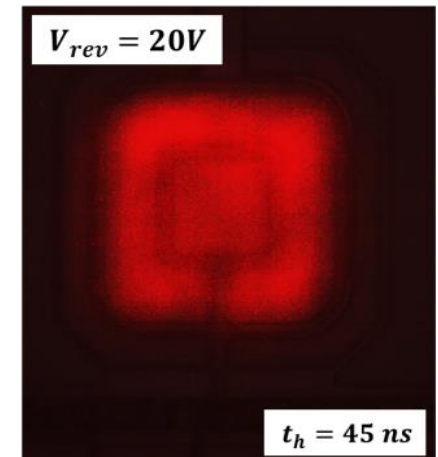
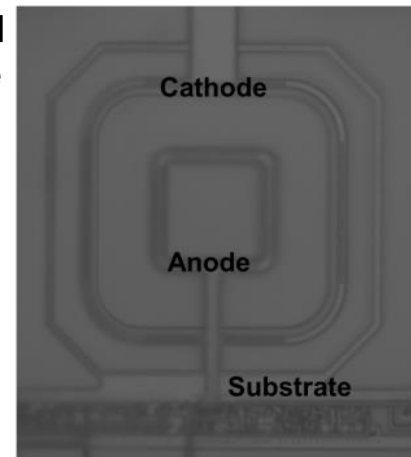
Breakdown voltage



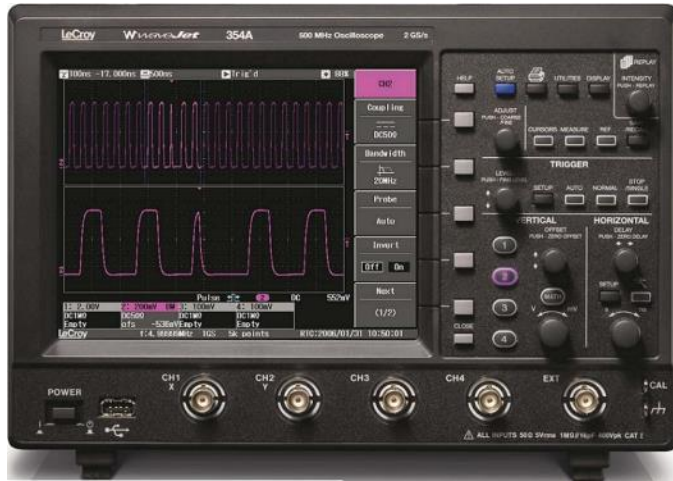
Luminescence imaging

Breakdown bias in Si diodes is accompanied with light emission in the visible spectrum range

- *Uniform light emission picture is obtained: uniform electric field distribution all over the active area*
- *Dark “rings” over the diode active area are due to shadowing effect by the anode metal ring.*
- *No PEB observed*



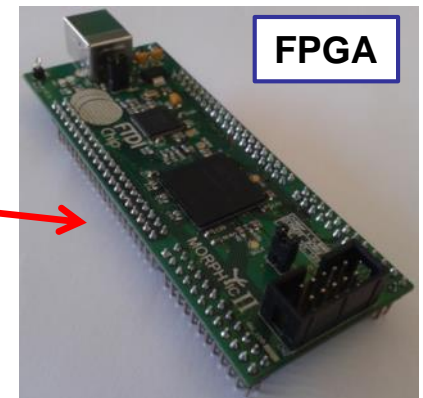
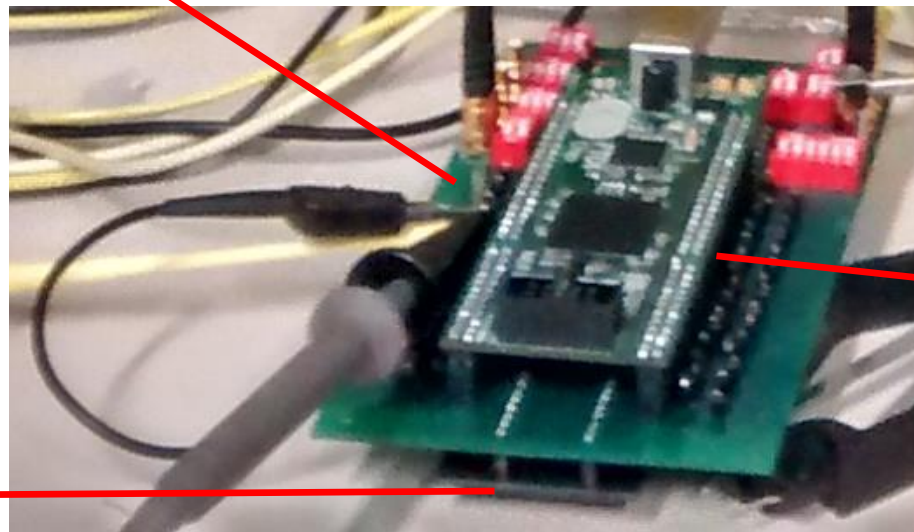
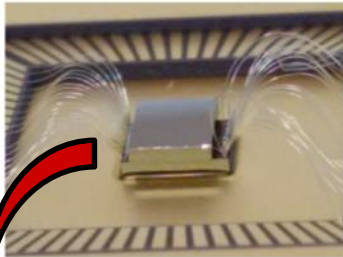
Characterization: geiger-mode operation



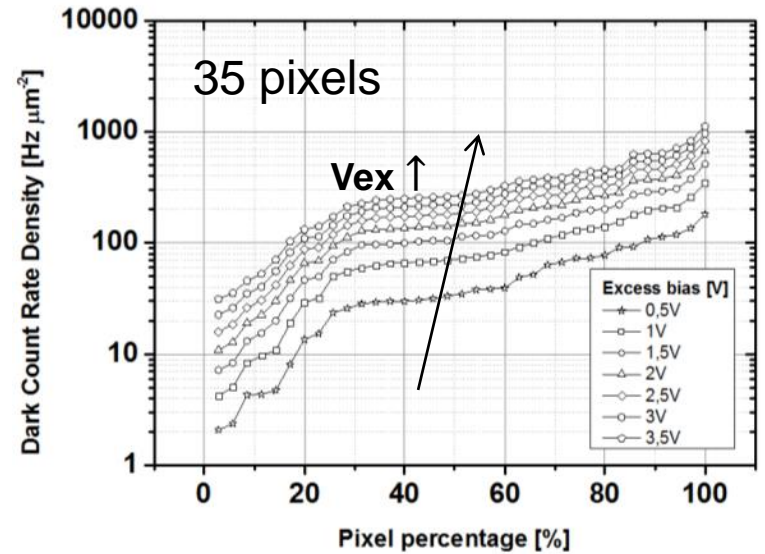
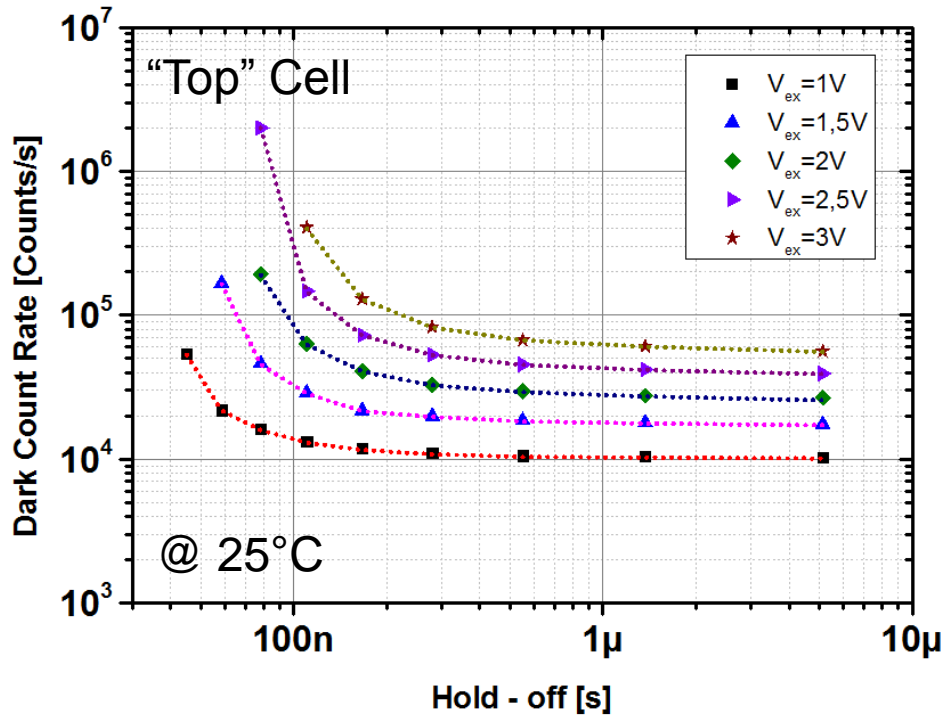
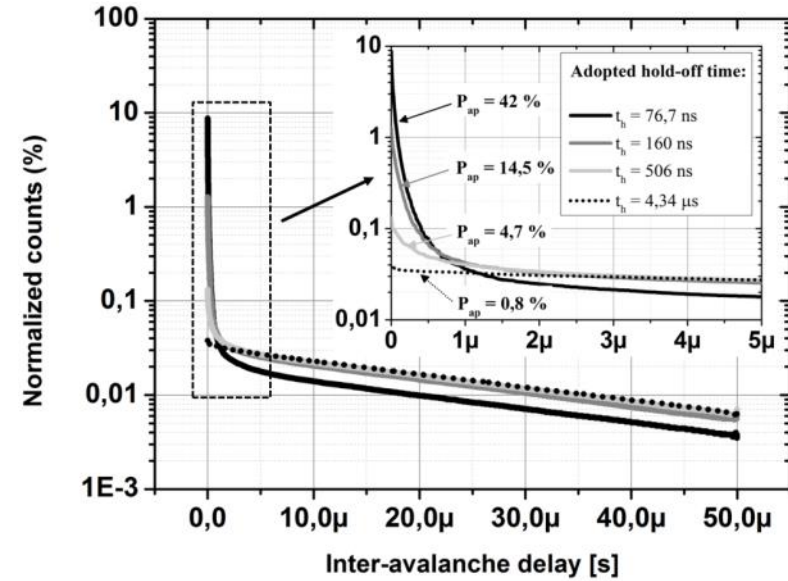
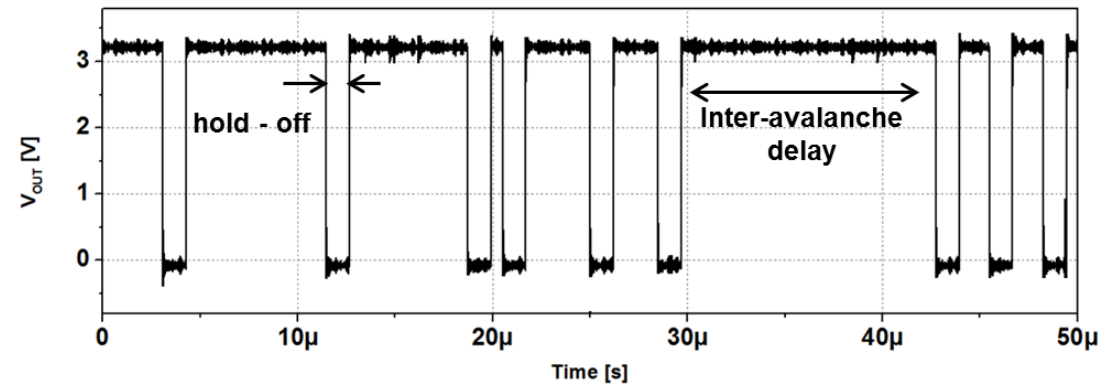
signal analysis



data acquisition
(via USB)

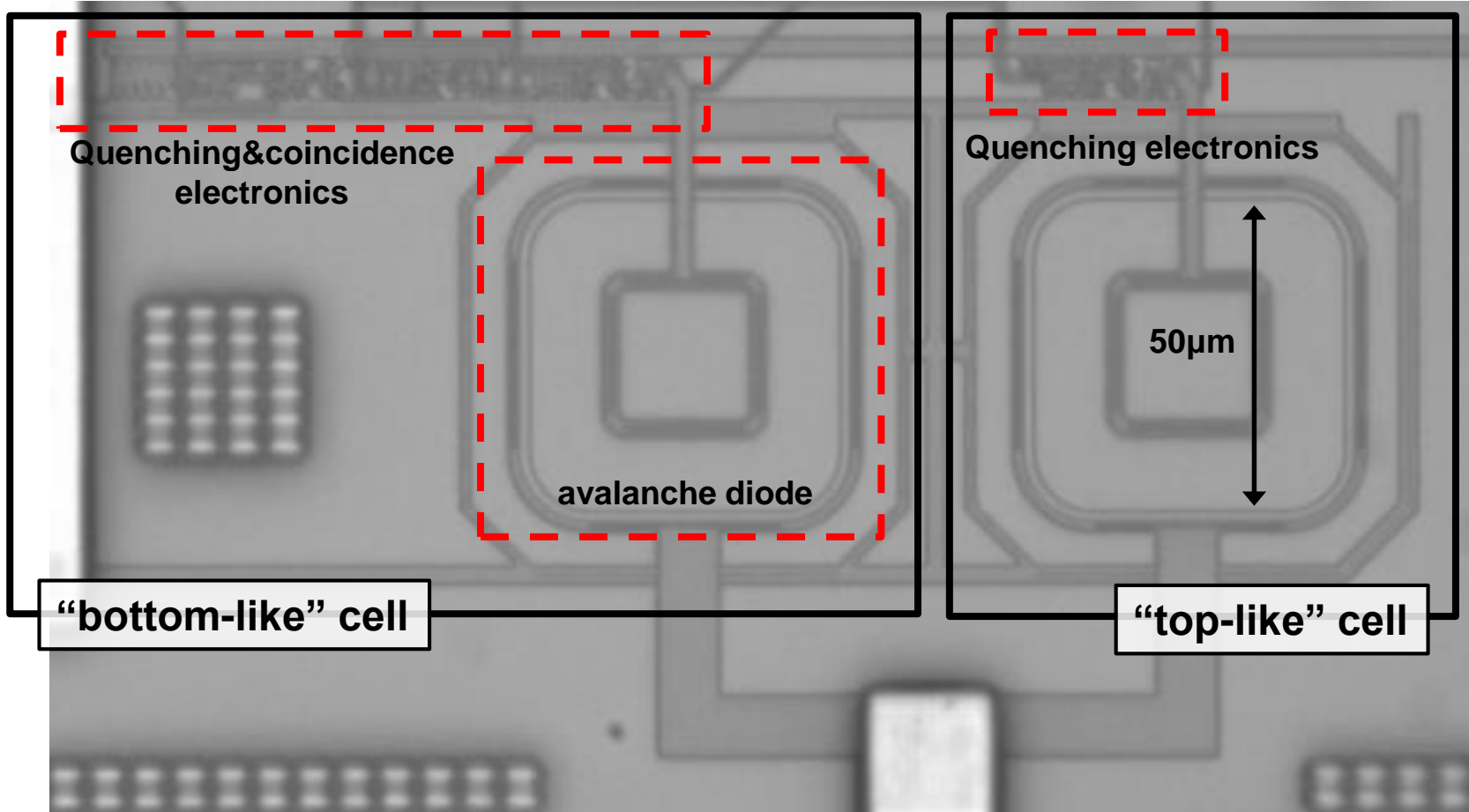


Characterization: DCR evaluation

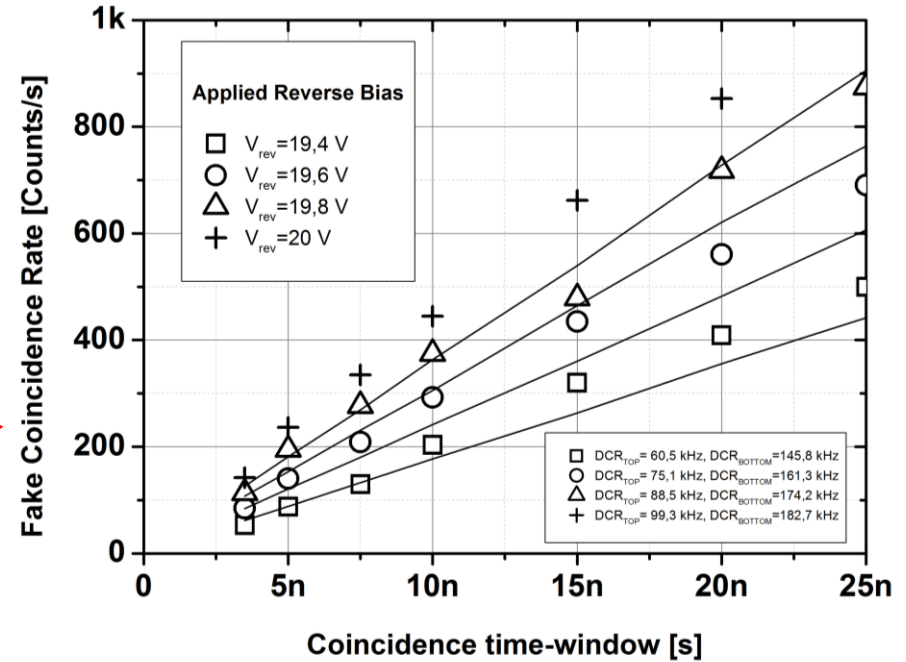
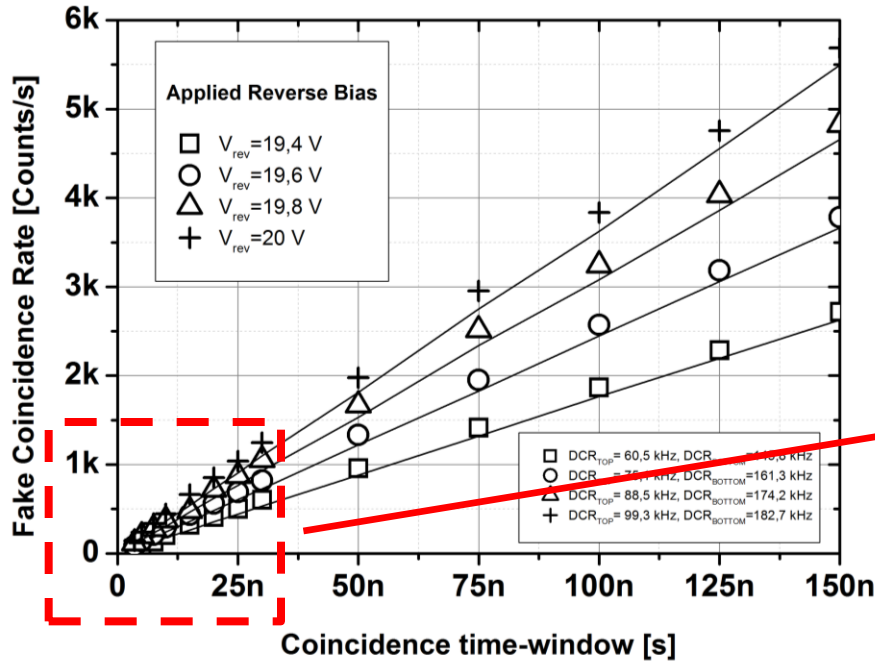


Characterization: on-plane coincidence

Check the coincidence between two adjacent SPAD pixel cells



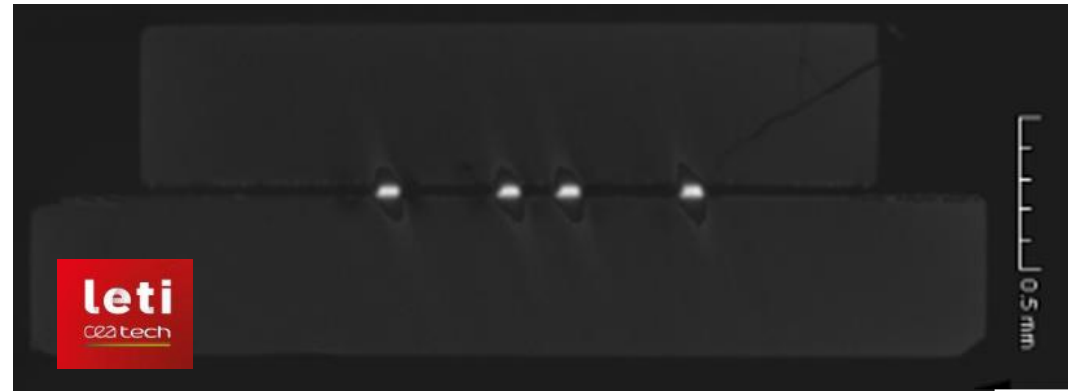
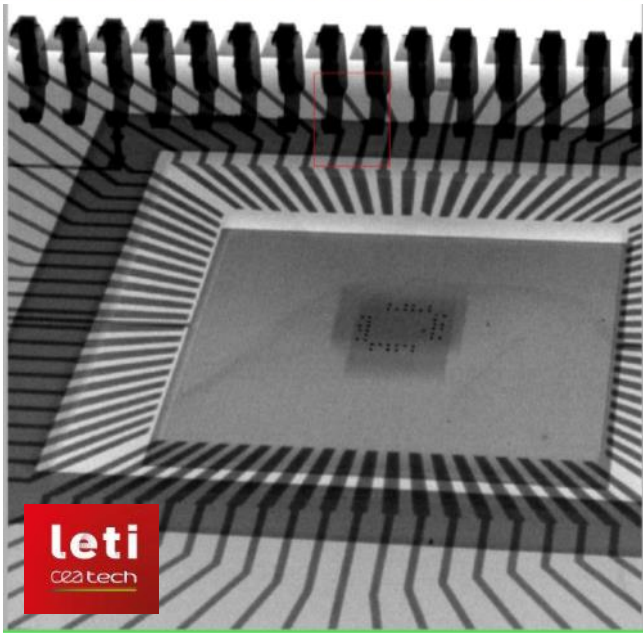
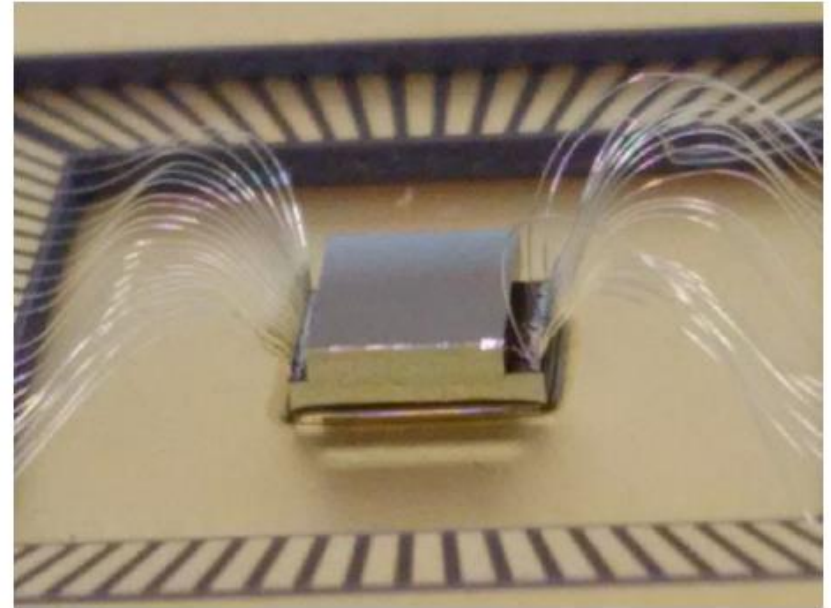
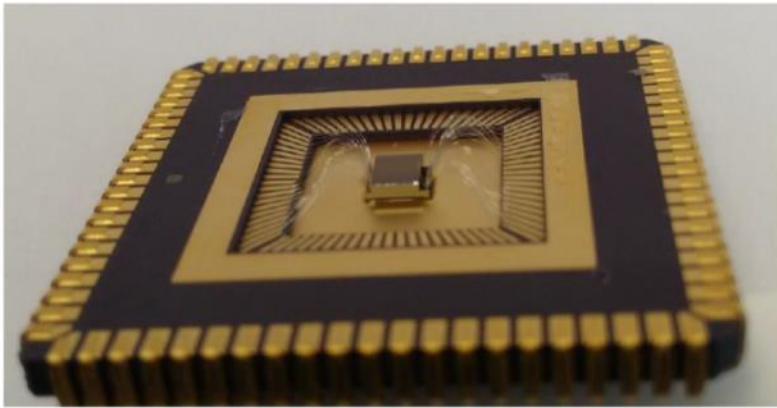
Noise evaluation: Fake Coincidence Rate (FCR) via FPGA



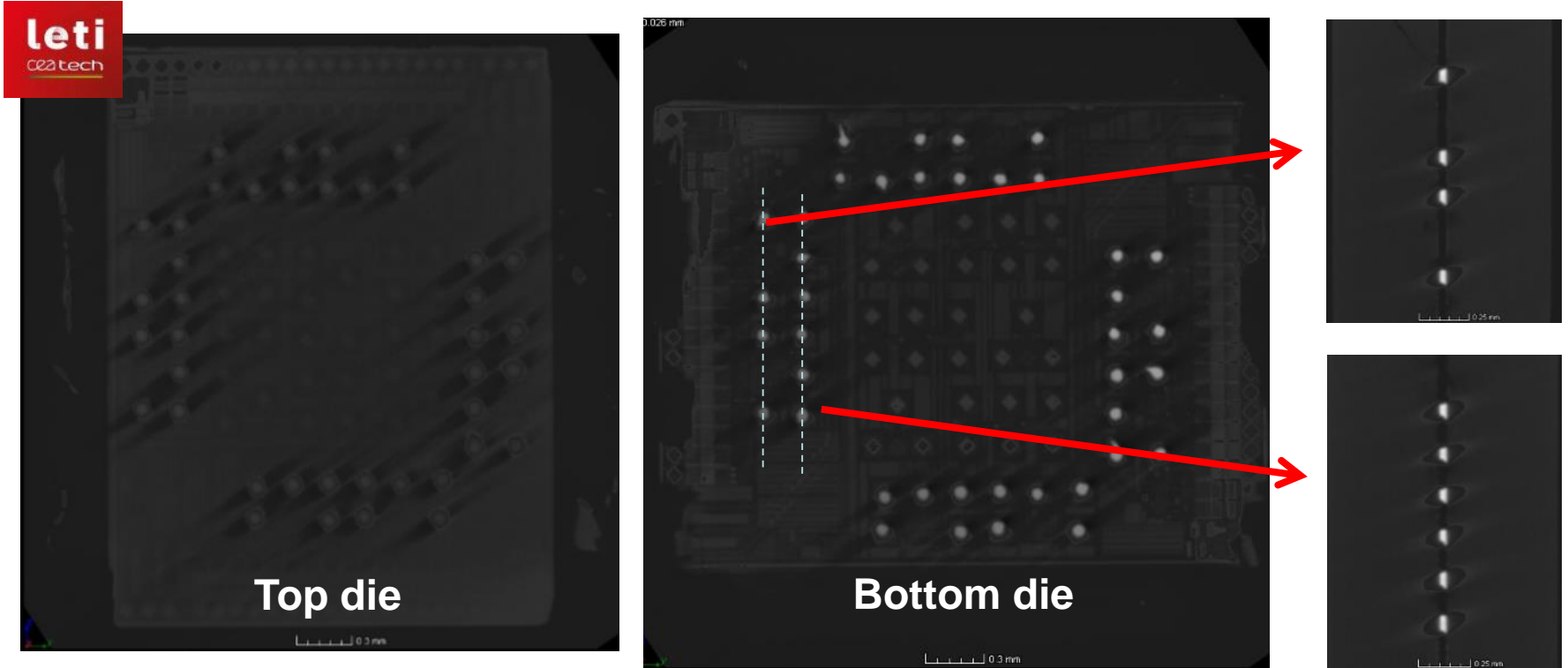
- $DCR_{TOP} = 60,5 \text{ kHz}, DCR_{BOTTOM} = 145,8 \text{ kHz}$
- $DCR_{TOP} = 75,1 \text{ kHz}, DCR_{BOTTOM} = 161,3 \text{ kHz}$
- △ $DCR_{TOP} = 88,5 \text{ kHz}, DCR_{BOTTOM} = 174,2 \text{ kHz}$
- + $DCR_{TOP} = 99,3 \text{ kHz}, DCR_{BOTTOM} = 182,7 \text{ kHz}$

- ✓ Experimental data is in agreement with the predicted FCR
- ✓ $NRF \sim 10^3$ for small coincidence time-window

3D prototype at CEA-LETI and CIME nanotech



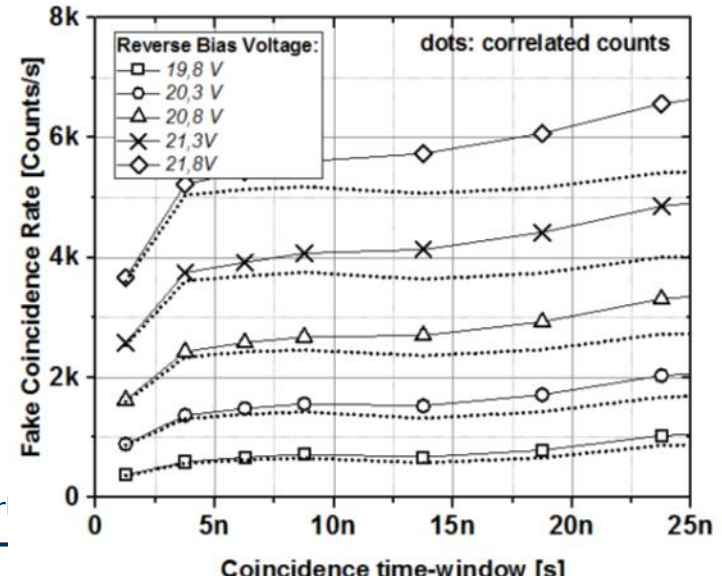
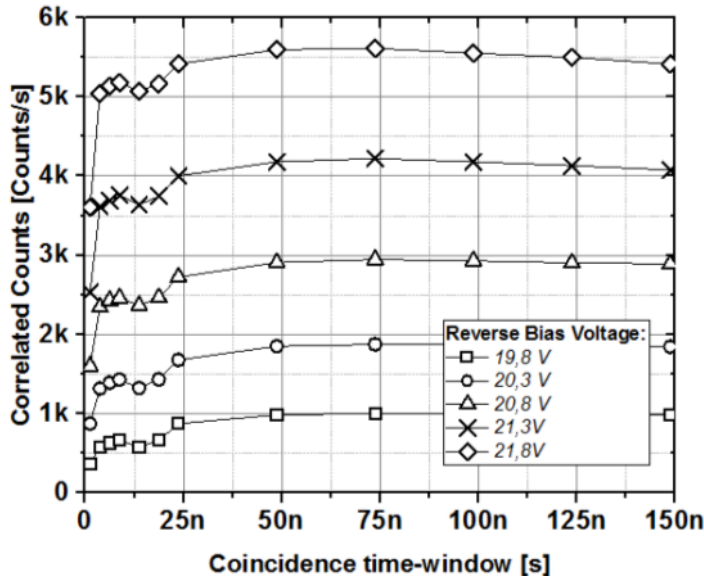
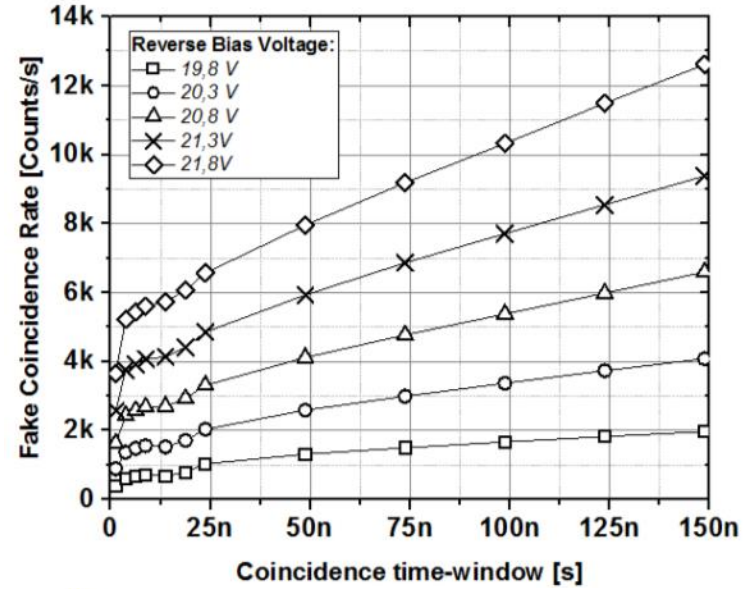
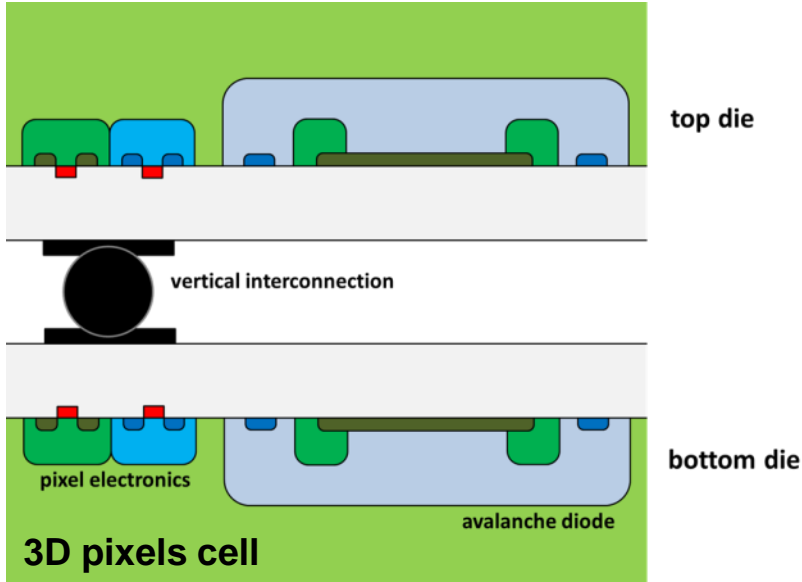
X-ray tomography of the assembled prototype



- *The two dies looks perfectly aligned*
- *The electrical connection cannot be validated because of a shadowing effect in proximity to the bonding surface due to gold bumps.*

Characterization: 3D prototype

Noise evaluation: Fake Coincidence Rate (FCR) via FPGA



- ✓ Avalanche Pixel concept

- ✓ Development

- ✓ Characterization

- Ongoing work

- ✓ Avalanche Pixel concept

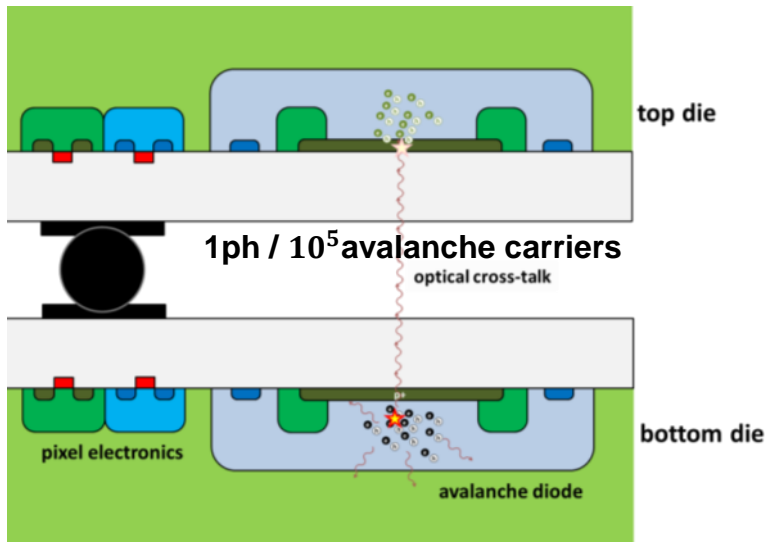
- ✓ Development

- ✓ Characterization

- **Ongoing work**

Characterization: 3D prototype

Possible source of correlated counts: optical cross-talk between the 2 sensing levels

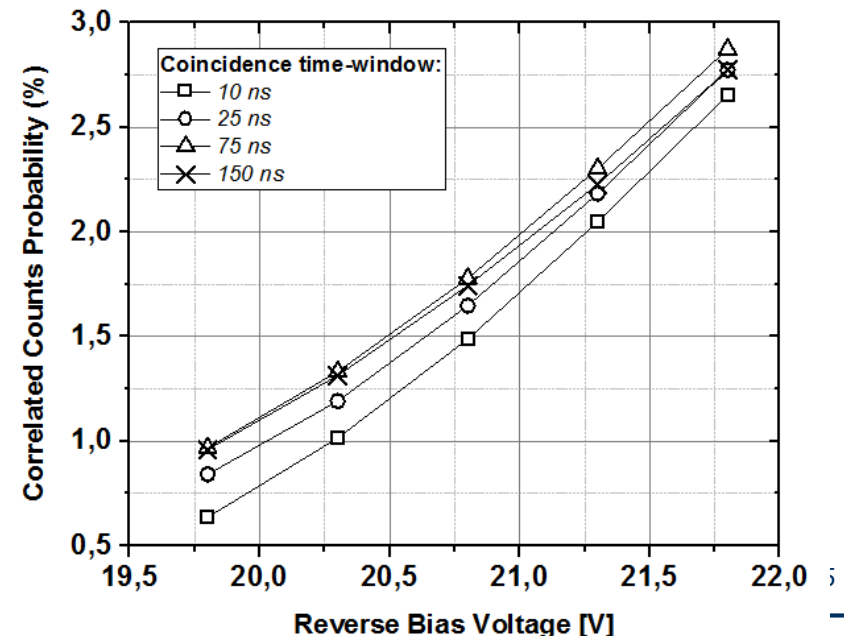
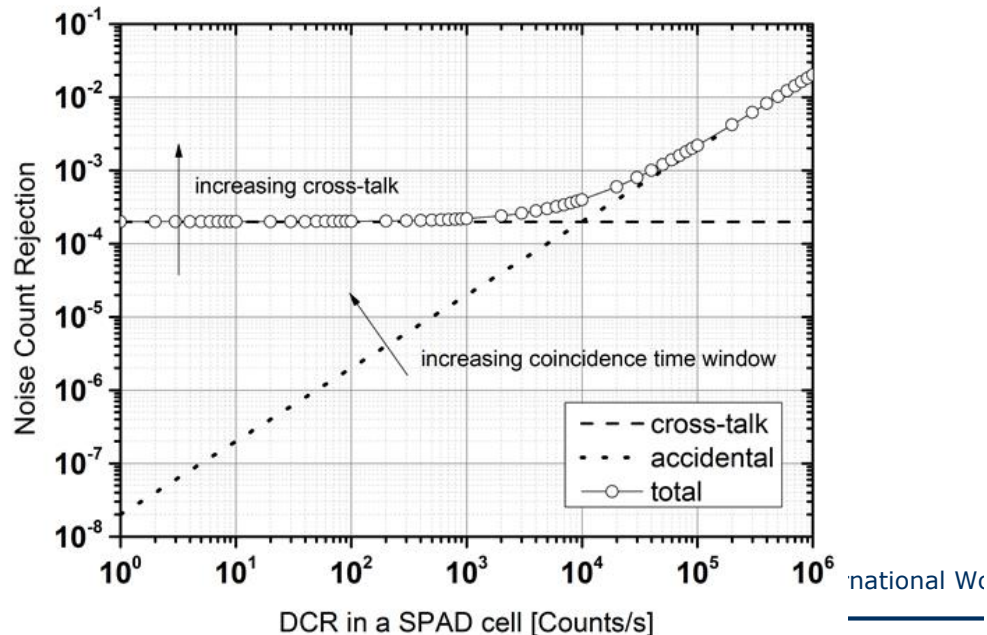


- **Optical cross-talk between the two sensing levels produces correlated coincidence events.**
- **Even very weak optical cross-talk ($p_X \approx 0.01\%$) can impact a lot when in coincidence**

FCR correction:

$$\lambda_{coinc} = 2\Delta t \lambda_T \lambda_B + \frac{p_X}{1 + p_X} (\lambda_T + \lambda_B)$$

$$\lambda_{coinc} \approx \lambda_{dark,coinc} + \lambda_{X,coinc}$$



- **Further characterization and data analysis on the available prototypes**
- **Understanding of the physical nature of the correlated counts**
- **3D prototype test under a Sr 90 radioactive source (β^- decay) @ IPNL (Lyon – France)**
- **65 MeV proton beam test @ “Lacassagne” hospital (Nice - France)**

Thanks