Trends in Silicon-Based Detectors

Ronald Lipton, Fermilab

Infieri 2016 at Fermilab

Outline

- Some Physics context
- Current Status and technologies
- Sensor Technologies
- Interconnect
- Summary

A PRIMER ON DETECTORS IN HIGH LUMINOSITY ENVIRONMENT

Or why you can't do physics at 10^{33}

R. Huson, L. M. Lederman and R. Schwitters
Fermi National Accelerator Laboratory*
Batavia, Illinois 60510

From Snowmass 1982

tracking efficiency; there is in fact a fair likelihood that these high multiplicities will render any of the tracking devices, as we now understand them, inoperable. PWC's have operated at ambient

confused by the integration, but it is also clear that a large enough number of random accumulations of 10 or 20 minimum bias events can generate fake physics.

The prognosis for instrumental breakthrough is mixed. Serious studies of high luminosity colliders started in 1972. We can look at this as a 15 year program of which 10 years have already been spent. Nevertheless, (and this is the principal motivation of this paper), work must continue on decreasing the integrating time of tracking detectors, preferably without breaking the bank by infinite readout channels. Calorimetry is fundamentally ugly; a cure here would be to improve resolution, decrease integrating time and find a cheap substitute for steel.

The Next Generations

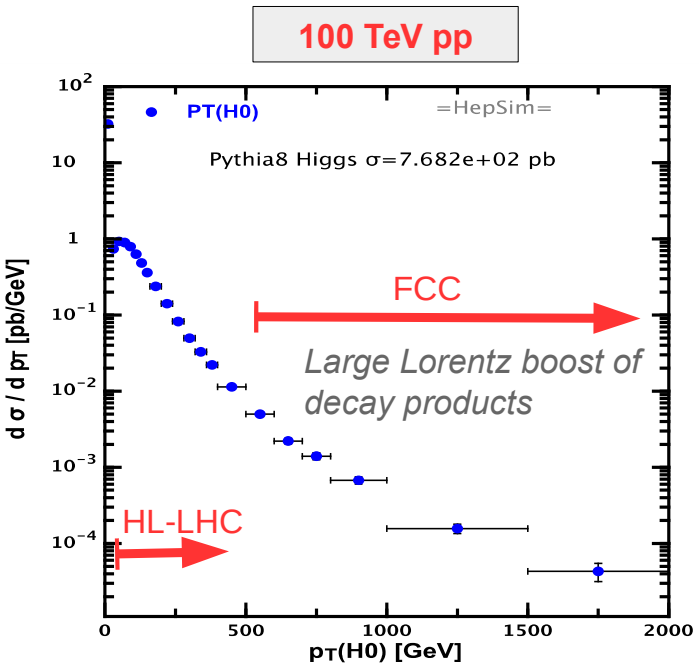
$$\frac{dp_T}{p_T} \mu \frac{p_T s_{rf}}{BL^2}$$

Future generations of experiments will deploy large areas of complex silicon sensors and electronics. At HL-LHC ~ 200 m^2 (20,000 6" wafers) each for the ATLAS and CMS trackers + 600 m^2 (~50,000 6", 30,000 8" wafers) for the CMS HGCAL

10x p_T ->
Larger detectors (L)
More precise trackers (σ)
Higher fields

Beyond that a future 100 TeV machine (FCC) with ~5 ns bunch spacing and L~5x10^{34}.

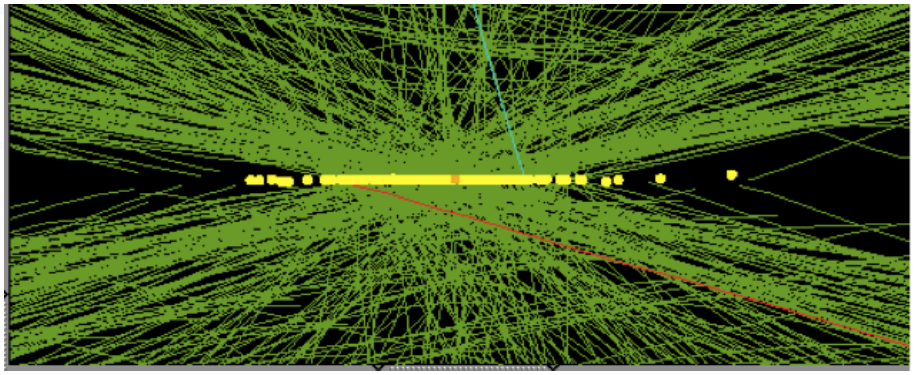
- Dense, high P_t jets require fine segmentation
- 100 TeV collider as a discovery machine will hunt for M~20-30 TeV particles that may decay to Higgs - reconstruct Higgs at p_T~10 TeV



[Chekanov, CPAD meeting]

A future linear or circular e^+e^- collider will be a precision machine that will require very low mass trackers and calorimeters with fine segmentation.

HL-LHC 10^{34}



HL-LHC detectors must be designed for ~200 int/crossing

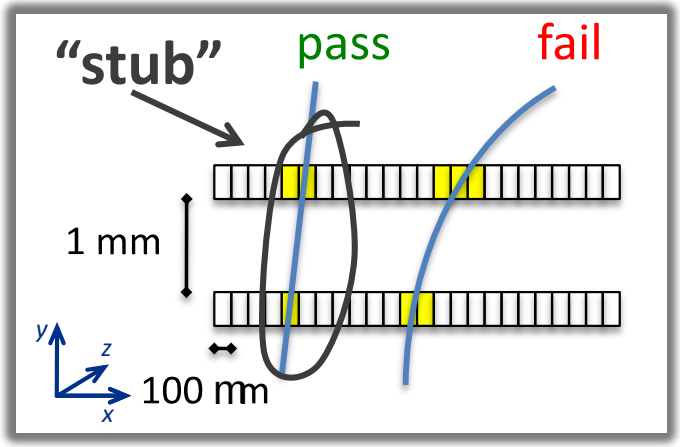
Dealing with the pileup:

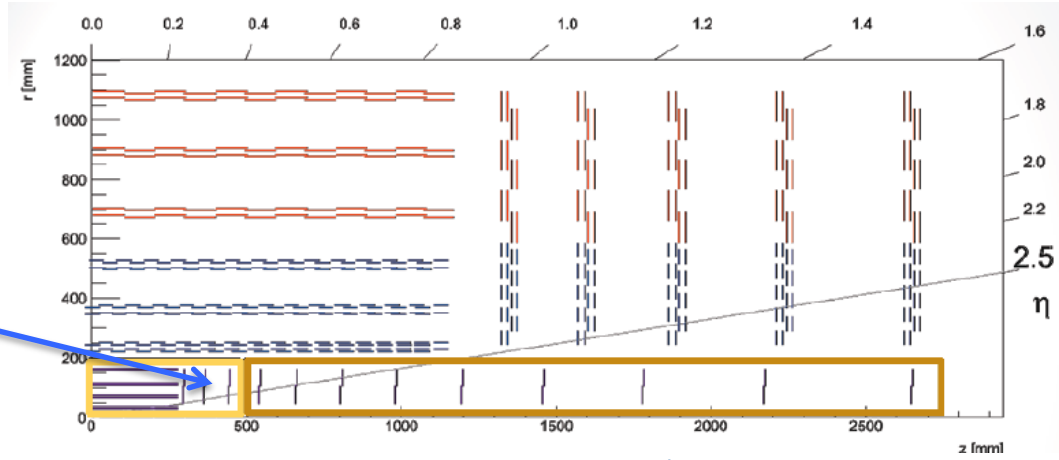
- Higher trigger bandwidth and latency (x 3 – 5)
- Add track information to L1
  - Pixelization at trigger level
  - Intelligent trackers (region of interest or standalone)
- Isolate primary vertices
  - By timing
  - By tracking

Plus extended forward coverage (VBF)

- Pixelated calorimeters
- Forward tracker disks (CMS)
  - Low field integral, high occupancy
- Fast timing for vertex tagging

CMS Track Trigger

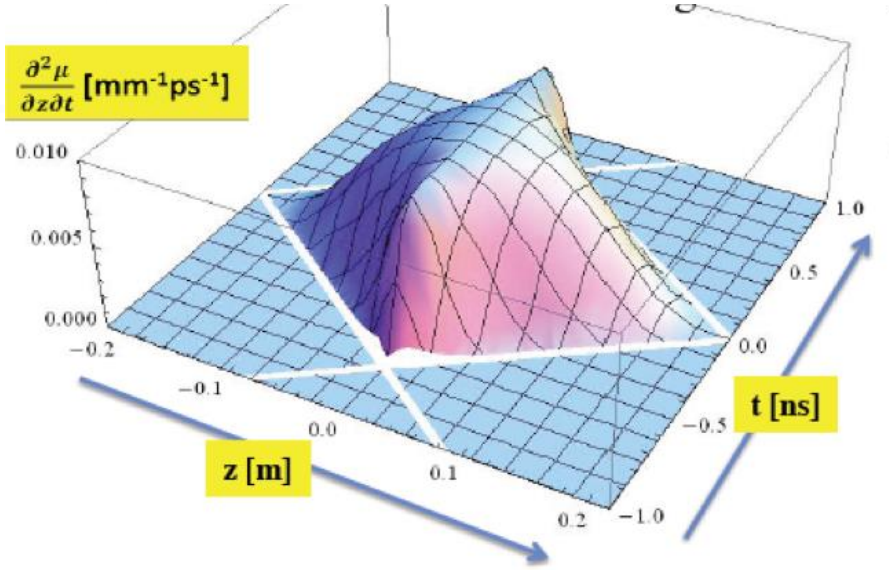


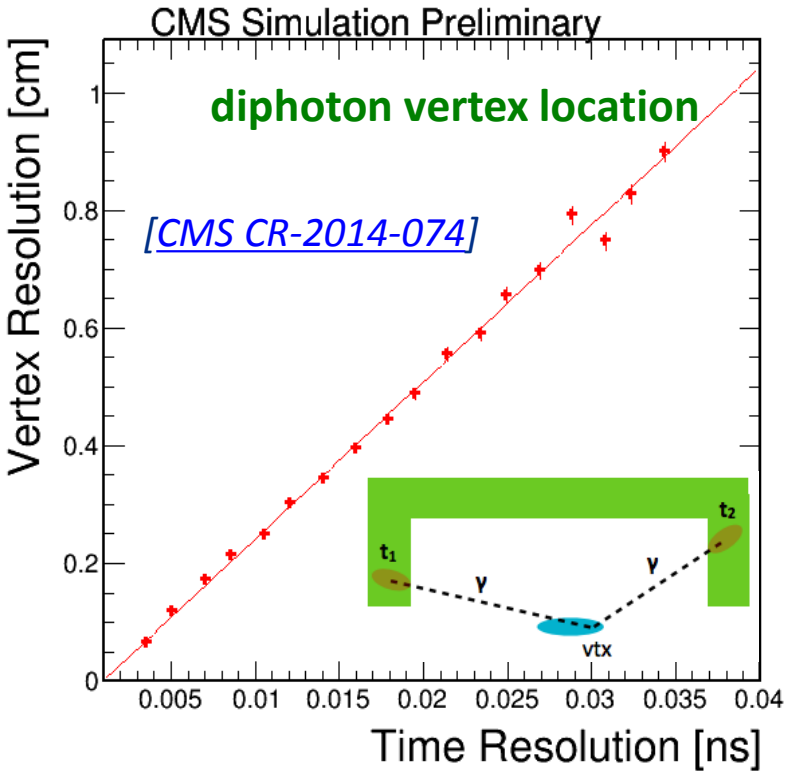


Pileup and timing

Event pileup at HL-LHC may reach 200 interactions per 25 ns crossing. To mitigate the confusion we would like to tag arrival times of tracks and showers to the ~20 ps level to correlate vertices of origin of jets/particles.

- Vertex Z is convoluted with beam width (crossing duration)
- Want to time tag both objects being correlated (i.e. central track and forward jet)





Radiation Hardness

Radiation induces trapping and leakage current centers in silicon. To mitigate these effects we must:

- Collect charge quickly – high fields
- Use thin detectors - thickness>trapping distance doesn't help
  - Higher fields in thin detectors
- Operate at low temperature to "freeze" out traps

Radiation increases leakage current

- Operate at low temperature

Extensive studies of "defect engineering" in RD 50

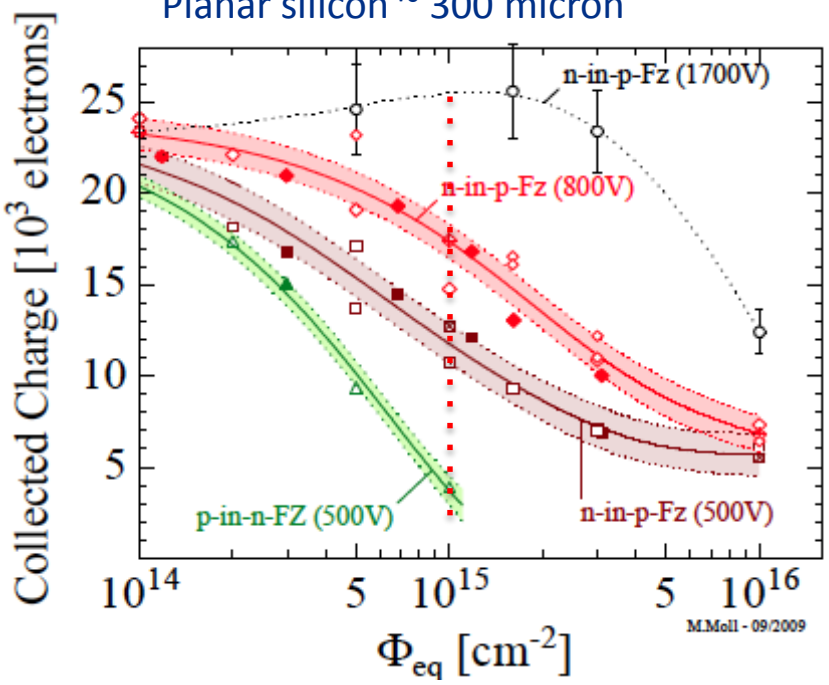
- Very complex pathology of traps and defects
- Oxygenation helps for charged particles, not neutrons.

Changes in surface charge distributions can change breakdown voltage – design is an art

Radiation Hardness

10^{15} n/cm^2

Planar silicon ~ 300 micron



FZ Silicon Strip Sensors

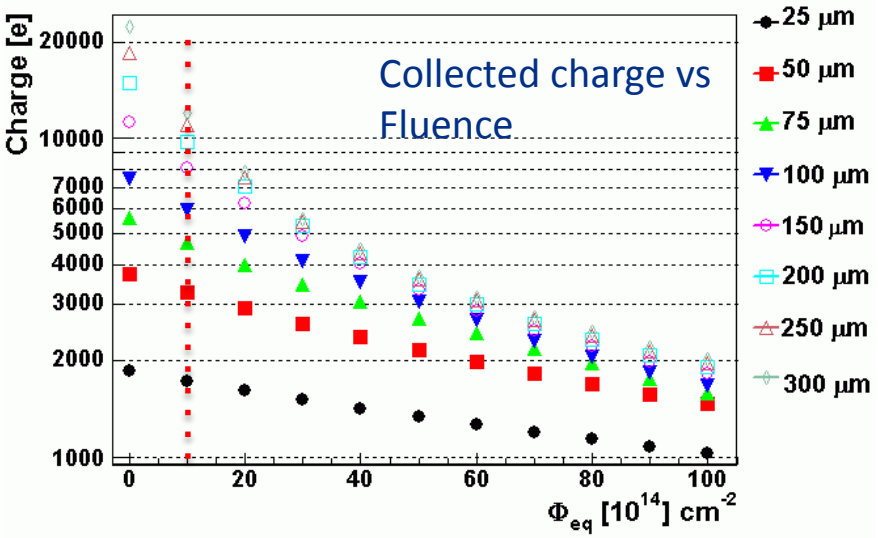
- n-in-p (FZ), 300µm, 500V, 23GeV p [1]
- n-in-p (FZ), 300µm, 500V, neutrons [1,2]
- n-in-p (FZ), 300µm, 500V, 26MeV p [1]
- n-in-p (FZ), 300µm, 800V, 23GeV p [1]
- n-in-p (FZ), 300µm, 800V, neutrons [1,2]
- n-in-p (FZ), 300µm, 800V, 26MeV p [1]
- n-in-p (FZ), 300µm, 1700V, neutrons [2]
- p-in-n (FZ), 300µm, 500V, 23GeV p [1]
- p-in-n (FZ), 300µm, 500V, neutrons [1]

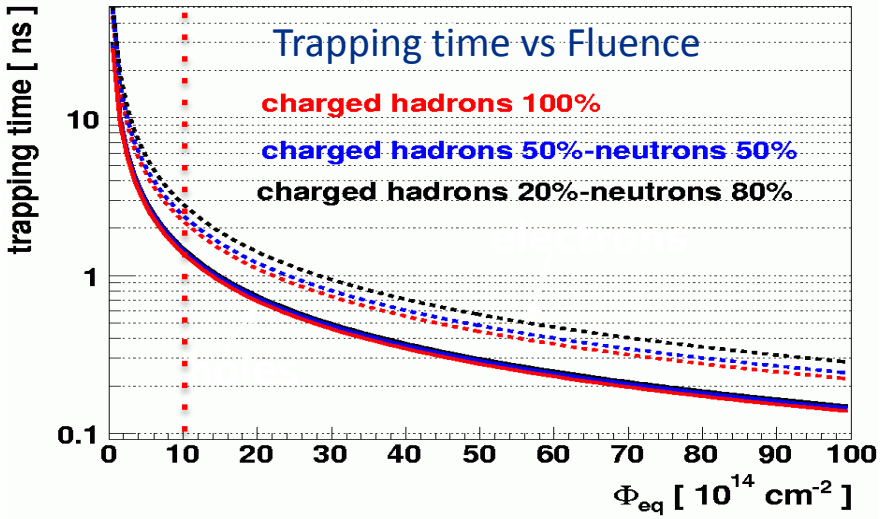
References:

[1] G.Casse, VERTEX 2008 (p/n-FZ, 300µm, (-30ºC, 25ns)

[2] I.Mandic et al., NIMA 603 (2009) 263 (p-FZ, 300µm, -20ºC to -40ºC, 25ns)

Thin, n-on-p appears to be the best choice

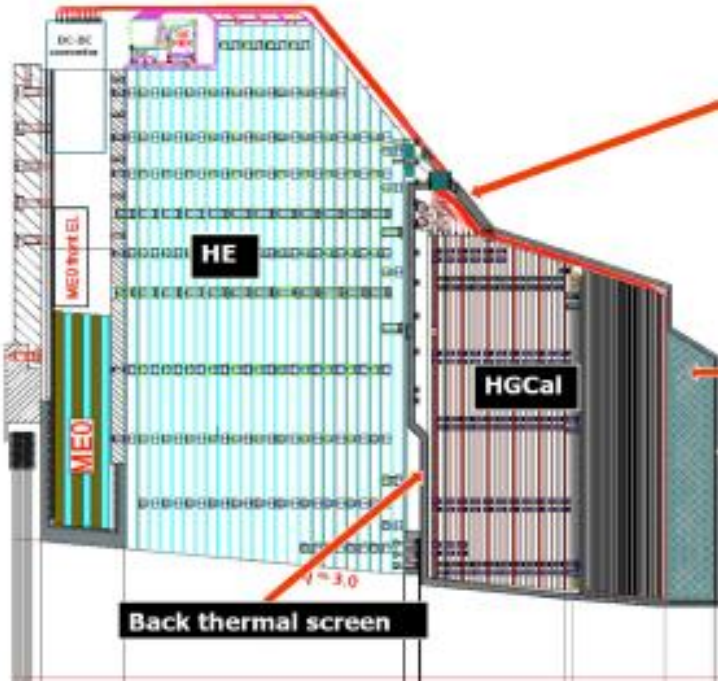


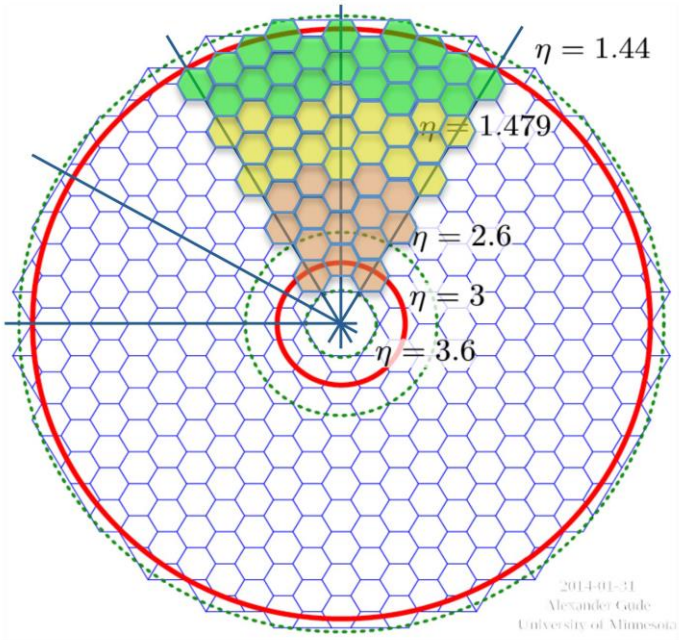


CMS High Granularity Calorimeter

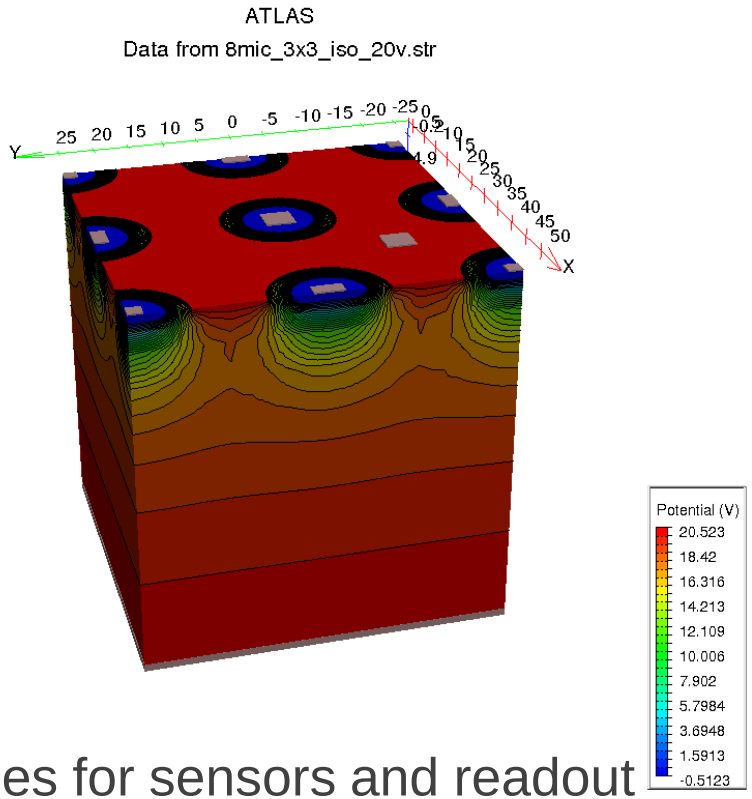
CMS is building a High Granularity Calorimeter for the endcaps in Phase 2 (~2025). The motivation is to develop a radiation hard detector with segmentation that accommodates particle flow, possibly with ~20 ps time resolution within a shower. Maximum fluence ~10^{16}.

- Based on particle flow reconstruction algorithms
- 28 (EM) + 12 (Hadronic) layers
- ~ 600 m^2 of silicon sensors operating at -30 deg C
- 100, 200, 300 micron thick sensors – possibly based on 8” silicon wafers





Tools



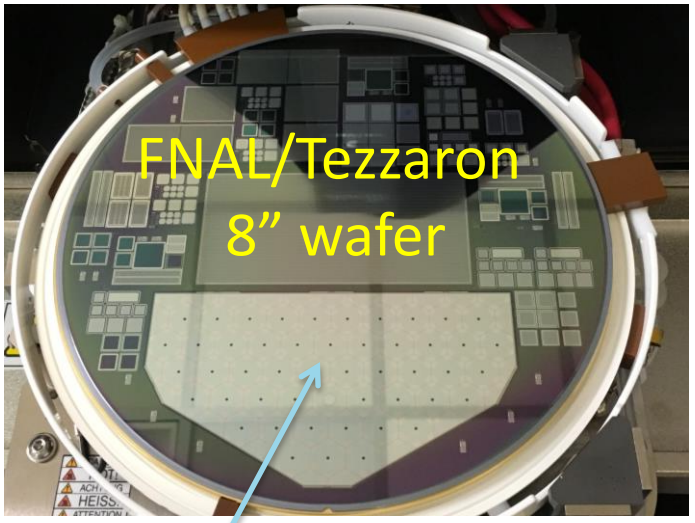
Particle Physics applications of silicon-based detector systems have benefited enormously from the tremendous R&D effort and infrastructure associated with the semiconductor industry, which is based on obsolescence of your iphone every ~ two years. We now have:

- Access to IC foundries *willing to collaborate* on innovative structures
- Development of novel interconnect technologies for sensors and readout chips
- Access to sophisticated TCAD simulation tools to design and simulate semiconductor systems

We can design and build systems that would have been far beyond our reach a few years ago

HEP often can act as a “first adopter” of these technologies – we are willing to take more risks than commercial ventures

Costs, Areas, and Yields



We hope to build large area silicon-based trackers and calorimeters with fine pixel pitch and low cost. We would like to integrate low cost “simple” sensor technology with complex readout.

- Cost of a CMOS silicon IC is about \$3/cm^2 not including startup mask costs
  - Area of an IC is limited to 2x3 cm^2 (or so) by the stepper reticule
  - Yields of 80-95%
- Cost of a silicon-based sensor is about \$4-10 cm^2
  - Area of a sensor can be as large as the 6” or 8” wafer size
  - The structures are simple and the yield can be high
- Fine pitch bump bonding of sensors to ROICs is expensive

To build large area devices:

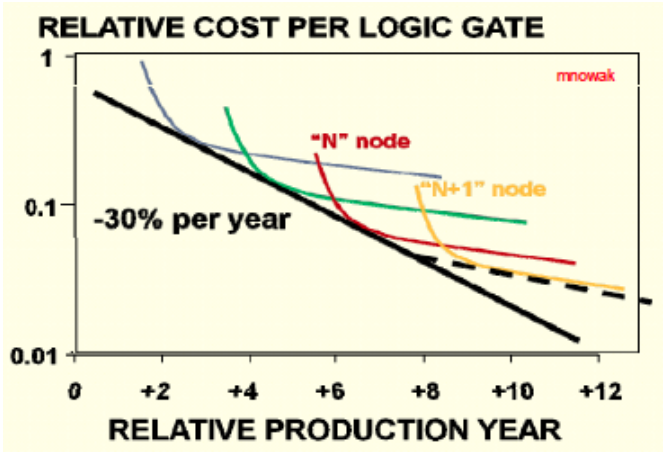
- Mate reticule-sized die readout ICs with die sized sensors
  - But there are edge effects that cause dead regions
- Assemble an array of readout die on a large sensor - YIELD!

A word about Electronics

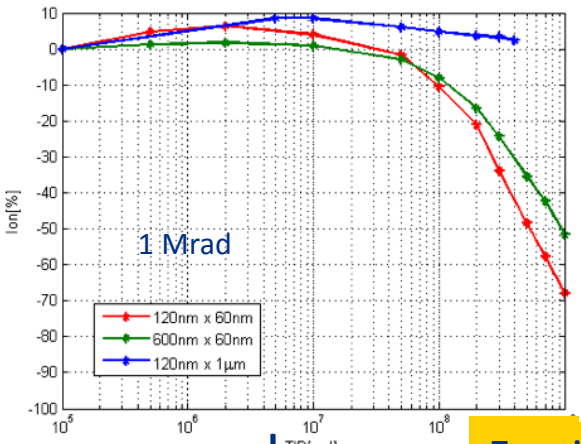
Commercial electronics are at the 14nm node and shrinking. HEP is three generations behind.

- Designs in the latest technology nodes are obscenely expensive
- Analog designs are problematic because of low voltage rails and poor transistor matching
- Leakage currents are high

RD53 has found significant radiation effects in 65 nm pmos transistors. Design for regions above 200 Mrad must avoid short channel PMOS transistors.



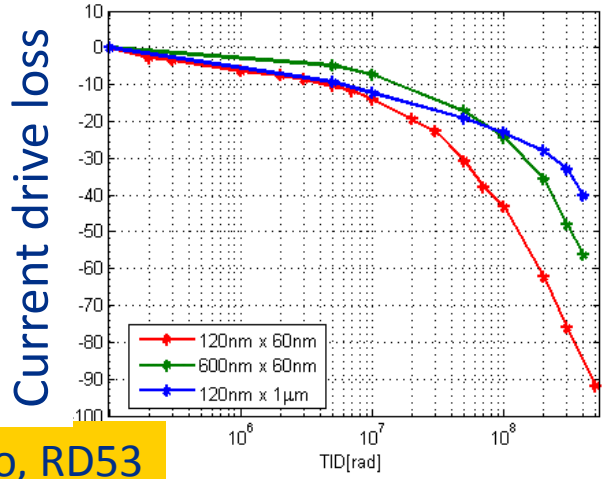
NMOS



dose

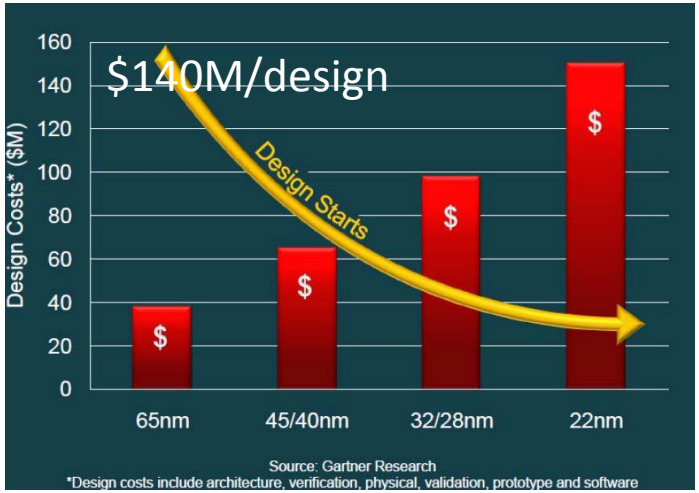
Current drive loss

PMOS



Faccio, RD53

Design Cost by Node



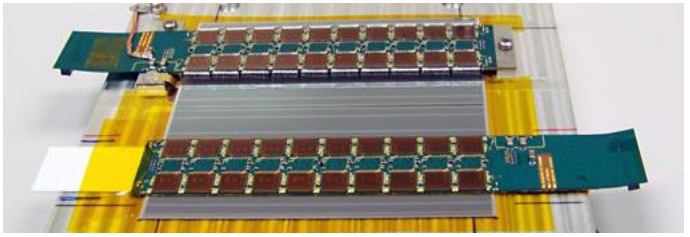
Current Technologies

Sensor wafers on 4” or 6” silicon

Readout chips with >65 nm feature size
(Industry is at 14 nm and shrinking)

Strip Modules ~10x10 cm (6” wafer), with readout at the periphery, wirebond interconnect

- 50 micron pitch



ATLAS tracker module

Pixel modules ~4x5 cm with bump bonded interconnect

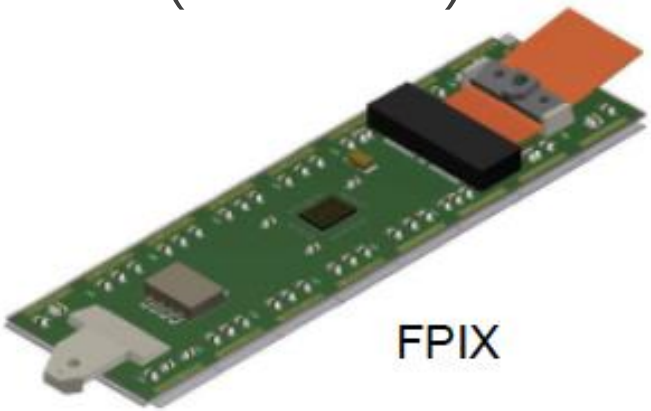
- 100 micron pixels
- 4-6 ICs per module

First applications of 3D structures for radiation hardness (ATLAS IBL)

Avalanche devices for photodetection only

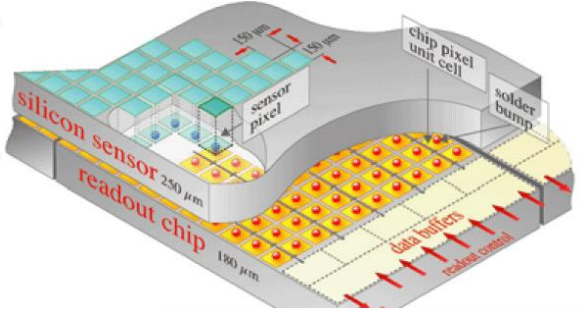
Radiation hardness achieved by:

- Deep submicron electronics
- Thin, oxygenated silicon
- Low temperature operation

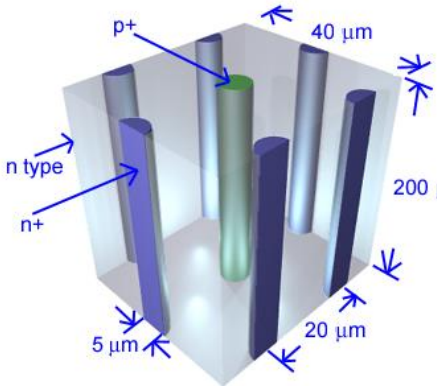


New Sensor/Interconnect Technologies

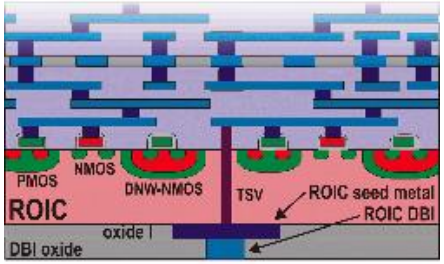
An embarrassment of options



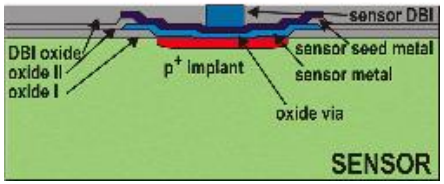
Hybrid bonding



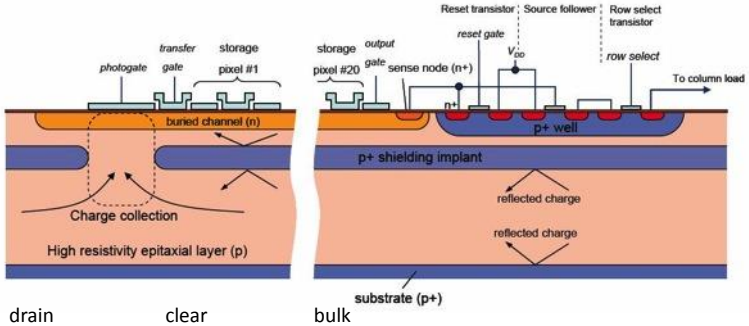
3D sensors

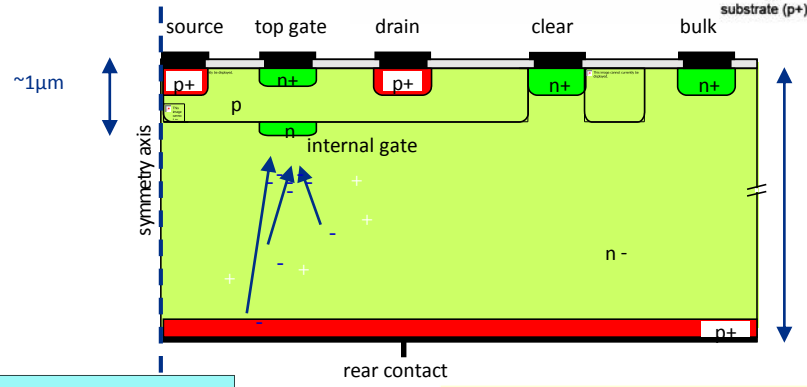


3D electronics

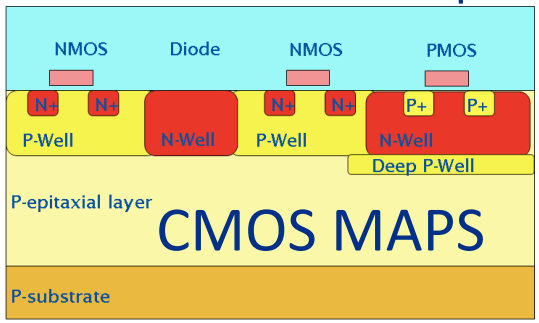


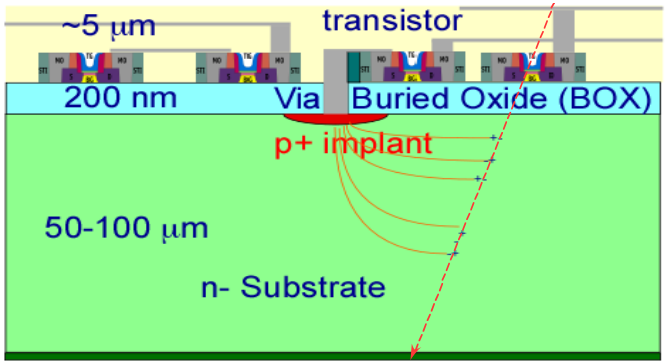
CCD (SLD)





DEPFET (Belle II)





SOI

Laser Annealed Ohmic contact

Monolithic Active Pixels (MAPS)

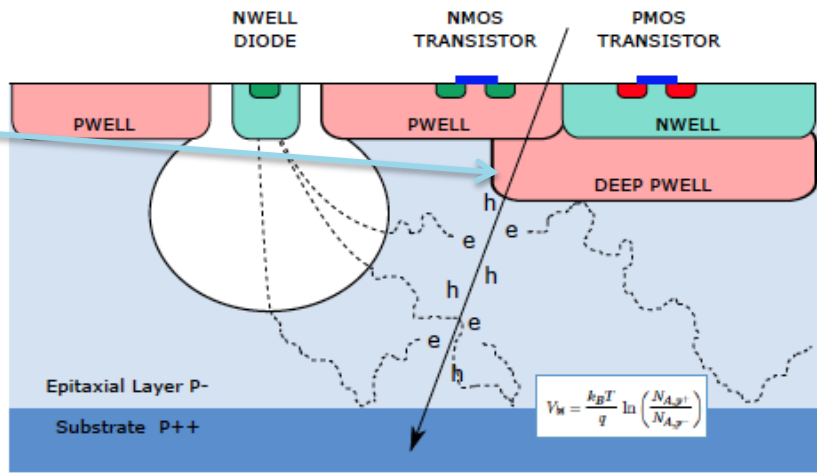
This technology is an outgrowth of the imaging industry- use a thin epitaxial high resistivity layer to collect charge from light exposure (or tracks).

- Uses “standard” CMOS processes
- Charge collection by diffusion (slow and rad soft)
- Parasitic charge collection by PMOS structures – protect by p-well
- Thin active layers
- Susceptible to digital-analog coupling due to thin layers – rolling shutter

Used in STAR at RHIC and ALICE upgrades. Moderate rates and radiation dose.

Problems can be addressed by adding a drift field to the structure…

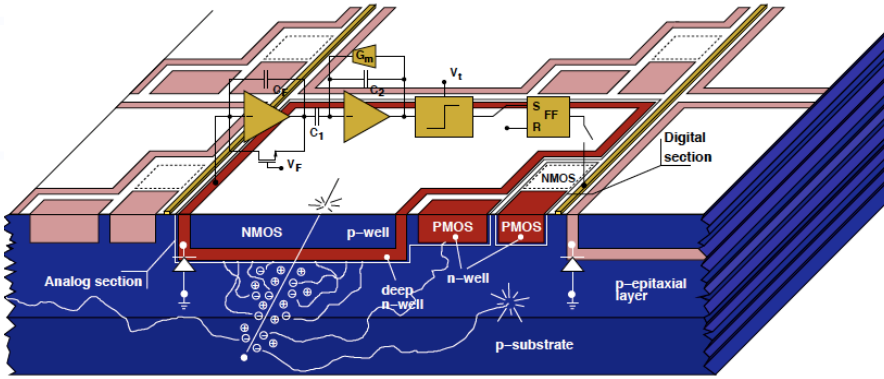
STAR HFT



ALICE MAPS sensor

Solving Problems - MAPS

MAPs – technology used in cameras using charge collection by diffusion in a thin(~5-15 μm) epitaxial layer



Slow-charge collection by diffusion

Low S/N

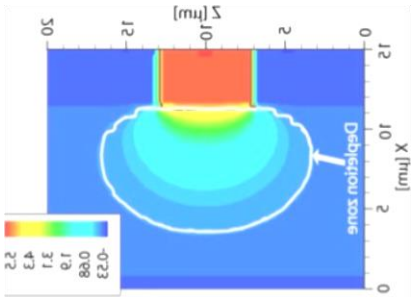
Charge lost to parasitic PMOS

Fully depleted substrates

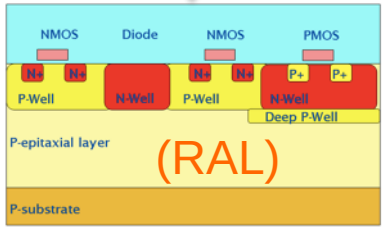
Thick, high resistivity epitaxial layers

4 Well process

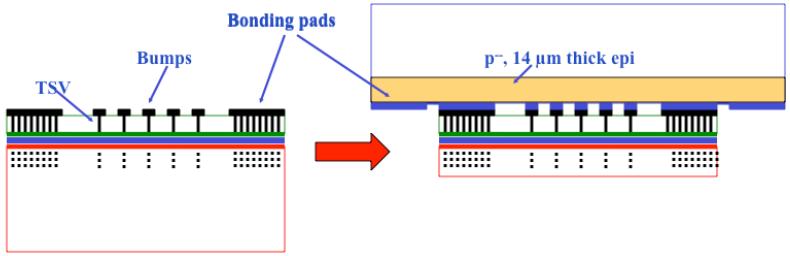
3D assemblies



(IPHC-DRS)



(RAL)



From Tezzaron/Chartered (2 tiers)

plus 0.35 XFAB and Ziptronix (3 tiers)

(IPHC-DRS)

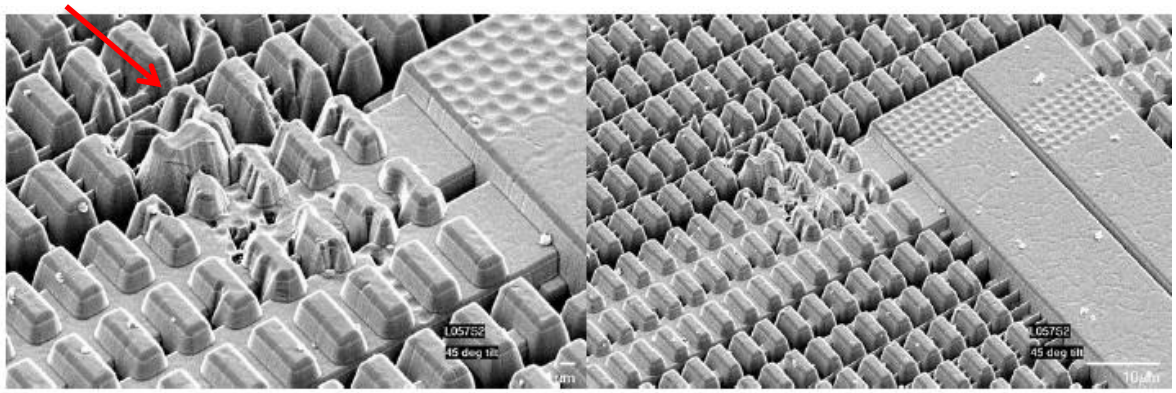
Thinning and backside processing

STAR HFT

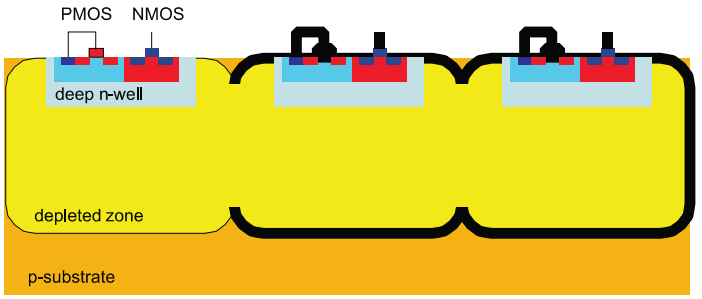
- STAR Heavy Flavor Tracker is the first MAPS deployment in a Collider experiment
  - Sensors thinned to 50 microns
  - Air cooled
  - Experienced latchup due to heavily ionizing particles – high local currents

  Because the sensors were thin and cooling was minimal there was a thermal runaway that locally melted the silicon

  …



HVCMOS



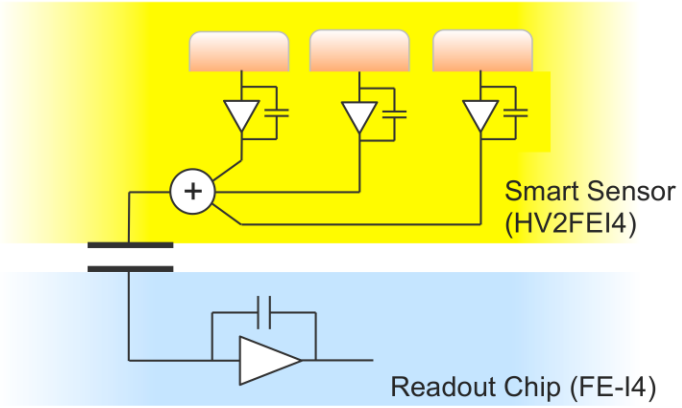
[Peric]

High resistivity substrates have become available with multi-well geometries in standard CMOS processes with HV transistors – HVCMOS

- An extension of CMOS MAPS with larger charge collection volume, faster collection, more radiation hard
- Ability to integrate amplification with sensor – take advantage of low detector capacitance
- Transistors able to withstand ~100V

But

- Depletion depth limited
- Larger capacitance due to shallow wells?
- Size limited by CMOS reticule



"3D" connection
To ROIC wafer

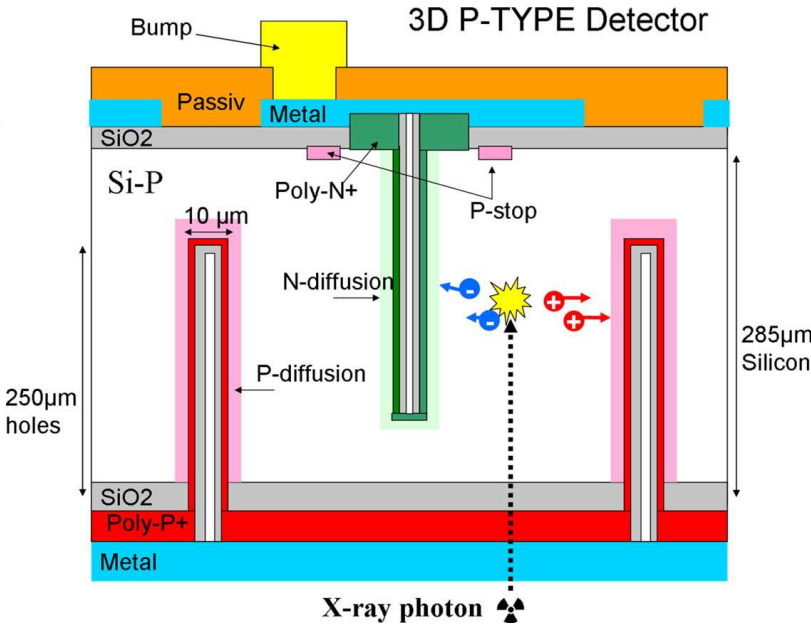
ATLAS looking at HVCMOS with a simple amp/disc to replace HR silicon material in strip detectors. Can this reduce costs?

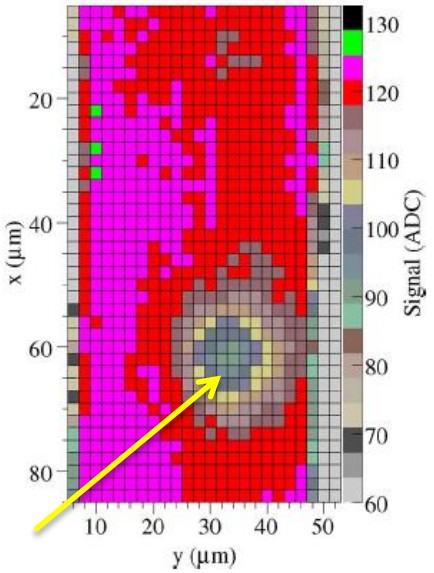
3D Silicon Detectors

3D detectors utilize technologies developed for MEMS, high aspect ratio deep reactive ion etching, to generate electrodes in bulk material rather than on the surface. This reduces the effective drift distance, increasing radiation hardness, while maintaining the full signal.

- Increases collecting fields
- Shortens collection time
- Reduces effect of trapping
- Relatively high capacitance
- Complex fabrication – high cost

Used in outer IBL sensors. This technology can also be used to fabricate active edge sensors





Loss of signal in electrode

Avalanche-based, "Ultra Fast" Detectors

Time resolution can be parameterized as

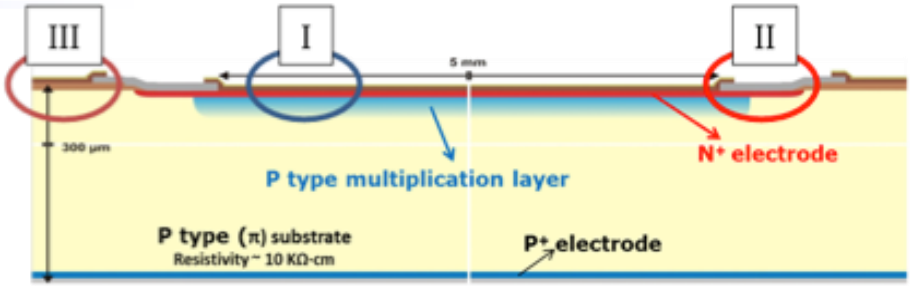
$$s_t = t_{rise} \left(\frac{N}{S} \right) + system\ effects$$

Silicon rise time is usually limited by drift velocity(<10^7 cm/sec) and sensor thickness. This can provide resolution or the 100's of ps level for single MIPs.

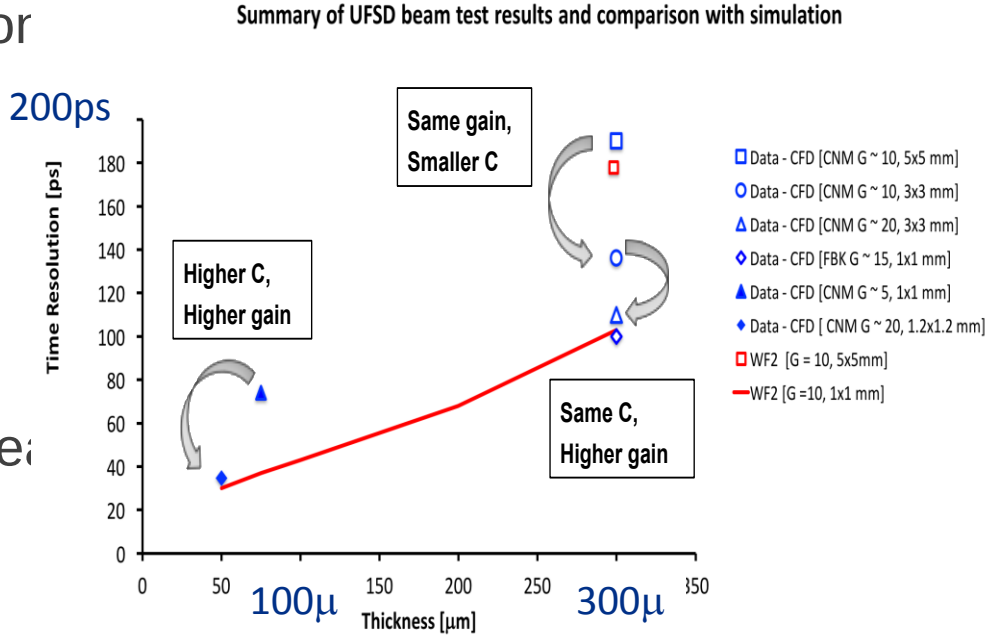
This can be improved by using an avalanche diode, that provides a large signal and fast rise time.

- Resolution must be demonstrated
- Cost effective production of large area
- Large levels of dark current
- Low gain avalanche diode (LGAD)

Benefits from LIDAR R&D. Challenges in power dissipation in fast amps



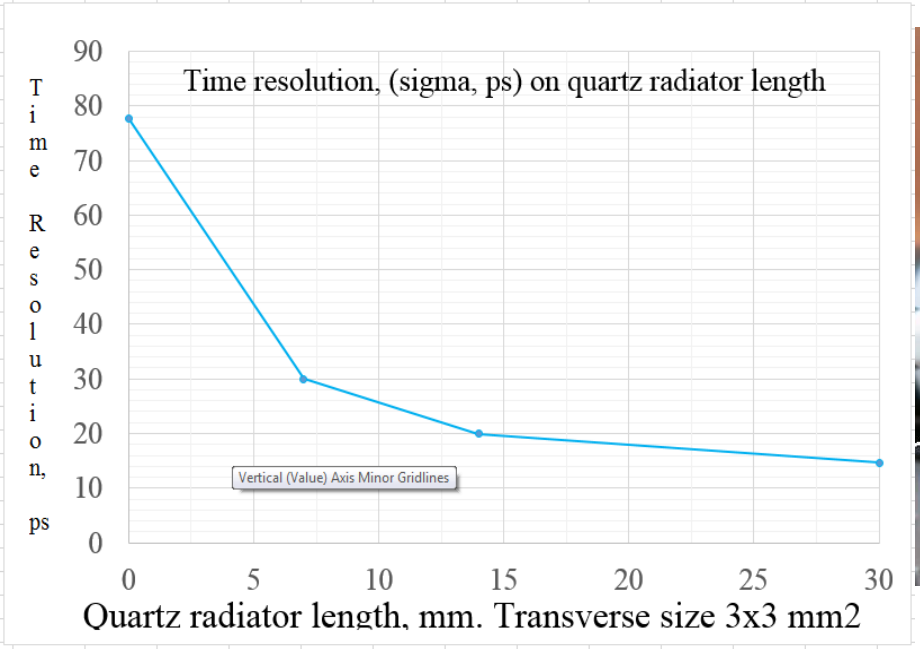
LGAD Cross section

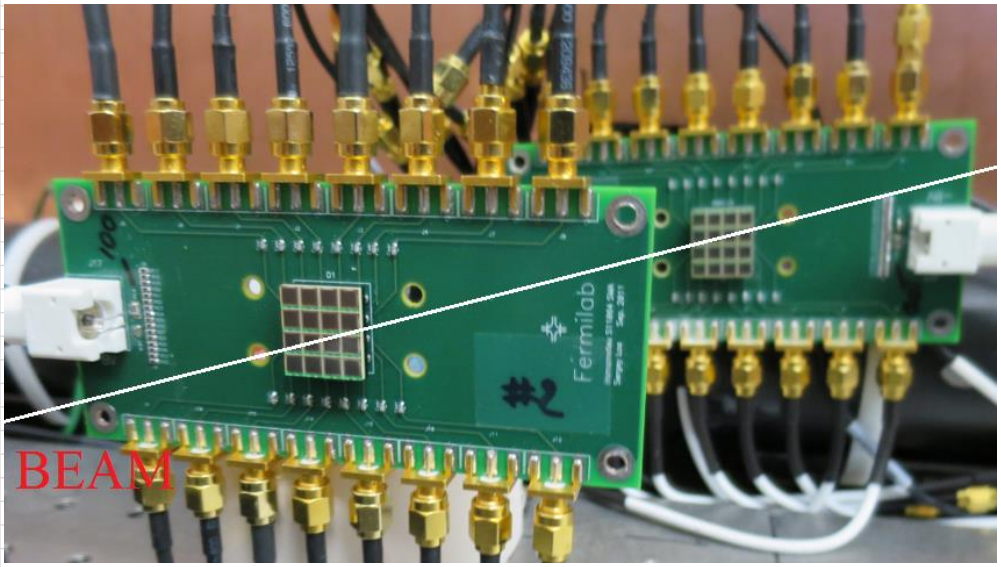


Summary the time resolutions achieved with different type of UFSD sensors.

SiPM Based fast tracking

- SiPMs are arrays of geiger mode avalanche diodes connected by bias and summing network
  - Low interconnect capacitance
  - Excellent multi-photon resolution and quantum efficiency
  - Sensitive to MIPs?

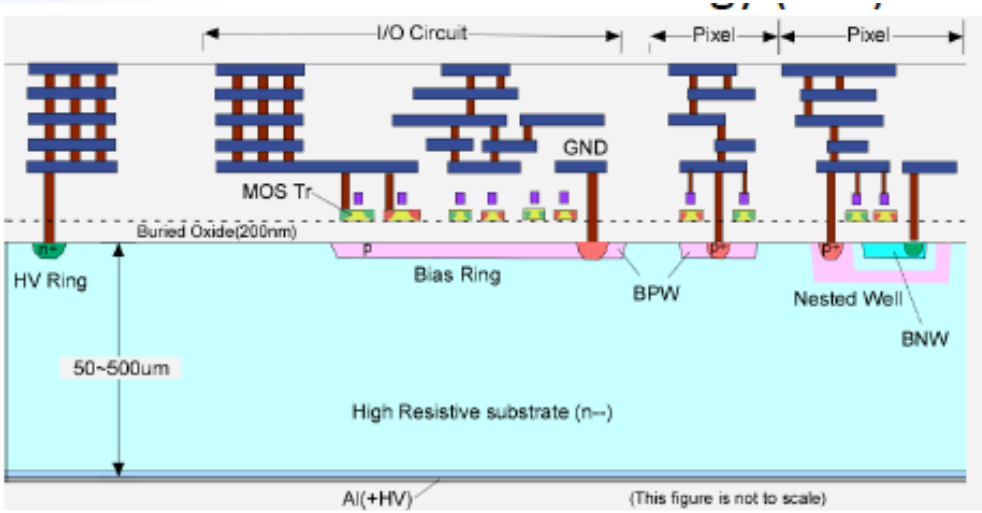




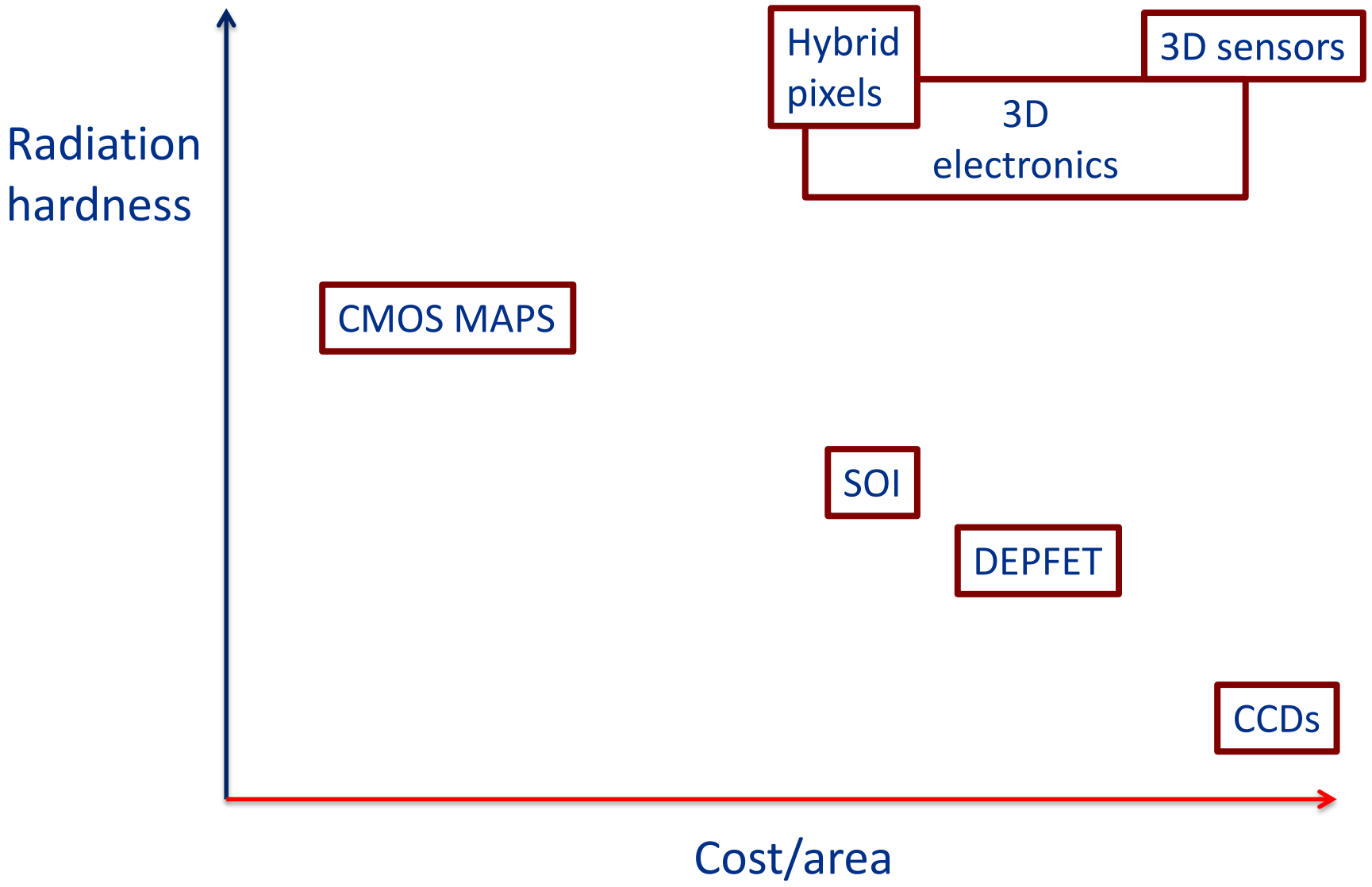
[Ronzhin]

Other Technologies

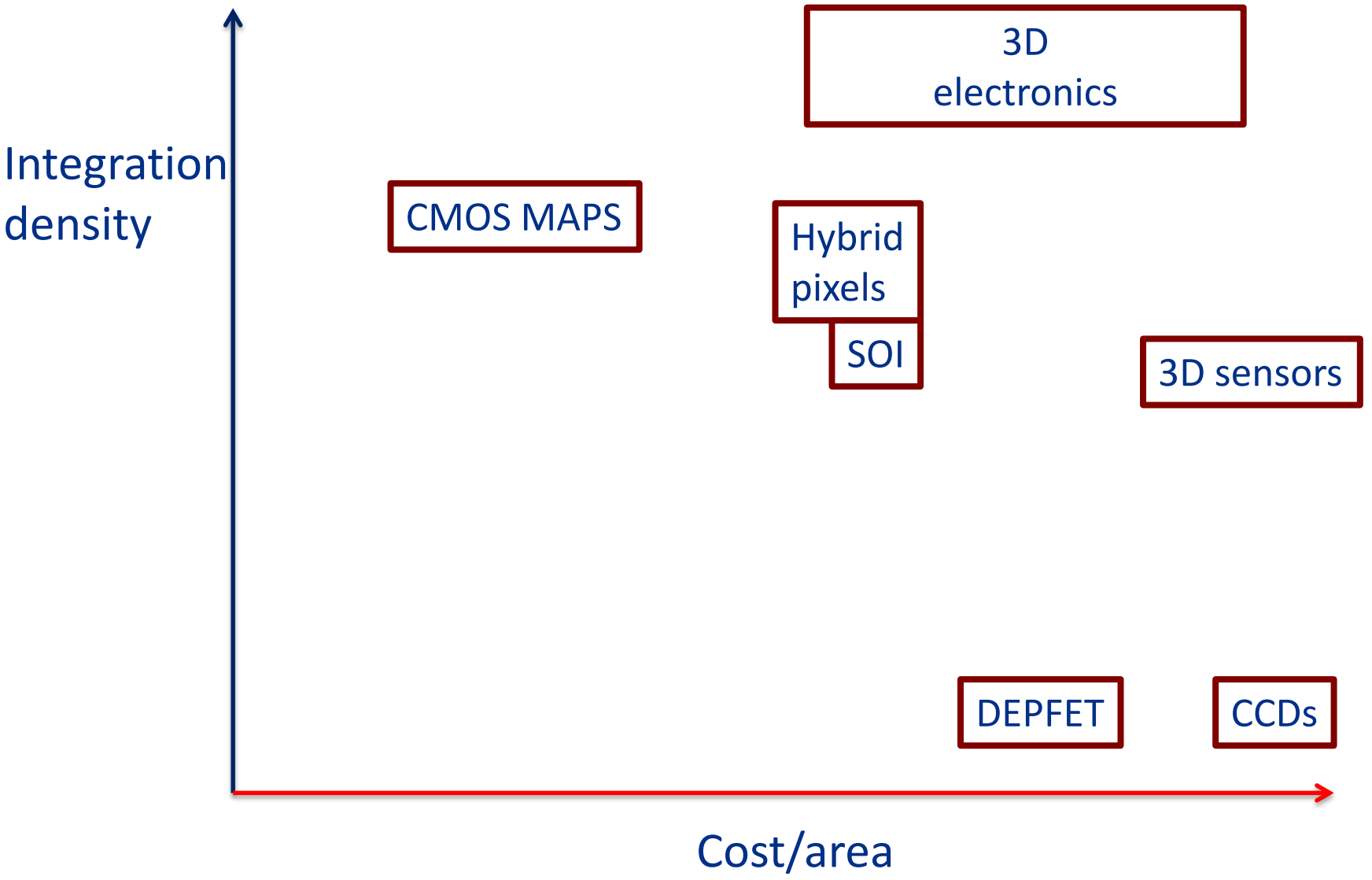
- DEPFET (MPI – Belle II)
  - Charge collected under DEPFET gate.
  - Low noise, moderate speed, not very rad hard
- SOI
  - Sensor in the handle wafer in an SOI stack
  - “Backgate Effect” field in bulk effects transistor operation
  - Radiation-induced charge in oxide affect transistors in top
- CCD
  - Variants proposed for ILC vertex



The Playing Field – thumb in the air plot



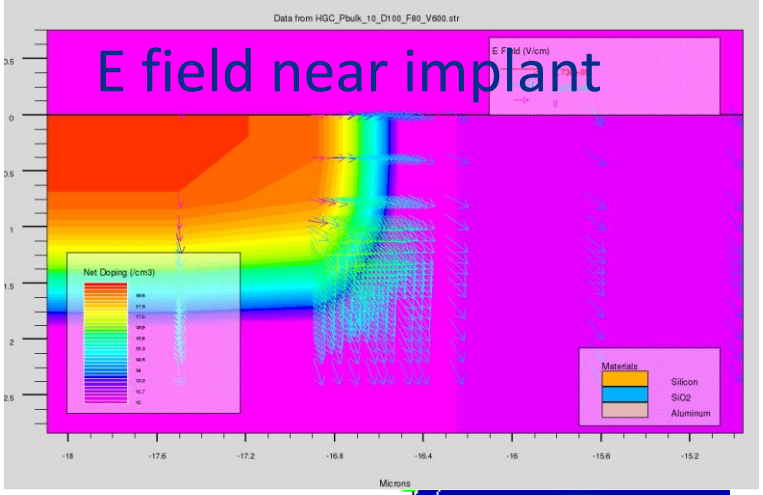
The Playing Field – thumb in the air plot II



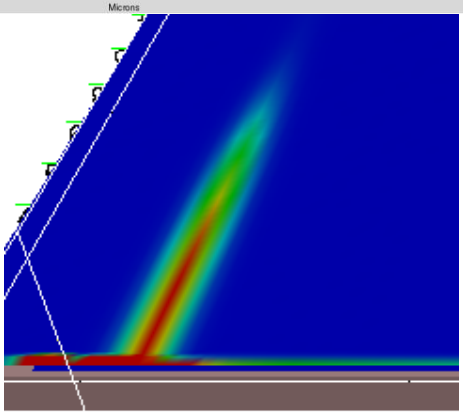
TCAD

Much of this work is enabled by the sophisticated TCAD software developed for the semiconductor industry

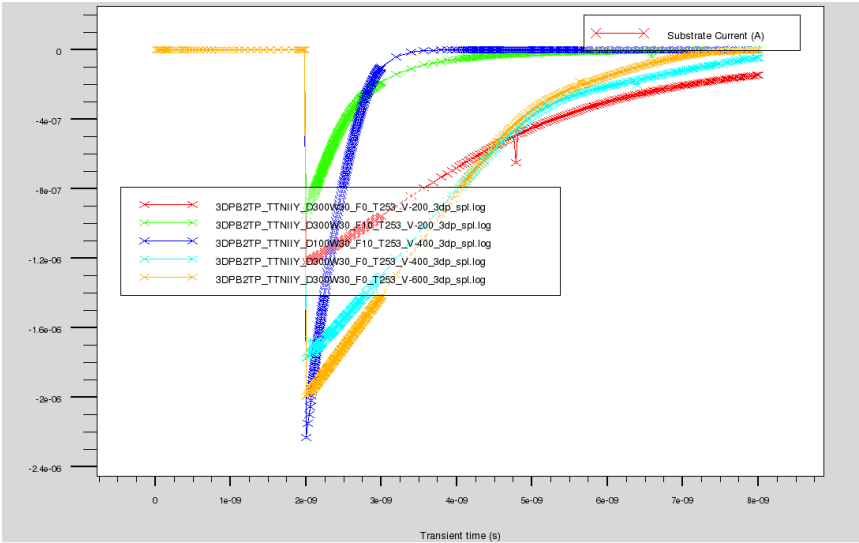
- Simulate full process flow (implantation, annealing…)
- Simulate internal fields and charge carriers
- Developed simulations of radiation damage due to induced traps.



MIP simulation



Current pulses for Various fluences And bias

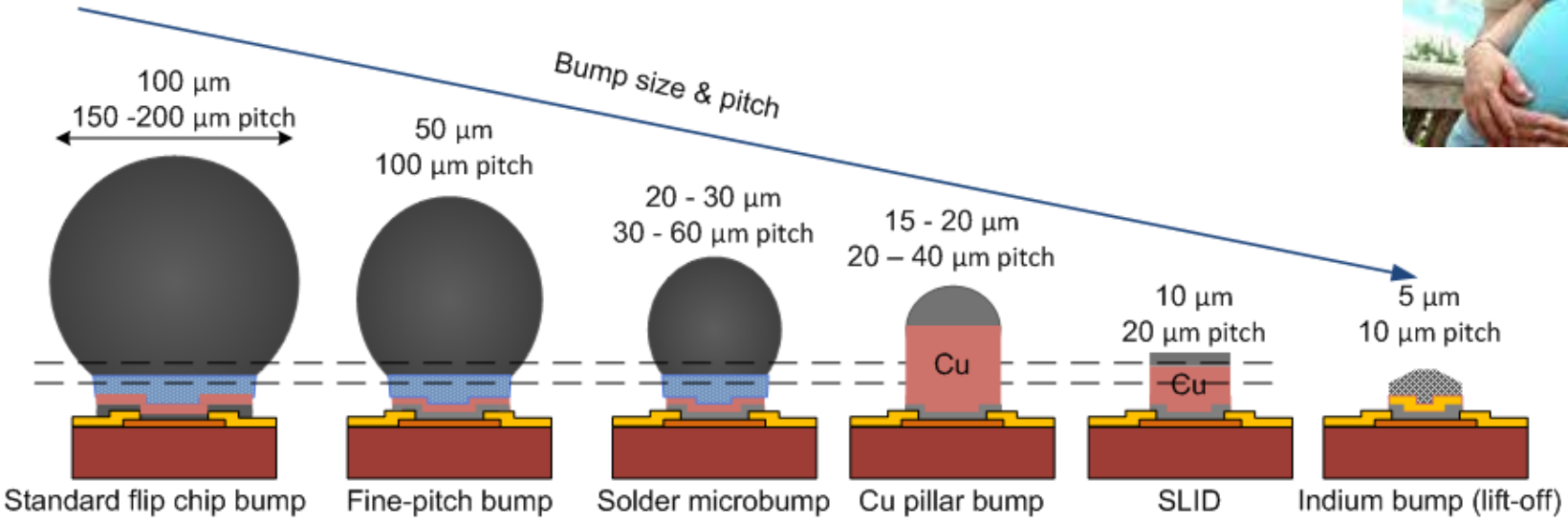


Interconnect Technologies

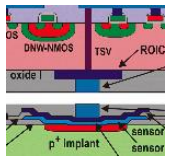
Continuous advance in technology – lower cost and finer pitch

- Solder and indium bumps
- Copper pillars
- DBI oxide bonding

Bump bonding
(Google search)



2 µm
4 µm pitch



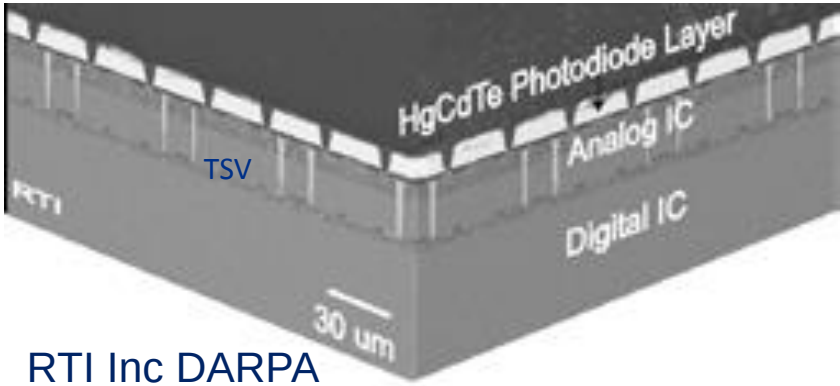
DBI

[Vaehanen]

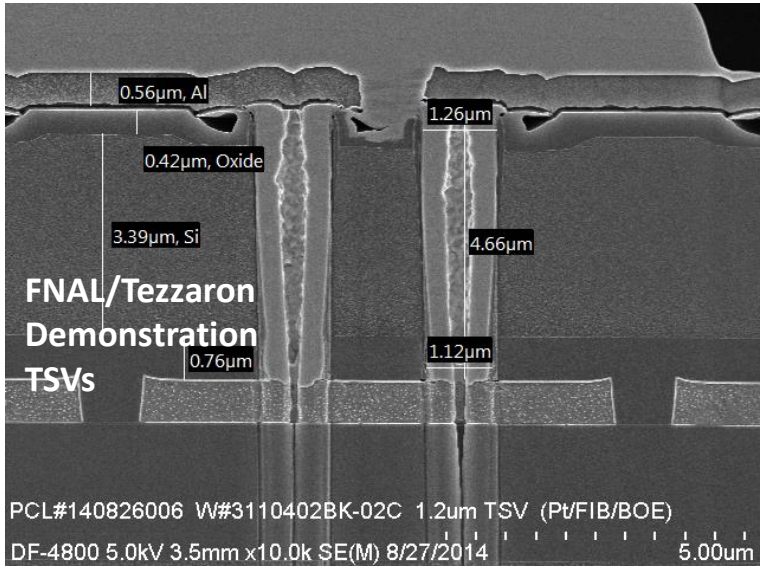
3D Integrated Circuit Technologies

A chip (structure) in three dimensional integrated circuit (3D-IC) technology is composed of two or more layers of active electronic components, integrated both vertically and horizontally by wafer bonding, thinning, and insertion of through silicon vias (TSV)

For the past decade Fermilab has worked with vendors to demonstrate and develop these technologies.

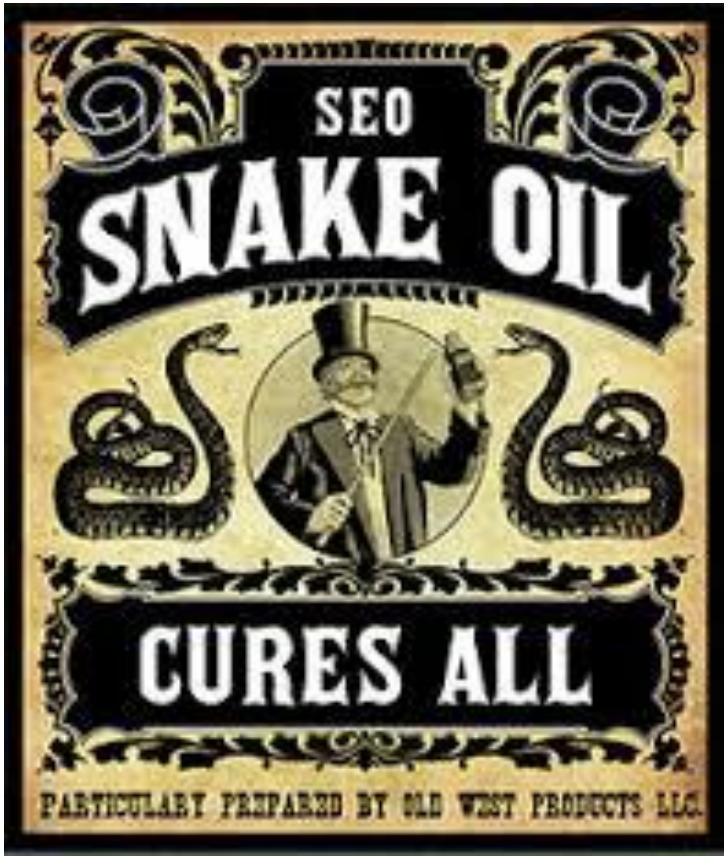


RTI Inc DARPA demonstrator



3D can solve all your ills!

- Low cost, very fine pitch bonding
- Much better power distribution and connectivity
- Radiation hard, thin sensors and readout
- Complex electronics without expensive process nodes
- Separation of analog and digital – lower thresholds
- Lower interconnect capacitance and power
- Tiled, large area devices

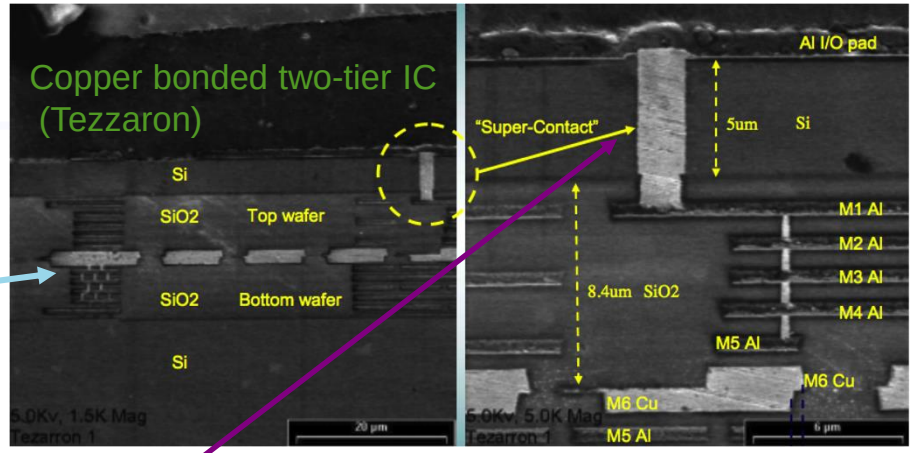


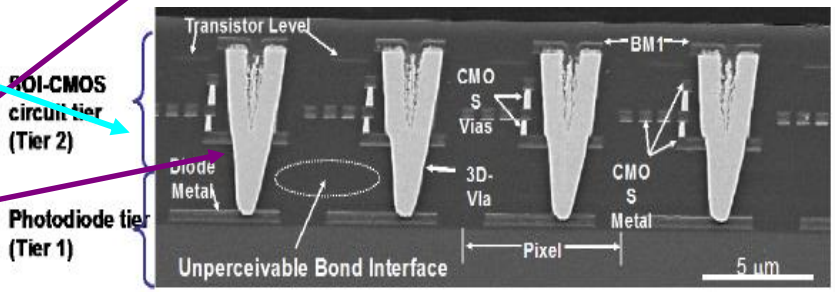
But we are dependent on commercial, large volume development

3D Interconnect Examples

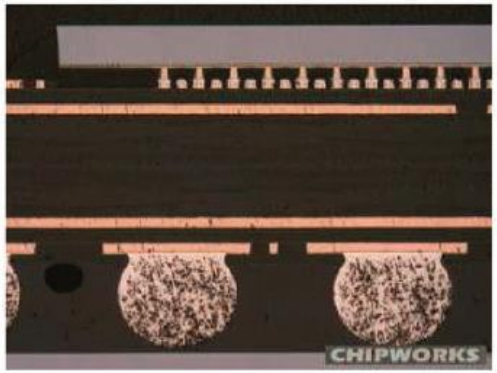
Technology based on:

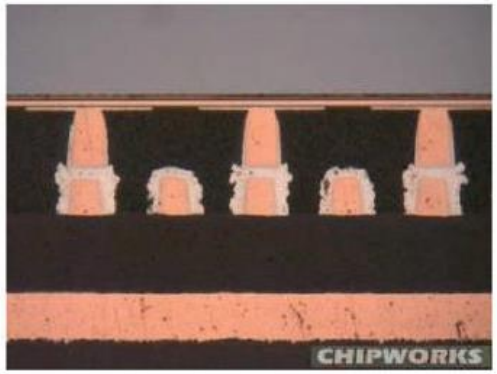
- Bonding between layers
  - Copper/copper
  - Oxide to oxide fusion
  - Copper/tin bonding
  - Polymer/adhesive bonding
  - Cu stud
- Through wafer via formation and metalization



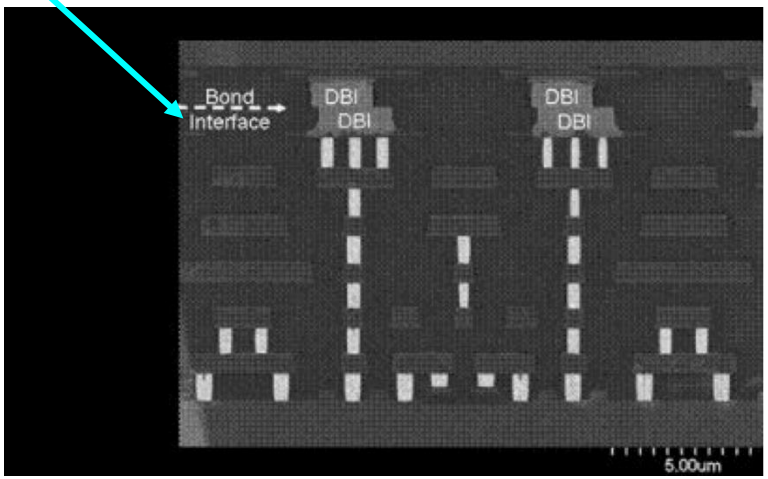


8 micron pitch, 50 micron thick oxide bonded imager (Lincoln Labs)





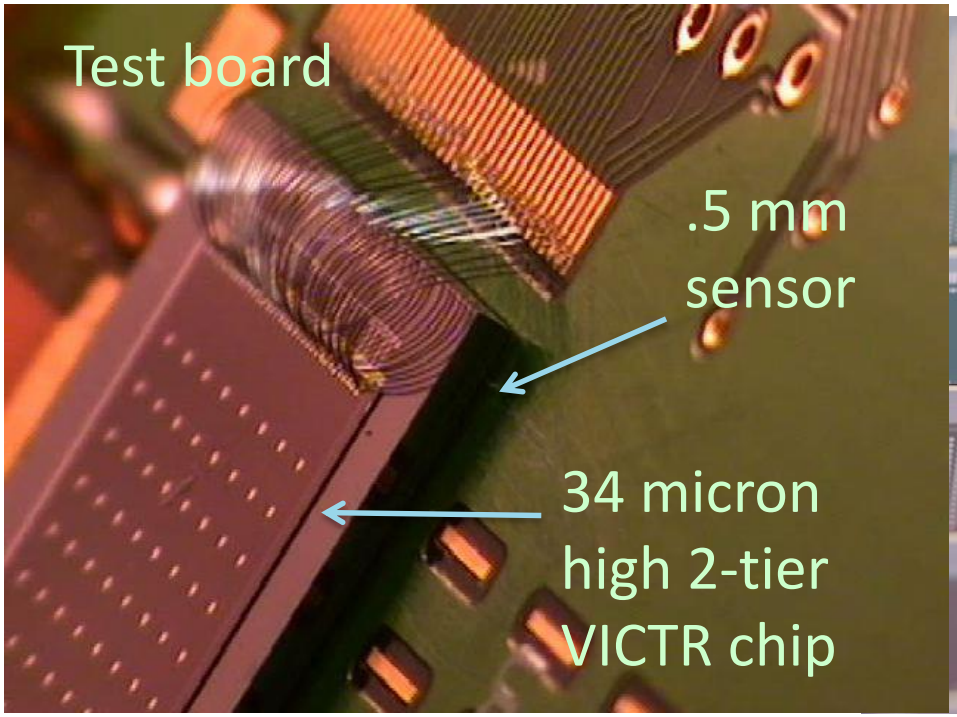
Cross-section of the TI XAM3715, a 45nm applications processor mounted on a BGA substrate

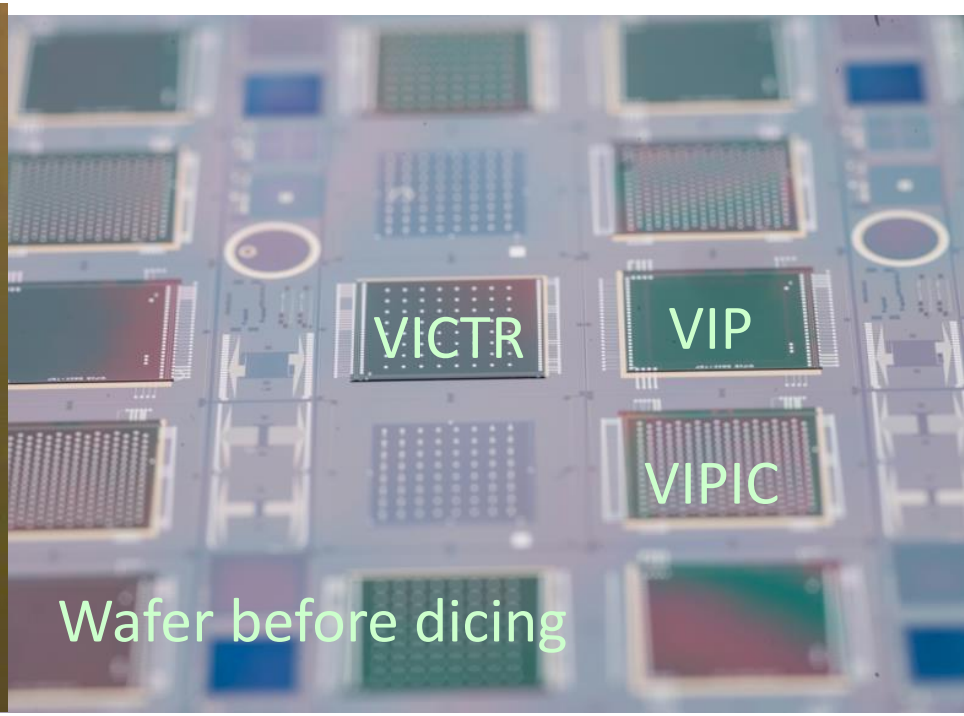


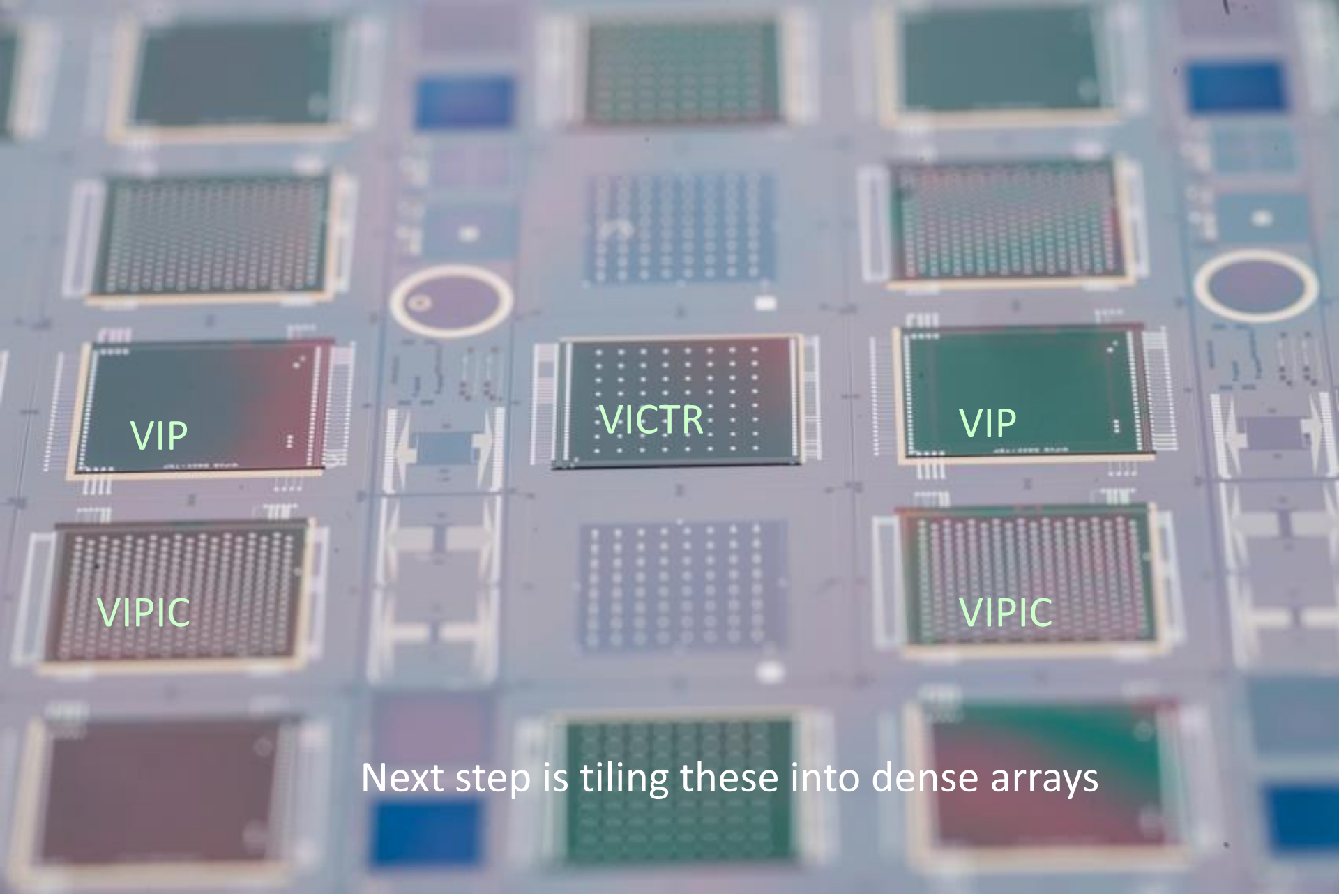
8 micron pitch DBI (oxide-metal) bonded PIN imager (Ziptronix)

3D Demonstration Project

A working 3D process was demonstrated in a FNAL/BNL *3-layer* (2 readout + 1 sensor) 3D wafer with chips for ILC, CMS and X-ray imaging (VIPIC) in collaboration with Tezzaron and Ziptronix.

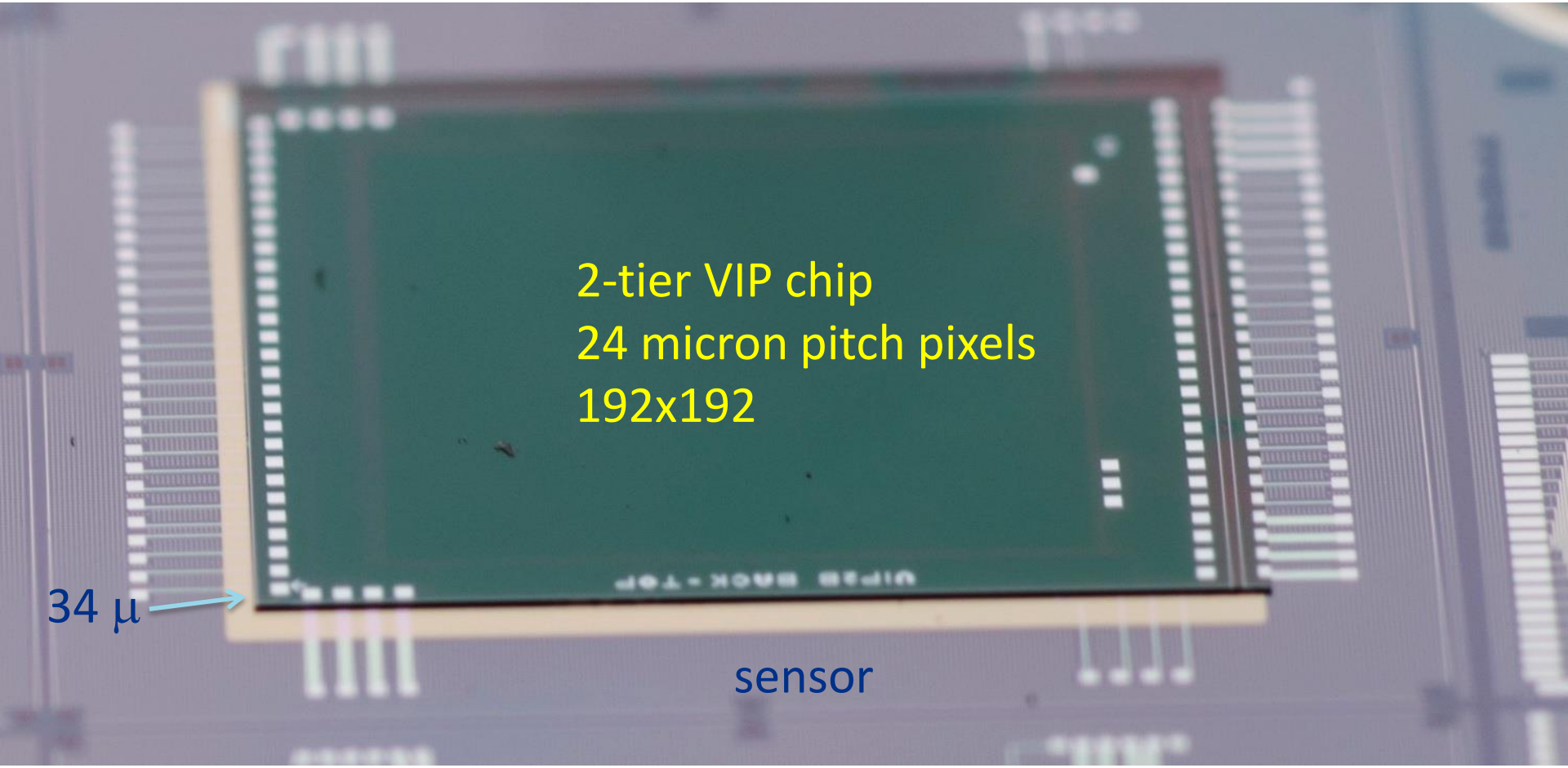






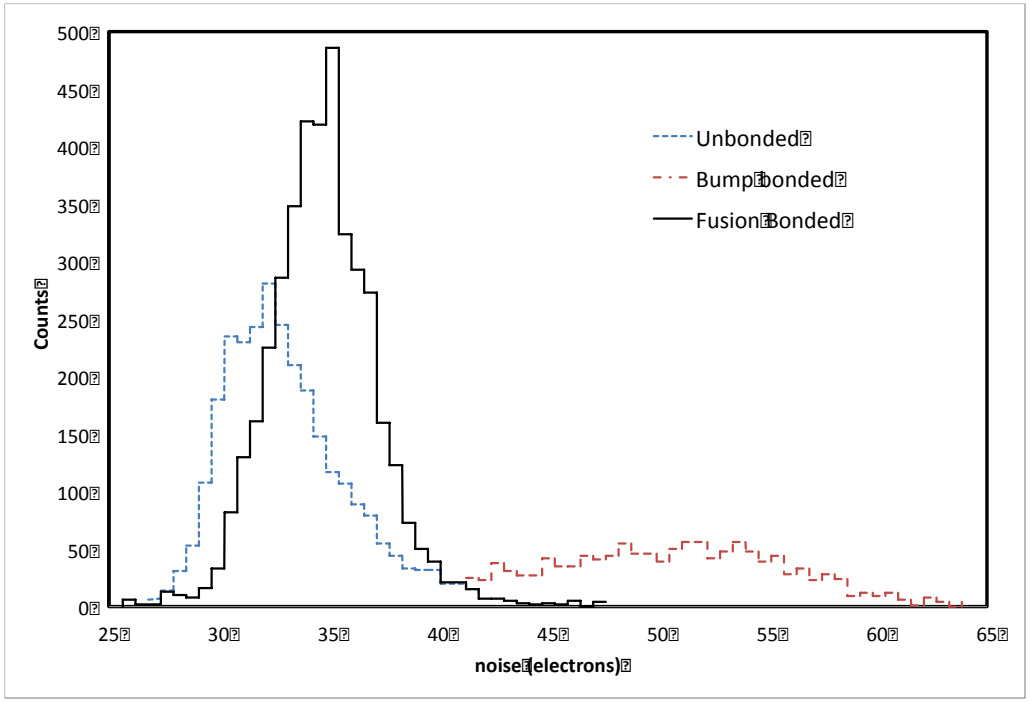
Next step is tiling these into dense arrays

VIP

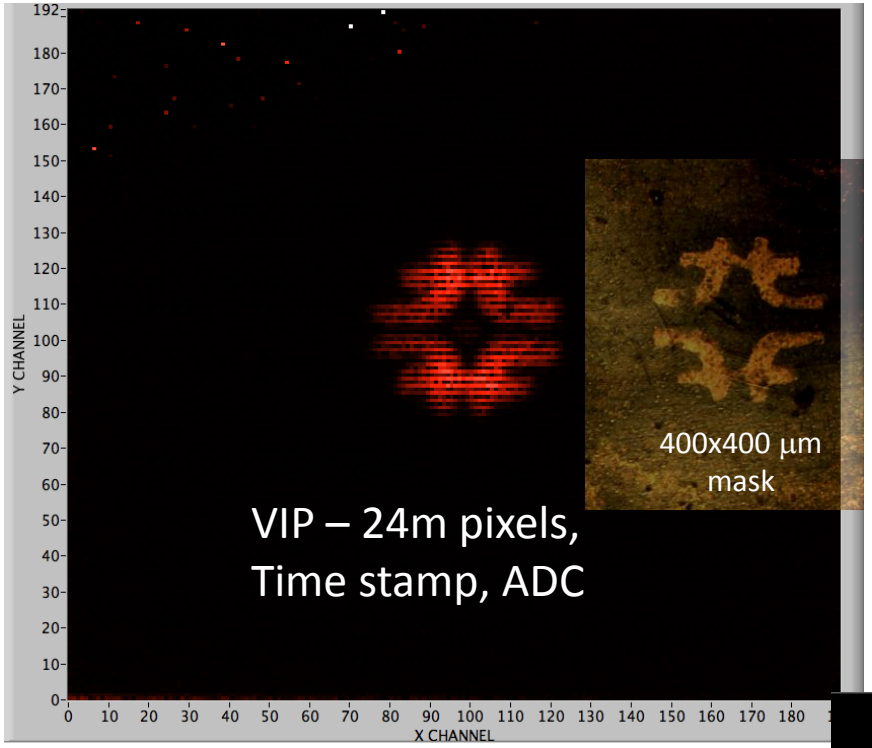


Some Results

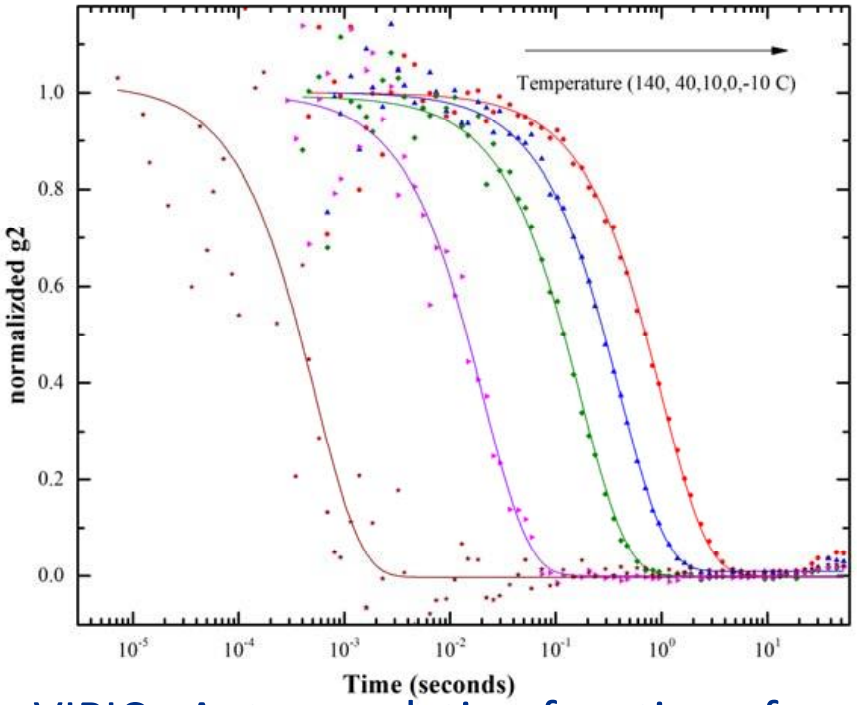
For the VIPIC x-ray imaging chip we were able to compare noise of the oxide-bonded pixels to the same chip with bump bonds. The noise in the oxide bonded pixels is almost a factor of two lower than the conventionally bump bonded parts due to lower capacitance.



More 3D Results



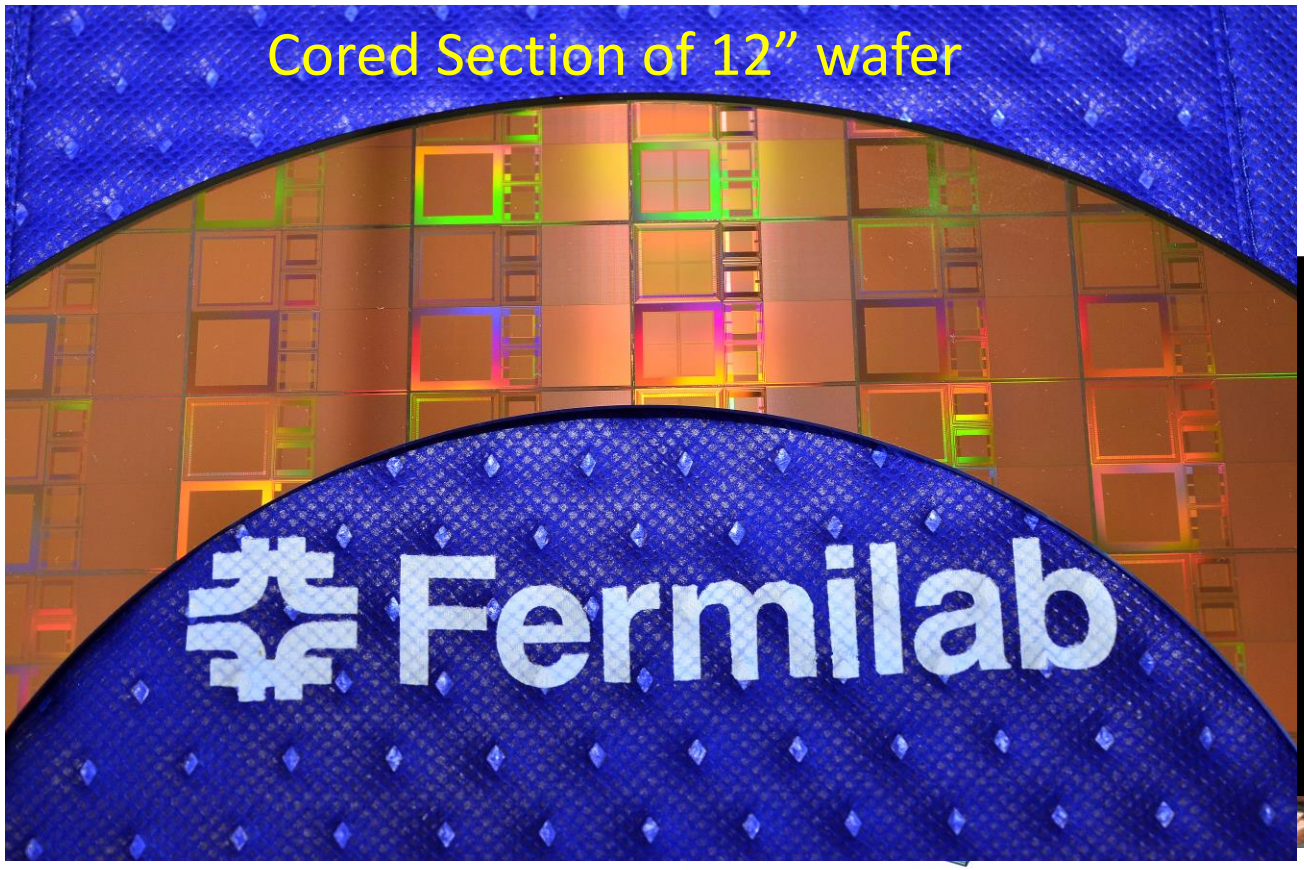
CD109 radiogram of tungsten mask

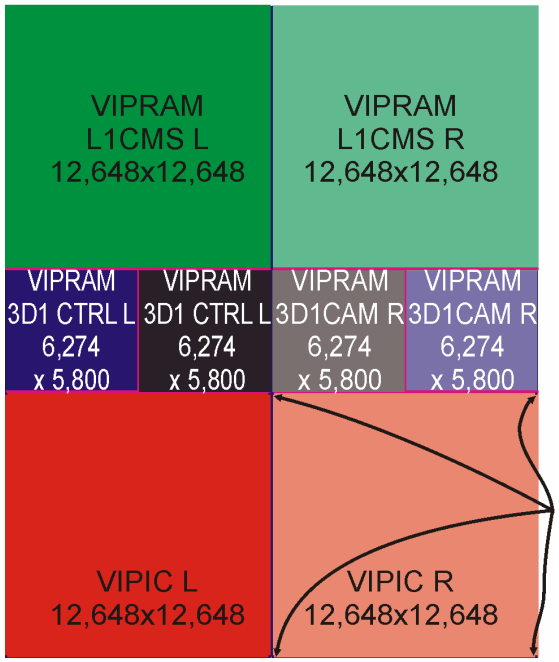


VIPIC - Autocorrelation function of polystyrene particles at Argonne APS

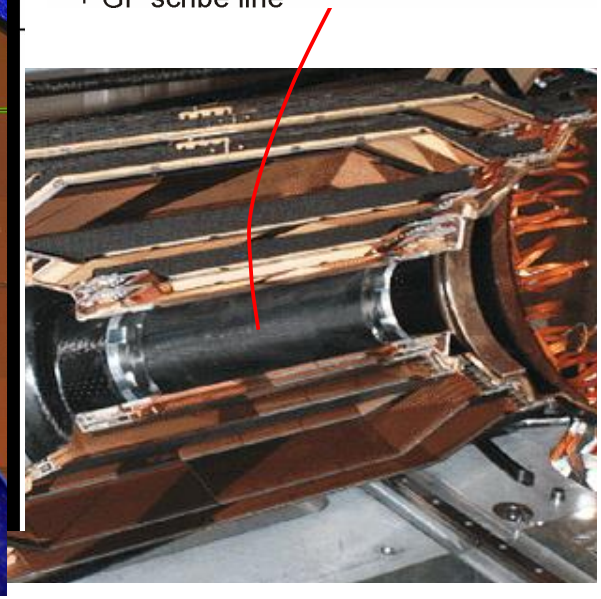
Next Steps

FNAL has been funded by BES to produce an second generation full sized VIPIC for x-ray imaging. The wafer will also include VIPRAM 3D track trigger associative memory chips for the CMS L1 Tracking trigger





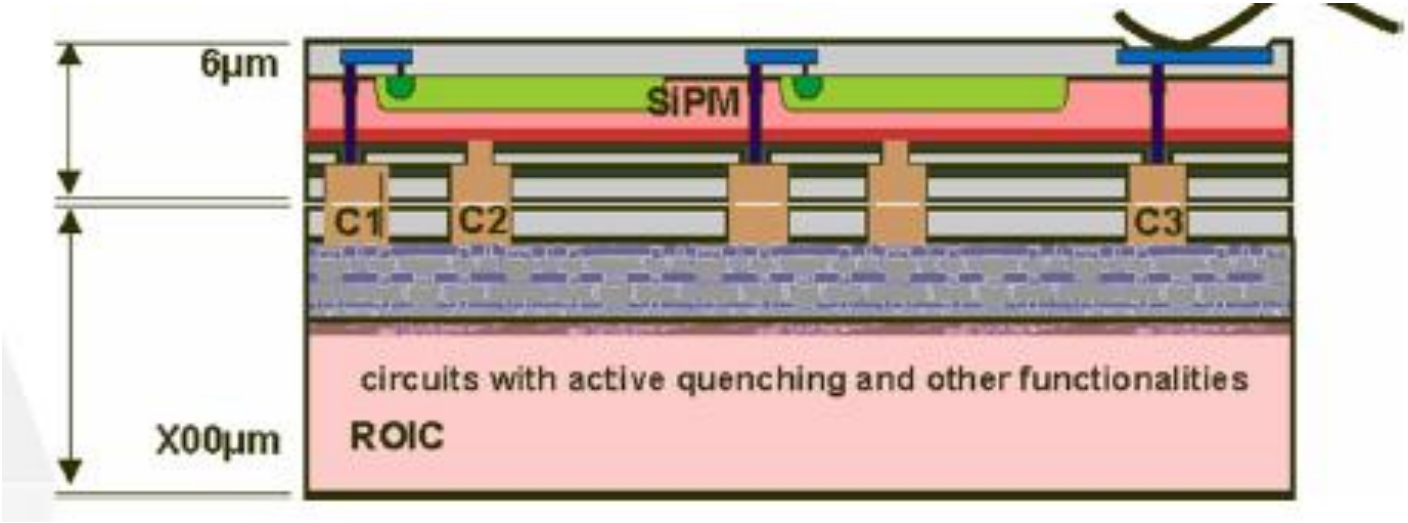
Fermi data = 25,396 um x 31,096 um
100um+22um+80um added from each side for: Tezzaron Scribe Line
+GF Crack Stop and Moisture Barrier
+ GF scribe line



Other possible applications - 3D SiPM

3D Integrate the SiPM with active quenching and digital readout

- Micropixel resolution, turn off noisy pixels
- Lower capacitance -> faster
- Active quenching -> Faster, less afterpulsing
- High fill factor
- Digital readout of a digital device…

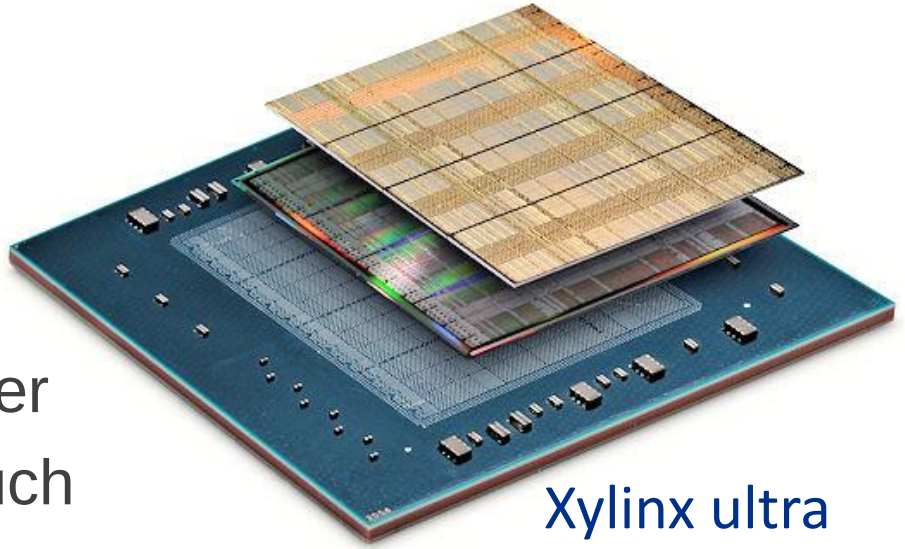


2.5D Assemblies

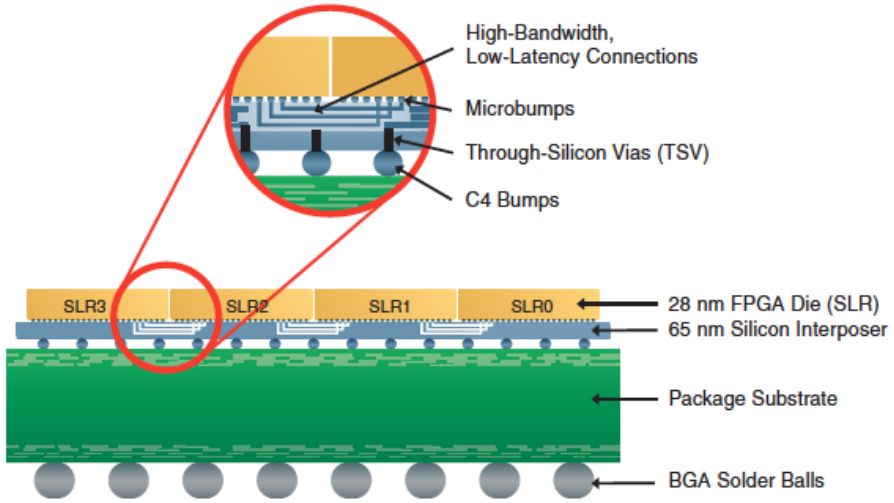
The commercial world is moving toward “2.5D” assemblies, using TSVs in a silicon or glass interposer

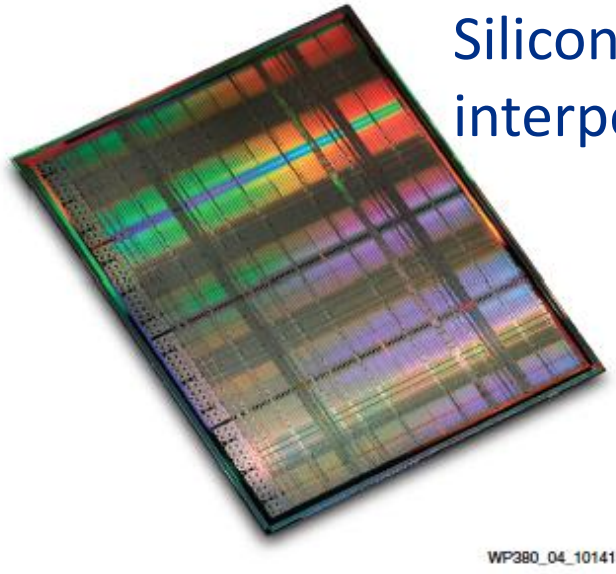
Higher speed assemblies, with much finer pitch (20x) than conventional PCBs.

Initial use on FPGAs



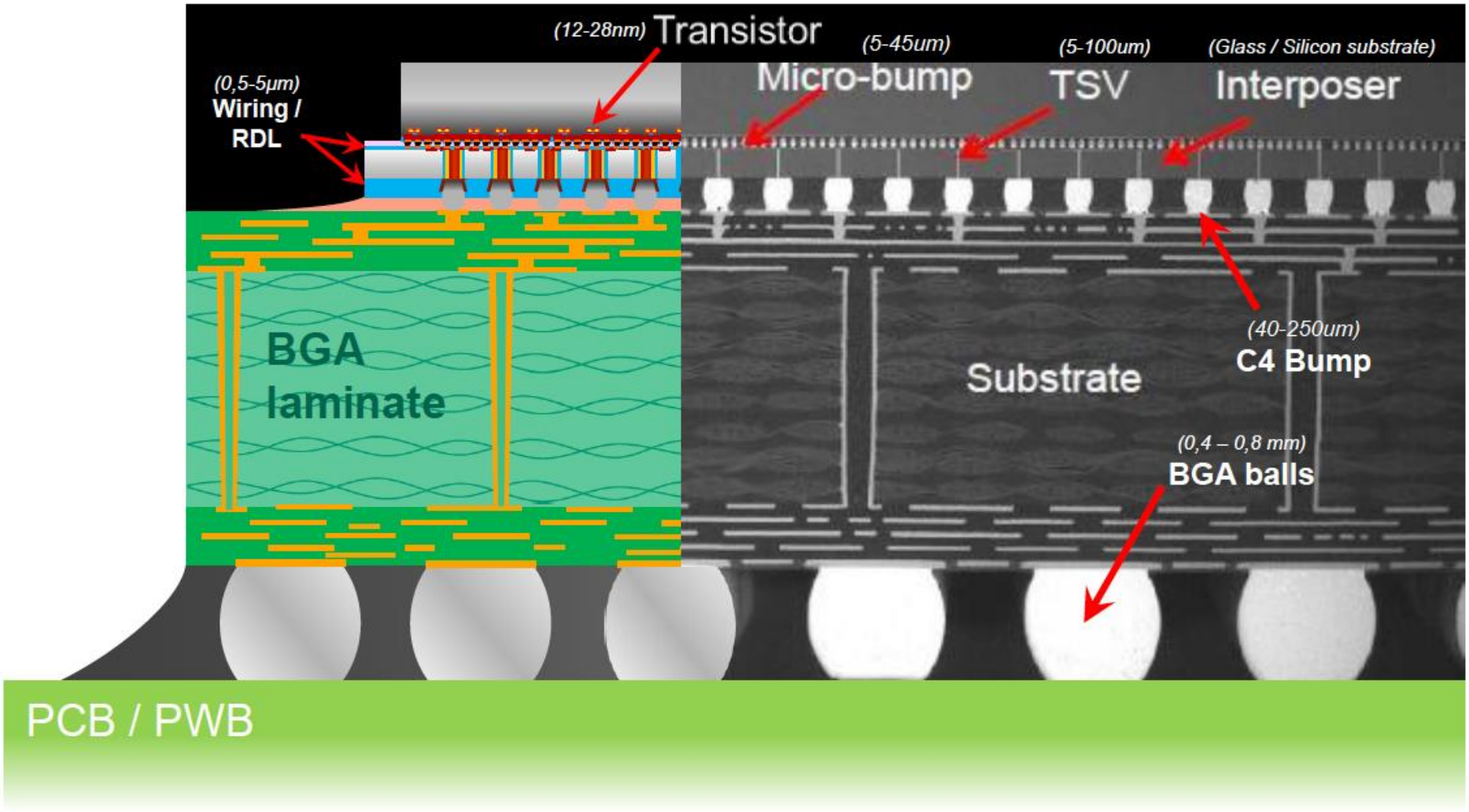
Xylinx ultra scale FPGA





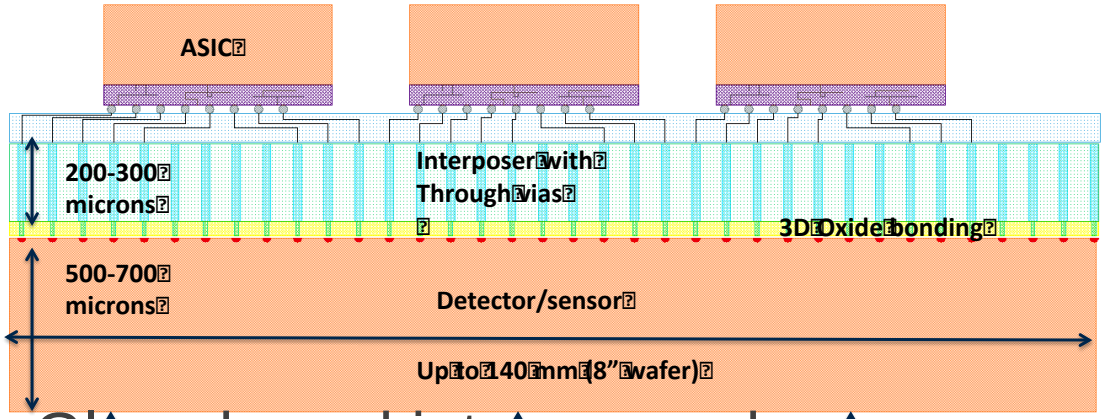
Silicon interposer

2.5D Interconnect Scales



Interposer based assemblies for tracking

Interposers can be used as pitch adapters to mate *large area* silicon sensors to readout ICs

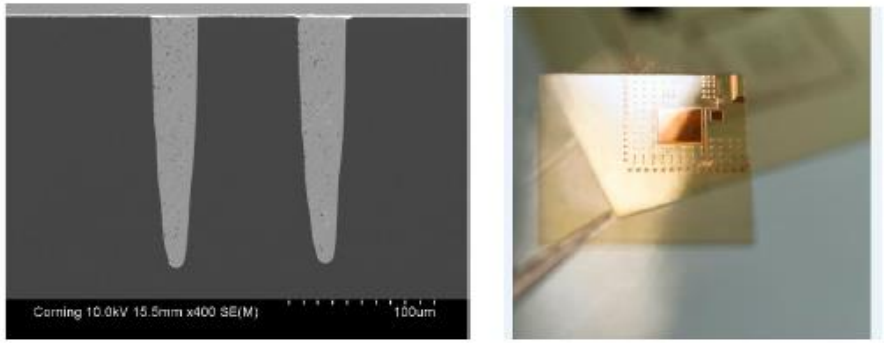


Fermilab design for FASTPAX X-ray imager

Glass-based interposers have low dielectric constant and can be fabricated in large panels. Lithography similar to silicon.

Can achieve 20 micron diameter

>10:1 aspect ratio



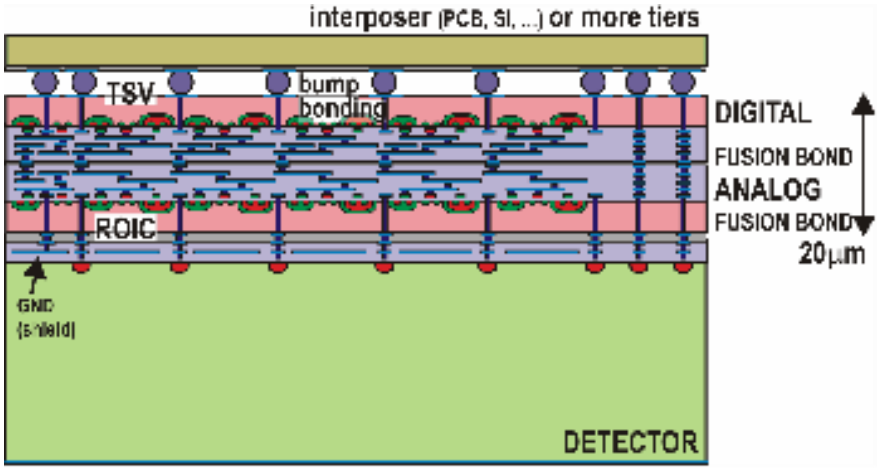
Cu filling performance with TGV substrate based on Corning fusion glass (top diameter ~ 30 μm, total depth ~ 180 μm)

Combining the two 3Ds

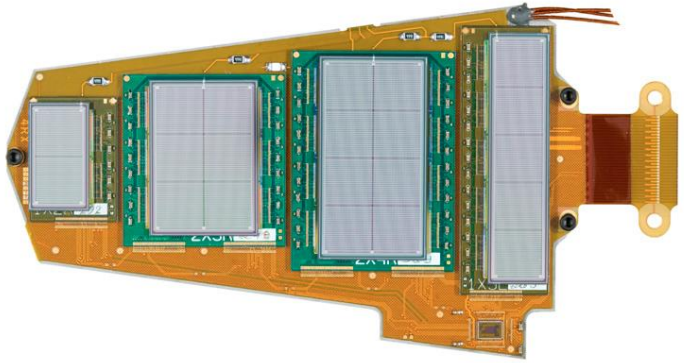
The goal is low cost, large area, thin, pixelated sensor planes with no dead regions.

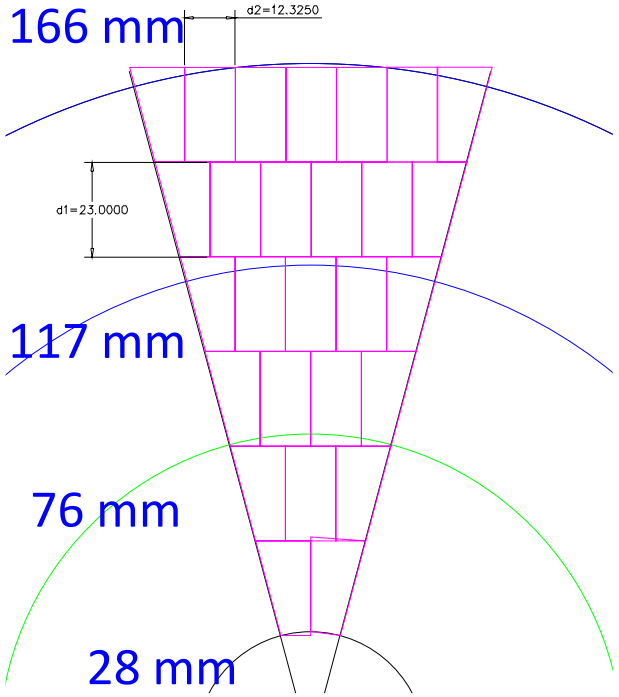
The key is to decouple bonding and array yields

- 3D provides backside interconnect to eliminate peripheral bond connections
- Sensors can be processed to have “active edges” using deep reactive ion etch so assemblies can be tiled.



CMS FPIX Plaquette



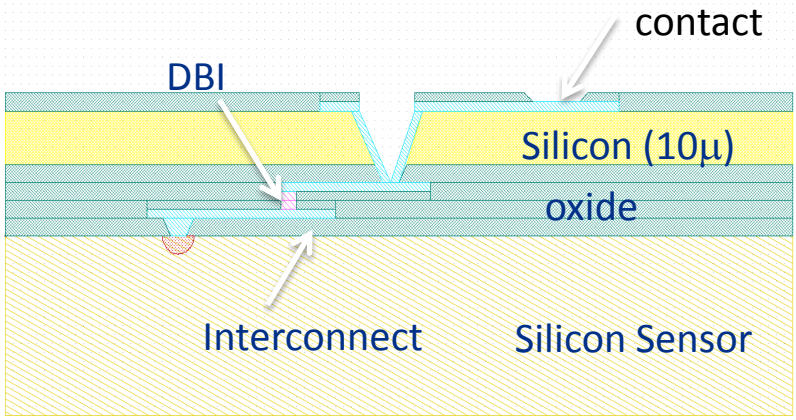


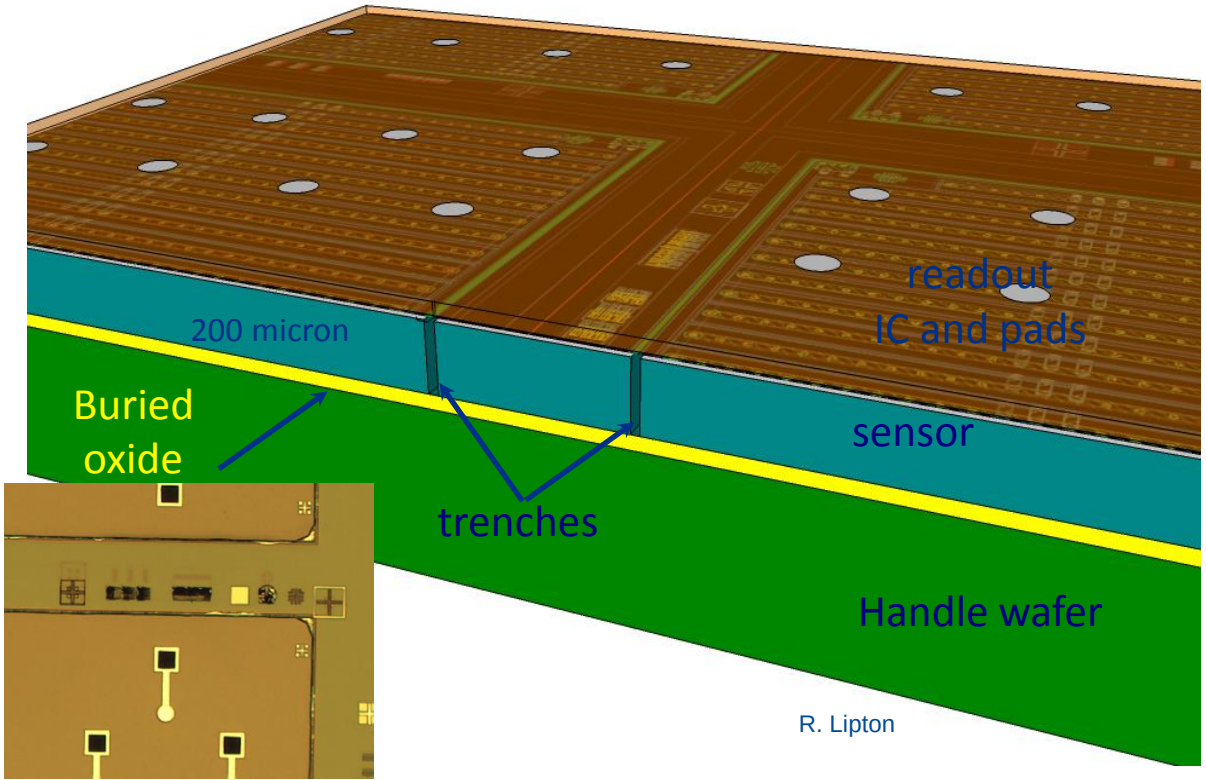
SiD (ILC) Outer pixel disk

How to build large area intelligent trackers?

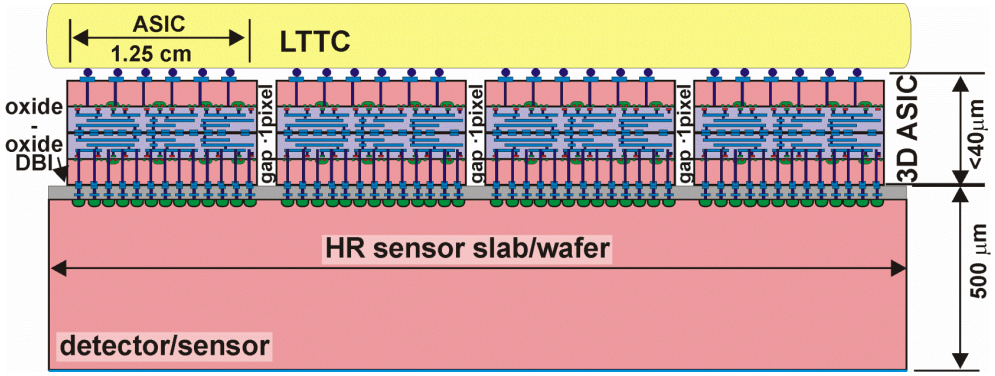
Combine active edge technology with 3D electronics and oxide bonding with through-silicon interconnect to produce fully active tiles.

- These tiles can be used to build large area pixelated arrays with good yield and reasonable cost
- Tiles can populate complex shapes with optimal tiling and low dead area
- Only bump bonds are large pitch backside interconnects
- High density and geometrical flexibility



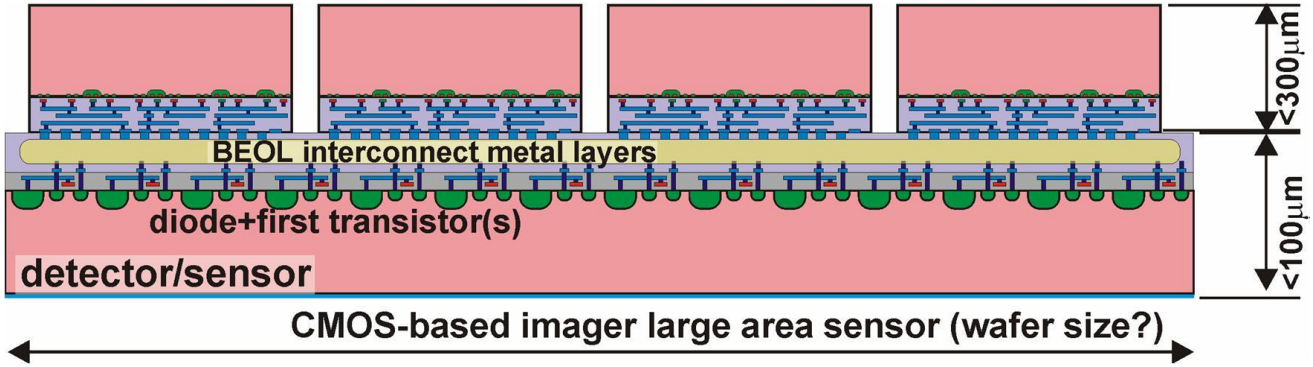


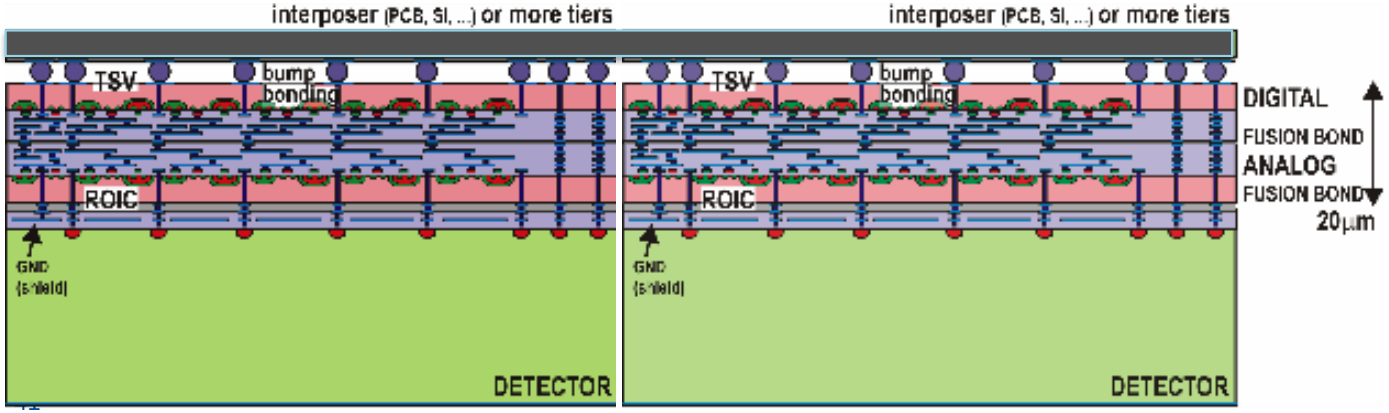
2.5/3D for Large area complex, pixelated tiled arrays



High resistivity Silicon sensor 3D integrated with wafer scale sensor (VIPIC)

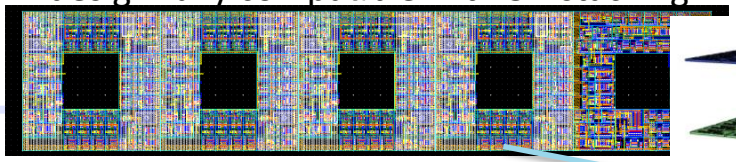
CMOS sensor 3D integrated with readout chips for very high dynamic range (FLORA)

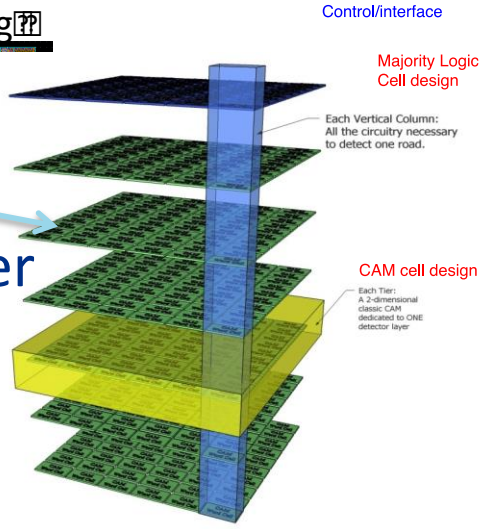




Single CMOS die 3D integrated with active edge sensors

“Killer” Applications

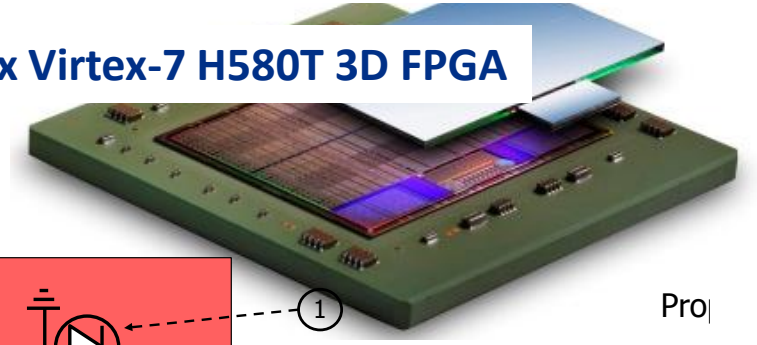




Each 3D layer processes a detector layer

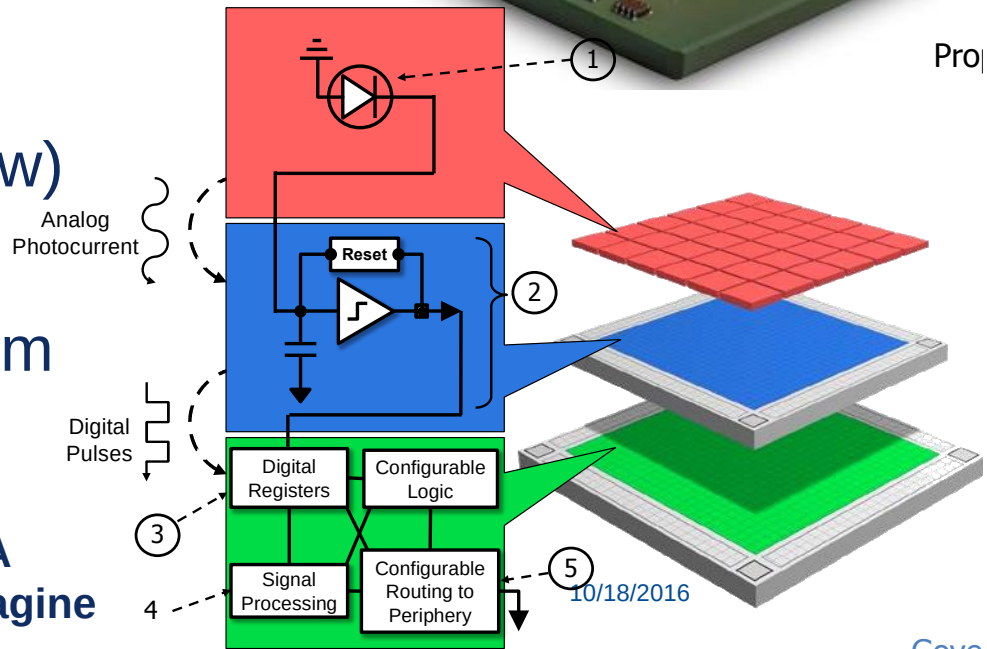
In Physics

- Large area tracking and imaging arrays with intelligent pixels and without dead regions (VIPIC-L, active edge integration)
- 3D associative memories for high speed correlations between detector layers



Commercial Thrusts

- Complex FPGA systems (now)
- Imaging systems
- Eventually - Integrated system processor/memory/IO on a heterogeneous die



DARPA REimiagine

Summary

Silicon technologies for HEP continue to offer opportunities for larger, faster, cheaper, more precise systems for trackers and calorimeters.

- Silicon-based fast tracker/time tagger systems could select vertices at HL-LHC to a few mm
- CMOS maps can provide cheaper, more precise Si trackers
- New forms of wafer-level (3D, 2.5D) interconnect can provide dense integration of sensors and readout with low mass
- Combining these technologies will enable large arrays of precise, smart, tiled sensors

Extras

The Tracking Detector Commandments

1. Thou shalt minimize mass
2. Thou shalt have high digital bandwidth
3. Thou shalt be radiation hard
4. Thou shalt not dissipate power
5. Thou shalt have complex functionality
6. Thou shalt maximize position resolution (minimize pitch)
7. Thou shalt minimize dead regions
8. Thou not covet thy neighbors signals
9. Thou shalt be affordable
10. Thou shalt have fast analog signal processing (396 ns -> 25ns -> 1-2 ns -> 100 ps)

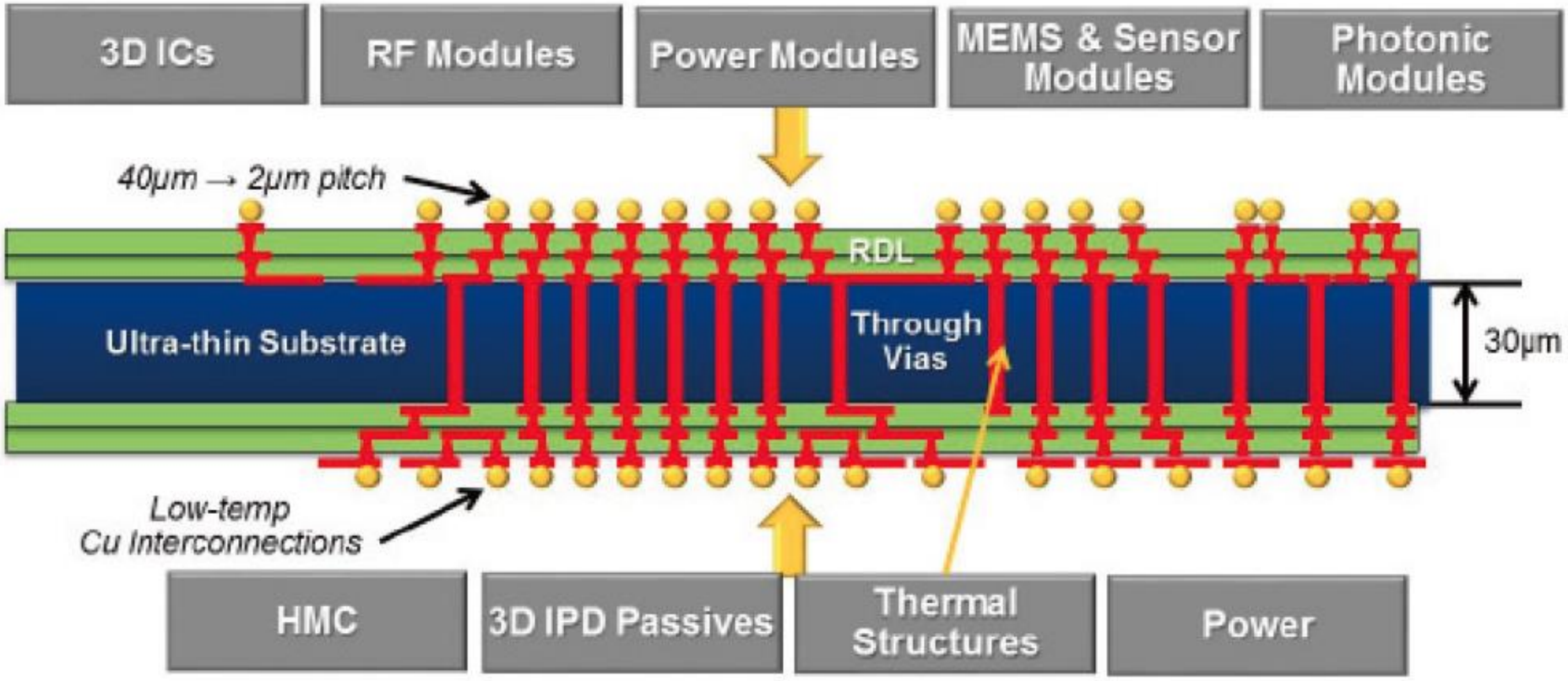
Obeying these “commandments” force us to push the technological and engineering envelope

Commercial Bonding Costs and Yields (old)

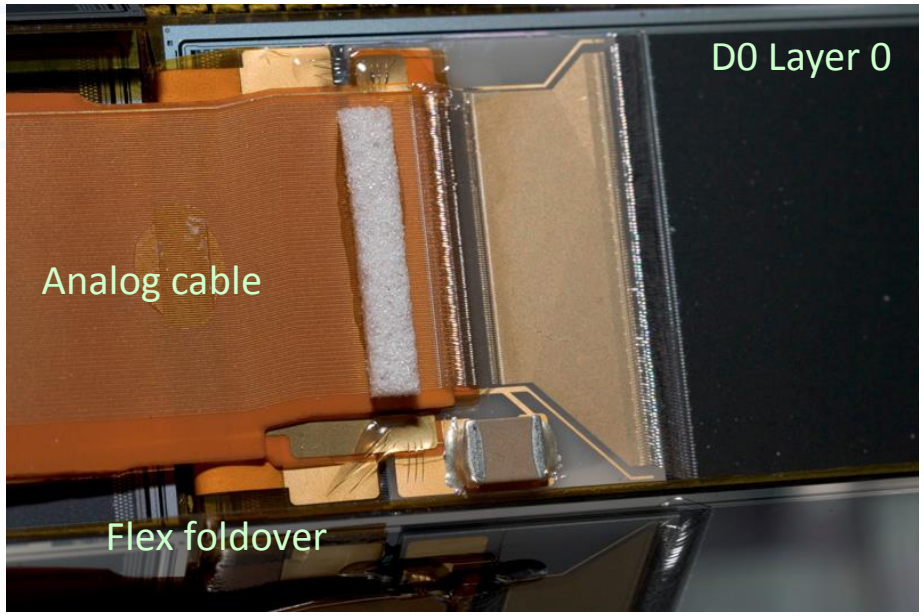
Component	Current or projected cost	Yield	Comment
Readout IC	\$8/cm^2[6]	65-70% [7]	Current 3D wafers and FEI4 prototype yield
Active Edge Sensors	\$53/cm^2	-	Current cost for prototype 150 mm wafers
Silicon Strip Sensors	\$10/cm^2	100%	CMS tracker costs
Bump bonding	\$213/cm^2	98%[8]	CMS forward pixel costs (2007) Yield ≡<20 bad bumps/chip
DBI bonding	<\$1/cm^2?	90%	Projected by Yole Development [9] for high volume production
Target Costs (2020s)	\$10/cm^2	90%	Assuming 200 mm sensor wafers and batch active edge process

Current and projected costs and yields for sensor/readout integration technologies

- Glass interposers



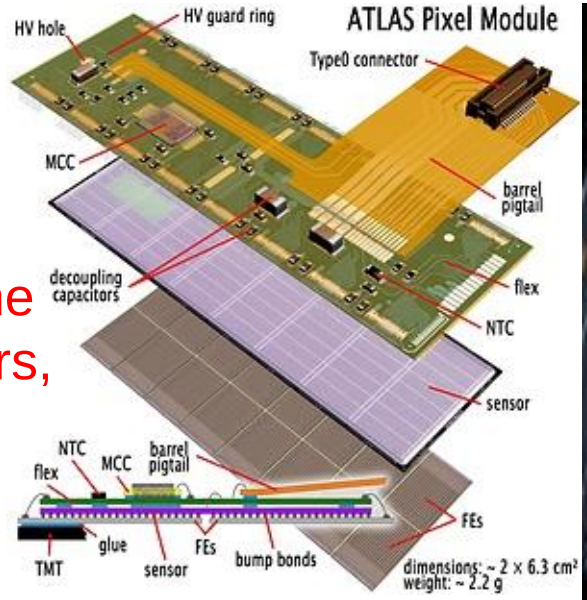
Silicon-based Tracking



Building these devices is essentially an electronics packaging problem, an unusual one…

- With billions of channels, 100's m^2 surface area
- With tbyte/sec bandwidth
- Cooled to -20 deg C
- With minimal mass
- Arranged to give us the information we need to do physics

Given the microscopic scale of the elements, the problems of sensors, readout, and interconnect are inexorably linked.

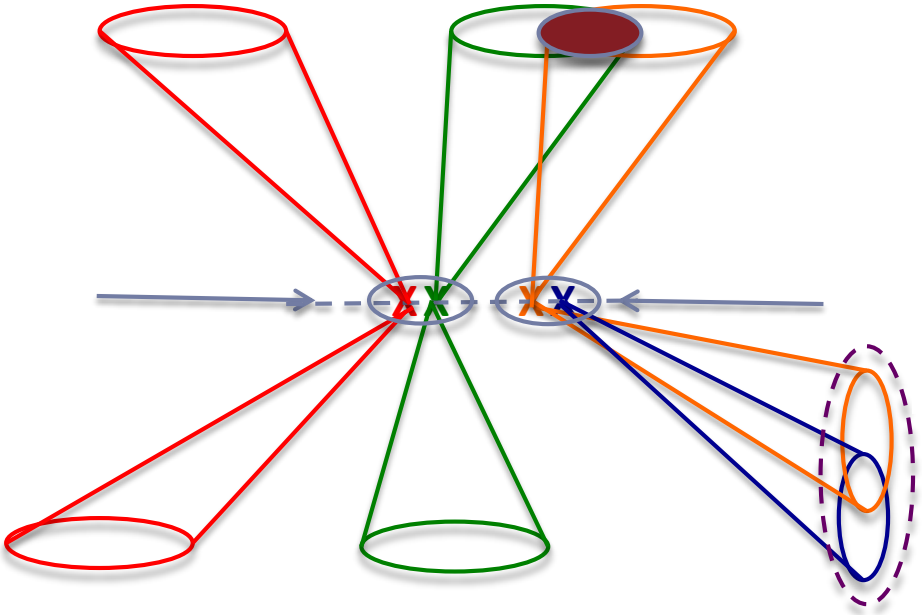


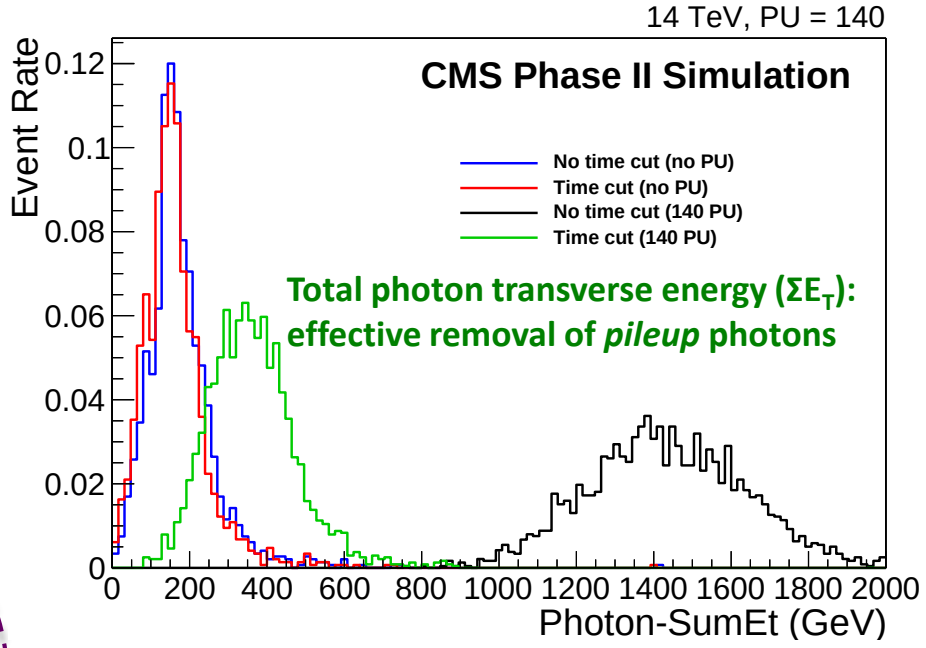
Timing For Pileup Reduction

High Luminosity LHC Experiments Workshop - 2014

Tommaso Tabarelli de Fatis

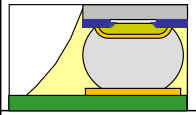
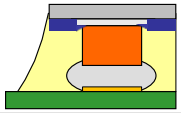
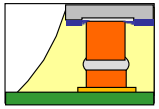
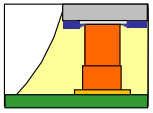
Extra energy in jets / isolation cones from overlap of (neutral) particles





Merged jets from spatially unresolved vertices

- With timing information for photons and charged tracks (vertex time):
  - Correct association of photons to jets
  - Improved jet definition / Identification of merged jets
  - Track / vertex compatibility

Bonding Method	C4 FC (Controlled Collapse Chip Connect)	C2 FC (Chip Connect)	Thermo Compression-Local Reflow Flip Chip	Thermo Compression Flip Chip
Schematic Diagram				
Major Bump Pitch Range at Application	> 130 um	140 um ~ 60 um	80 um ~ 20 um	< 30 um
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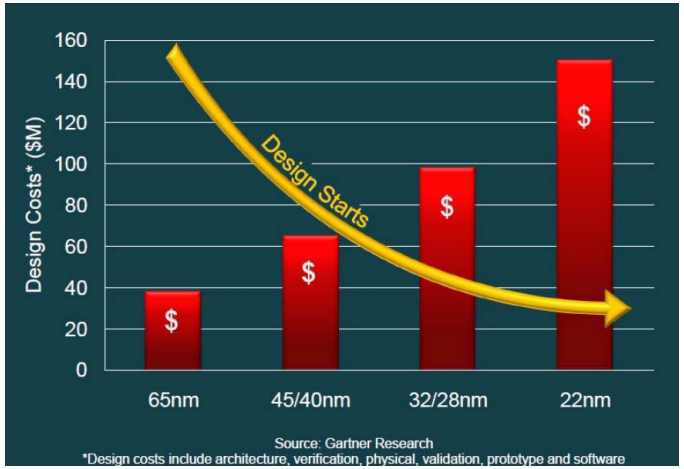
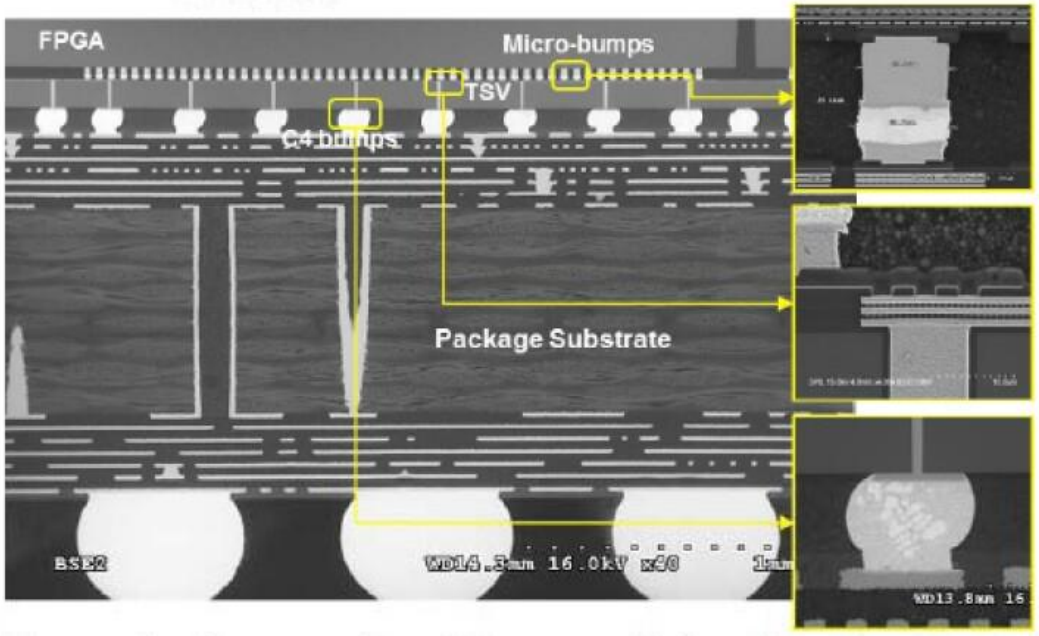
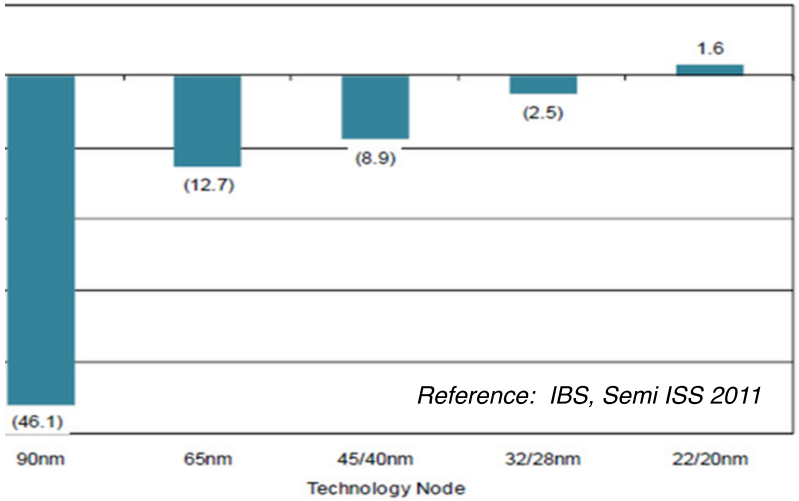
Bump Metallurgy	Solder (SnAg or SnAgCu)	Cu + Solder (SnAg or Sn)	Cu + Solder (SnAg or Sn)	Cu

Design Cost by Node



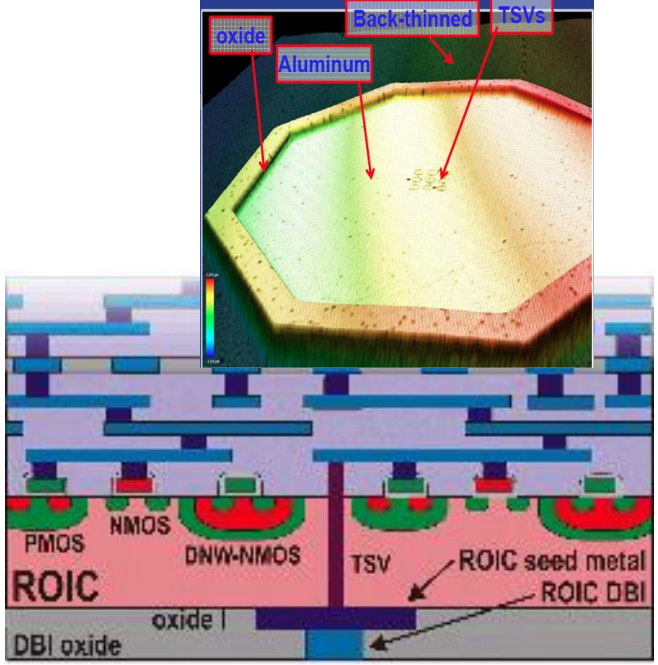


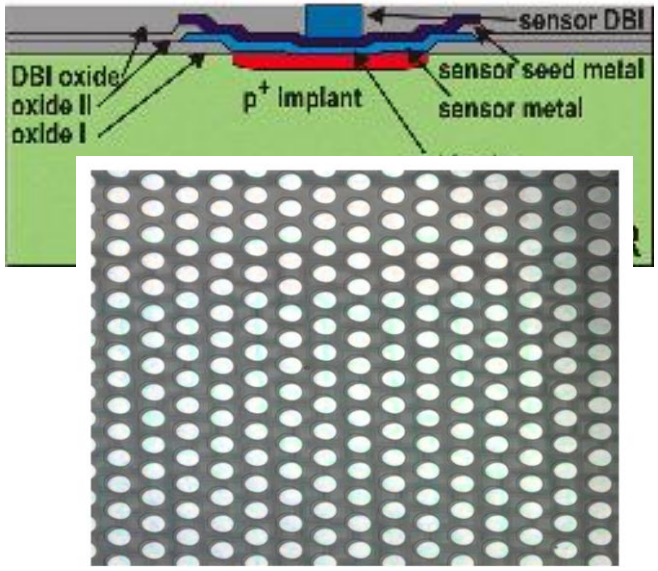
: Limitations on Scaling Below 22nm



Sensor Oxide Bonding

- A promising fine pitch bonding technology the direct bond interconnect (DBI) oxide bond process from Ziptronix
  - No bump bonds – planar resulting wafer
  - Very fine pitch - 4 microns used for 3D Tezzaron wafers
  - Mechanical strength enables aggressive post-bond thinning
  - Uses standard IC processes - CMP and metalization
  - Can withstand high temperatures
- Wafer-wafer bond can be reworkable
- In principal can be low cost





4 micron pitch

Hierarchy of interconnect

Cables ~ mm

- PC Board ~ 500 micron
  - Bump/wire bonds ~ 100's of micron
    - C4 bumps ~ 100 micron
      - Micro-bumps ~ 10-20 micron
        - 3D Interconnect ~ 2-5 micron

Chamber Type	Accuracy (rms)	Resolution Time	Dead Time
Bubble	± 75μ	≈ 1 ms	≈1/20 s[a]
Streamer	±300μ	≈ 2 μs	≈100 ms
Optical spark	±200μ[b]	≈ 2 μs	≈ 10 ms
Magnetostrictive Spark	±500μ	≈ 2 μs	≈ 10 ms
Proportional	⩾±300μ[c,d]	≈50 ns	≈200 ns
Drift	±50 to 300μ	≈ 2 ns[e]	≈100 ns

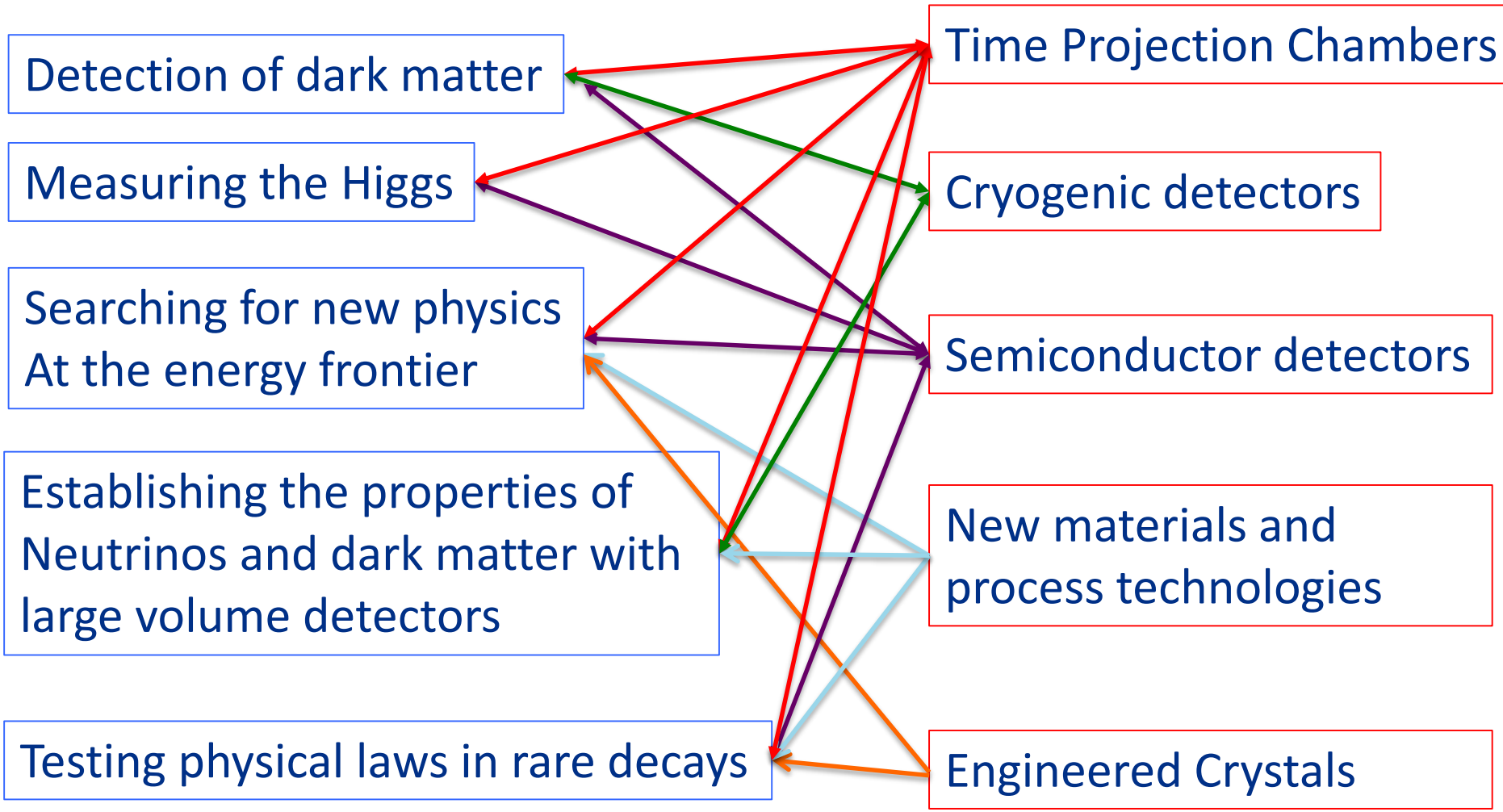
Review of Particle Properties (1978)

New

Detector Type	Intrinsinc Spatial Resolution (rms)	Time Resolution	Dead Time
Resistive plate chamber	$\lesssim$10 mm	1–2 ns	—
Streamer chamber	300 μm[a]	2 μs	100 ms
Liquid argon drift [7]	~175–450 μm	~ 200 ns	~ 2 μs
Scintillation tracker	~100 μm	100 ps/n[b]	10 ns
Bubble chamber	10–150 μm	1 ms	50 ms[c]
Proportional chamber	50–100 μm[d]	2 ns	20-200 ns
Drift chamber	50–100 μm	2 ns[e]	20-100 ns
Micro-pattern gas detectors	30–40 μm	< 10 ns	10-100 ns
Silicon strip	pitch/(3 to 7)[f]	few ns[g]	$\lesssim$50 ns[g]
Silicon pixel	$\lesssim$10 μm	few ns[g]	$\lesssim$50 ns[g]
Emulsion	1 μm	—	—

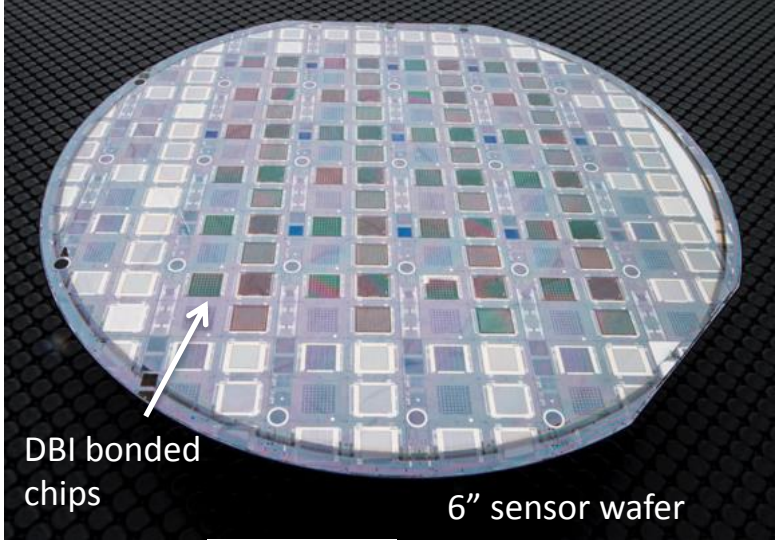
Review of Particle Properties (2011)

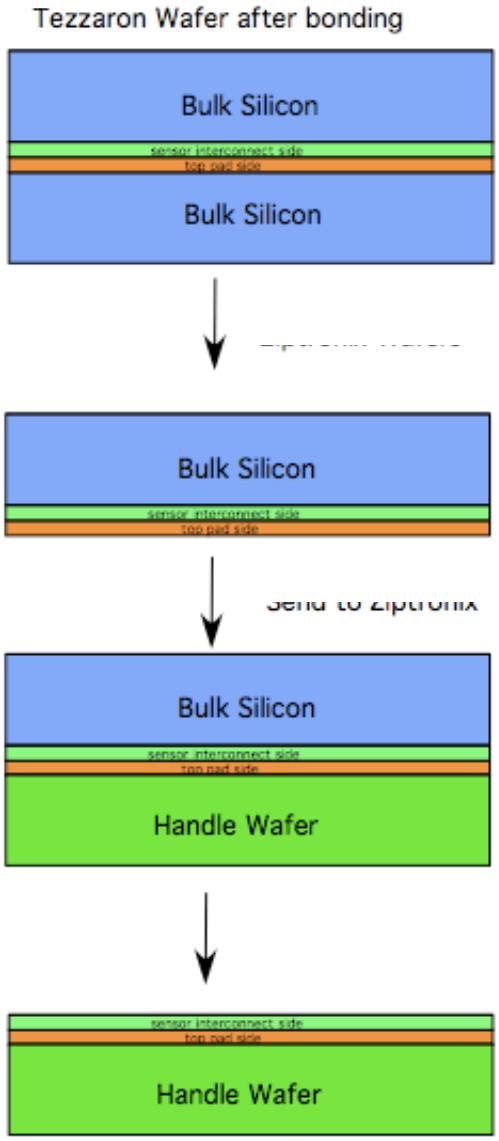
Technologies across boundaries



Chip-to-Wafer bond

DBI bonding of ROICs (VICTR, VIPIC, VIP) to BNL sensor wafer



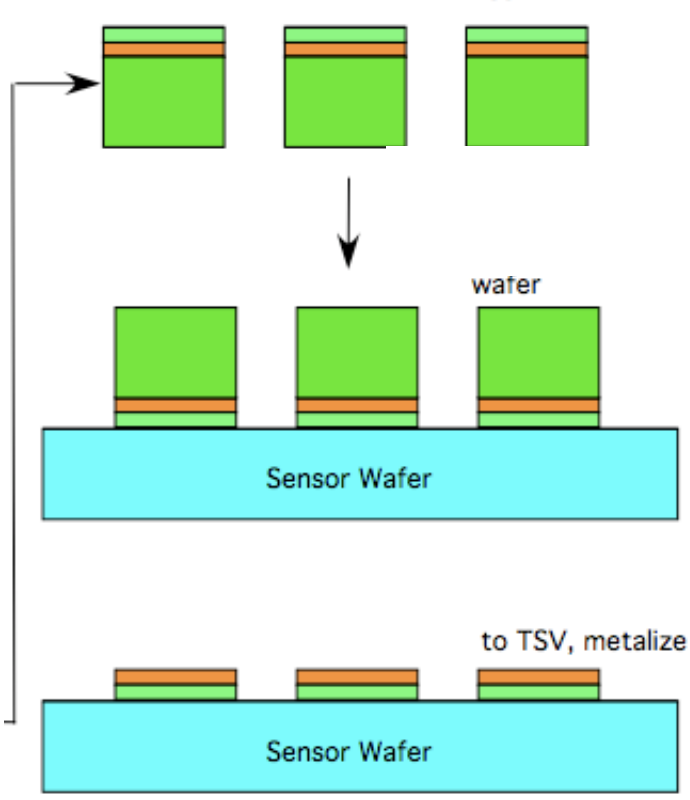


Wafer-wafer 3D Bond

Expose TSVs, pattern Top aluminum

Oxide bond Handle wafer

Expose sensor side TSVs, pattern DBI structures



Dice

DBI bond ROIC chips to sensor wafer (RT pick+Place)

Grind and etch to expose top connections

Future Costs (Ziptronix)

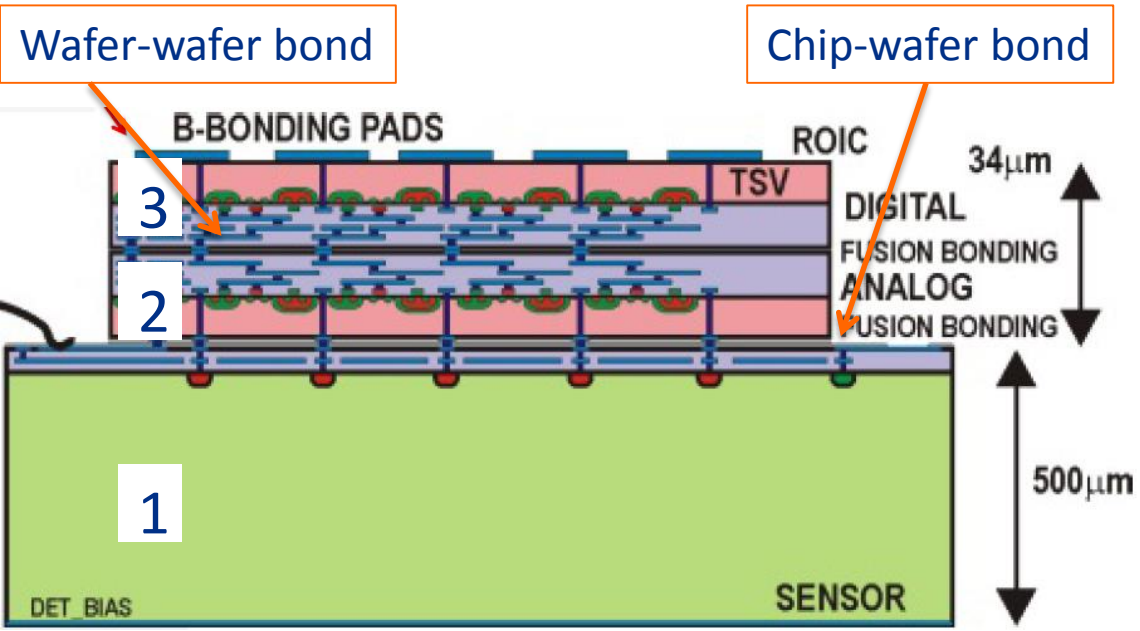
Stacking Technology	"per pixel" Interconnect Limit	"per pixel" Interconnect Limit Driver	ROM Cost/ Wafer	Cost Driver(s)
Bump Bonding	~ 10 um	Non-planar bumps	< $200	Bump formation
Adhesive + TSV	~ 10 um	TSV	< $400	TSV
Direct Bond + TSV	~ 10 um	TSV	< $400	TSV
Copper Thermo-Compression	~ 3 um	Bond Area	< $150	Bond Cycle Metallization
Adhesive Hybrid Bonding	~ 2 um	Bond Distortion	< $150	Bond Cycle Metallization
DBI® Hybrid Bonding	< 1 um	Wafer Align/ Place	< $100	Metallization

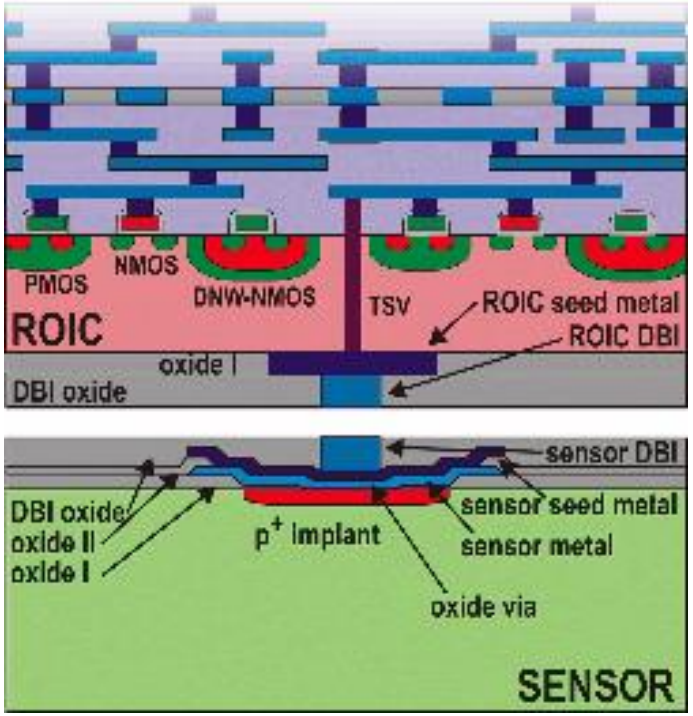
Of all the stacking technologies, DBI® Hybrid Bonding demonstrates the best pitch scaling, 3D interconnectivity, and cost. (Source: Ziptronix)

The company just announced an industry-first in **demonstrating a 3 layer stacked image sensor device** in collaboration with Fermilab National Laboratory, to **improve the performance of high-end 3D sensor arrays**, which are used for particle detection in large-scale particle physics and x-ray imaging experiments.

Sensor Integration –Three tier devices

- We then chip-to-wafer oxide (DBI) bonded 3D chips to BNL sensors to form three-tier integrated sensor/electronics assemblies
  - VIP(ILC), VICTR(CMS), and VIPIC(X-Ray) assemblies





Hybrid Bonding

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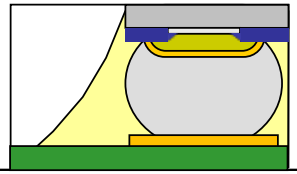
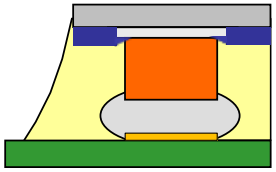
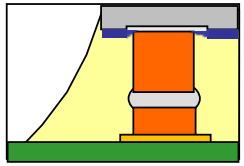
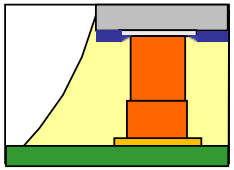
Schematic Diagram				
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Bonding Method	Conventional Reflow	Reflow with Cu pillar	Thermal Compression with Cu pillar	Thermal Compression
Bump Metallurgy	Solder (SnAg or SnAgCu)	Cu + Solder (SnAg or Sn)	Cu + Solder (SnAg or Sn) Cap	Cu
Bump Collapse	Yes	No	No	No
Underfill Method	- Capillary - No flow	- Capillary - No flow - Wafer Level	- No flow - Wafer Level	- No flow - Wafer Level