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FCP130, IFCP65 and incorporation in RD53A

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Basic CMS HL-LHC assumptions*

*RD 53 Collaboration

- Cluster size: ~4 (average)
  - Cluster size and shape varies significantly over pixel detector:
    - Middle barrel, End barrel, End cap disks, tracks from collision point, Machine background/halo, loopers, etc.
- Rate: Worst case HL-LHC (layer locations as in Phase1)
  - **Layer 1** (3.0cm): ~500MHz/cm^2 tracks -> **~2GHz/cm^2 hits**
  - Layer2 (6.8cm): **~½** of layer 1
  - Layer3 (10.2cm): ~½ of layer 2 -> **~¼** of layer 1
  - **Layer4** 16.0cm) : ~½ of layer 3 -> **~1/10 of layer 1**
    (50MHz/cm^2 tracks, 200MHz/cm^2 hits)
  - End-caps ?
- Pixel chip: ~6.5 cm^2
- Pixel size: ~25x100um = 2500um^2
  - Or 50um x 50um (same area but square)
  - (50um x 100um if more area required per pixel, No major effect on readout rate)
- Pixel regions: 4 x 4 or 2 x 2
- Pixels per chip: ~256k
- Tracks/hits per chip per Bx:
  - **Layer 1**: 50KHz/pixel, 75 tracks/IC/Bx, **300hits/IC/Bx**
  - **Layer 4**: 5KHz/pixel, 7.5 tracks/IC/Bx, **30hits/IC/Bx**
- L1 Trigger: 1MHz, 20us (10us) now baseline for all new Phase2 detectors

Preliminary specification*

Specification	
Pixel size	25x100um^2 ; 30x100um^2 ; 50x50um^2
Sensor	2D, 3D, Diamond, MAPS ?
Chip size	> 2cm x 2cm
Transistors	**~1G**
Hit rate	1-2 GHz/cm^2
Hit memory per chip	**>16Mb**
Trigger rate	1MHz (CMS)
Trigger latency	6 - 20us
Readout rate	**~5Gb/s per chip (inner)**
Radiation	**1Grad**
Technology	**65nm ?**
Architecture	**Digital**
Power	¼ - ½ W/cm^2 ?

RD53:

- Common technology platform for 65nm pixel chips
- Working groups: Radiation qualification, Analog design, Basic building blocks (IP), Simulation and verification framework, top level, etc.
- R&D collaboration with clearly defined goals: Project.
- A common or two different pixels chips can be made for CMS & ATLAS

*RD 53 Collaboration -Borrowed from J.Christiansen

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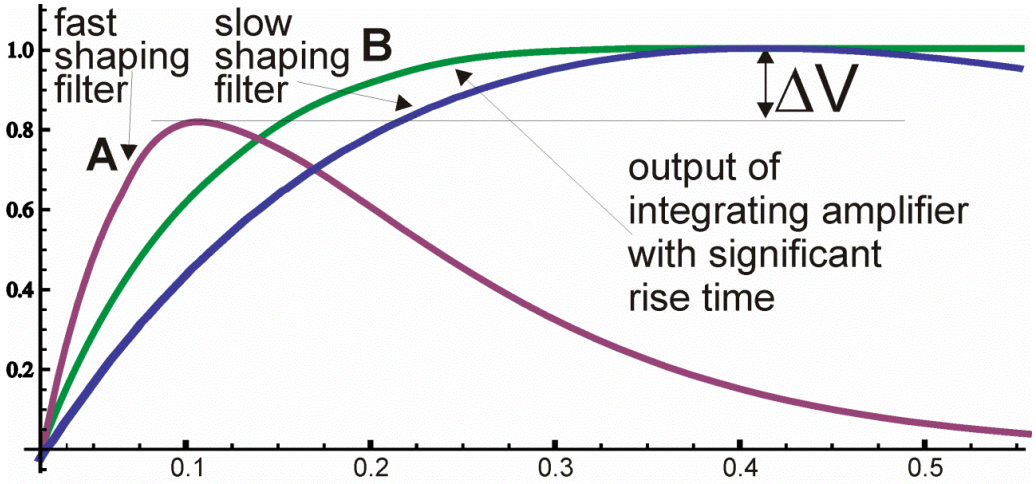
Fermi CMS Pixels (FCP130)

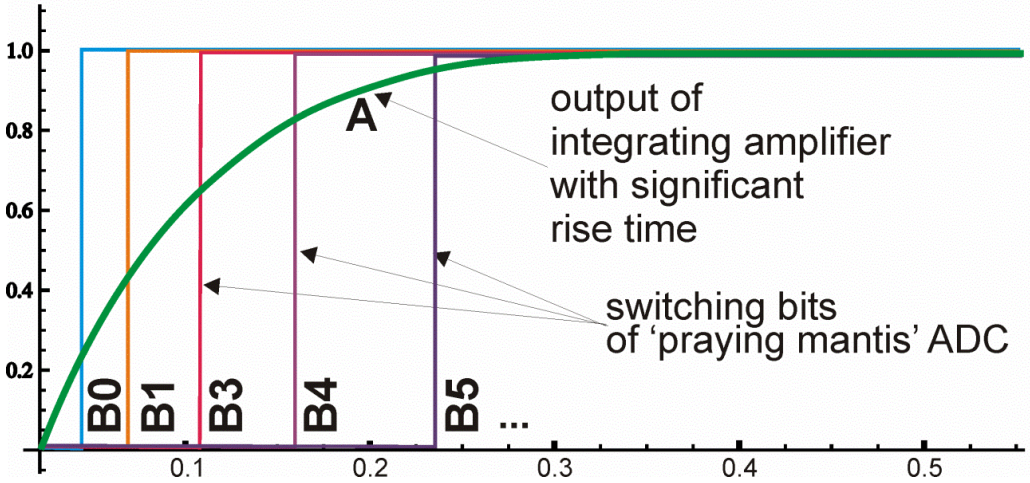
Fermi CMS Pixel (FCP130)- Design of a test CMS pixels chip

- **Test platform of Synchronous frontend with an Asynchronous output data flow**
- **Technology platform: GF130nm – Preliminary architectural investigation before 65nm.**
- ASIC size: 5.5 mm x 8.5 mm
- Pixel size: 30 µm x 100 µm (Analog part: 20 µm x 100 µm; Digital Part: 10 µm x 100 µm)
- Rows x Columns: 48 x 160 (4 columns are grouped to create a superColumn (192 pixels))
- Each ASIC has 40 super columns.
- Analog Pixel options:
  - **1) Preamplifier + 3 bit Flash ADC + hit comparator (independent of ADC to get hit in the processing – to be reviewed on final realizations)**
  - 2) Preamplifier + 3 bit ADC based on asynchronous conversion using in-pixel oscillator triggered by signal (more power consumption but more compact + perspectives for other uses)
- Digital Pixel: 8:3 bit encoder, hit processor, priority encoder for data sparsification
- End of column: FIFO to daisy chain then asynchronous data transfer through CONFLUX

Basic concepts: Synchronous front-end ?

✓ The Analog Front-End includes a **charge preamplifier** and **synchronous comparators** used for A-to-D conversion **within one BXClk period**





Fast shaping may worsen S/N due to ballistic deficit

Conversion begins as soon as charge starts being integrated and continues until signal reaches maximum or conversion time is over.

→ **no dead time for conversion**

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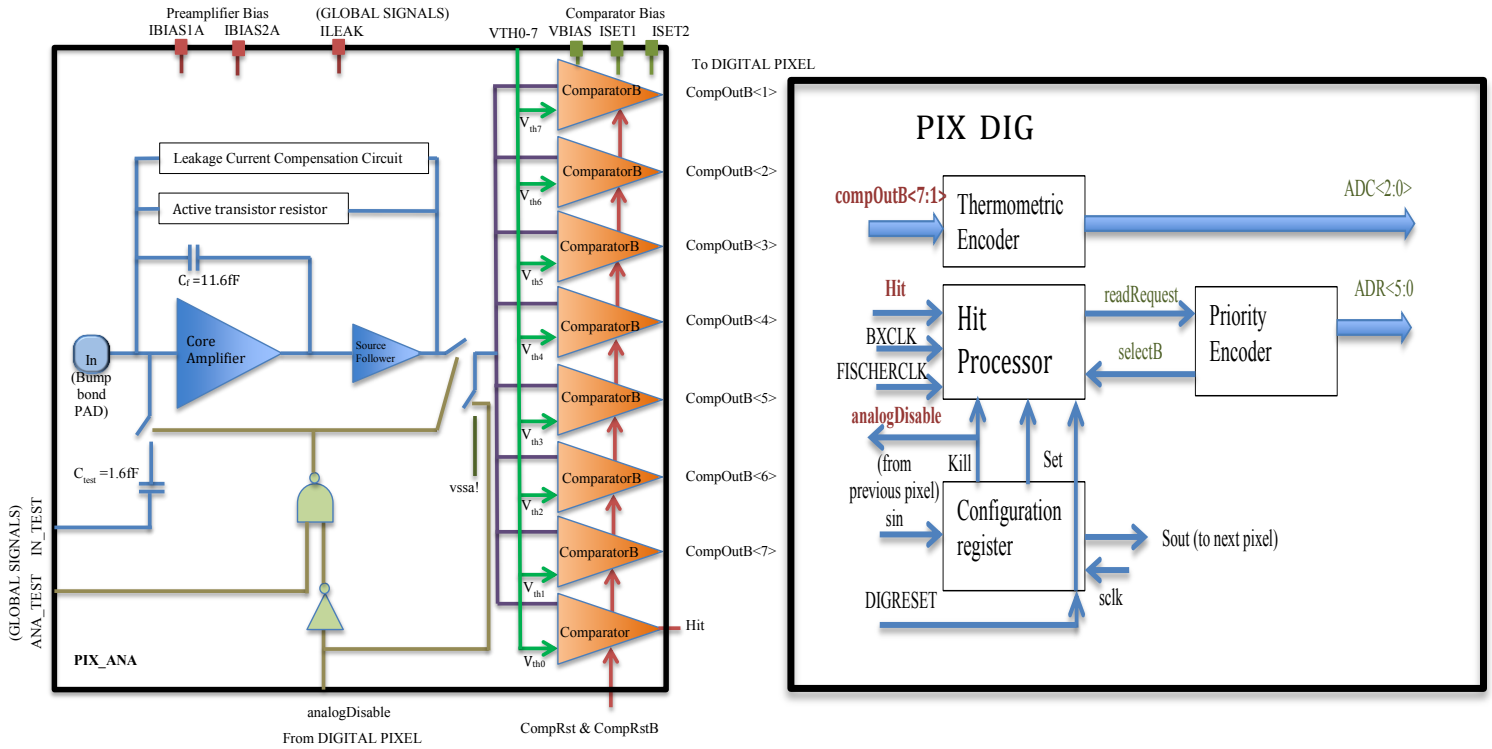
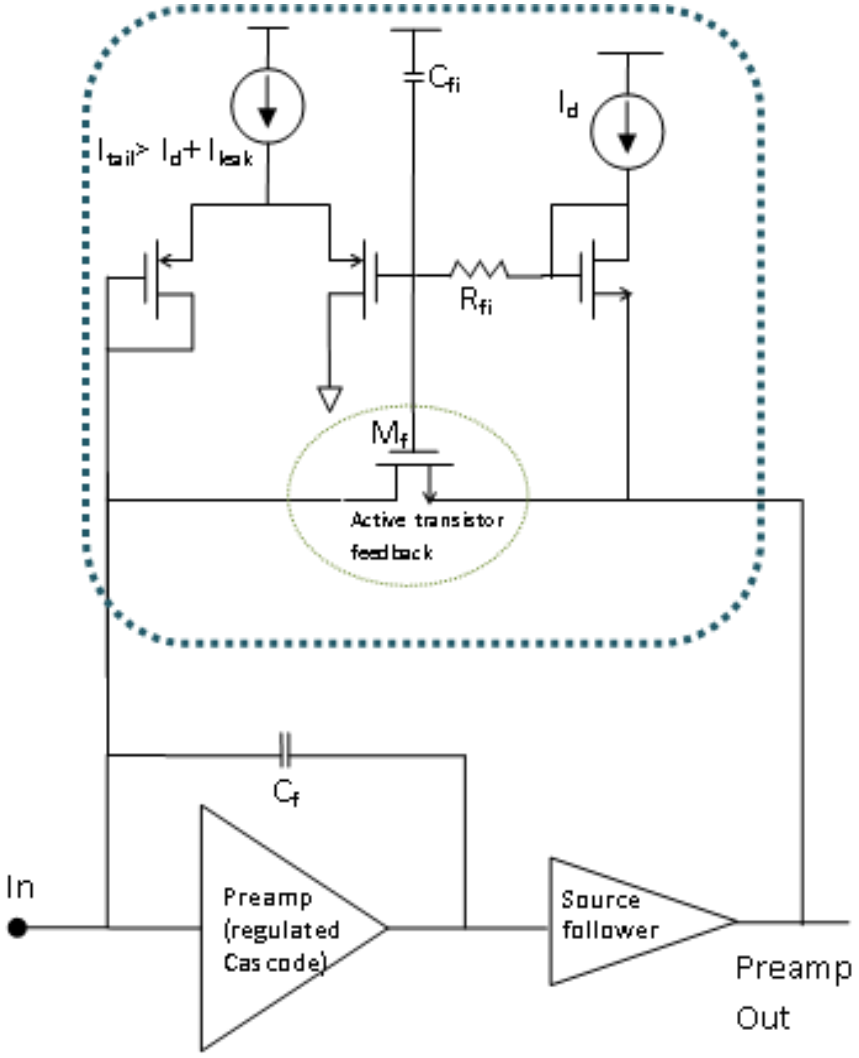
Pixel Architecture



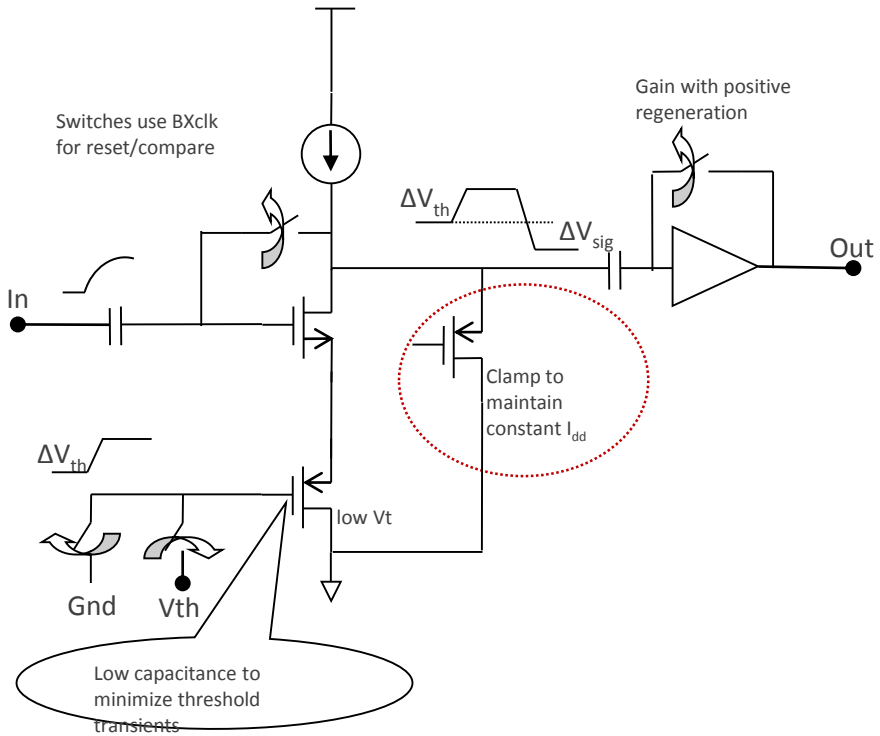
- Synchronous front-end (utilize BXClk time structure)
- No continuous time filtering
- Insensitivity to absolute design parameters (e.g. shaping time)
- Increased noise immunity – digital conversion immediately after preamplifier
- Data Conversion within 1 BXClk cycle
- Processing insensitive to pileups

Preamplifier

- Dynamic range 0.25fC – 2.5fC
- Power Consumption : 5µA x 1.5V
- Regulated Cascode design
- Feedback capacitor : 11.58fF
- Active transistor resistor feedback
  - Large signals behaves as a constant current source
  - Small signals Rf = 1/gm
- Leakage current compensation upto 5nA
- AC coupled to comparator
- Preamp, return to baseline is longer than 200ns, but only has to prevent output level from saturating



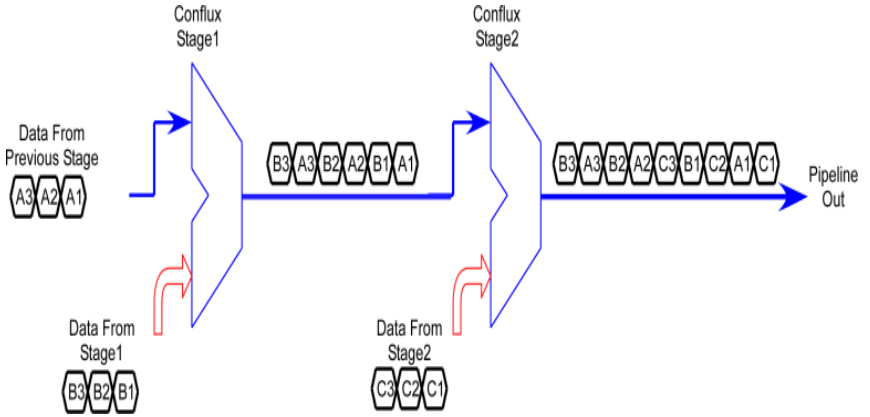
Comparator

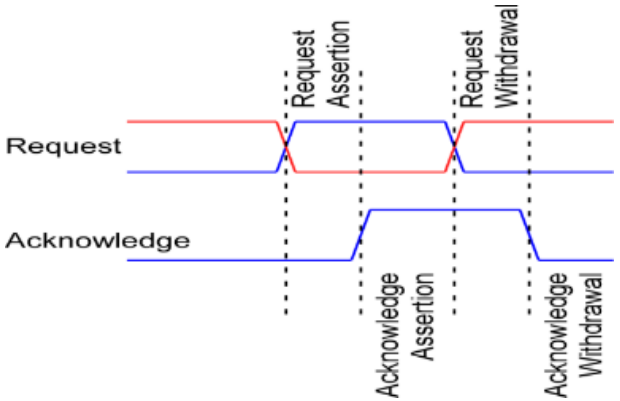


- Compact, single-ended architecture.
- Auto-zeroed, “lurk-trigger-done” – praying mantis.
- Correlated double sampling
- Does not require trimming DACs
- 12.5ns reset phase; 12.5ns active comparison.
- Low-power, fast, insensitive to corners
- 2 stage design with additional gain and positive regeneration in 2nd stage.
- Require distribution of BXclk across a large chip

Conflux: Asynchronous Data transfer

- Conflux is based on a classic 4-phased bundled-data asynchronous protocol (Request Assertion → Acknowledge Assertion → Request Withdrawal → Acknowledge Withdrawal).
- Conflux blocks across several chips and/or boards can be chained together and no clock is necessary.
- No global control signals are necessary either.
- Each link in the chain passes on data from its predecessor to its successor and adds its own data to the stream.
- Each Conflux readout can be seen as an asynchronous 2-to-1 multiplexor for Time Division Multiplexing (TDM).





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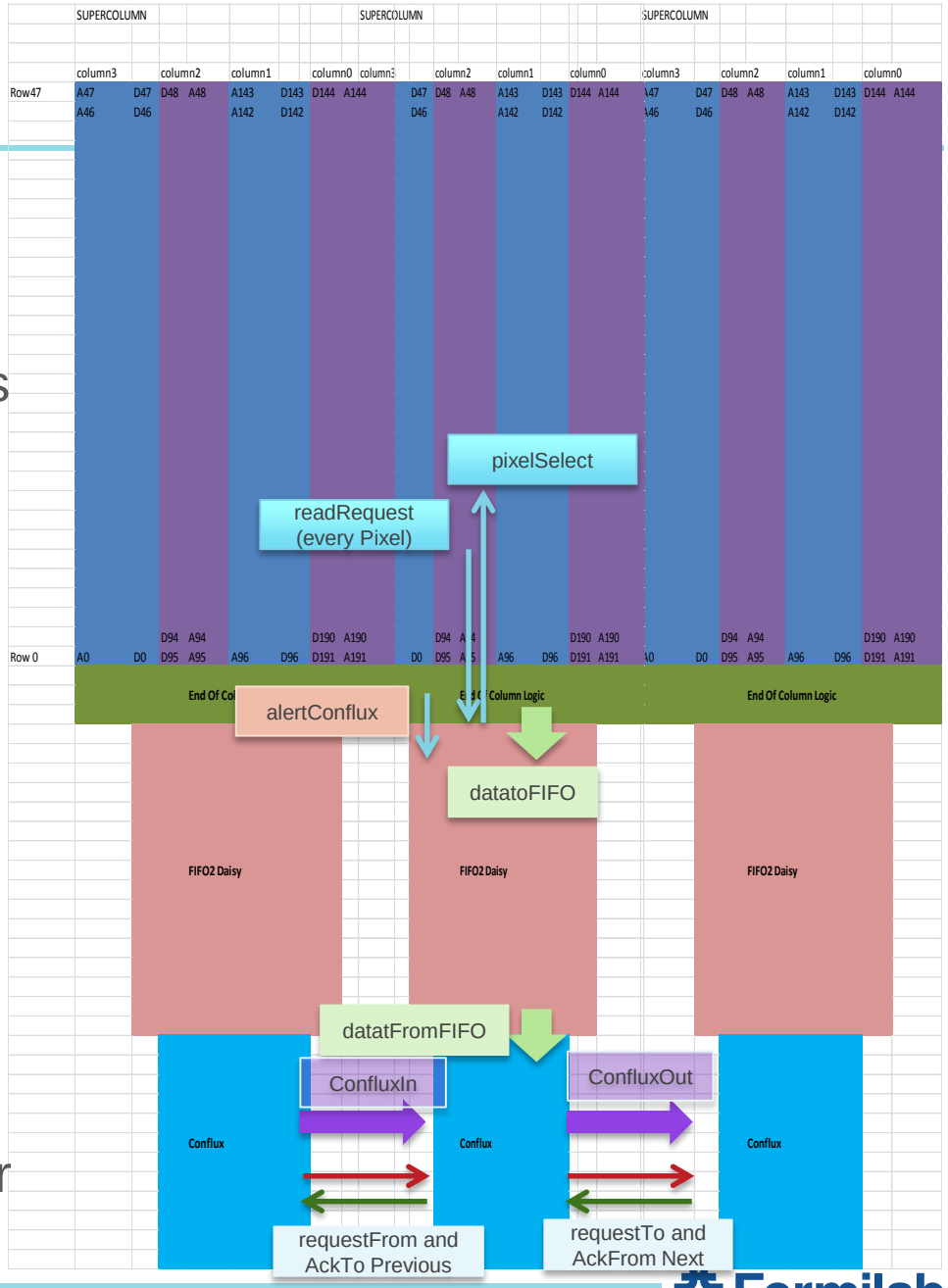
ASIC dataflow

- Hit signal from each pixel in a superColumn is “ORed” to create “alertConflux”
- Every pixel which is hit, generates a “readRequest”
- This is cancelled if the End of Column Logic issues a “selectPixel” signal at posedge of each “rStrobe”
- During 1 BXClk cycle, alertConflux remains active until all pixels which are active are read and data is transferred to FIFO2daisy. This then resets
- Data from FIFO2daisy is transferred to Conflux using a four phase asynchronous scheme



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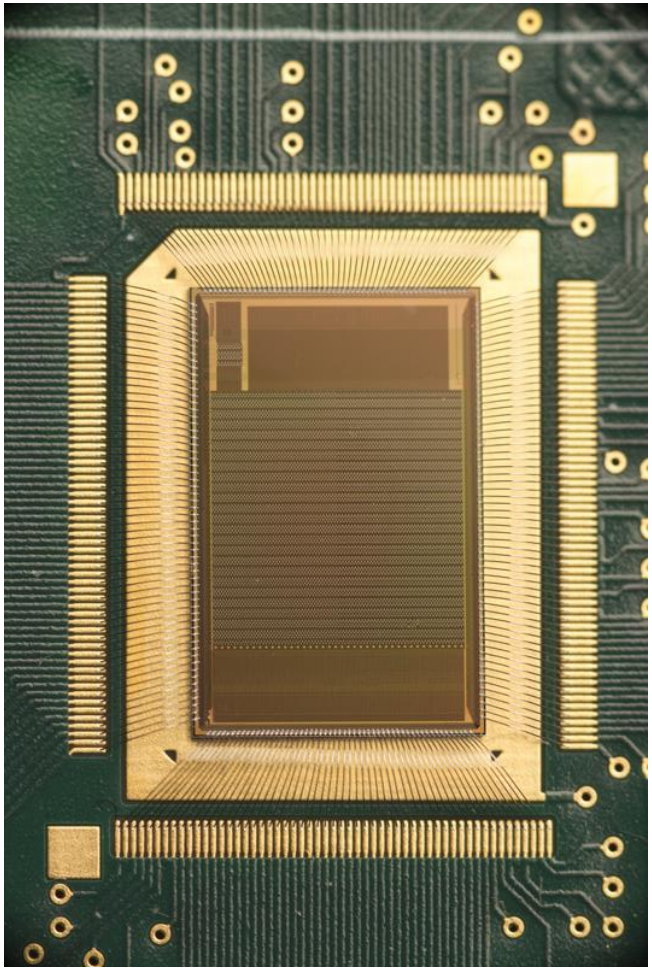
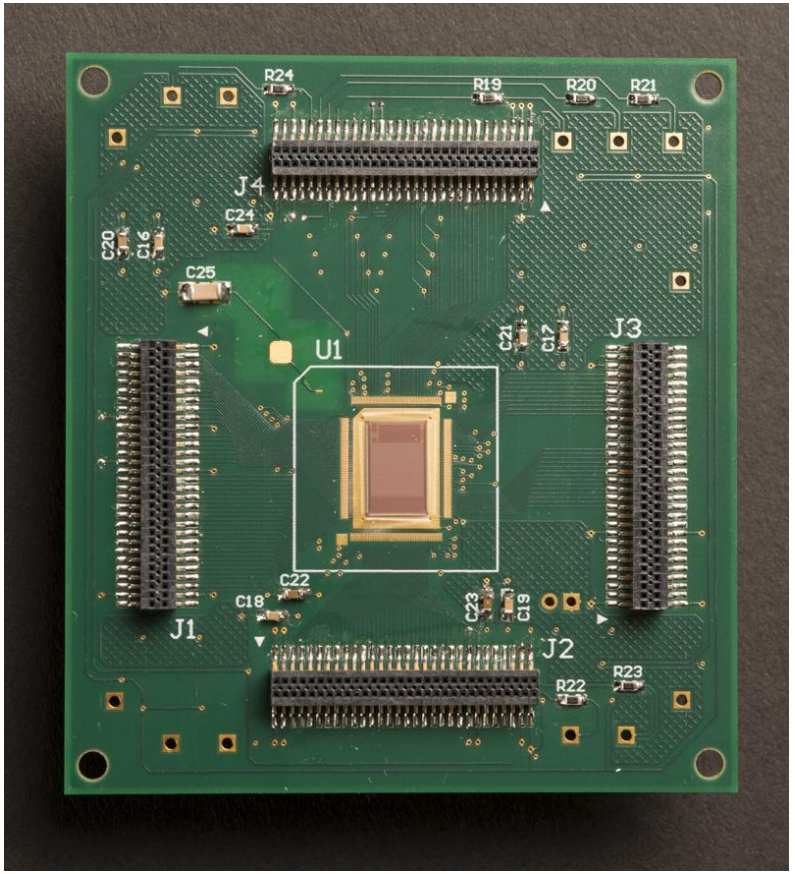
FCP130





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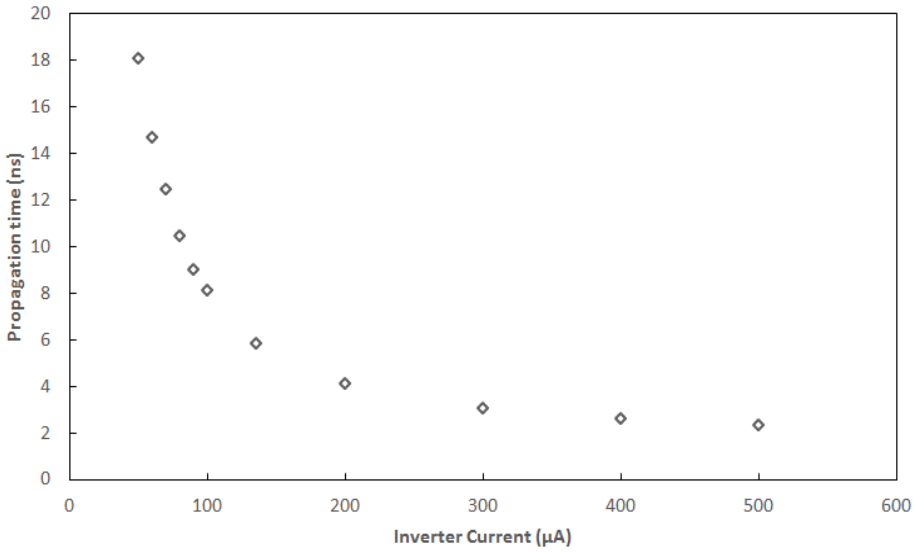
FCP130: Single pixel tests

- Successful Preliminary Qualitative analysis
  - Preamplifier response can be monitored; change of current is feedback loop changes the return to baseline.
  - All comparator response times are changing with change in threshold voltage.

FCP130: other functional tests

- Configuration register is able to able to correctly program the pixels
- The serial mode of transfer in FIFO 2 daisy can correctly send data Out
- The Spy signals for last superColumn (Pixel Hit, ADC value and address can be correctly monitored)
- Asynchronous data transfer (Conflux) was successfully verified



FCP130: issues and next steps

- Antenna diodes – were shorted to the substrate
- Floating deep nwell's
- Due to layout errors detailed analog tests of the entire matrix could not be characterized

- FCP130_v2 with bug fixes and enhanced versions of the preamplifier and comparator is being submitted Dec 2016

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INFN - Fermi CMS Pixels (IFCP65)

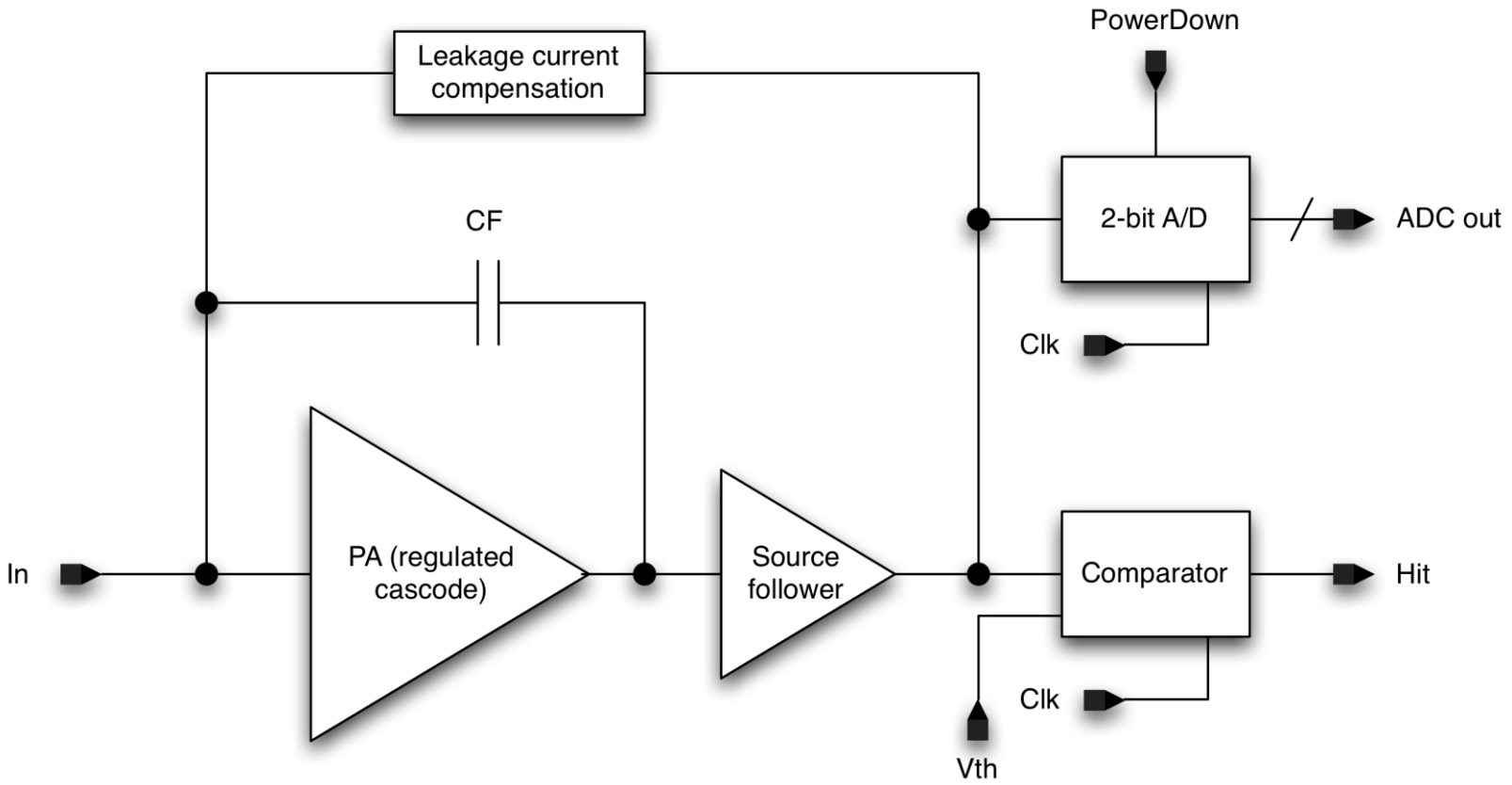
Translation of FCP130 to 65nm by U. Bergamo (INFN)

Adaptation of FCP130nm concept to 65nm: IFCP65 (collaboration with INFN (U.Bergamo))

- ✓**Accurate time allocation** of hits requires the discriminator to detect the smallest signal within the BXClk period
- ✓This may be difficult to achieve in a system with continuous time shaping → hits just above threshold can improperly be assigned to the **subsequent BXClk period**
- ✓**ToT systems** may requires several BXClk periods in order to perform full A-to-D conversion
- ✓Continuous time processing has to face **baseline drifts** due to charge pile-up or DC coupling of consecutive stages

→ This AFE exploits the **synchronous environment** of the LHC to detect and determine incoming particle energy **within one BXClk period**

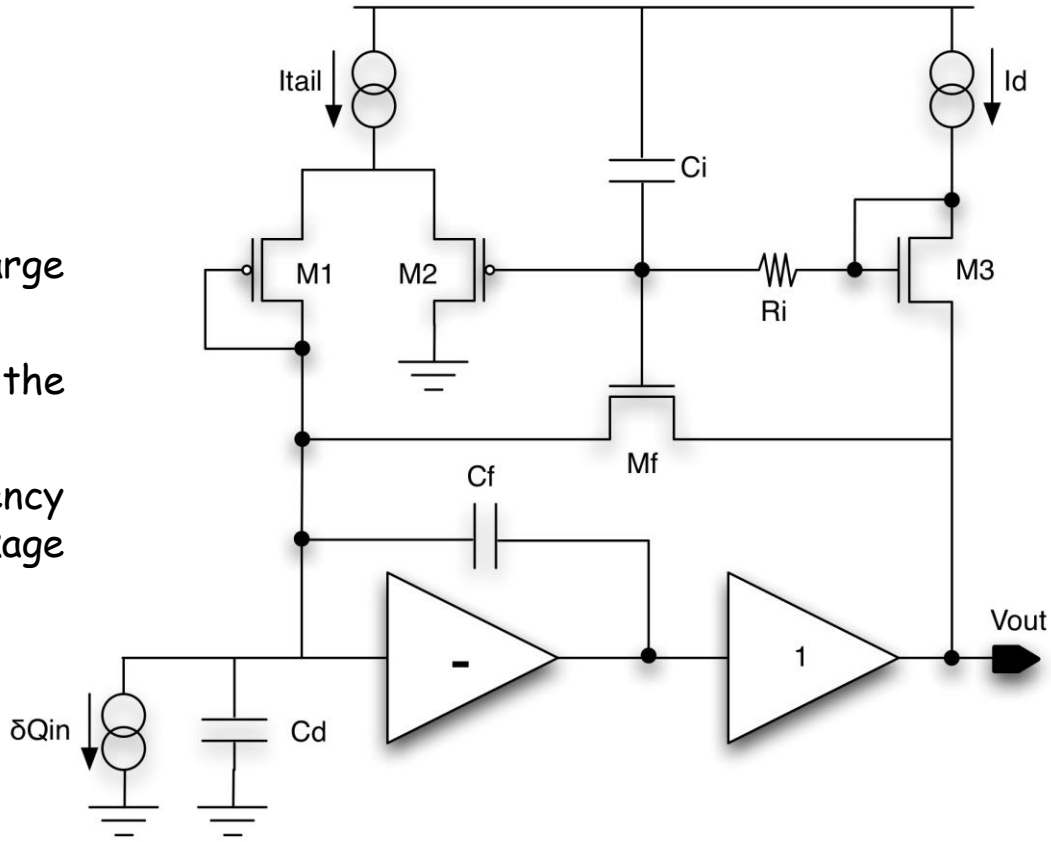
Pixel analog front-end



- ✓ **Synchronous** front-end with **zero dead time**
- ✓ Preamplifier (Regulated cascode) featuring a leakage current compensation circuit
- ✓ **Digital conversion** immediately after the preamplifier
- ✓ No in-pixel **charge injection** circuit. 15fF injection capacitance connected to the PA input

Charge sensitive amplifier

- ✓ **Regulated cascode** design
- ✓ Active feedback transistor Mf:
  - ✓ **1/gm resistor** for small signals
  - ✓ **Constant current source** for large signal.
  - ✓ M1 provides a DC path for the **detector leakage current**
  - ✓ Ri + Ci ensures low frequency operation of the leakage compensation circuit
- ✓ **Current consumption** ~ 4.0 *μA*



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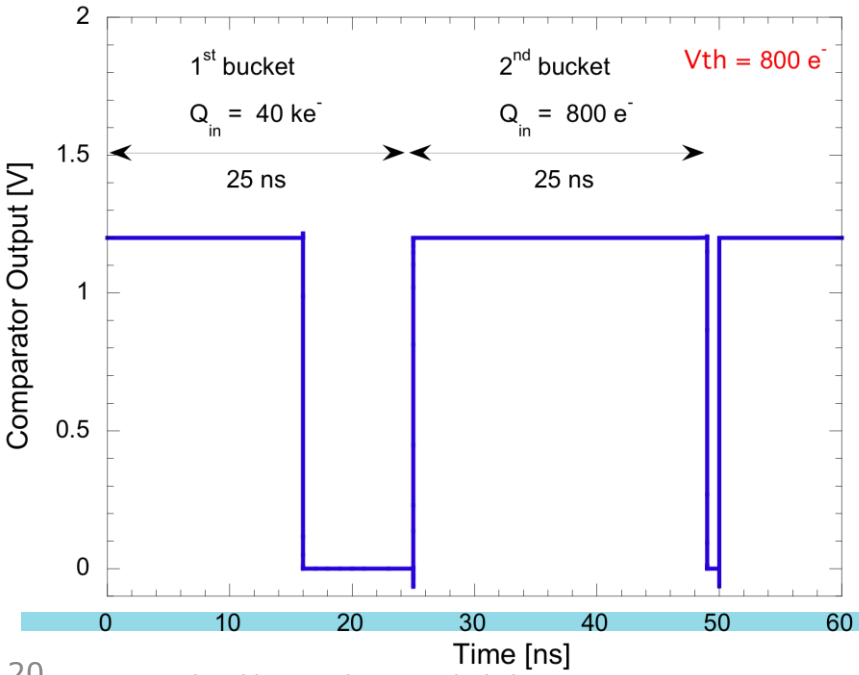
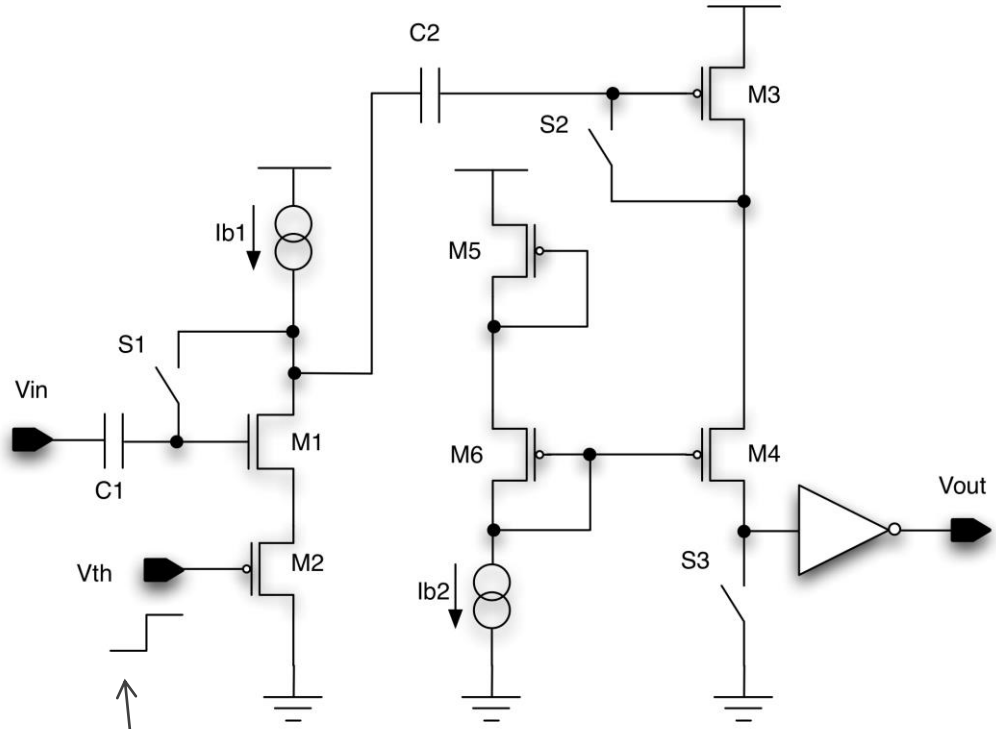
Comparator

- ✓ Compact, single-ended architecture
- ✓ **AC coupled** to the preamplifier
- ✓ **Correlated double sampling:**
  - ✓ Auto-zeroed
  - ✓ Increased pileup immunity
  - ✓ No need for trimming DAC

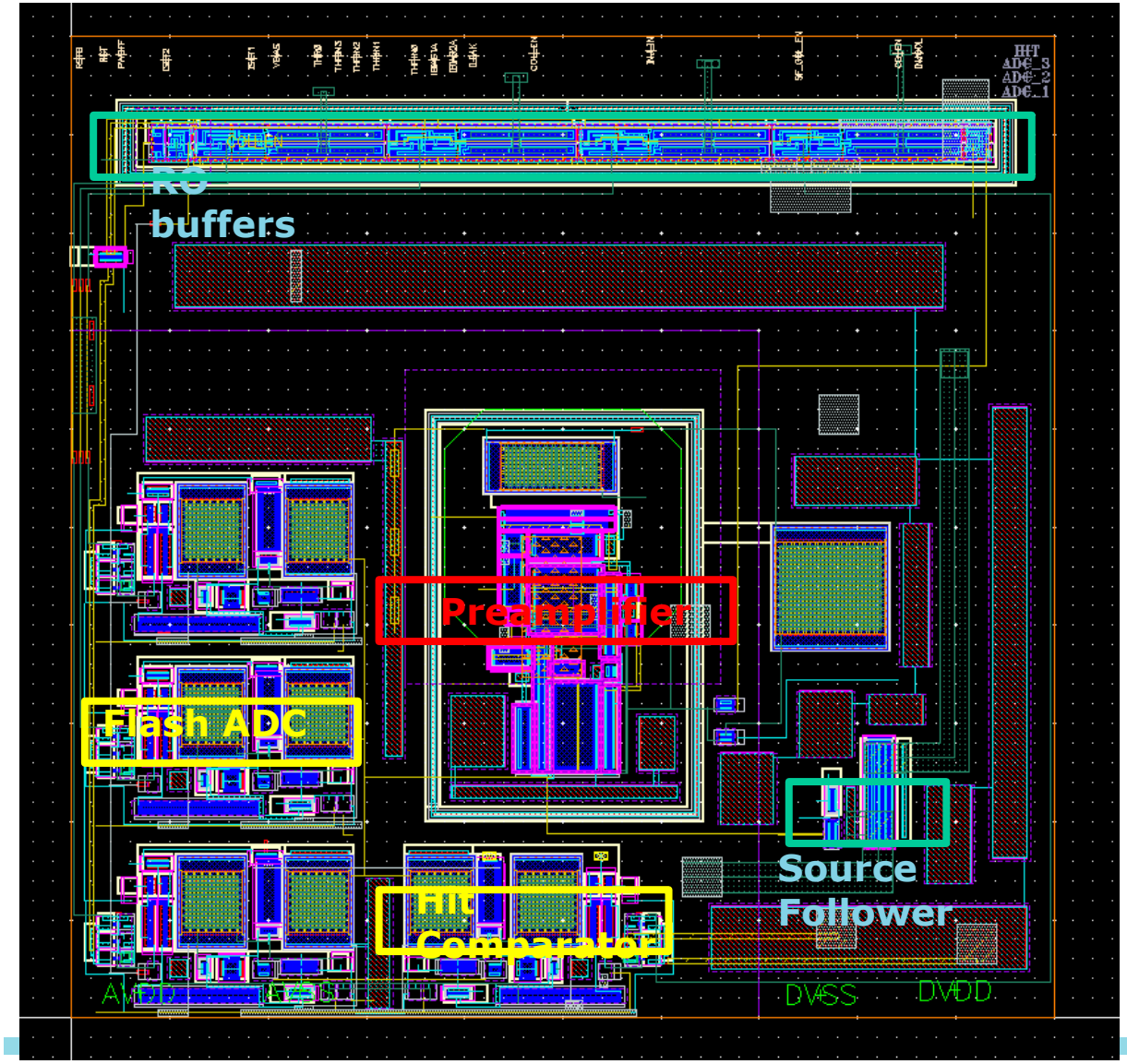




Vth step generated in-pixel

- ✓ 12.5ns **reset phase**; 12.5ns **active comparison**
- ✓ **~ 1μA current consumption**

Layout



- ✓ RO buffers and Source follower included in the miniasic version of the AFE
- ✓ All the devices in the global P-substrate
- ✓ MIM feedback cap
- ✓ Nwell guard ring surrounding the preamplifier

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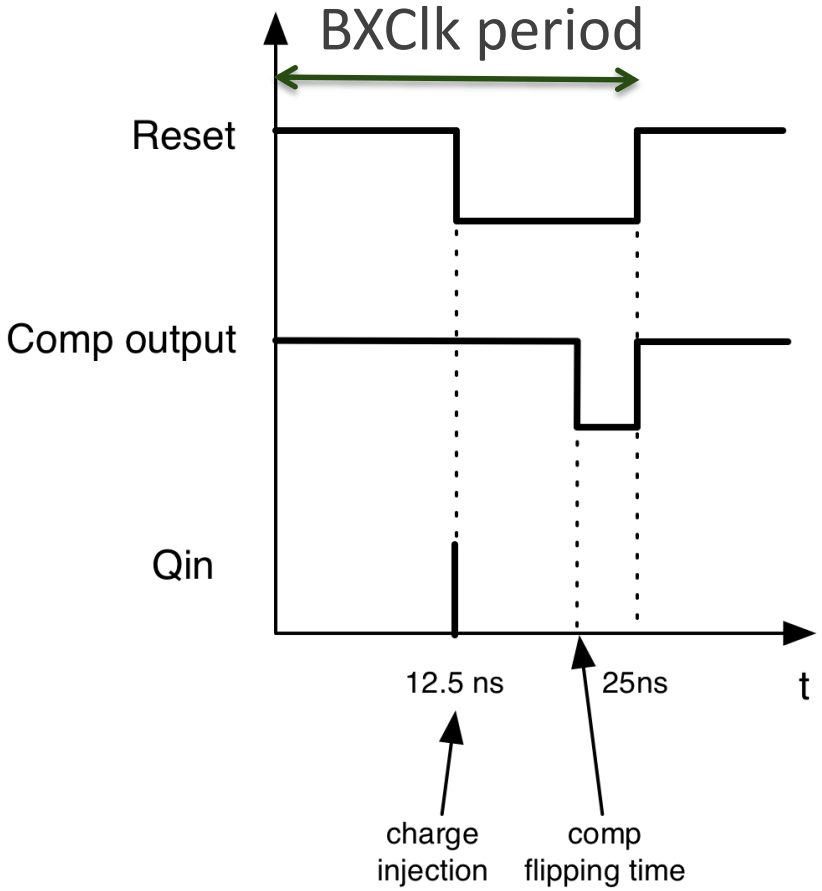
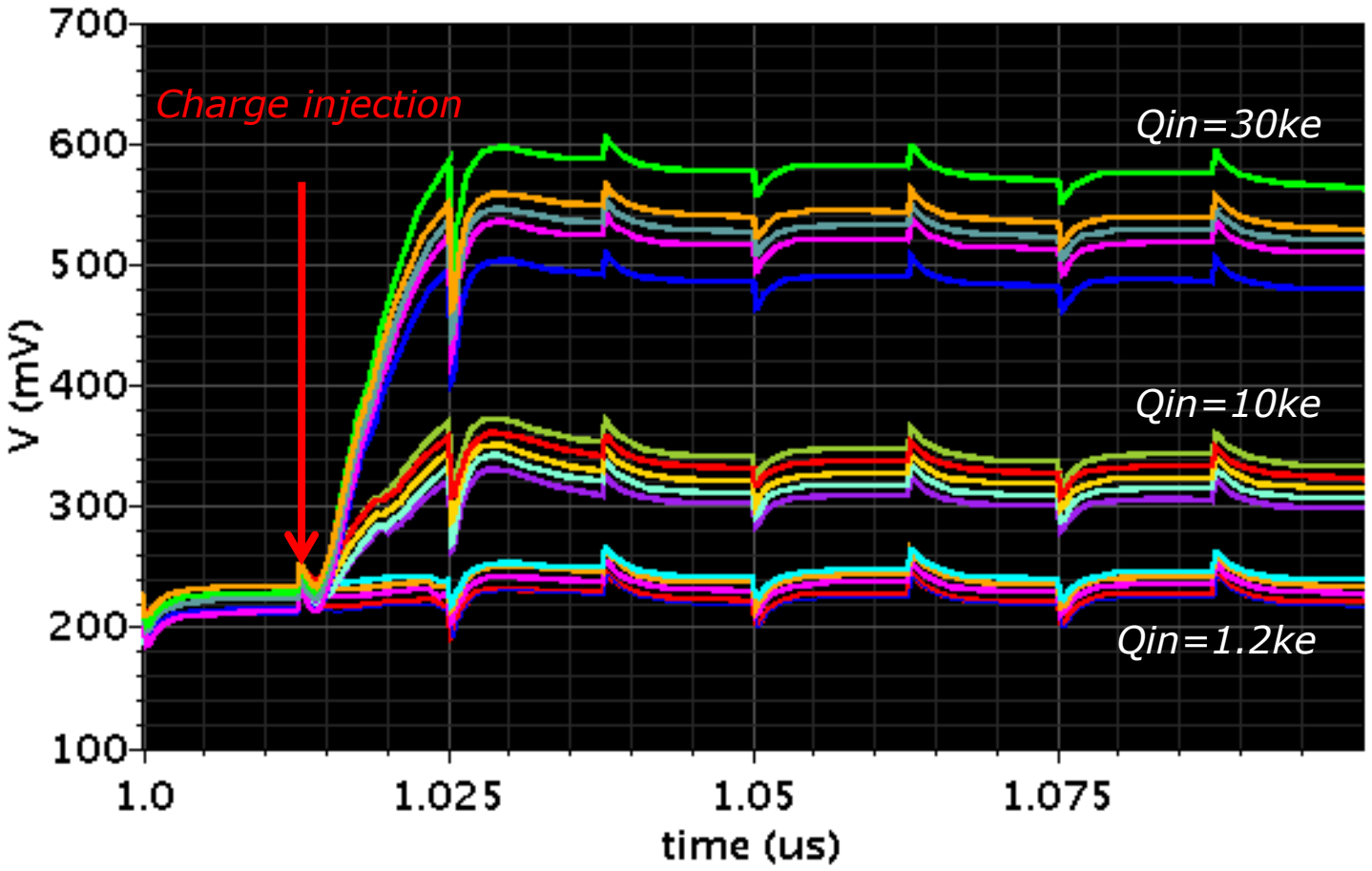
Timing Diagram



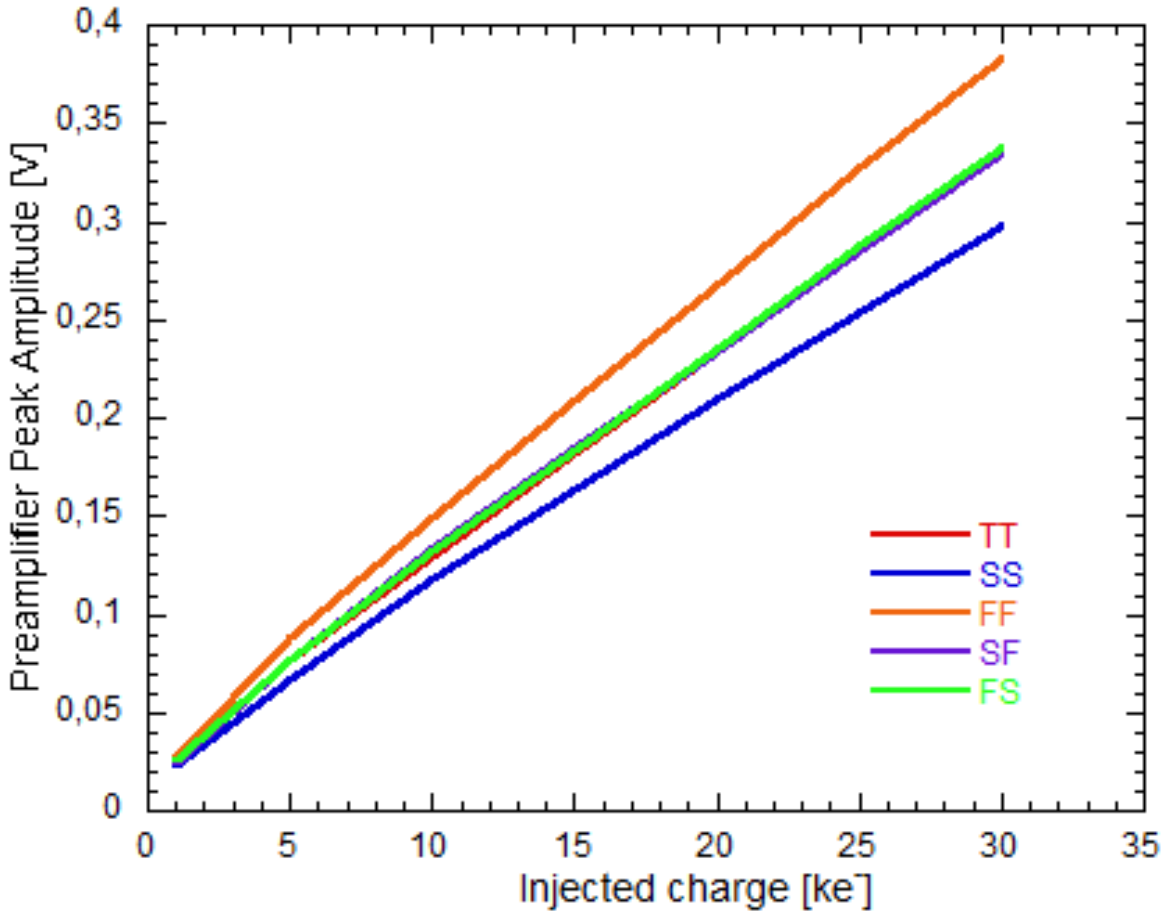
- **Charge injection** takes place as soon as the reset is released
- **40 MHz** reset signal

Preamplifier output – 4C simulations



- **PA output** for Qin=1.2ke-, 10ke-, 30ke. CD=50fF, Qth=600e-
- ± 14% variation (wrt TT) in the **PA peak amplitude** (mainly due to the MIM feedback cap)

Preamplifier peak amplitude – 4C simulations



- **PA peak amplitude** as a function of the injected charge
- **Good linearity** in all the corners
- Non-negligible changes in **charge sensitivity** due to the MIM feedback cap

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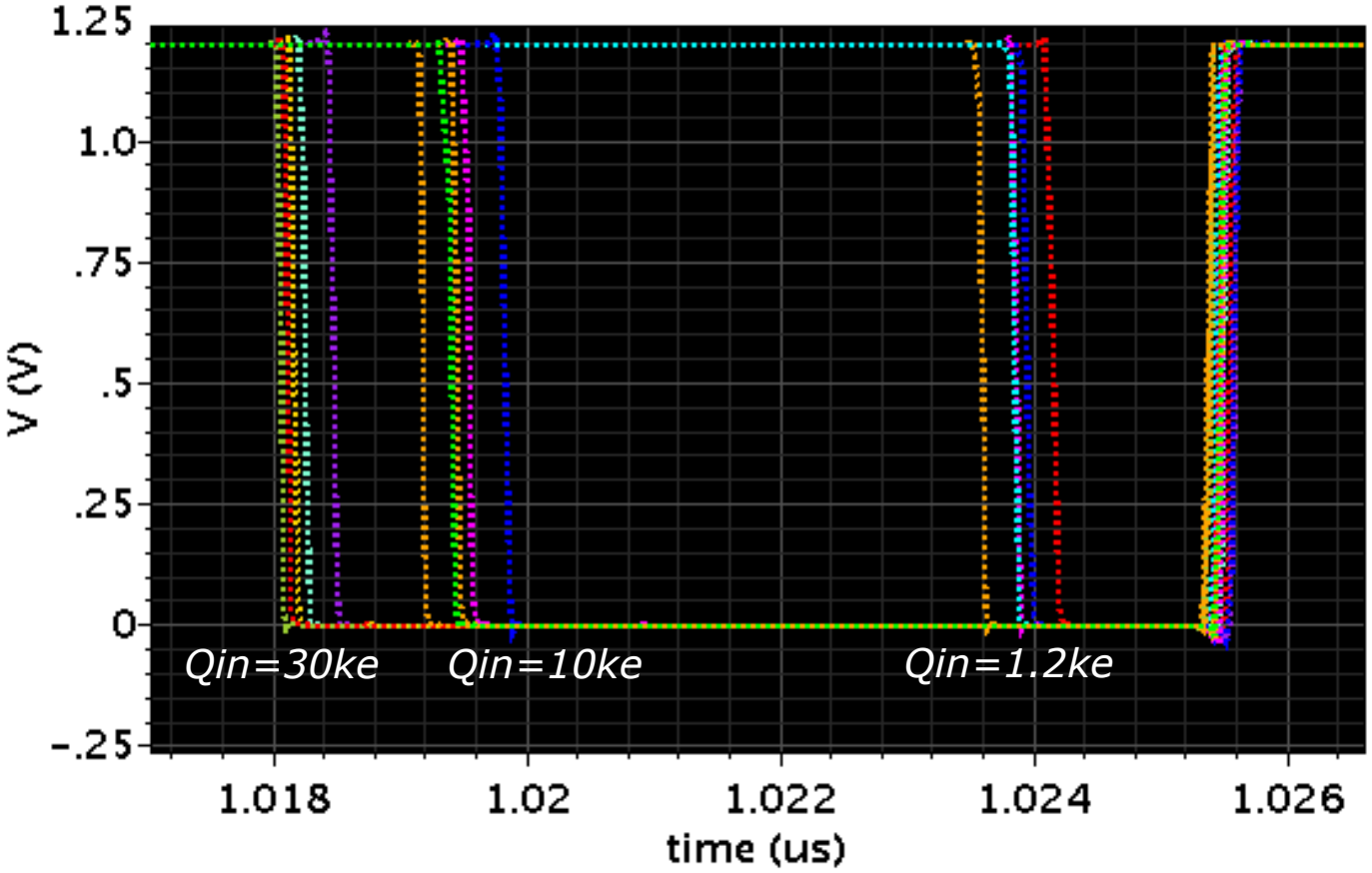
Comparator output – 4C simulations



- **Comparator output** for Qin=1.2ke-, 10ke-, 30ke. CD=50fF, Qth=600e-
- < ±400ps changes (wrt to TT) in comparator flipping time

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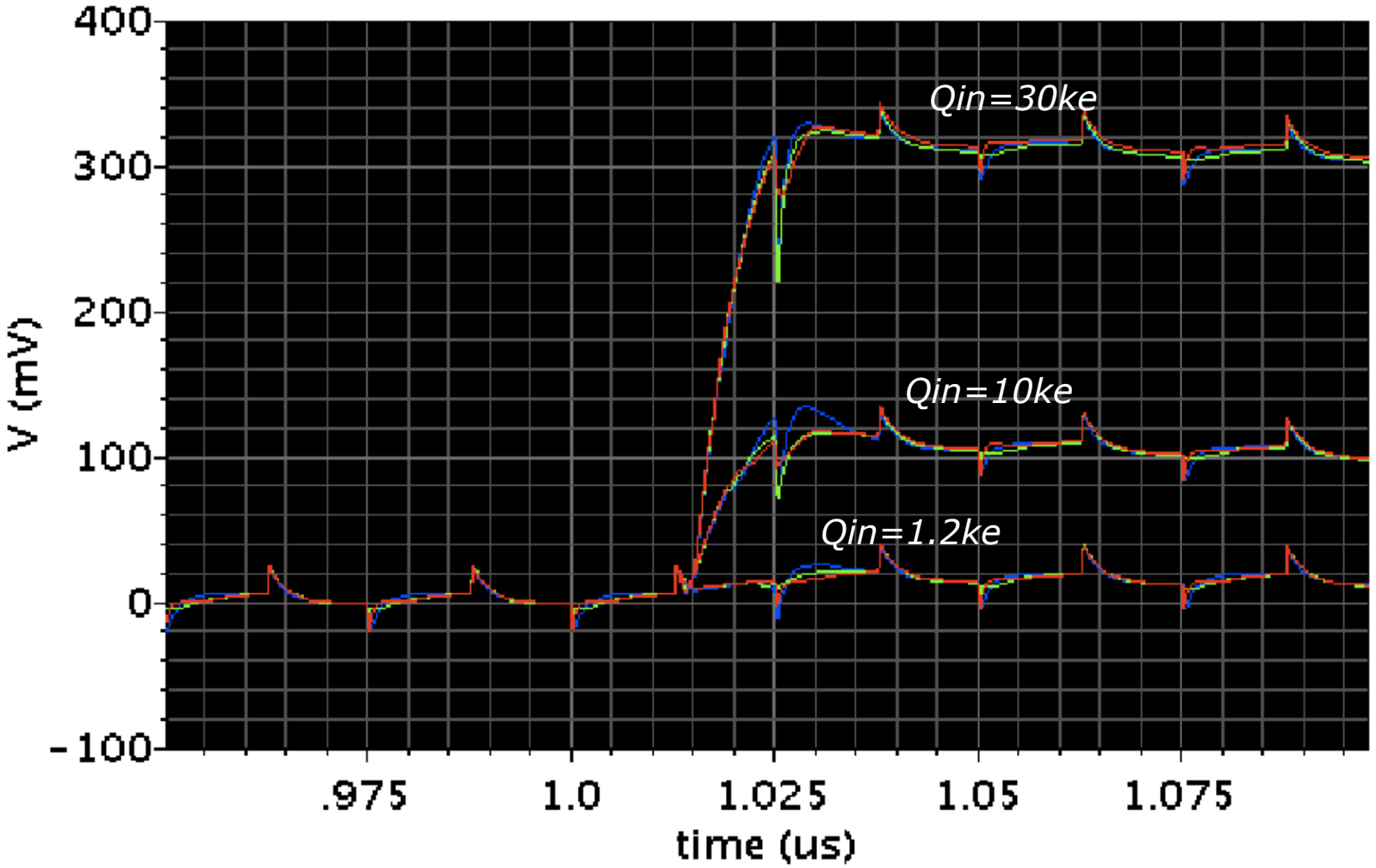
Preamplifier output – Radiation corners



- **PA output** for Qin=1.2ke-, 10ke-, 30ke. **TT+200Mrad+500Mrad corners**. CD=50fF
- **Negligible changes in PA output response** in the different corners

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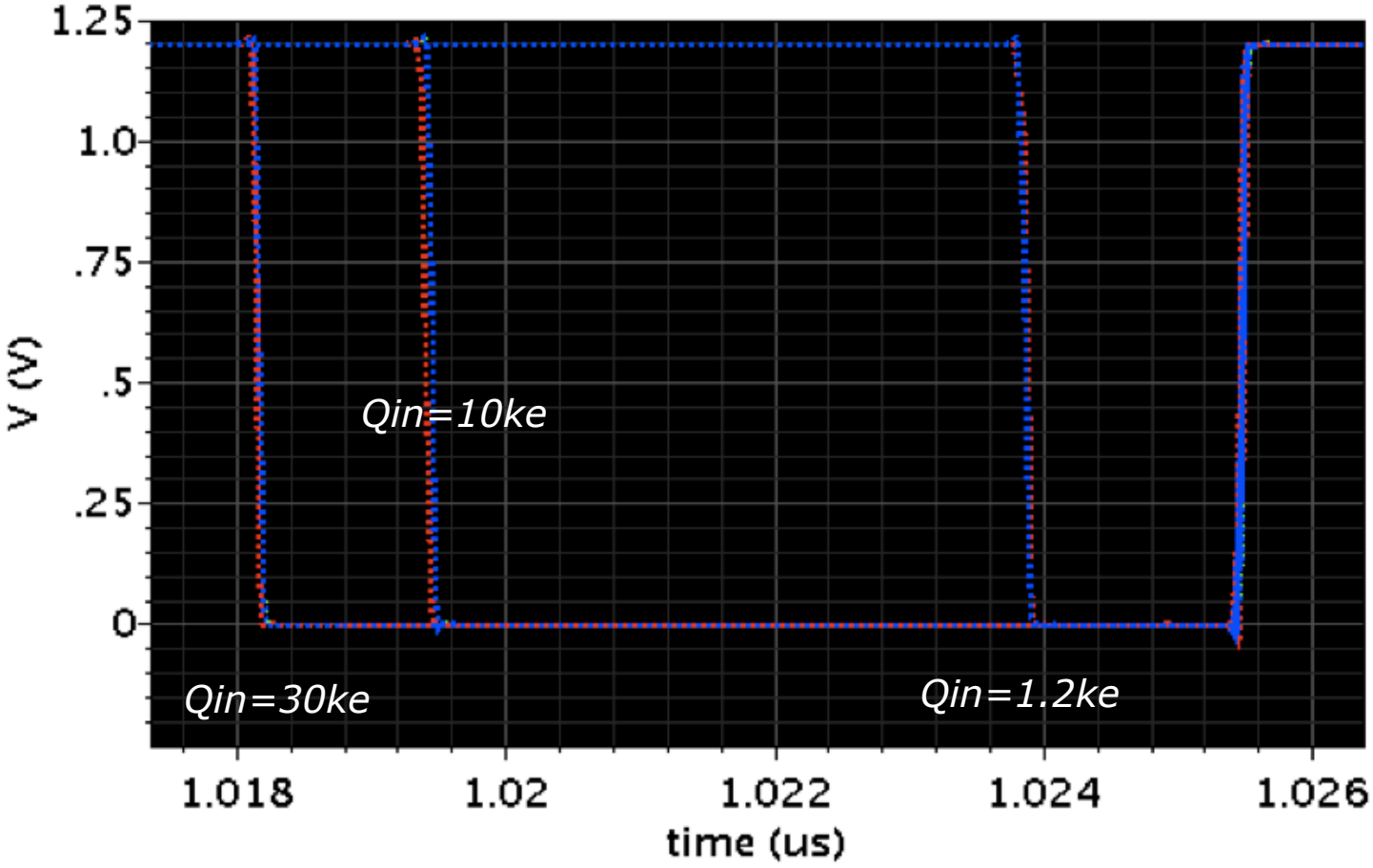
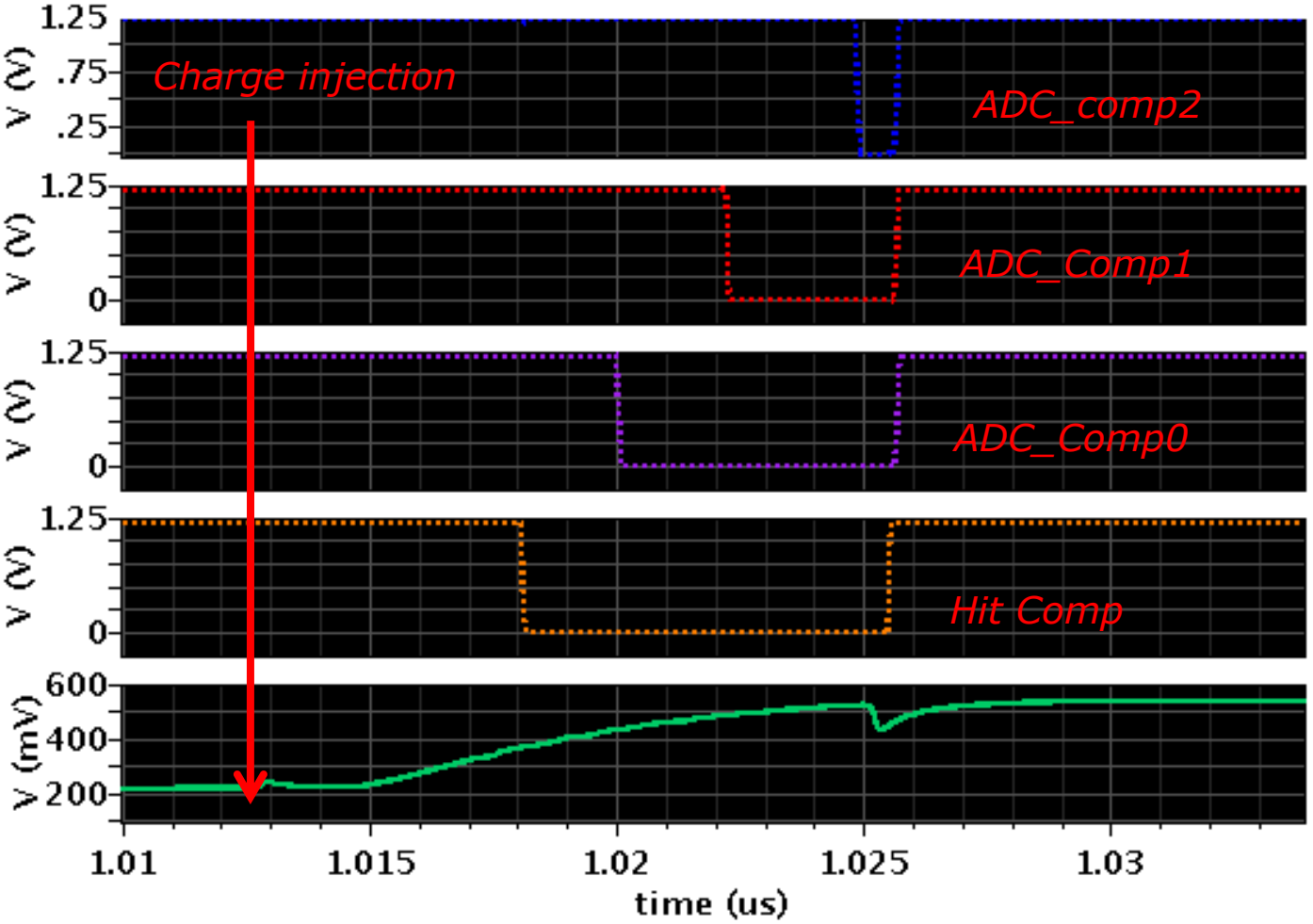
Comparator output – 500 Mrad corner



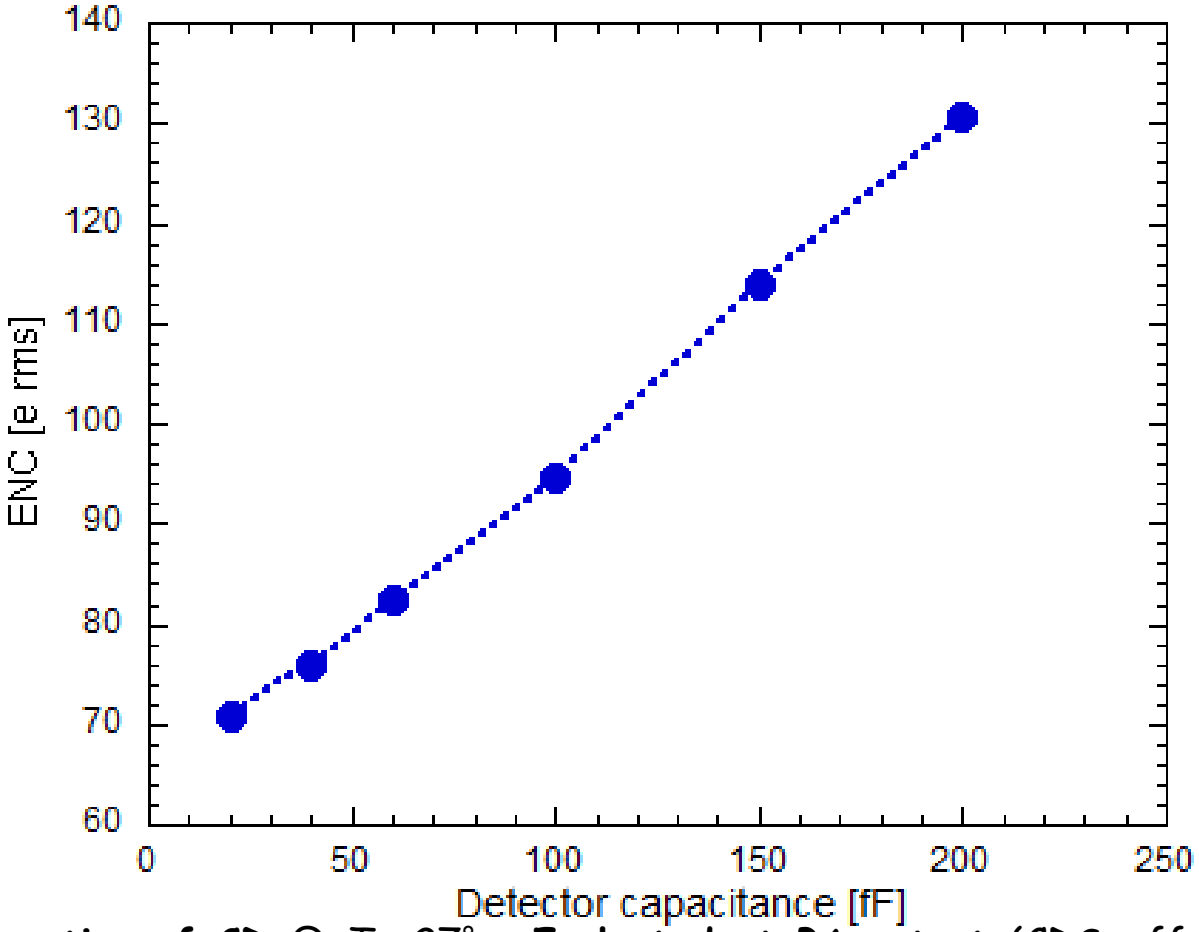
- **Comparator output** for Qin=1.2ke-, 10ke-, 30ke-. TT + 500Mrad corners. CD=50fF, Qth=600e-
- Negligible changes in **comparator flipping time**

Hit Comparator and ADC comparator outputs



- **Hit Comparator** and **ADC comparators** outputs for Qin=30ke-
- Threshold for the different comparators can be **set up independently** by means of bias lines distributed through the matrix columns

Equivalent Noise Charge



- **ENC as a function of CD** @ T=+27° . **Evaluated at PA output** (CDS effects not simulated here)
- ENC≈80e @ CD=50fF.
- ENC obtained with a proportional calibration constant for small input charges (0 to 2ke)

Recap Table #1

	TT	TT 500 Mrad	SS	FF	FS	SF	spec
Charge sensitivity [mV/ke]	10.3	10.2	9.1	11.7	9.9	10.4	-
ENC rms [e]	79	79	82	76	83	77	<<126
Threshold dispersion σ(Qth) rms [e]	35						<<126
$\sqrt{(ENC^2 + \sigma(Qth)^2)}$ [e]	86						≤126
In-time overdrive [e-]	Not applicable						≤ 600
Current consumption [μA/pixel]	7.4*	7.2					≤ 4
Delay time [ns]	10.8	12.1	11.0	10.5	10.8	10.9	-
ADC Conversion time [ns]	12.5	12.5	12.5	12.5	12.5	12.5	-

- Post-layout simulations, default configuration
- Detector capacitance CD=50 fF, T=27° C
- In-time overdrive→ "0" in this AFE
- Delay time (comp flipping time – charge inj time) → 600 e-, Qin=1200 e-

* ~5 uA/pixel when in binary mode. Comparator dynamic current not included

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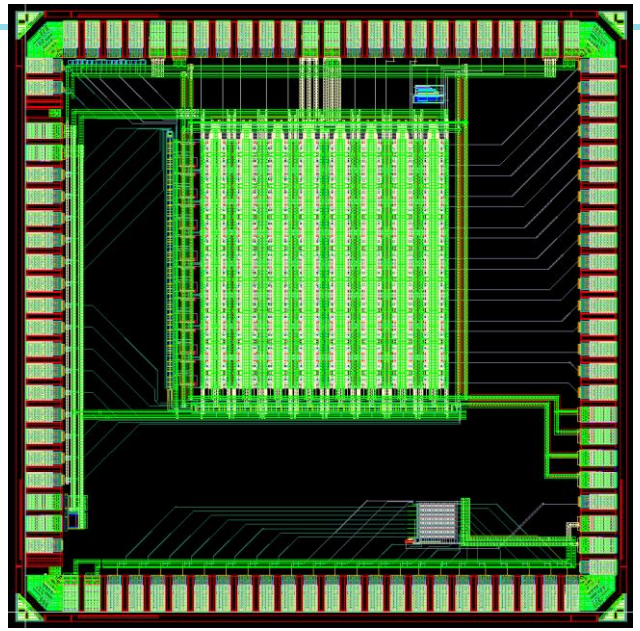
Recap Table #2

	27° C	-20° C	spec
Charge sensitivity [mV/ke]	10.3	9.0	-
ENC rms [e]	79	82	<<126
In-time overdrive [e-]	Not applicable		≤ 600
Current consumption [μA/pixel]	7.4*	7.2	≤ 4
Delay time [ns]	10.8	9.9	-
ADC conversion time [ns]	12.5	12.5	-

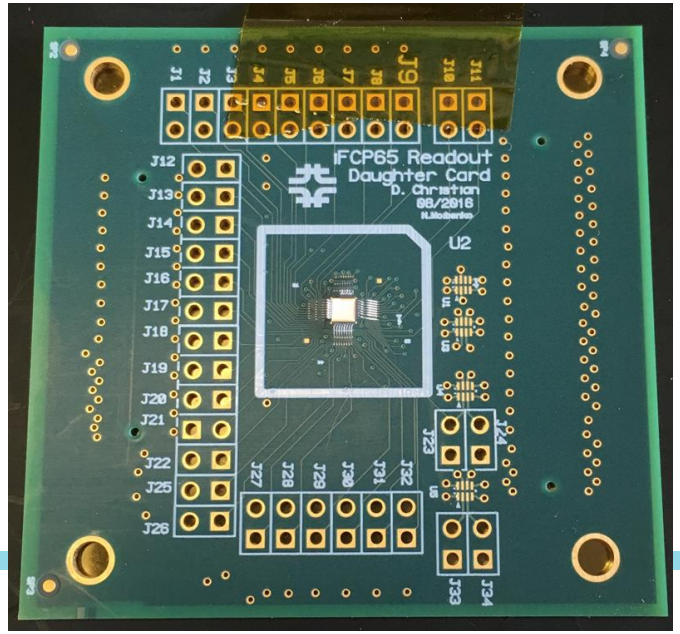
- Post-layout simulations, default configuration
- Detector capacitance CD=50 fF, T=27° C
- In-time overdrive→ "0" in this AFE
- Delay time (comp flipping time – charge inj time) → 600 e-, Qin=1200 e-

* ~5 uA/pixel when in binary mode

IFCP65 mini ASIC submission



- ✓16x16 matrix
- ✓Charge injection and readout controlled via three independent SIPO shift registers
- ✓16 independent outputs (one for each row) to read out the pixel preamplifier output

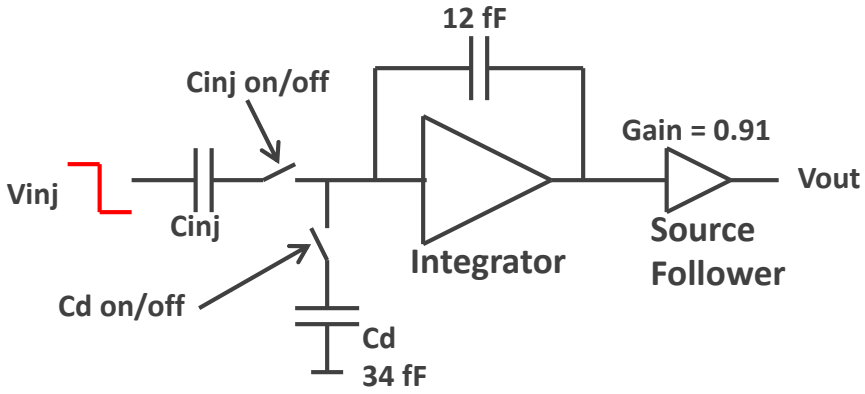


- ✓Test boards fabricated and populated
- ✓ASIC's wire bonded
- ✓Tests started last week

Initial FCP65 test results -Tom Zimmerman

Integrator Gain

Assumptions:
Cfb = 12 fF, Source Follower gain = 0.91



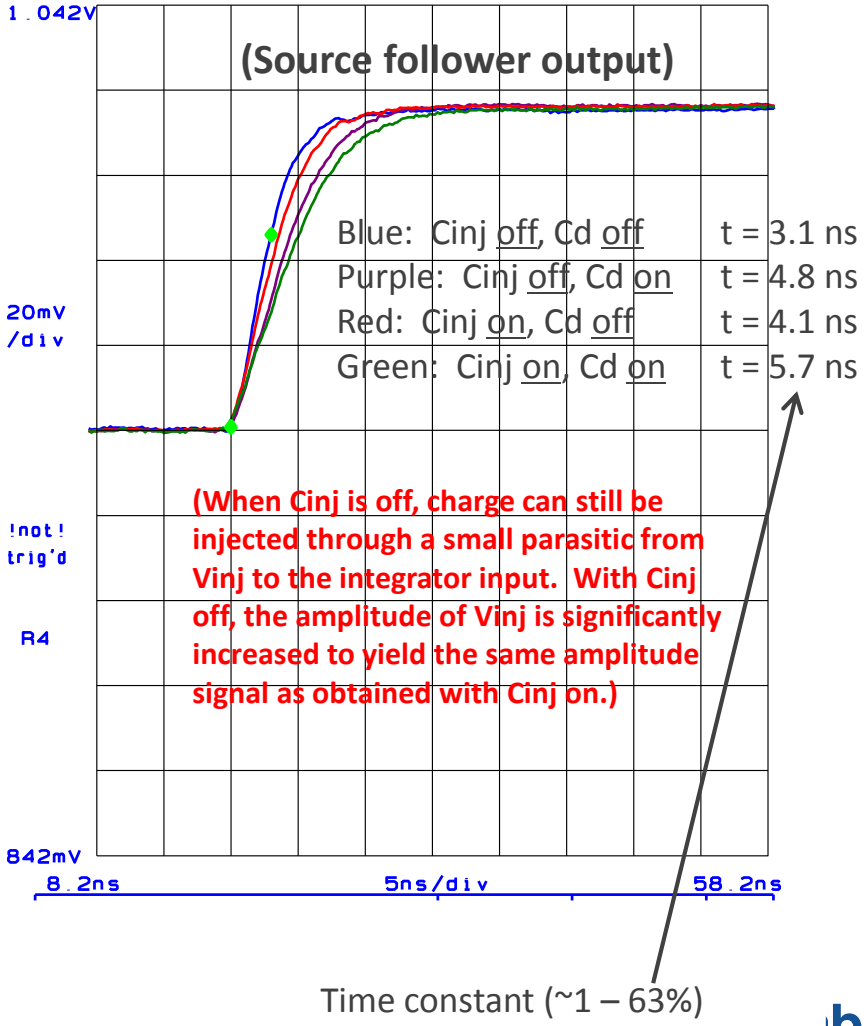
"Measure" Cinj:
Apply a step input and measure Vout:
If Vinj = -146 mV, then Vout = 122.4 mV

Therefore: Cinj = 11.1 fF.

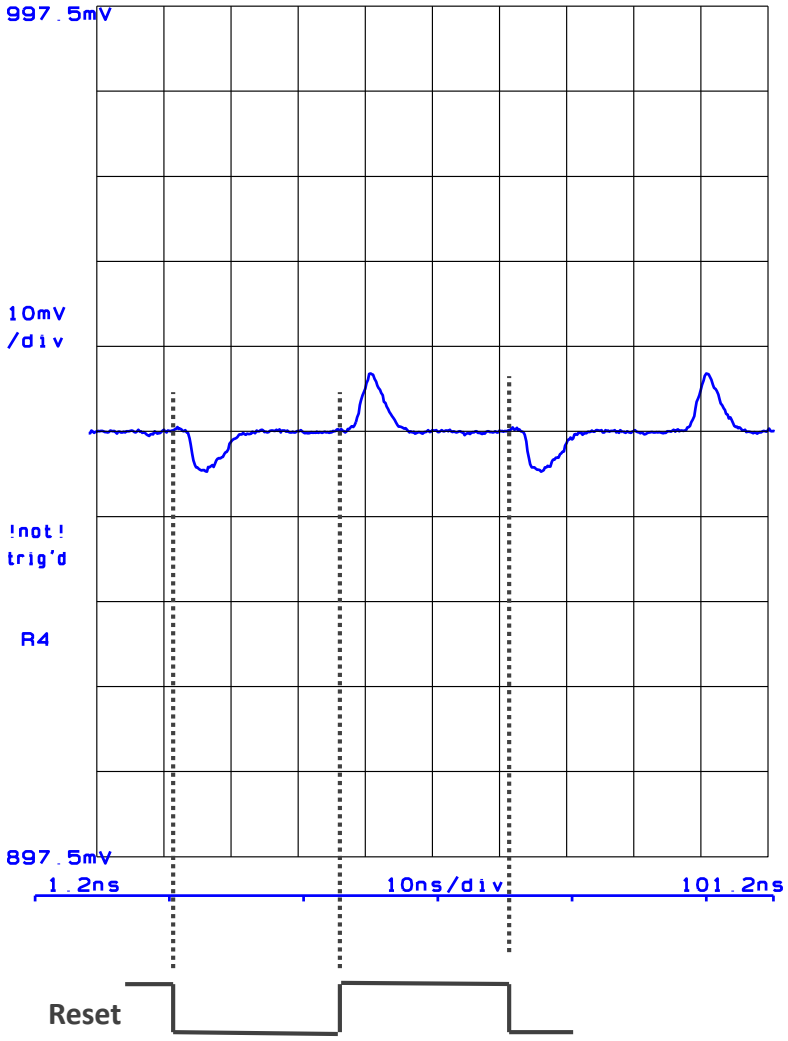
Pixel-to-pixel gain variation across the array is less than 2% -- good.

Integrator Time Response

(Vinj = 90 mV with Cinj on)



Integrator output while operating Reset (no signal)



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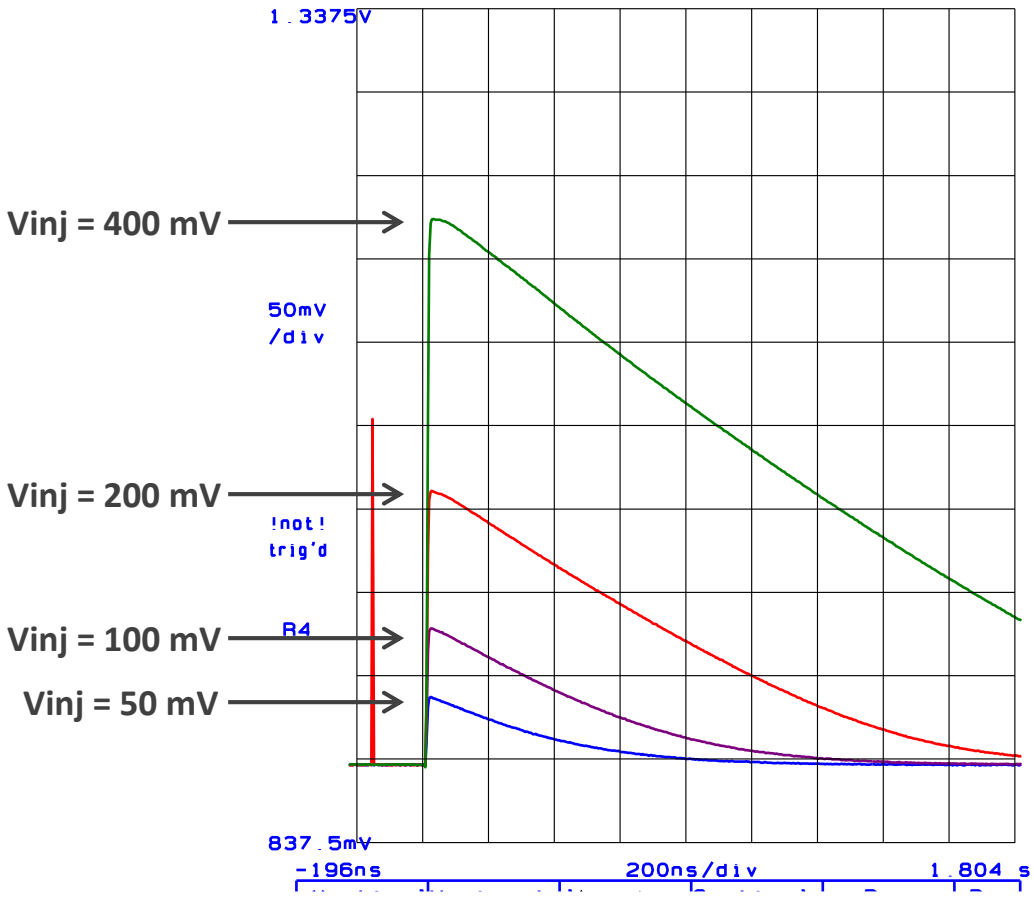
Integrator return to baseline

(Ileak at nominal setting)



Looks good

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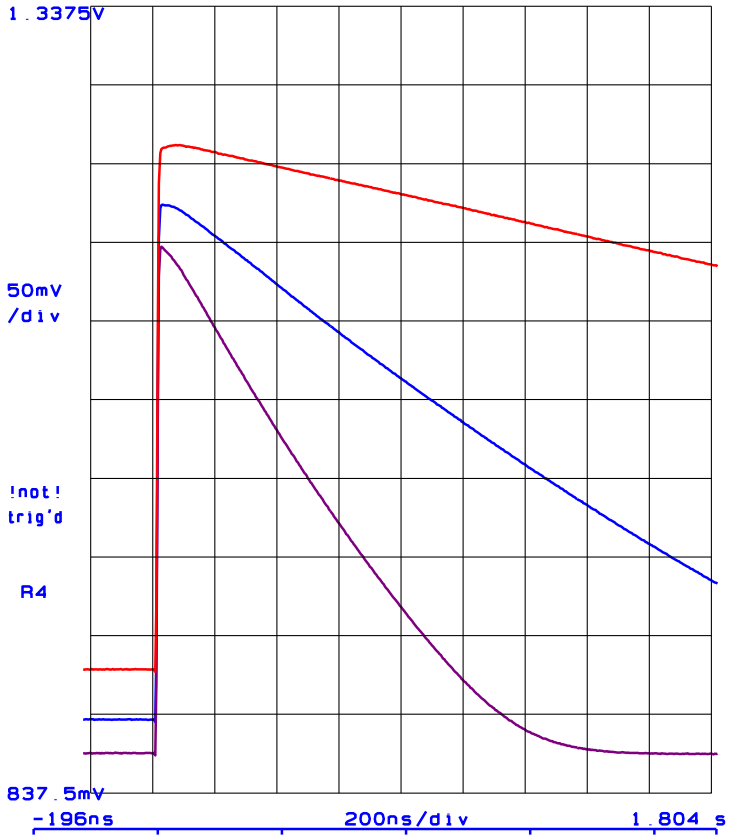
Vary Ileak

(Vinj = 400 mV)



Looks good

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RD53A:

Following slides from RD53A design review

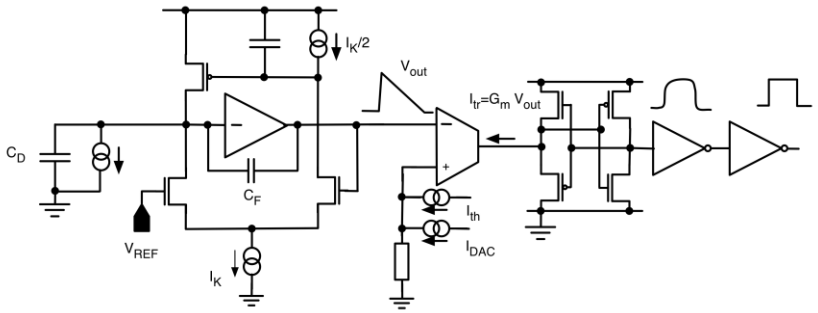
RD53A MUST demonstrate

- Small pixels: 50 x 50um^2
- Low in-time effective threshold: 1200e-
  - Very good digital/analog isolation
- ~4bit charge at high rate
- High hit rate: 3GHz/cm^2
  - Dead time loss < 1%
- Time walk: < 25ns
- Digital buffering/processing: 12.5us
- Trigger rate: 1MHz
- Acceptable power consumption: < 3W + 1W SLDO (< 1W/cm^2)
- Serial powering
- High radiation tolerance: 500Mrad
- Working with bump-bonded sensors in test beams

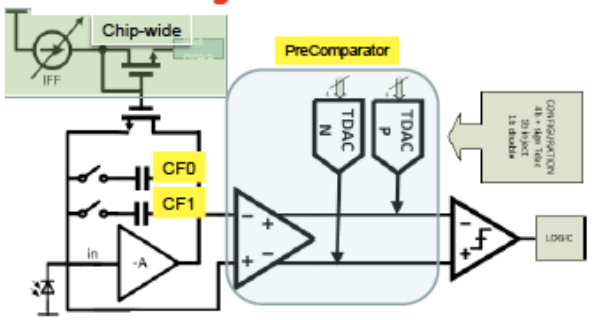
Defined in: https://cds.cern.ch/record/2113263

RD53A: Analog front-ends

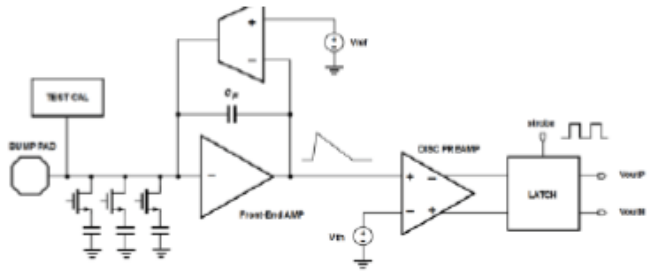
INFN Pavia/Bergamo design



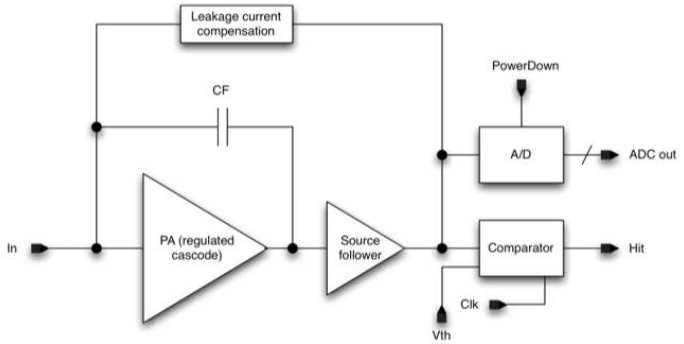
LBNL design in FE65-P2



INFN Torino design



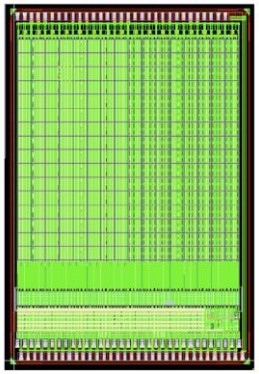
INFN-FNAL design

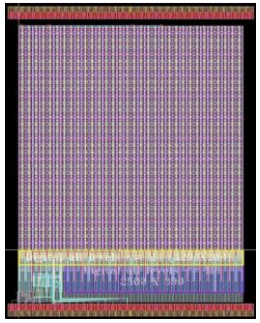


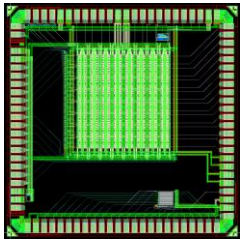
- **4 different AFEs. Test results** on available prototypes look good (also after **irradiation**) – (INFN-FNAL design not yet tested)
- **FE65-P2** and the **CHIPIX65** demonstrators are going to provide essential information and experience in view of the integration of the analog FE in the RD53A chip. Test results on the FE65-P2 very encouraging
- The RD53A demonstrator will include several versions of the analog FE. They should be **fully tested** (also after irradiation) in their (almost) final version (schematic and layout) so that they qualify to be safely included in RD53A

65 nm CMOS analog front-end prototypes

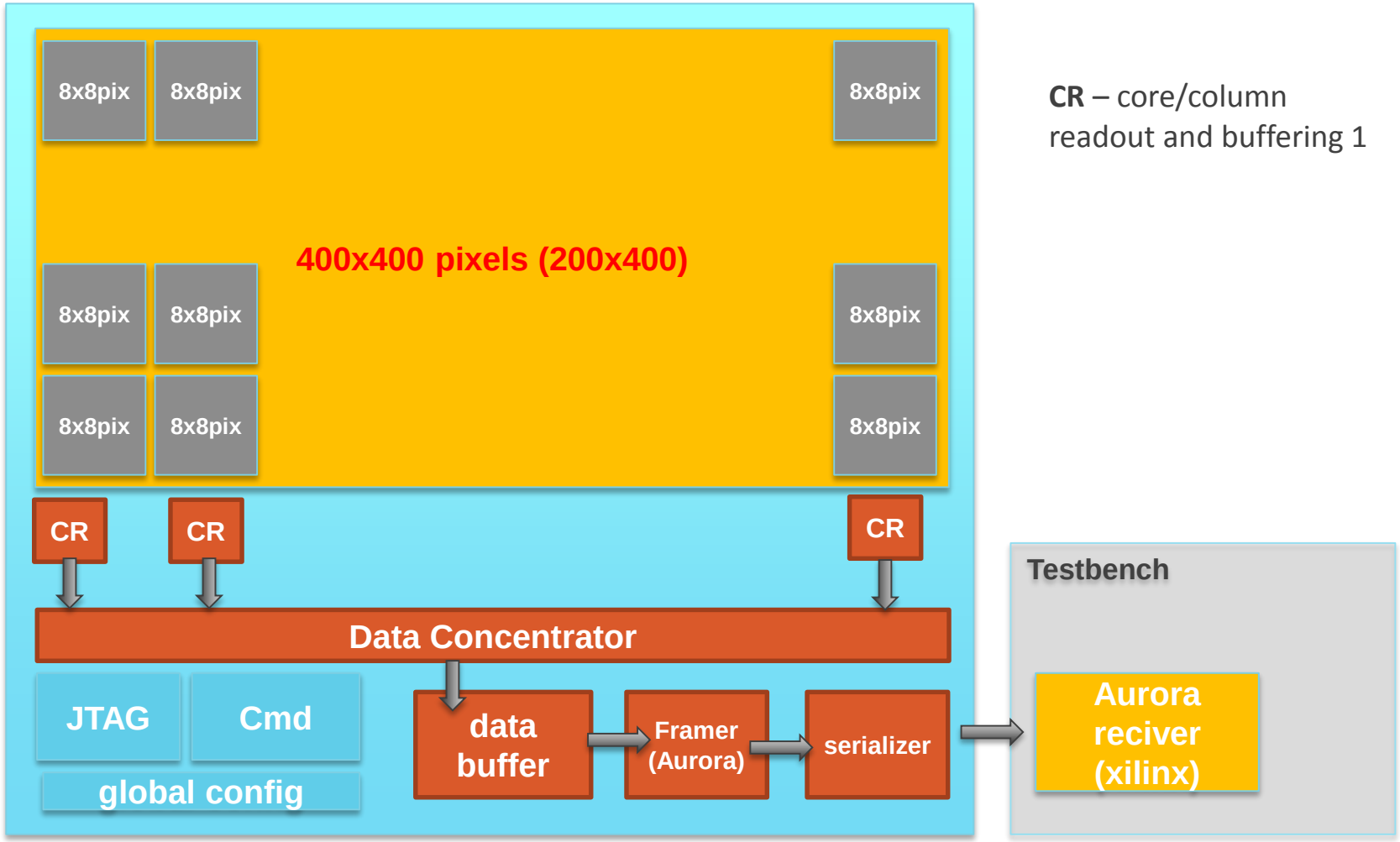
- **INFN** (Pavia, Torino) submitted (May 2015) small prototypes with two different versions (asynchronous, synchronous) of the analog front-end. Encouraging results from test
- These two different analog front-end will be included in the **CHIPIX65** demonstrator (end of June)
- Another design for the analog front-end (asynchronous) is included in the **FE65-P2** that is currently being tested, with promising results
- **Fermilab/INFN** recently submitted (May 2016) an analog front-end with zero dead time and Flash ADC; characterization has just started







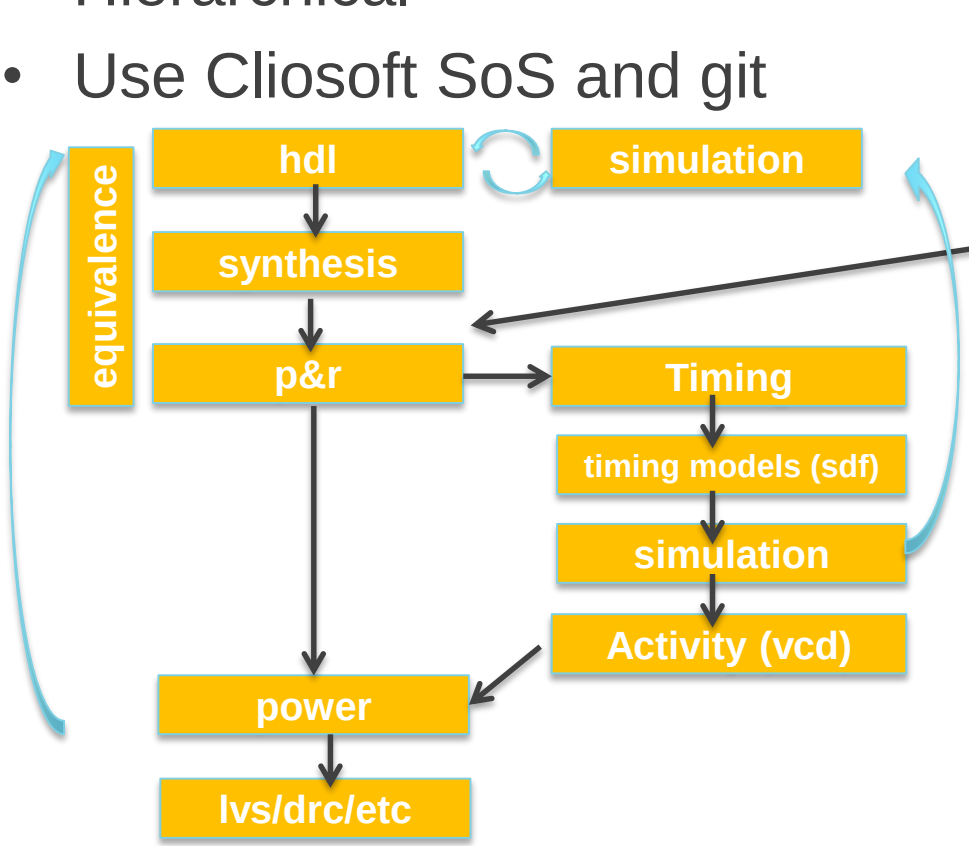
Digital RD53A

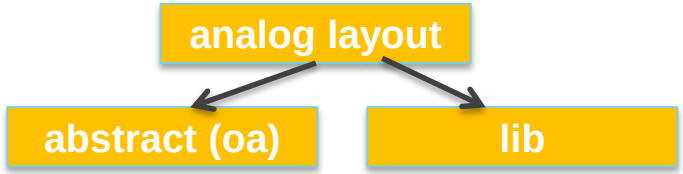


CR – core/column readout and buffering 1

Custom Design Methodology Flow

- OpenAccess mixed signal (modified flow CERN)
- Industry standard tools (complex and expensive)
- Hierarchical
- Use Cliosoft SoS and git





Hierarchy:

- 8x8 core first
- 50x50 array + periphery

Pixel sensor and bump-bonding
- Signal, charge, pixel size, etc.
- Bump pad layout
- - - - -

RD53A chip: Jorgen, Maurice
- Specifications
- Documentation
- General organization

Test system: TBD (Bonn, CERN, Pisa, ?)
- Requirements, specifications
- Hardware, Firmware, Software
- Chip test/characterization: wafer level, chip level, beam tests
- Radiation testing

RD53A chip integration/verification: Flavio, Deputy: Tomasz

Floorplan: Flavio, Dario
- Pixel array, Bump pad
- EOC
- Power distribution
- Bias distribution
- Analog/digital isolation
- Integration/verification

Analog FEs (3/4) with biasing: Luigi, Valerio, Ennio, Dario, IP designers
- Specification/performance
- Interface (common)
- Analog isolation
- Digital/timing model
- Abstract
- Verification of block: Function, radiation, matching, etc.
- Shared database
- Integration in design flow
- Distribution of global analog signals
- Verification of integration

Monitoring: Francesco, Mohsine, IP designers
- Specification/performance
- Interface
- Analog isolation
- Digital/ timing model
- Abstract
- Verification of block: Function, radiation, matching, etc.
- Shared database
- Integration in design flow
- Verification of integration

Digital: Tomasz
- **Simulation Framework: Elia,** Sara,
  - Framework
  - Hit generation/ import MC
  - Reference model / score board
  - Monitoring/verification tools
  - Generic behavioural pixel chip
  - SEU injection
- **Architecture: Elia,** Sara, (Andrea, Luca)
  - Evaluation – choice: Performance, Power, Area, ,
  - Simulation/Optimization
  - **Functional Verification**
  - SEU immunity
- **Pixel array/pixel regions: Sara, (**Andrea)
  - Latency buffer
  - Core/column bus
- **Readout/control interface: Roberto,** Paris
  - Data format/protocol
  - Rate estimation / Compression
  - Implementation
- **Configuration: Roberto**, Mohsine, (Luca)
  - External/internal interface
  - Implementation
- **Implementation: Dario, Sara, (Luca, Andrea),**

  Script based to "quickly" incorporate architecture/RTL changes
  - RTL - Synthesis
  - Functional verification
  - SEU verification
  - P&R
  - FE/IP integration
  - Clock tree synthesis
  - Timing verification
  - Power verification
  - Physical verification
  - Final chip submission

Digital lib.:Dario, Sandeep, Mohsine
- Customized rad tol library
- Liberty files (function, timing, etc.) Characterized for radiation
- Custom cells (Memory, Latch, RICE)
- Integration with P&R
- Radiation tolerance
- Integration in design kit

Power: Michael, Sara, Stella, Flavio
- Shunt-LDO integration
- On-chip power distribution
- Optimization for serial powering
- System level power aspects
- Power Verification

IO PAD frame: Hans
- Wirebonding pads, ESD, SLVS, Serial readout**, Shunt-LDO**, analog test input/output

Testing/Yield optim.: Sandeep, Luca
- Testability
- Scan path
- BIST
- Redundancy
- Bump-bonding test/verification

Support and services:
- Tools, design kit: Wojciech, Sandeep
- Cliosoft repository: **Elia, Dario,** Sandeep, Wojciech
- Radiation effects and models: **Mohsine**10/18/2016

Questions?