A new Front-End design for RD53A

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Outline

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- Charge injection circuit
- New readout architecture to evaluate
- Conclusions and future plans

Introduction

Goal of RD53A*:

- Design and characterization of full scale demonstrator pixel chip
  - demonstrate in a large format IC the suitability of the technology (including radiation tolerance), the stable low threshold operation, the high hit and trigger rate capabilities, required for HL-LHC upgrades of ATLAS and CMS.
  - It contains 4 different analog readout channel
  - not intended to be a production chip
  - It contains design variations for testing purposes

** https://cds.cern.ch/record/2113263?ln=it*

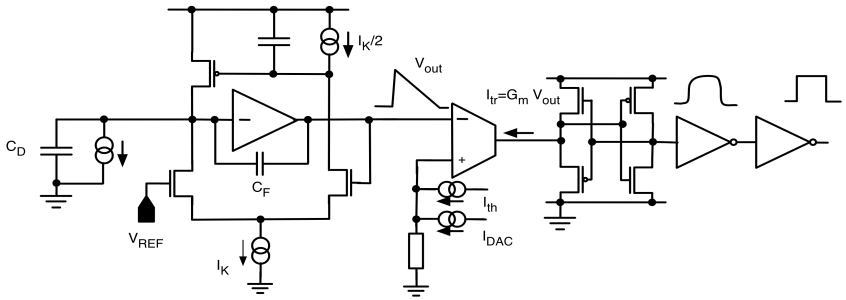
RD53A chip requirements

- Small pixels: 50x50 μm^2
- Low in-time effective threshold: 1200 e-
  - Very good digital/analog isolation
- High hit rate: up to more than 3 GHz/cm^2 (high pileup ~200)
- Time walk: < 25 ns
- Radiation tolerance: 500 Mrad
- Trigger rate up to 1 MHz: ~12.5 μs trigger latency
- Acceptable power consumption: < 3W + 1W SLDO (<1W/cm2)
- Serial powering
- Working with bump-bonded sensors in test beams

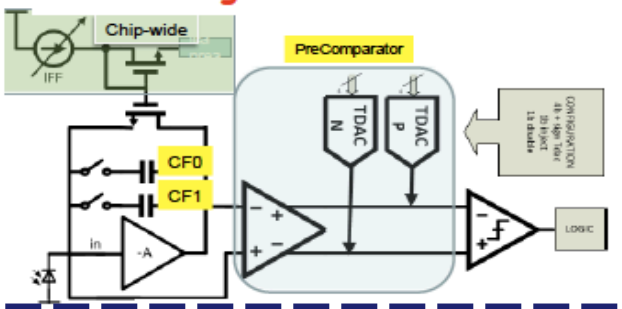
Specification defined in: https://cds.cern.ch/record/2113263

RD53A: Analog front-ends

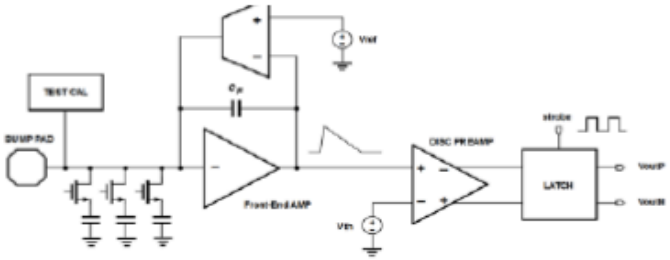
INFN Pavia/Bergamo design



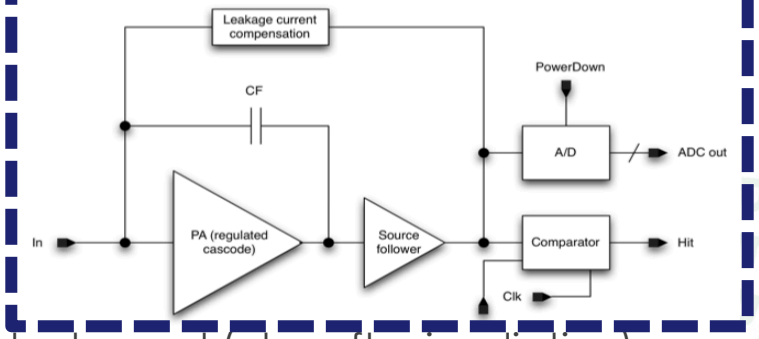
LBNL design in FE65-P2



INFN Torino design

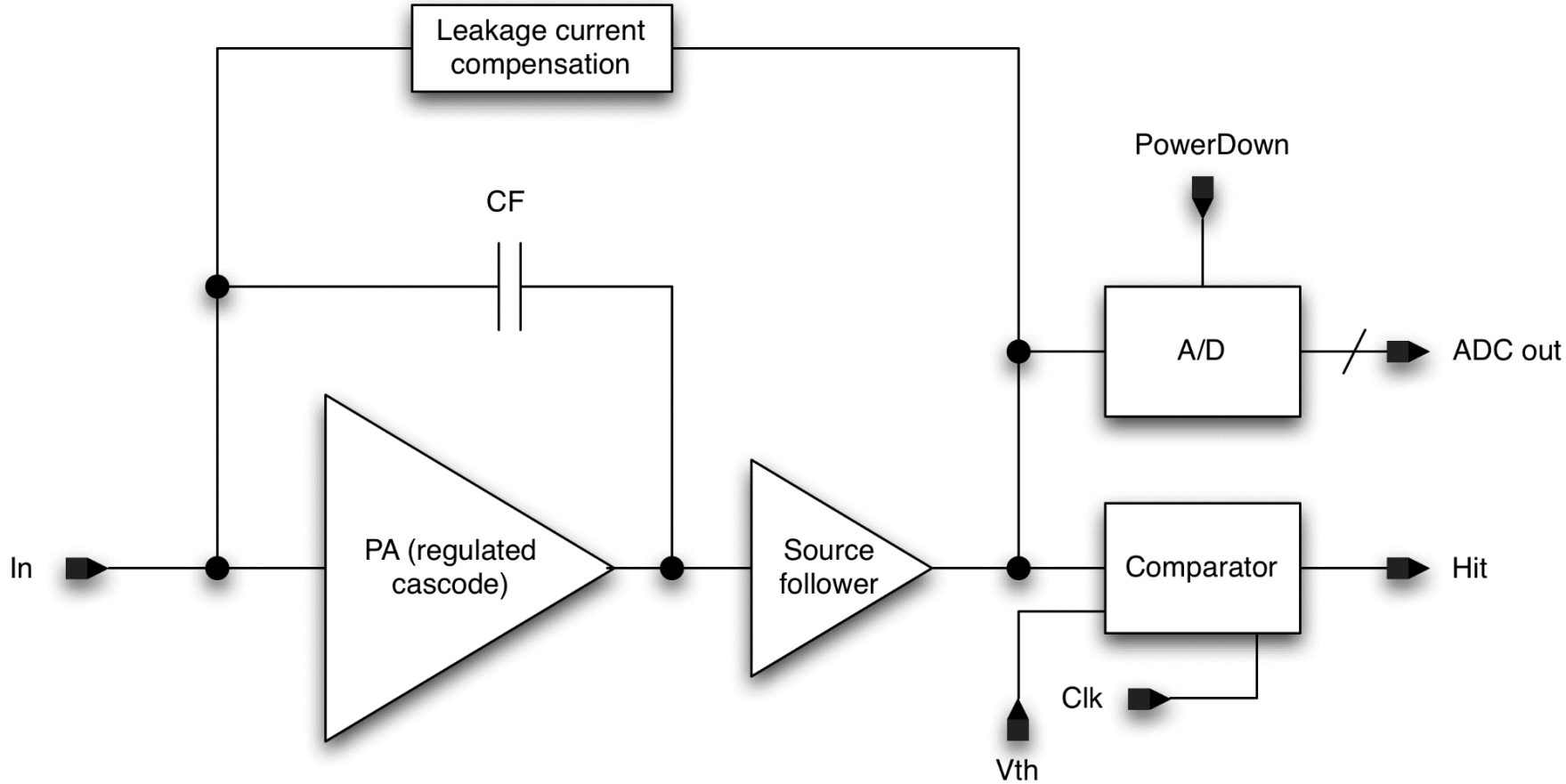


INFN-FNAL design



- 4 different AFEs. Test results on available prototypes look good (also after irradiation) – (INFN-FNAL design not yet tested)
- FE65-P2 and the CHIPIX65 demonstrators are going to provide essential information and experience in view of the integration of the analog FE in the RD53A chip. Test results on the FE65-P2 very encouraging
- The RD53A demonstrator will include several versions of the analog FE. They should be fully tested (also after irradiation) in their (almost) final version (schematic and layout) so that they qualify to be safely included in RD53A

IFCP65: Pixel analog front-end architecture



- Synchronous front-end
- Preamplifier (regulated cascode) featuring a leakage current compensation circuit
- Digital conversion immediately after the preamplifier

Post-layout simulation results (1/3)

	TT	TT 500 Mrad	SS	FF	FS	SF	RD53A spec
Charge sensitivity [mV/ke]	10.3	10.2	9.1	11.7	9.9	10.4	-
ENC rms [e]	79	79	82	76	83	77	<< 126
Threshold dispersion σ(Qth) rms [e]	35	-	-	-	-	-	<< 126
$\sqrt{(ENC^2 + \sigma(Qth)^2)}$ [e]	86	-	-	-	-	-	≤ 126
In-time overdrive [e-]	Not applicable						≤ 600
Current consumption [μA/pixel]	7.6*	7.2	7.6	7.6	7.6	7.5	≤ 4
Delay time [ns]	10.8	12.1	11.0	10.5	10.8	10.9	-
ADC Conversion time [ns]	12.5	12.5	12.5	12.5	12.5	12.5	-

- Detector capacitance CD=50 fF, T=27 °C
- In-time overdrive→ "0" in this AFE
- Delay time (comp flipping time – charge inj time) → 600 e-, Qin=1200 e-
- * ~5 uA/pixel when in binary mode. Comparator dynamic current not included

Post-layout simulation results (2/3)

	27°C	-20°C	RD53A spec
Charge sensitivity [mV/ke]	10.3	9.0	-
ENC rms [e]	79	82	<<126
In-time overdrive [e-]	Not applicable		≤ 600
Current consumption [μA/pixel]	7.6*	7.4	≤ 4
Delay time [ns]	10.8	9.9	-
ADC conversion time [ns]	12.5	12.5	-

- Detector capacitance CD=50 fF, T=27°C
- In-time overdrive→ "0" in this AFE
- Delay time (comp flipping time – charge inj time) → 600 e-, Qin=1200 e-

* ~5 uA/pixel when in binary mode. Comparator dynamic current not included

Post-layout simulation results (3/3)

- Data obtained by applying an AVDD'=AVDD-ΔV, AVSS'=AVSS+ΔV to the pixel and AVDD, AVSS to the peripheral biasing blocks

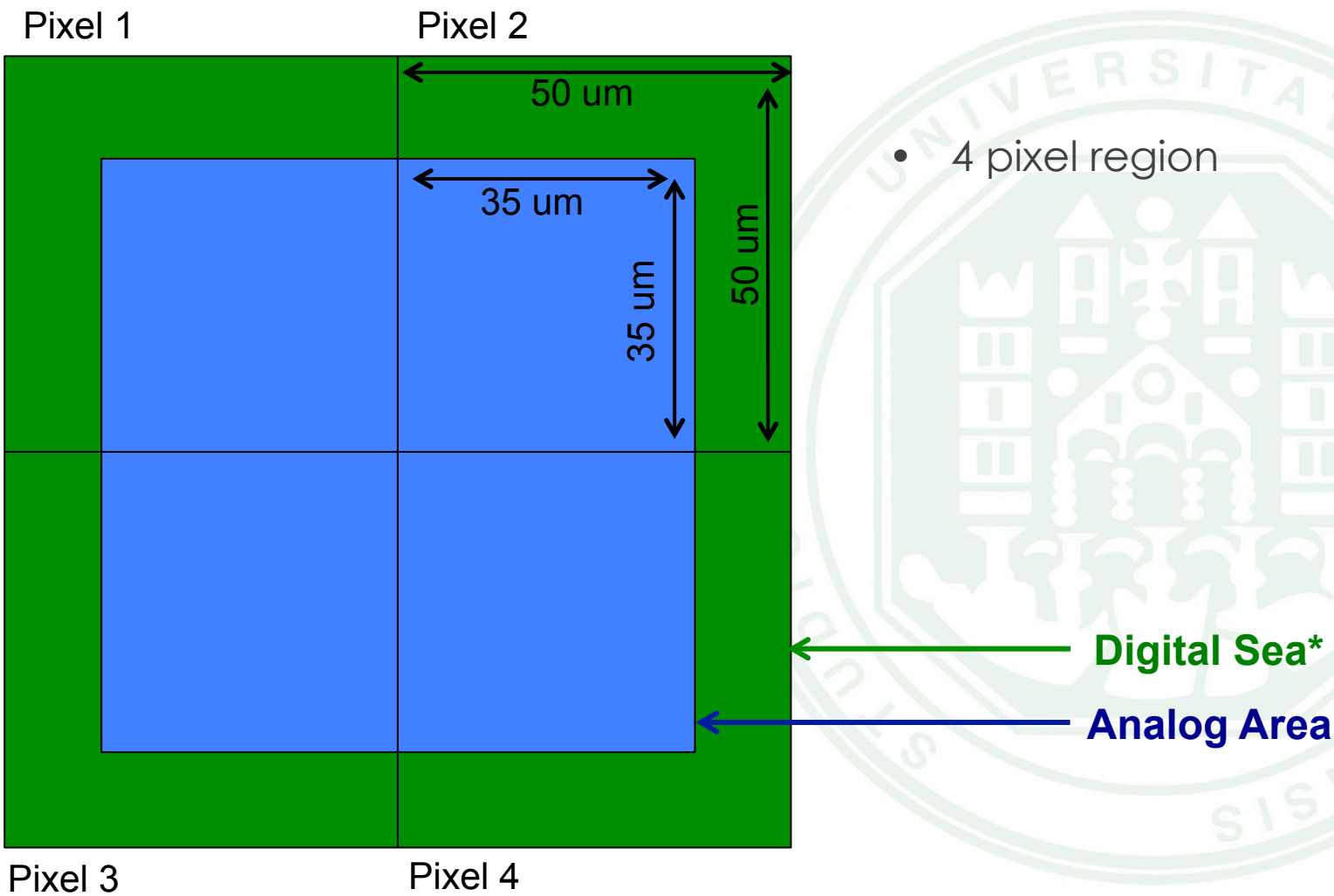
	ΔV=0mV	ΔV=10mV	ΔV=20mV	RD53A spec
Charge sensitivity [mV/ke]	10.3	9.9	9.7	-
ENC rms [e]	79	82	84	<< 126
In-time overdrive [e-]	Not applicable			≤ 600
Current consumption [μA/pixel]	7.4*	6.7	6.1	≤ 4
Delay time [ns]	10.8	10.7	11.6	-
ADC conversion time [ns]	12.5	12.5	12.5	-

•Detector capacitance CD=50 fF, T=27°C
•In-time overdrive→ "0" in this AFE
•Delay time (comp flipping time – charge inj time) → 600 e-, Qin=1200 e-
* ~5 uA/pixel when in binary mode. Comparator dynamic current not included

Changes on IFCP65 for RD53A

- The analog Front End is NOT integrated in the global substrate.
- 2 different Deep - Nwell:
  - 1 analog
  - 1 digital
- Preamplifier surrounded by a guard-ring
- 3-level calibration circuit integrated in the pixel
- 2 comparators for performing 2-bit ADC + 1 Hit comparator

Pixel layout floorplan

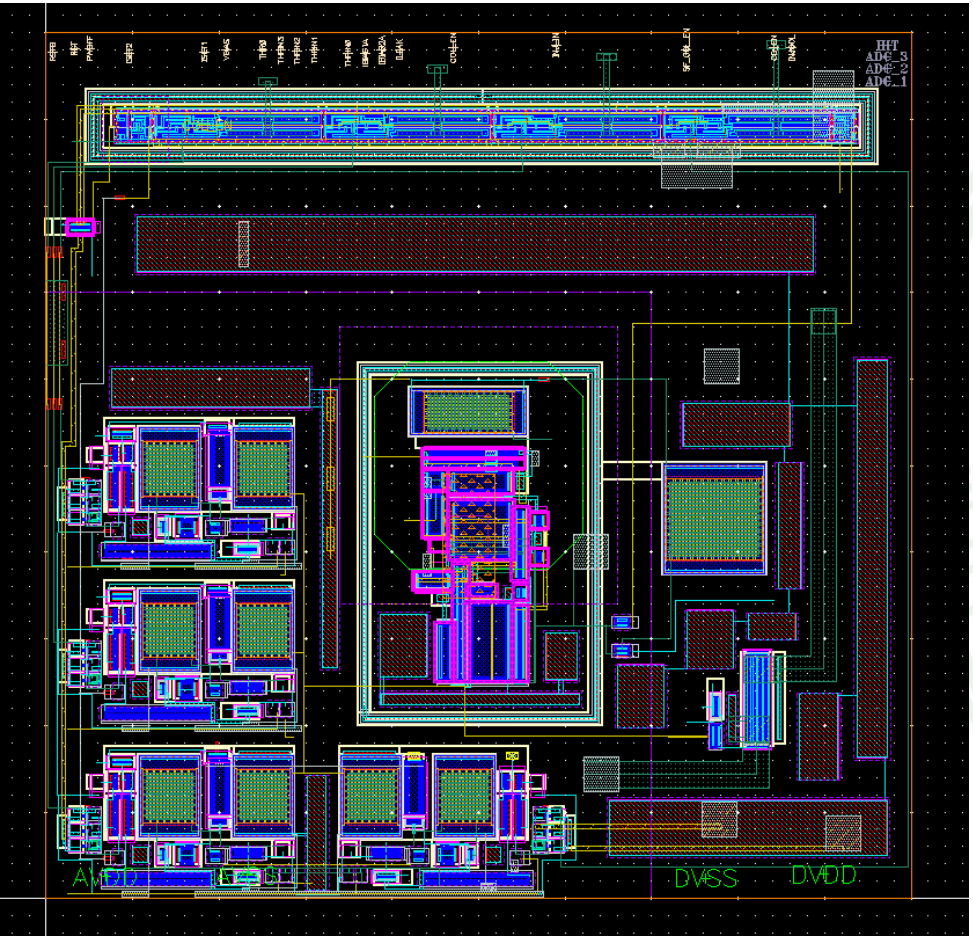


- 4 pixel region

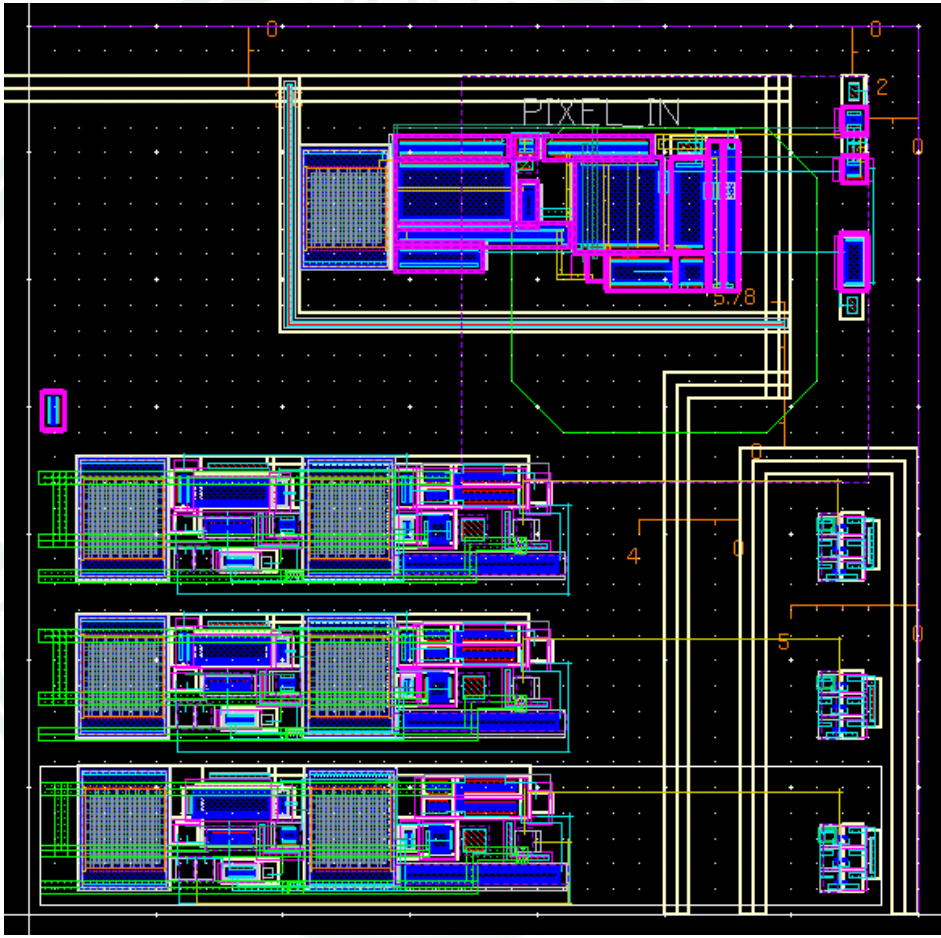
* *see Farah F. presentation for details*

Pixel layout comparison

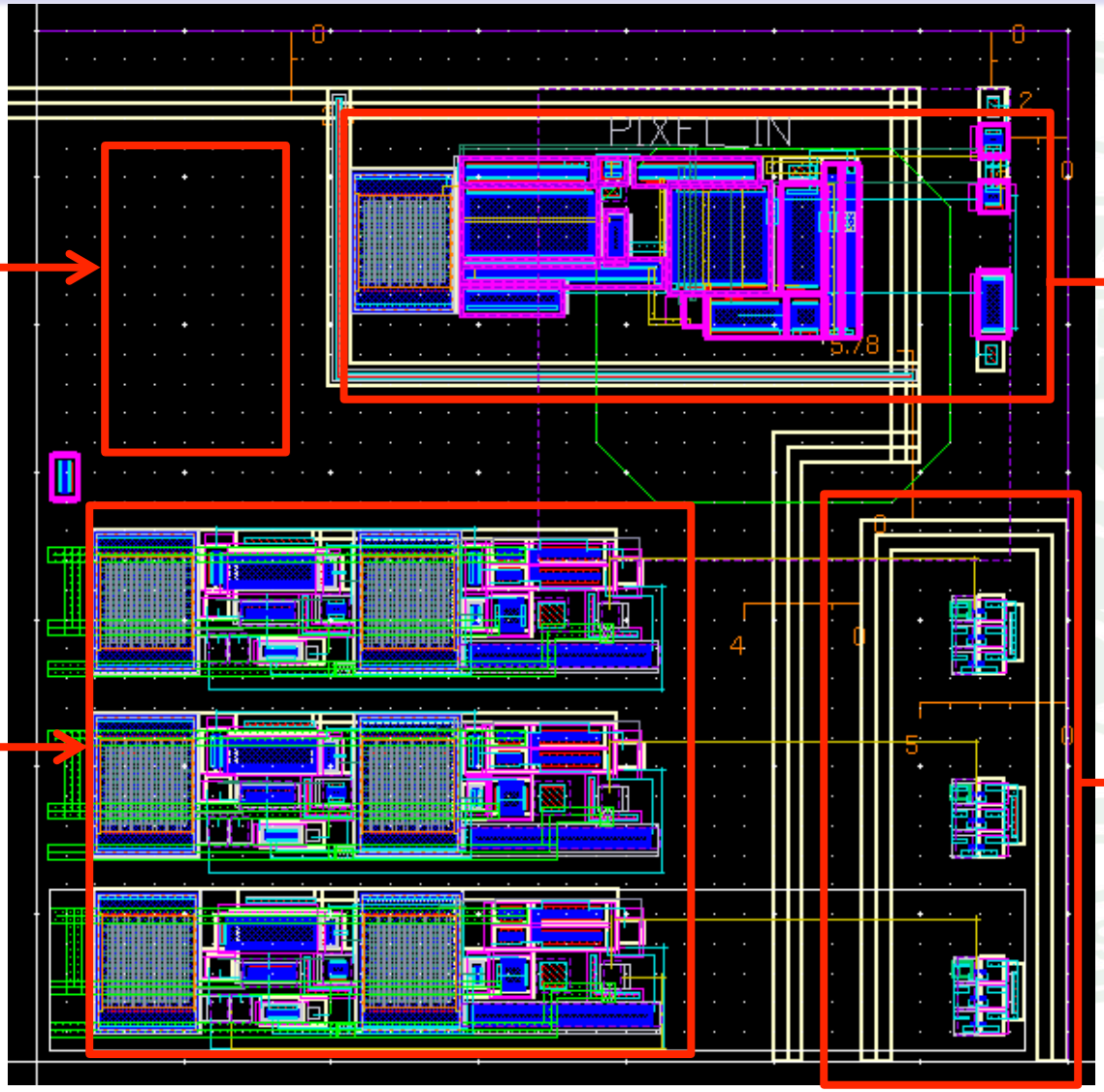
IFCP65



IFCP65 for RD53A



Pixel layout



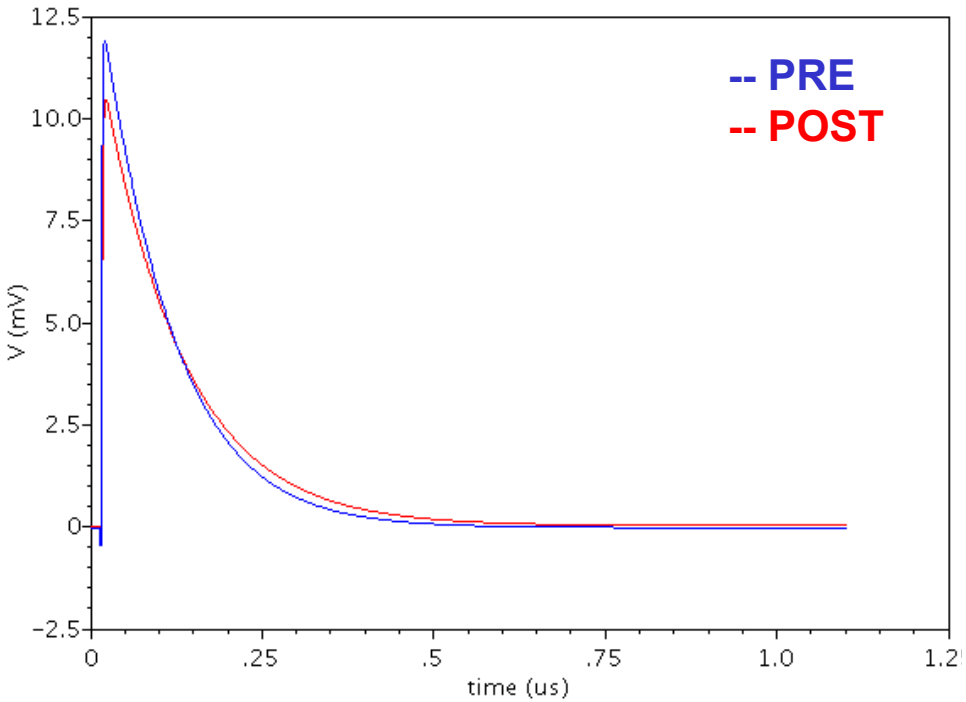
Calibration circuit

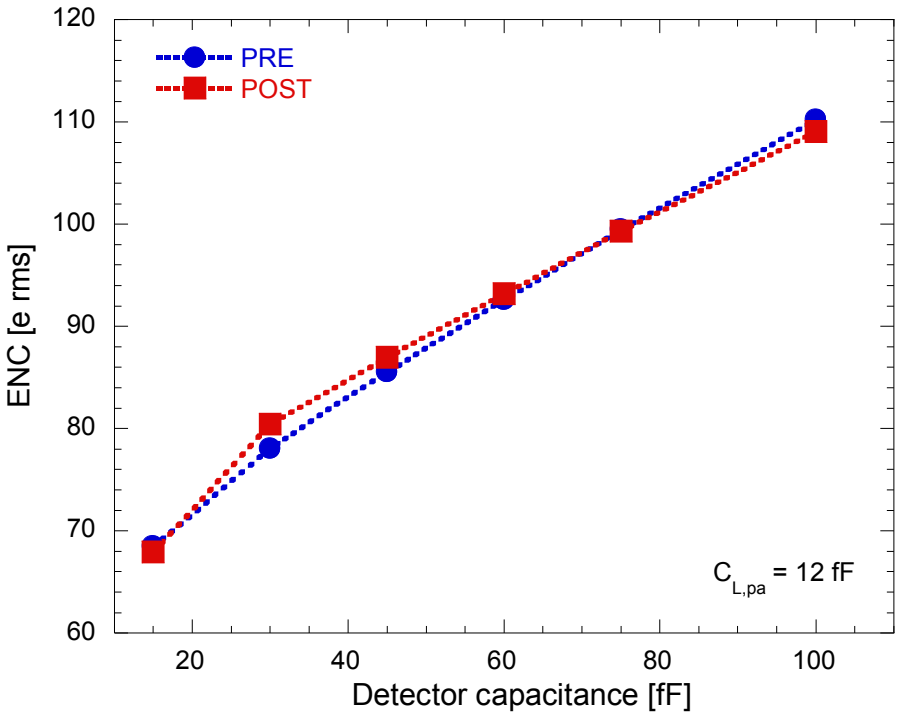
Preamplifier

2 bit ADC

Digital DNW

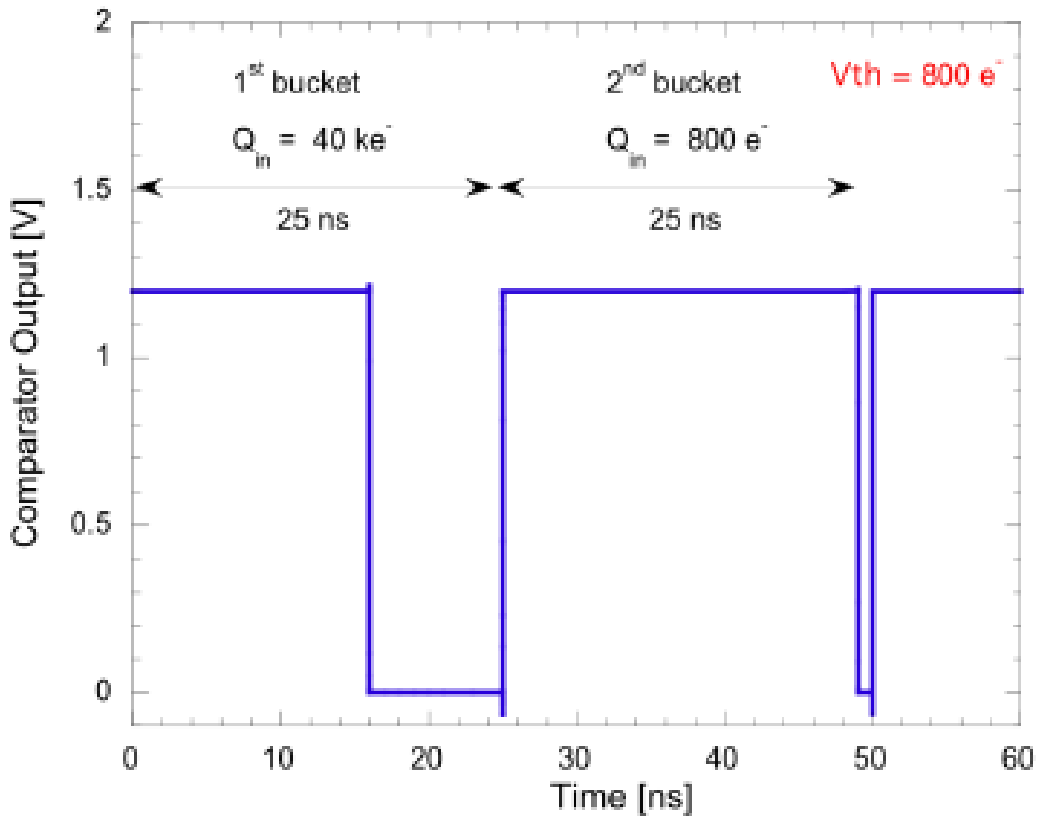
Preamplifier output response and noise





- ≈ 3 ns PA rise time @ Qin = 1ke-
- Leakage compensation circuit works fine for detector current up to 14 nA
- ENC < 110 e- @ CD = 100 fF

Comparator transient simulation



- Comparator able to detect two consecutive hits (large signal followed by a signal closed to threshold)

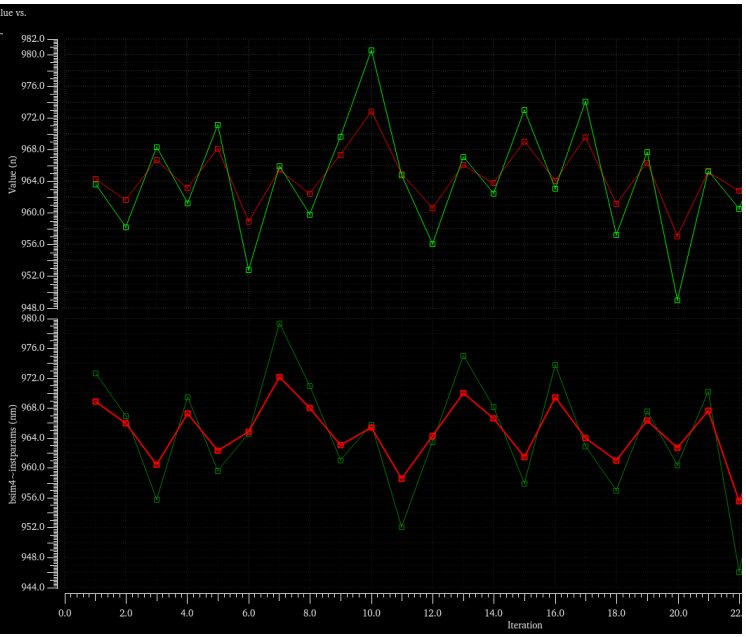
Monte-Carlo simulations

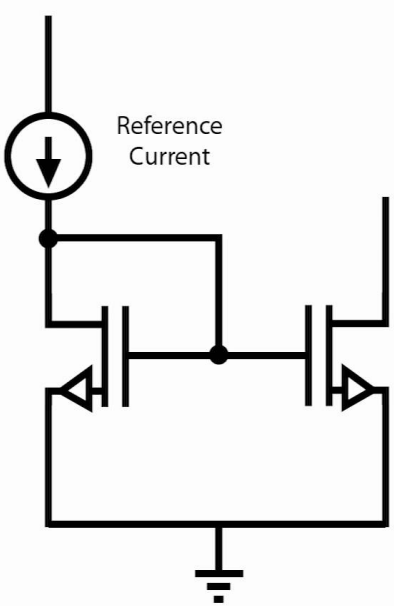
- *Definition*:

Simulations used to model the probability of different outcomes in a process that cannot easily be predicted due to the intervention of random variables.

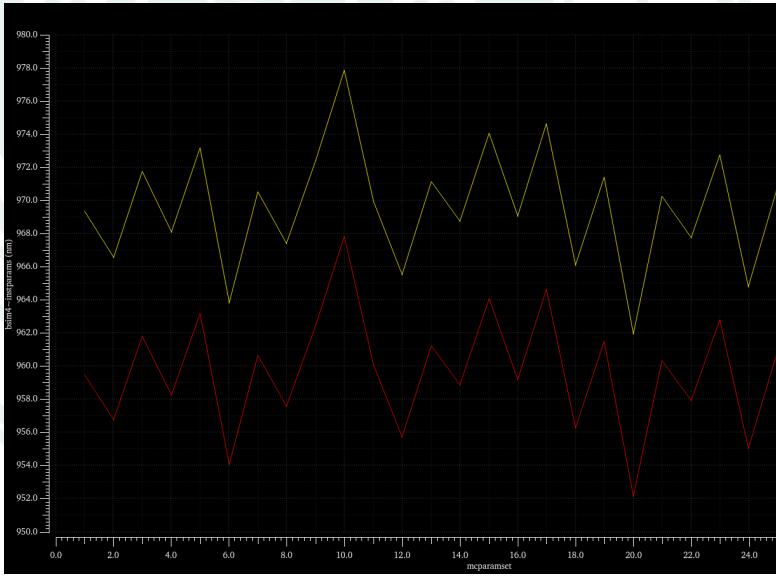
- *Parameters correlated on Mismatch*
  - *Mismatch_sigma = Mismatch factor in Gauss distribution;*
  - *Local mismatch effect = this function provides an option for mismatch effect;*

σ variation



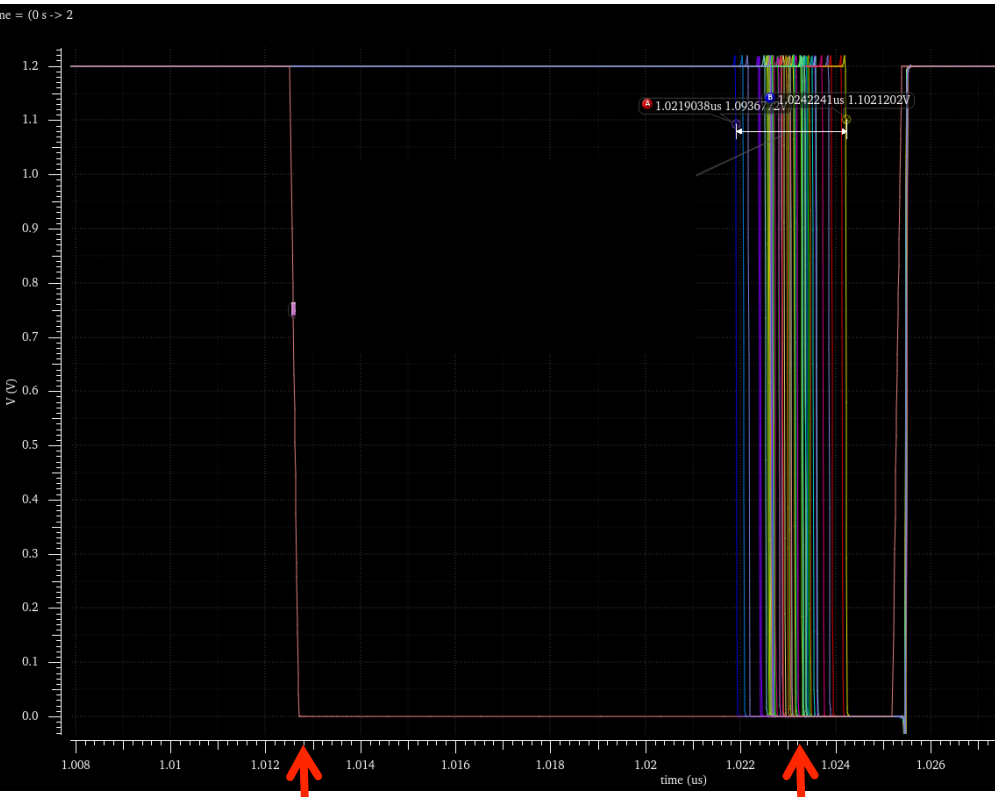


4 corner MC simulation



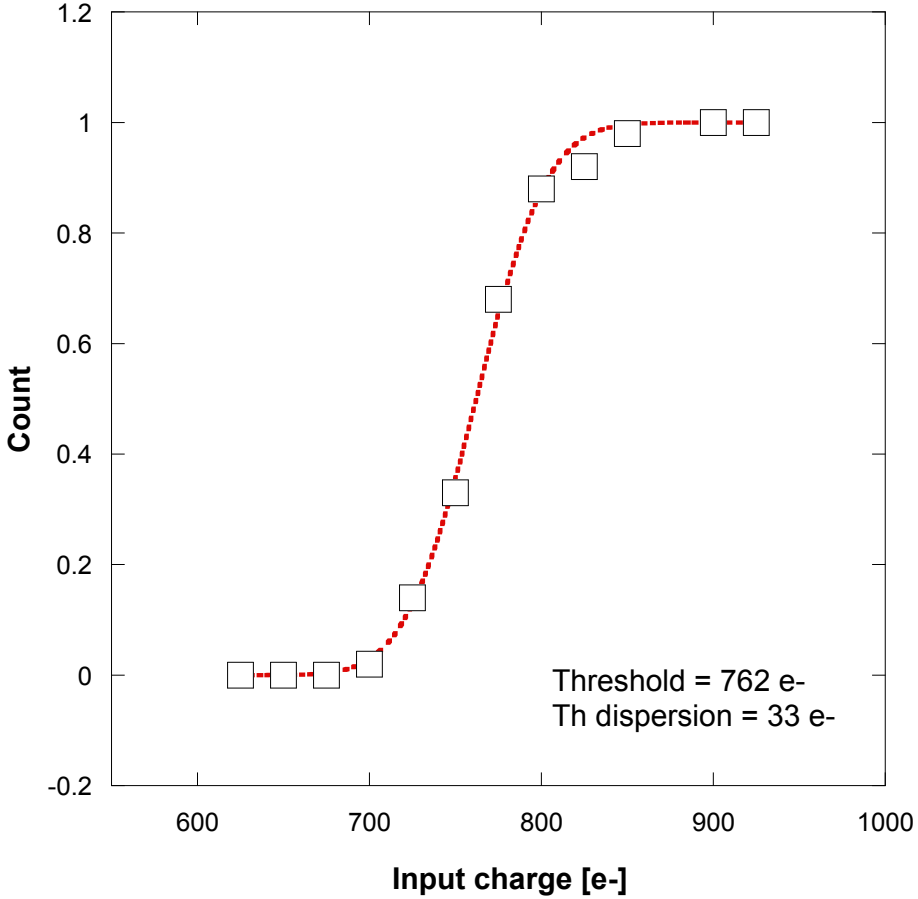
Monte-Carlo results

- *Threshold dispersion analysis*



Reset

Hit comparator outputs



AFE analog bias

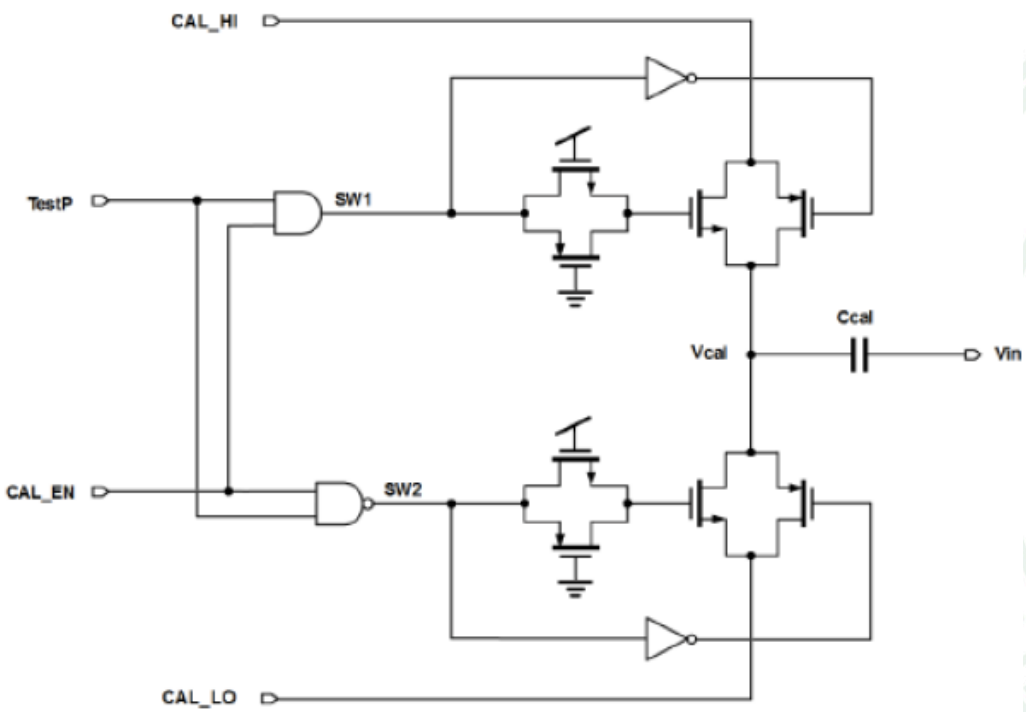
Preamplifier:

- Preamplifier input branch current reference: **2 uA**
- Preamplifier source follower branch current reference: **2 uA**
- preamplifier ileak: **16 nA**

Threshold discriminator:

- Comparator input branch current reference: **750 nA**
- Comparator second branch current reference: **150 nA**
- Voltage reference for the cascode device in the comparator first branch: **800 mV**
- Threshold voltages for the four comparators

Charge injection circuit



- Local generation of the analog test pulse starting from well defined DC voltages distributed to all pixels
- The calibration system features the possibility of randomly selecting the pixel cells where pulses are injected
- Three-level calibration circuit allowing for charge injection in consecutive BX periods
- A step voltage signal will be provided to selected pixels
  - Fall time of the step voltage signal: < 5 ns
  - Qin up to 25 ke-

Digital readout architecture

The architecture of signal processing & data:

Design of ASIC front end for COMPACTIFICATION

- ***SPARSIFICATION: data reduction***
- ***CLUSTERIZE information from the detector including Intelligence and digitize on Front-End signal***
- ***Organize the flux of data in the overall DAQ system***

New readout architecture to evaluate*

Courtesy of FE-I4 summary, Malte Backhaus, DESY course, April 2011

- Hit storage in pixel array; data passed to periphery only if there is a trigger.
- Minimum amount of logic in pixel array; all complexity associated with trigger is in chip periphery.

- Hit anywhere in column cause BX number to be stored in CAM
- Design a low-power and compact **Content Addressable Memory (CAM)** in End-Of-Column

** see D. Christian's presentation*

Conclusion and future plans

- First version of the analog front-end with low power **preamplifier** and high speed **comparator layout** has been designed.
- Such a design is in accordance with specification and rules of RD53A
- Develop and test new ideas for the intelligent digital readout of pixel detectors at extreme data rates.

Acknowledgments

RD-53 Collaboration

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