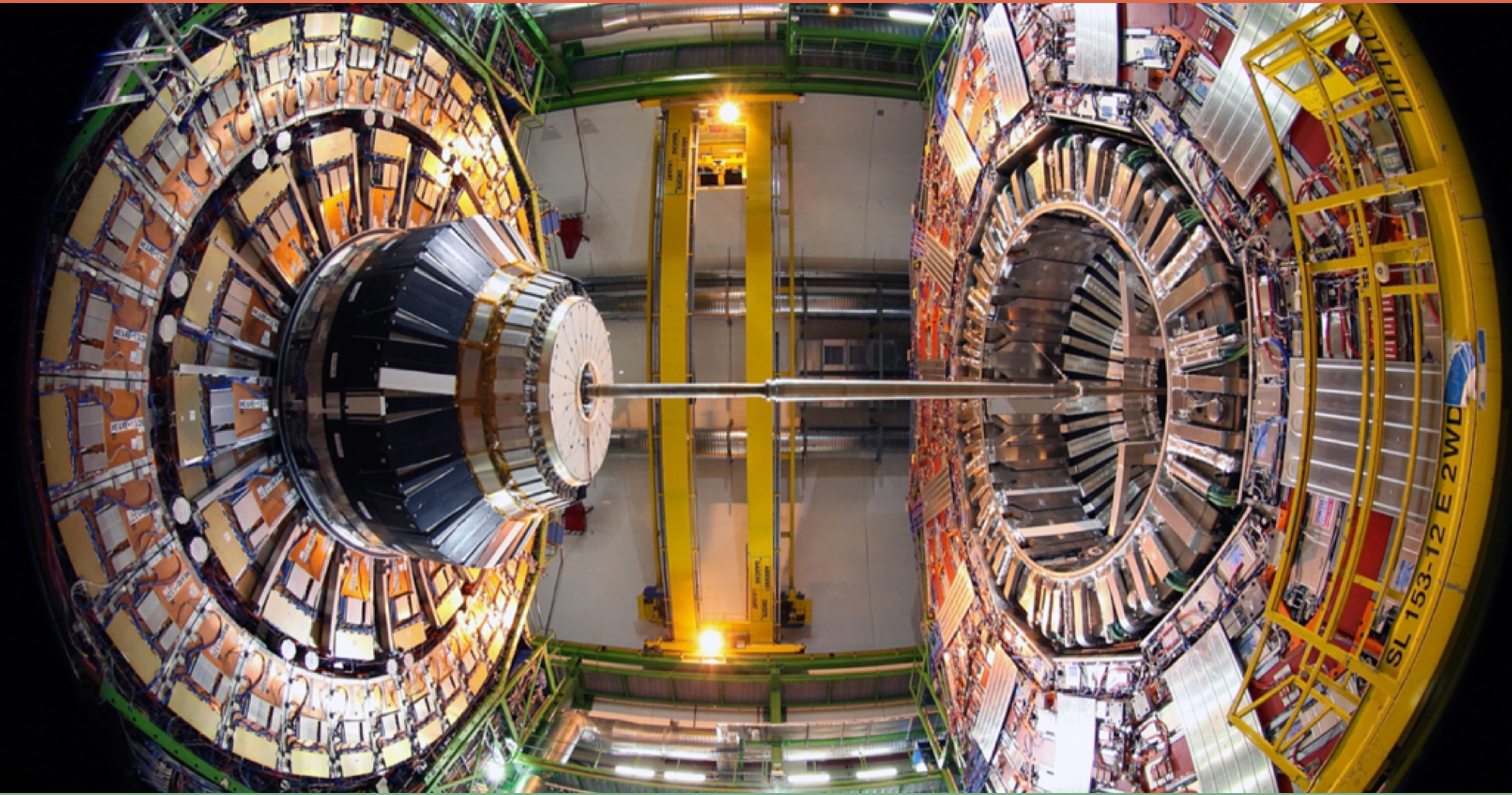
CMS Endcap Calorimeter Upgrade, HGCal



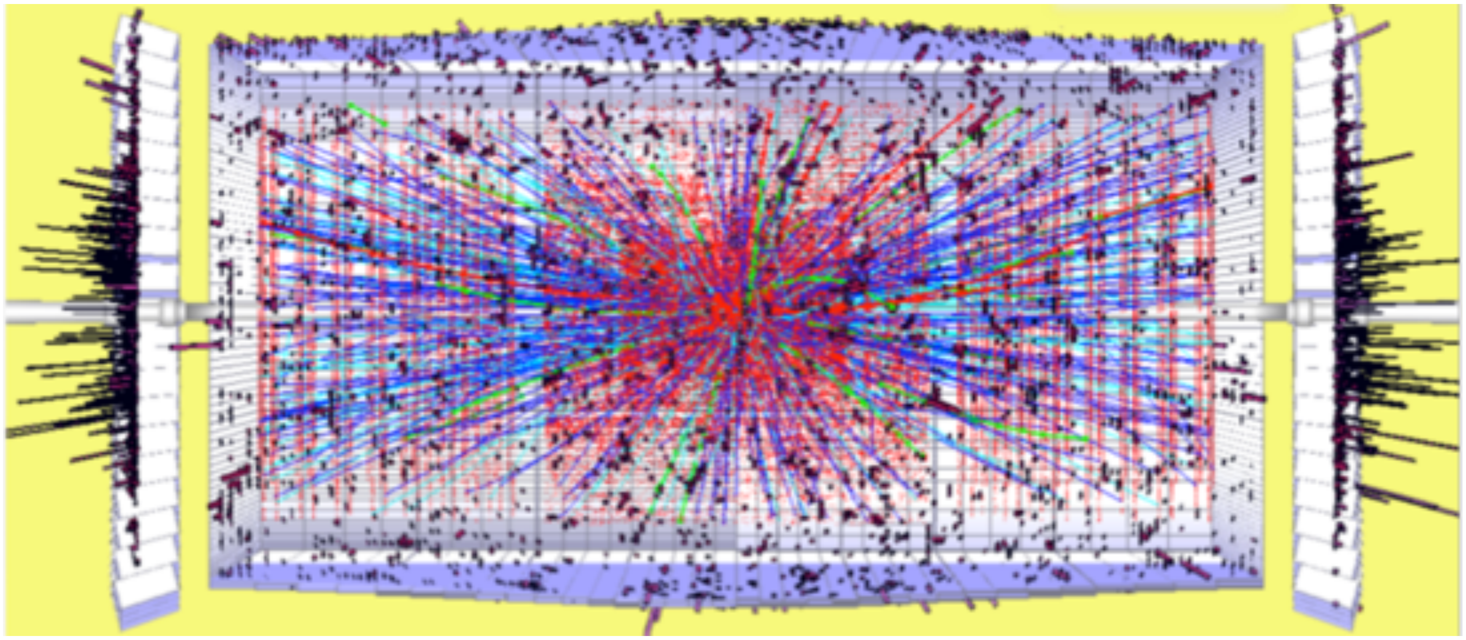
Zoltan Gecse Fermilab

On behalf of CMS Collaboration

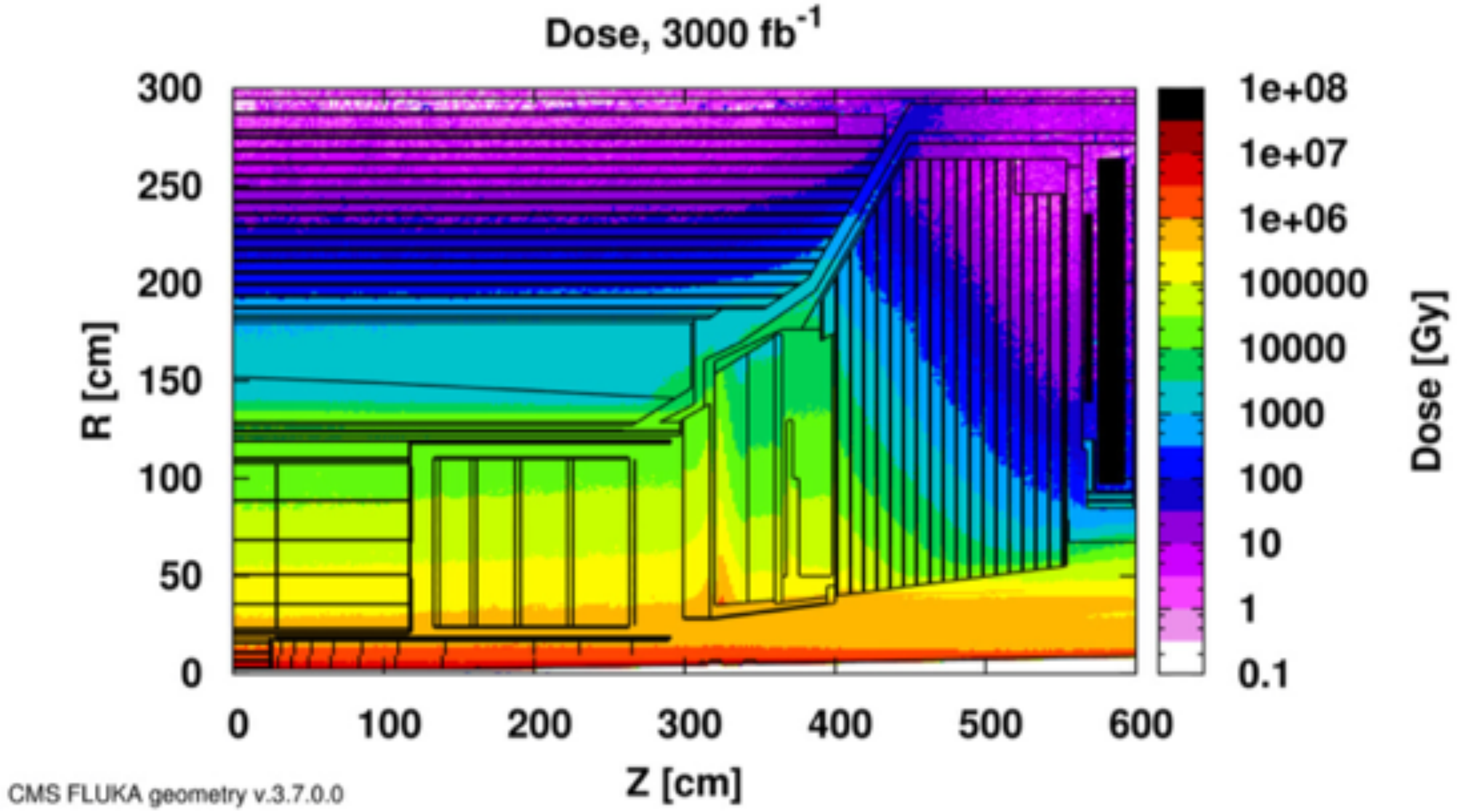
October 17, 2016, INFIERI

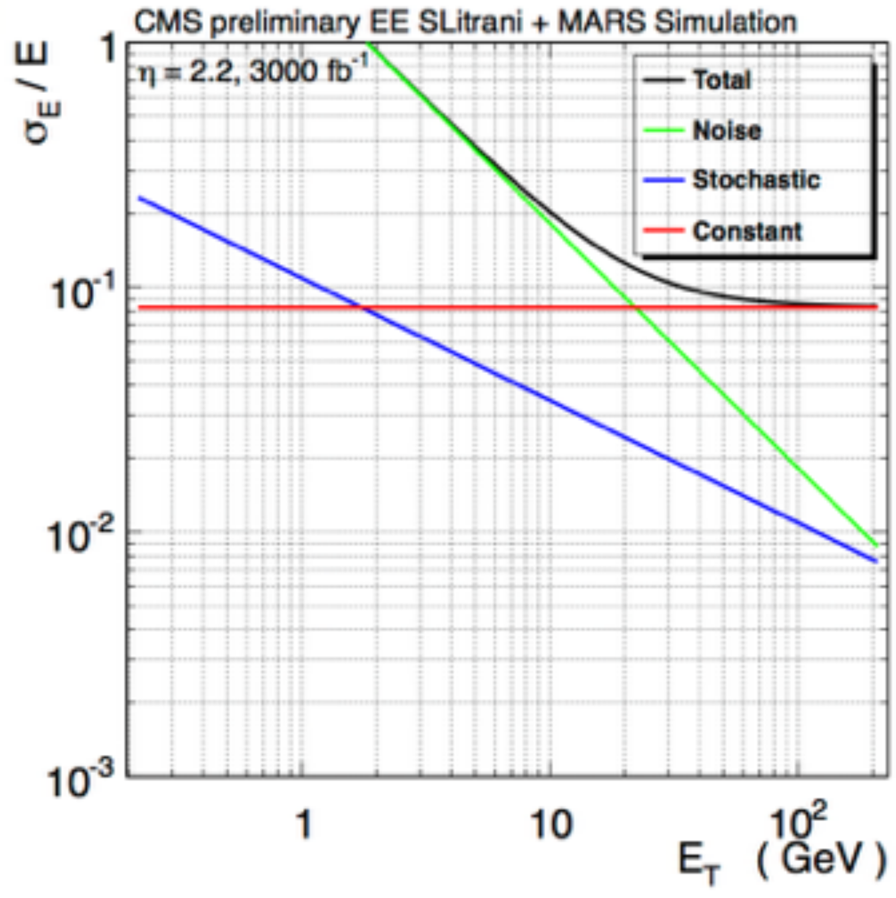
Challenges at HL-LHC

- **HL-LHC plans 5e34/cm^2/s instantaneous luminosity and 3000/fb integrated**
  - High pile-up conditions (200 PU)
  - High radiation dose (150Mrad, 10^{16}n/cm^2)
  - Resolution of current endcap EE increases to O(10%)

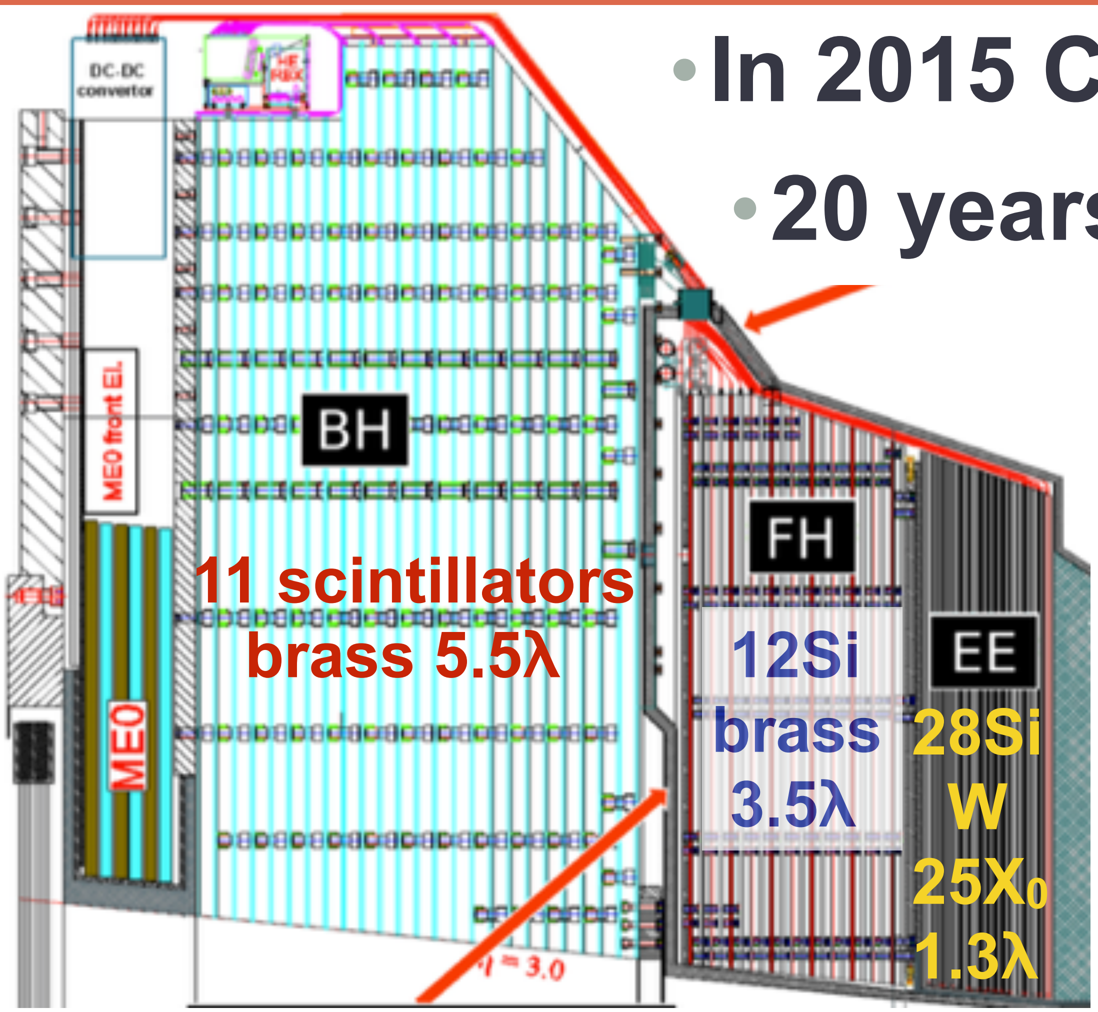


- **Endcap Calorimeter needs replacement**





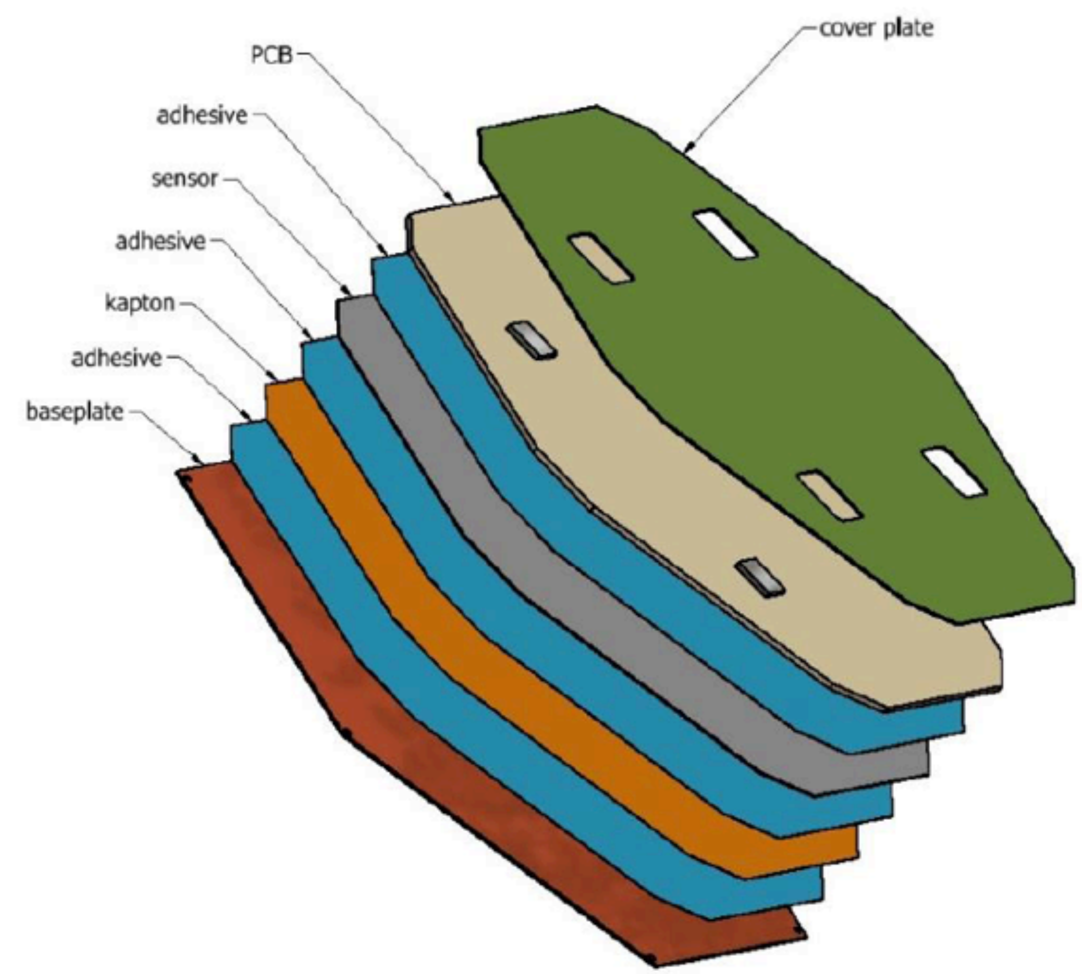
The HGCal Endcap Design

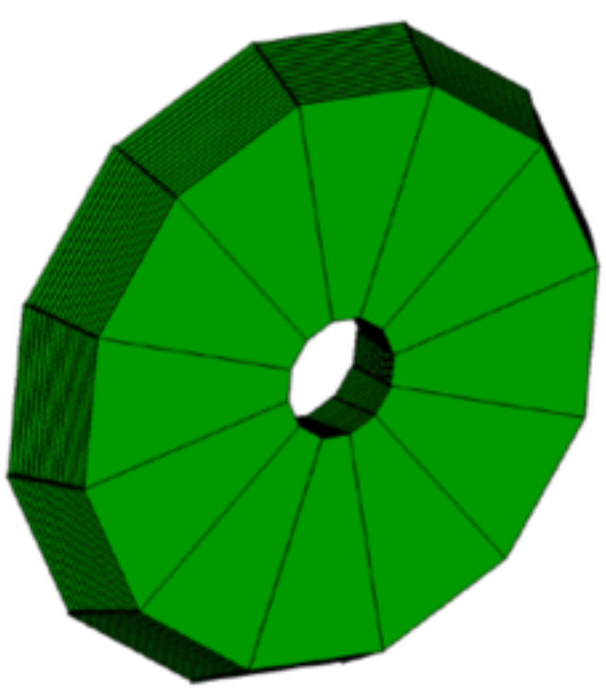


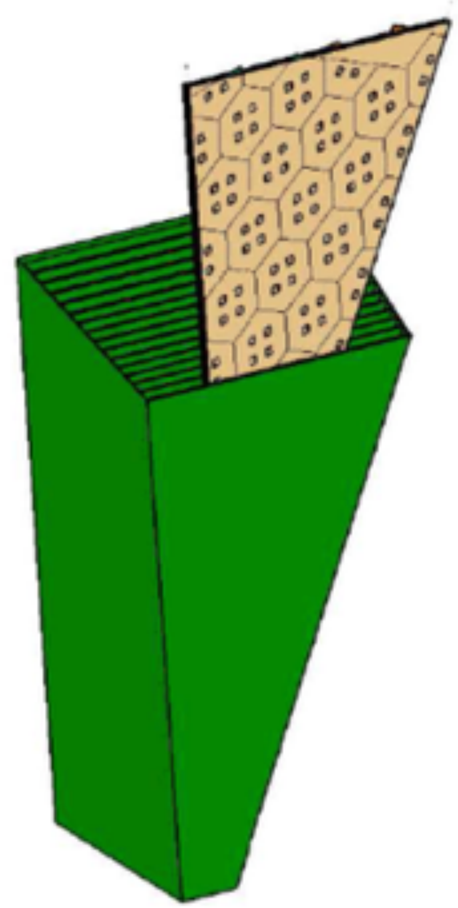
- **In 2015 CMS chose a silicon based calorimeter**
  - **20 years of experience from tracker and pixel**
    - **Radiation effects are well understood and manageable with -30C temperature operations**
    - **High granularity and fast timing capability help mitigate pile-up**
    - **Electronics in 130/65nm allows low noise and low power readout even for large dynamic range**
- **Key parameters:**
  - 600 m^2 of silicon
  - 6M readout channels, 0.5-1 cm^2 area cells
  - 21660 modules (8” or 2x6” sensors)
  - 115kW power at end of life

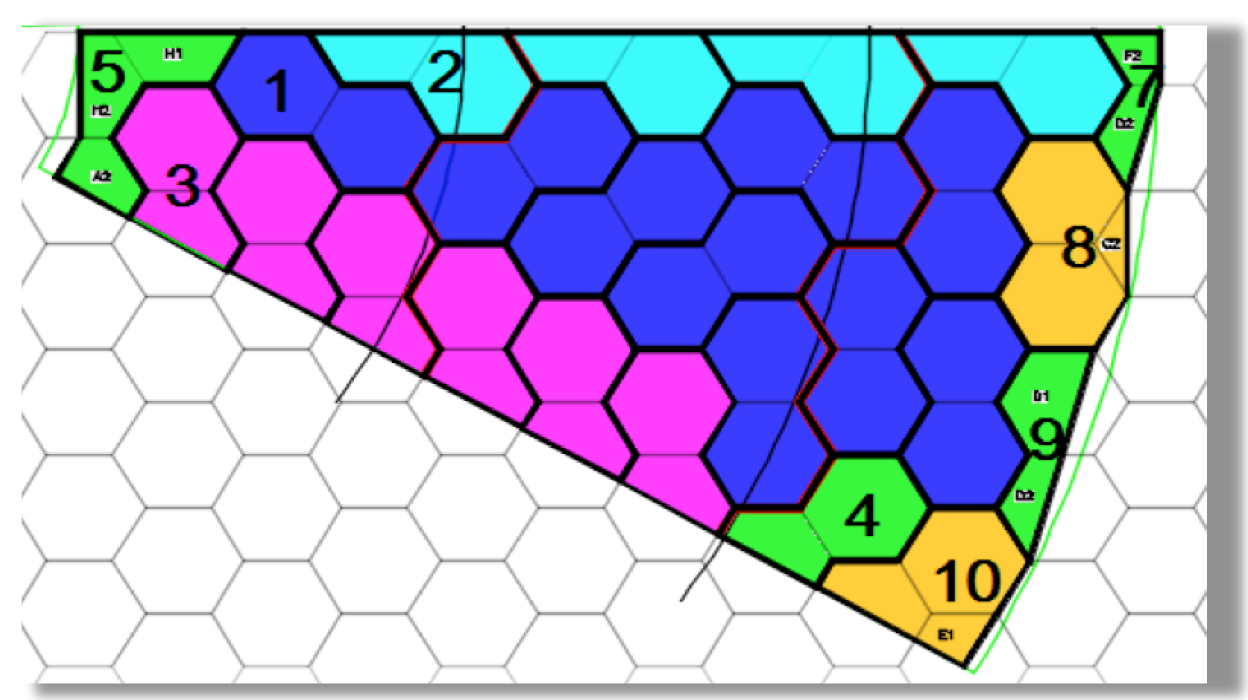
Construction

- Modules built from W/Cu baseplate,hexagonal sensors and readout PCB
- Cassettes built from modules and Cu cooling plate
- Cassettes inserted into absorber





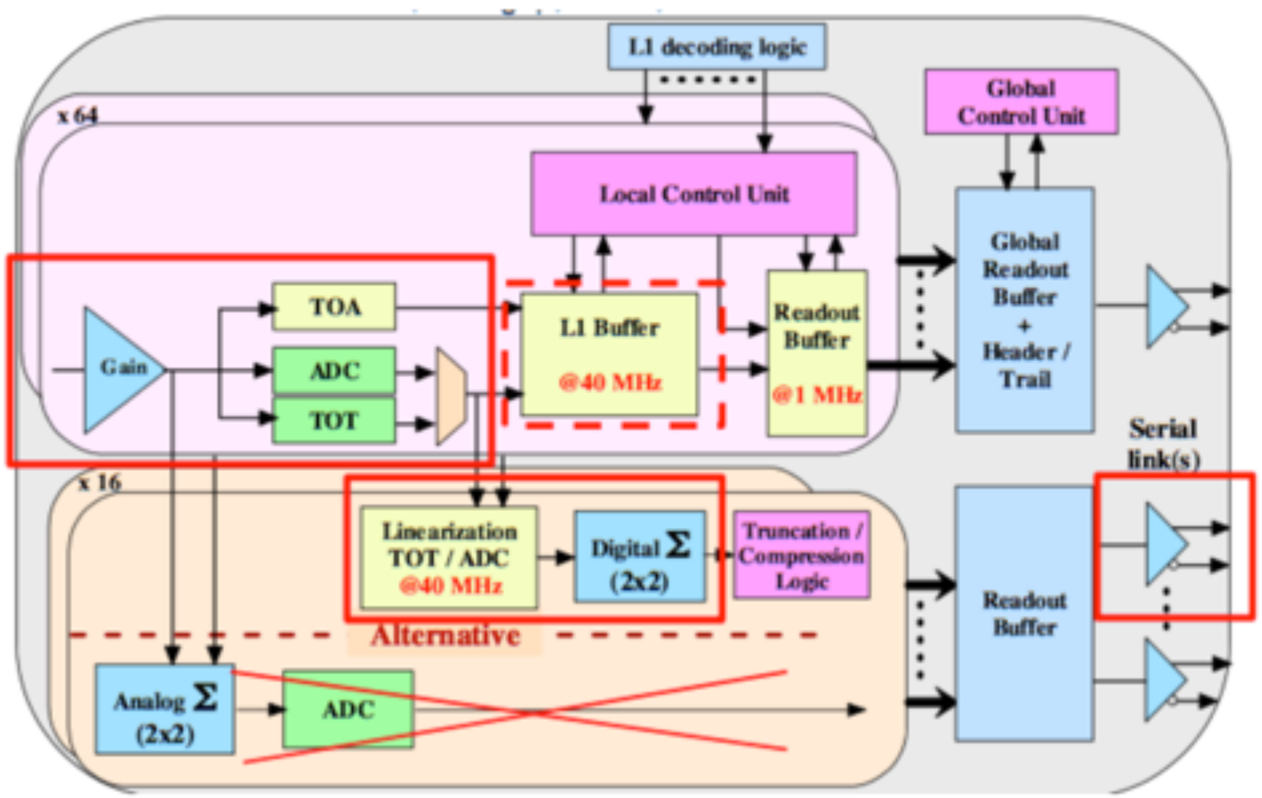




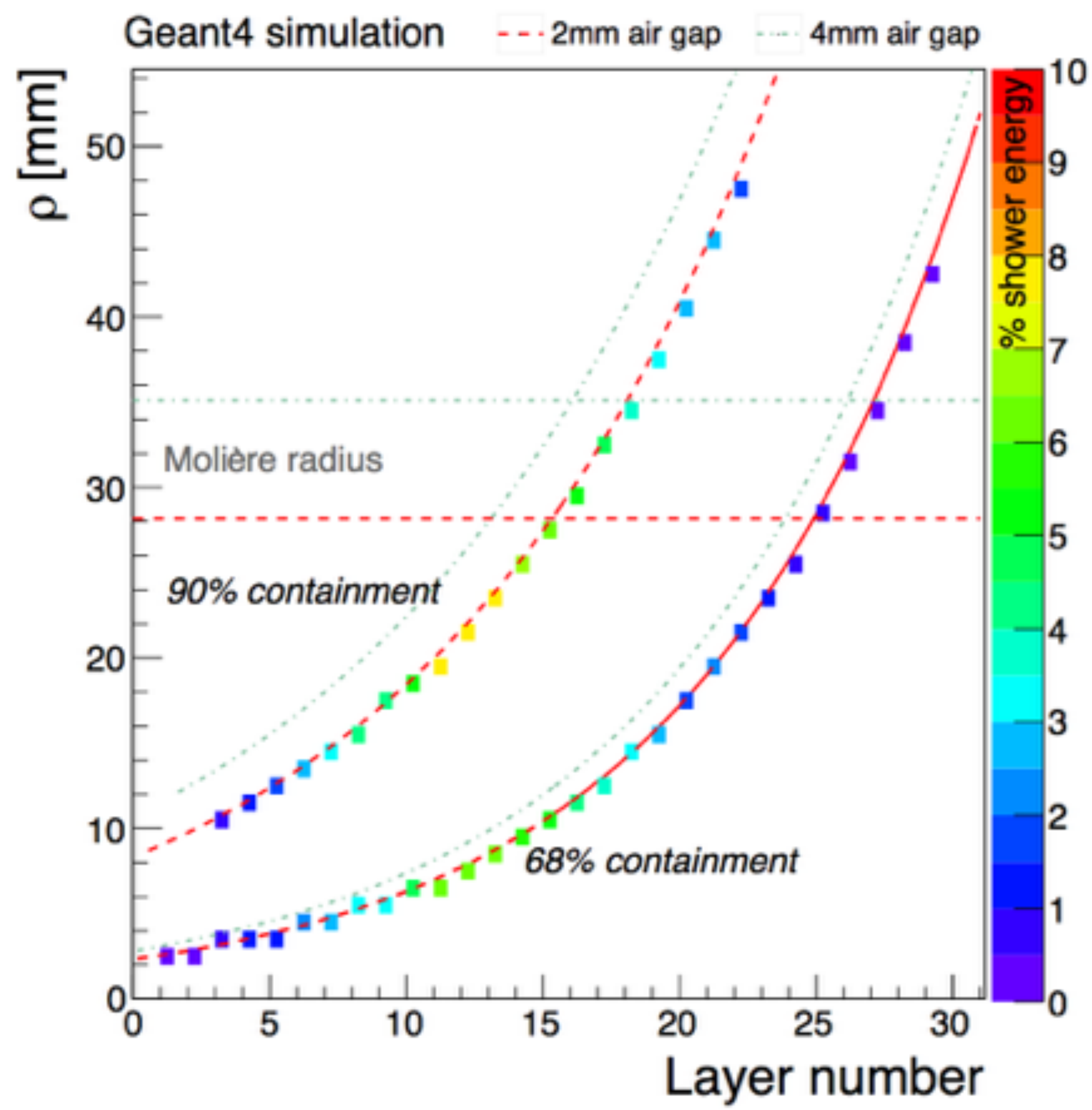
Front-end Electronics

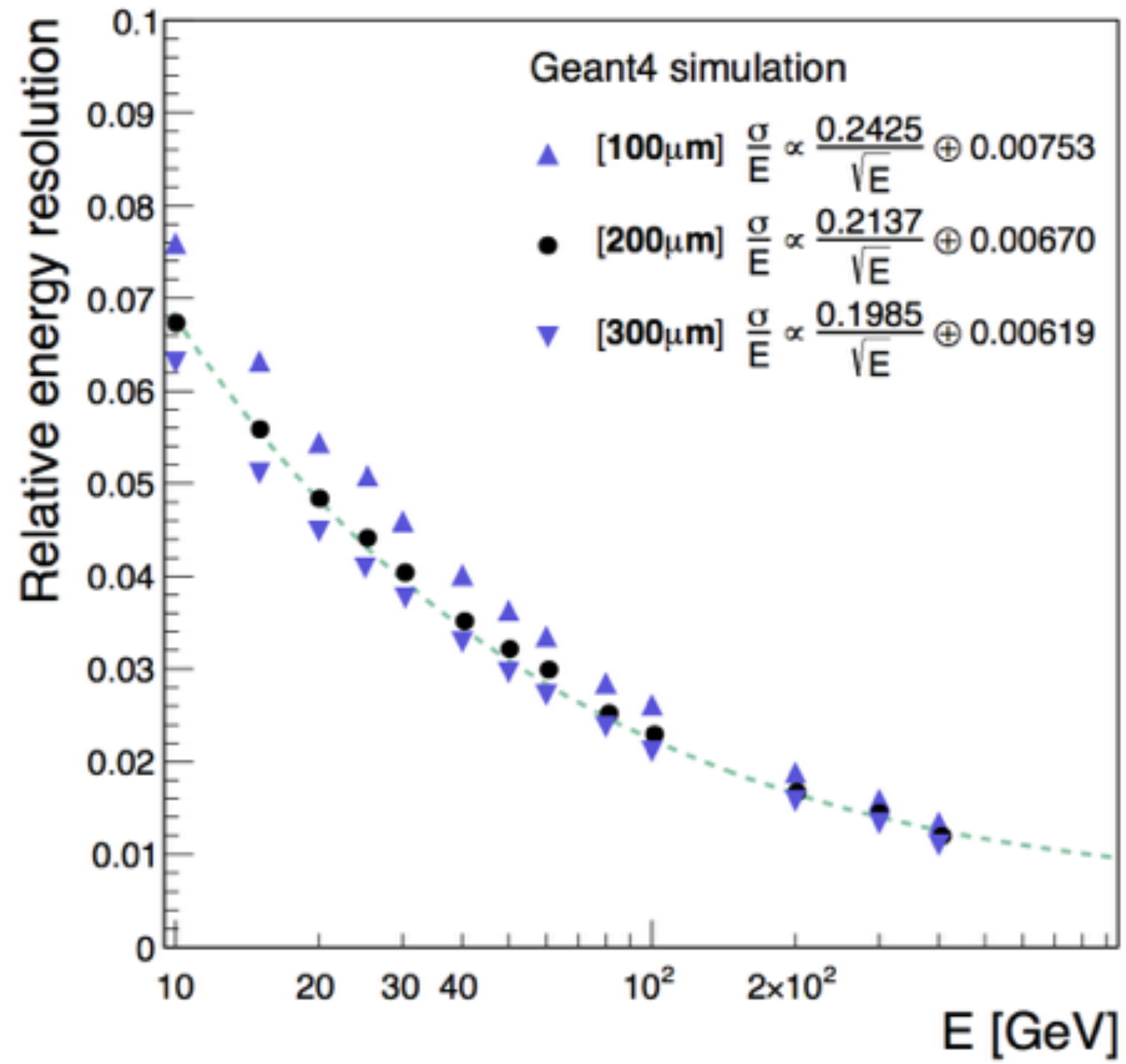
Very stringent requirements for Front-End Electronics

- Large dynamic range 0.4 fC – 10 pC (15 bits)
  noise < 2000 e- to keep MIP visibility for low thickness sensors after 3000 fb-1
- Leakage current compensation
- Low power budget < 10 mW/channel
- Timing information 50 ps accuracy
- System on chip (digitization, processing), high speed readout (>Gb/s), large buffers to accommodate 12.5μs latency of L1 trigger
- Preferably compatibility for positive and negative inputs.
- High radiation resistance (150 MRad, 10^{16} n/cm^2)



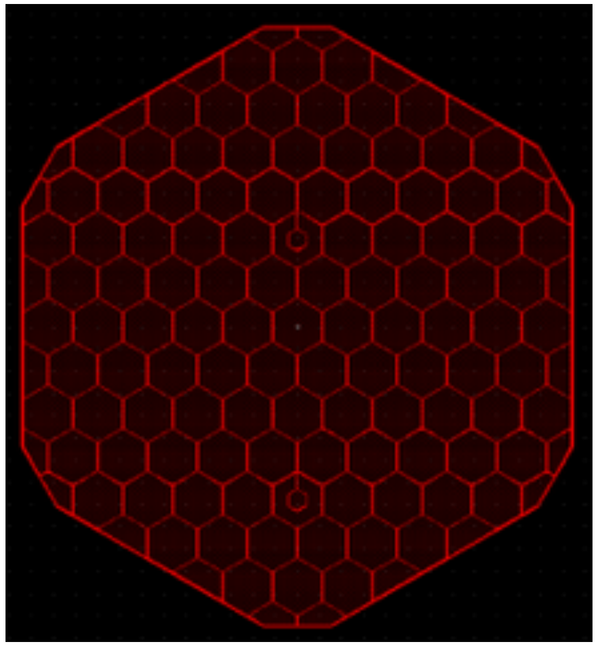
Expected Performance

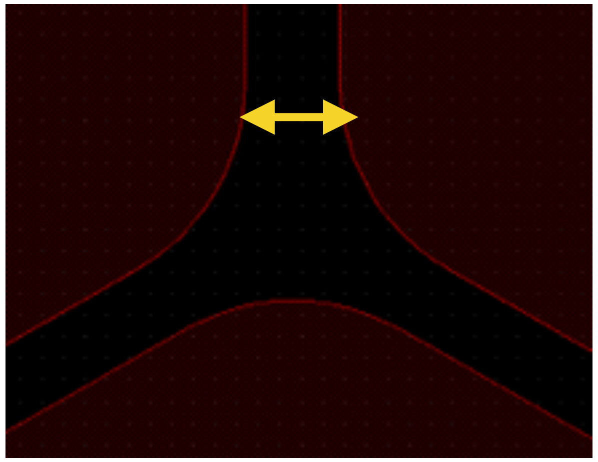


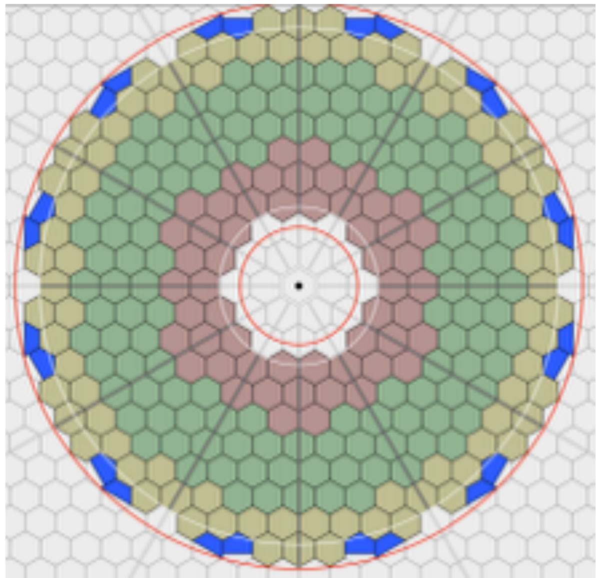


- **Electromagnetic showers narrow**
  - pile-up rejection
  - good separation for particle flow approach
  - minimize thickness in design
- **Energy resolution EM**
  - stochastic term ~20%
  - target constant term < 1%

Silicon Sensor R&D



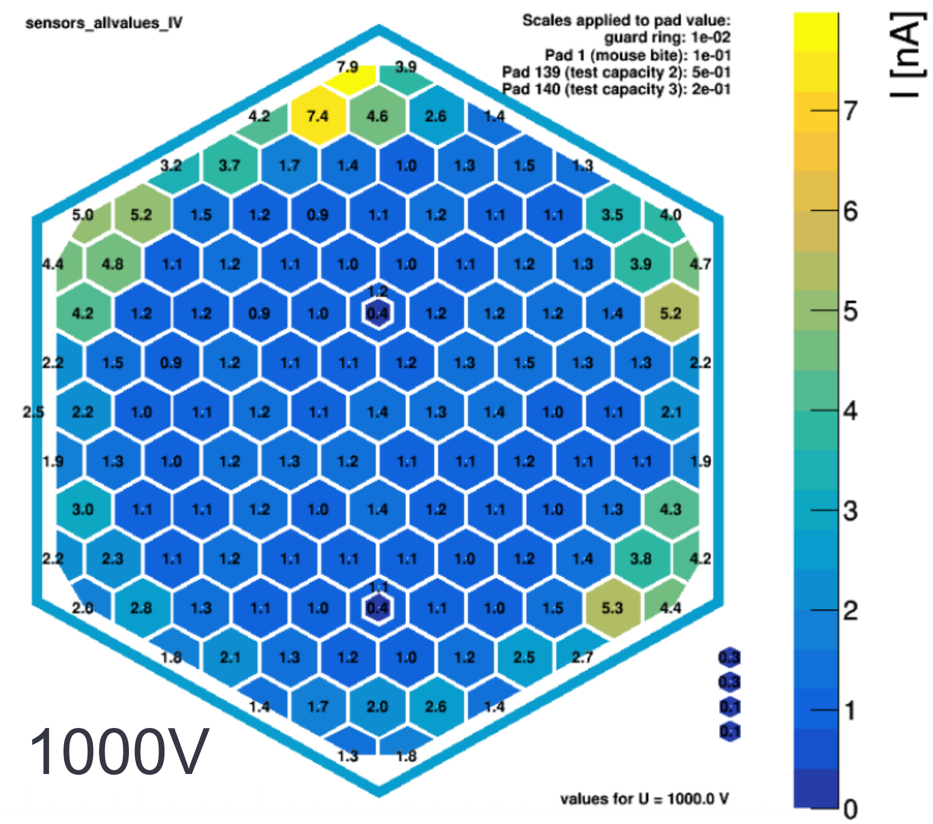


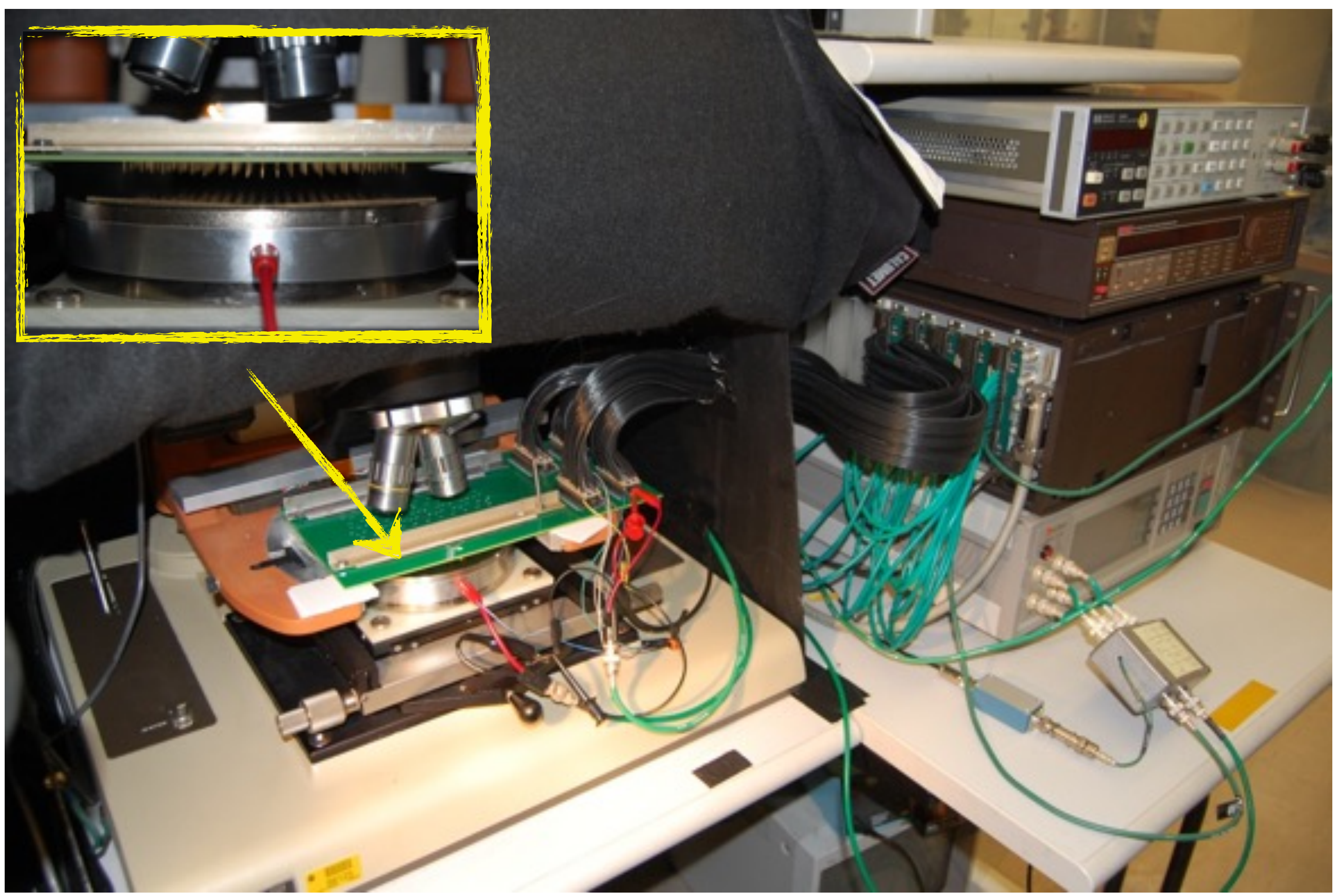


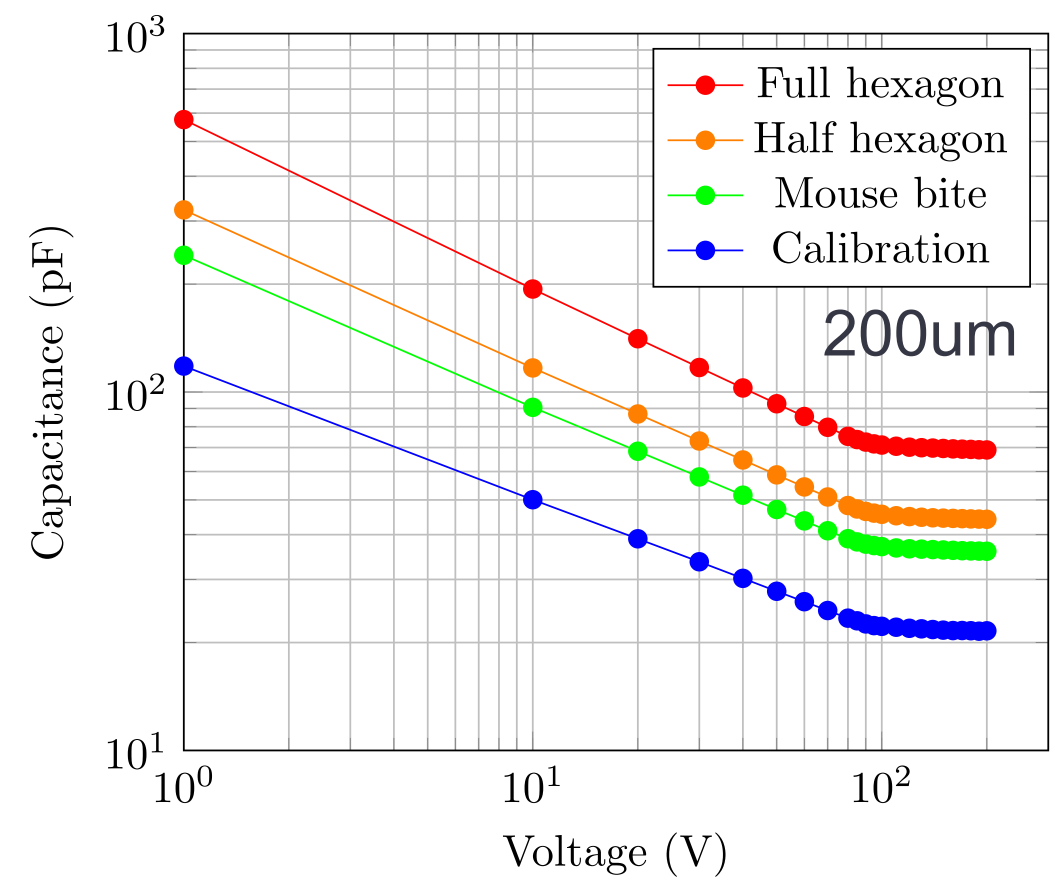
- **Hexagonal sensors from 6” vs 8” wafers**
  - 8” wafers offer lower costs
- **Inter cell distance (20um - 80um)**
  - The larger the distance the smaller the inter-cell capacitance
  - The smaller the distance the larger the break down voltage
- **p-type vs n-type**
  - n-type are cheaper but at highest fluences less radiation tolerant
- **Active layer thickness (100um - 300um)**
  - at high fluences thinner ~100um sensors give more absolute collected charge than 200 or 300um ones
- **Comparison of performance of sensors from various vendors**
  - HPK: 6” n-type fabricated and tested, p-type to be ordered
  - Infineon and HPK: 8” p-type are being fabricated
  - Novati: half of 6” p-type from 8” wafer being tested

HPK Sensor Testing at Fermilab

- **Prototype 6” n-type sensors from HPK**
  - Testing with custom probe card, contacting all channels with spring loaded pins
  - 50 tested sensors showed expected performance and excellent quality: no breakdown till 900V

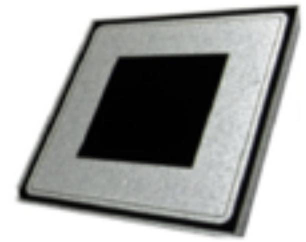


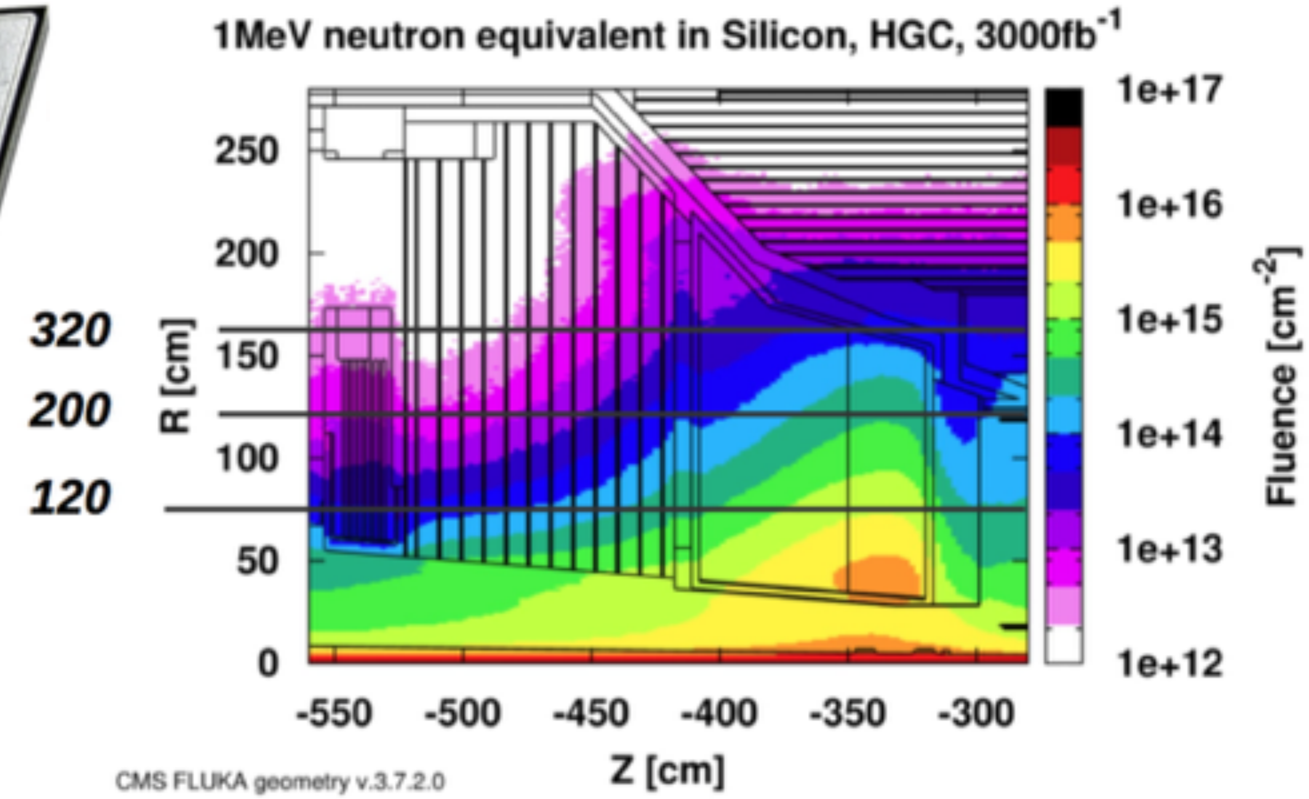




Irradiation Studies of Si Diodes

- **Types of diodes**
  - Silicon growth technique:
    dd-FZ: float zone deep diffusion
    Epi: epitaxial layer
  - n-on-p (p type), p-on-n (n-type)
  - Active thickness: 50um - 320um
  - Size: 5mm x 5mm





- **Goal: investigate performance after neutron irradiation up to 1.5e16 n/cm^2**

List of sensors and status:

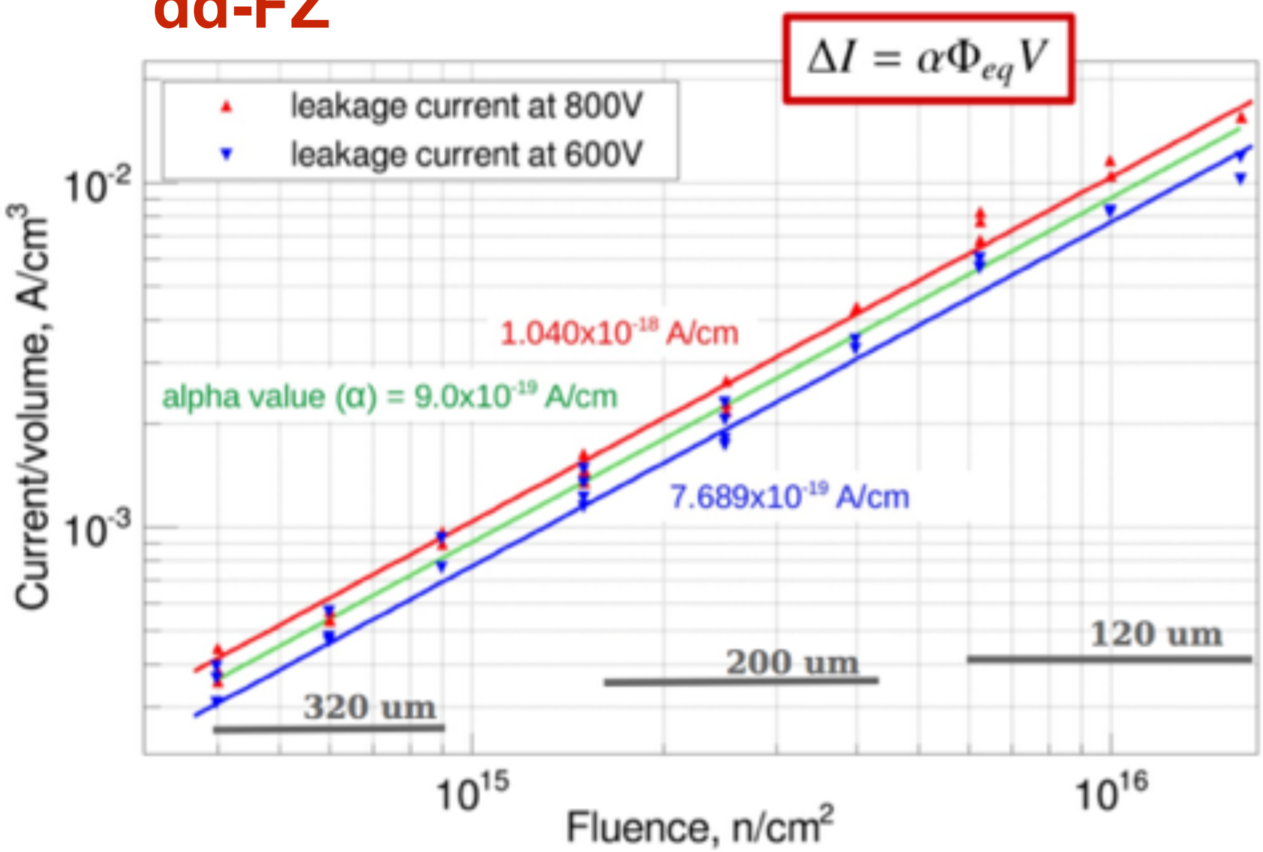
Thickness (um)

Fluence n/cm2	Float zone			Epitaxial	
	320	200	120	100	50
4.00E+014	1 n-on-p, 1 p-on-n				
6.00E+014	2 n-on-p, 2 p-on-n				
9.00E+014	1 n-on-p, 1 p-on-n				
1.50E+015		1 n-on-p, 1 p-on-n			
2.50E+015		2 n-on-p, 2 p-on-n			
4.00E+015		1 n-on-p, 1 p-on-n			
6.25E+015			2 n-on-p, 2 p-on-n	2 n-on-p	
1.00E+016			1 n-on-p, 1 p-on-n	2 n-on-p	2 n-on-p, 2 p-on-n
1.60E+016			1 n-on-p, 1 p-on-n		2 n-on-p, 2 p-on-n

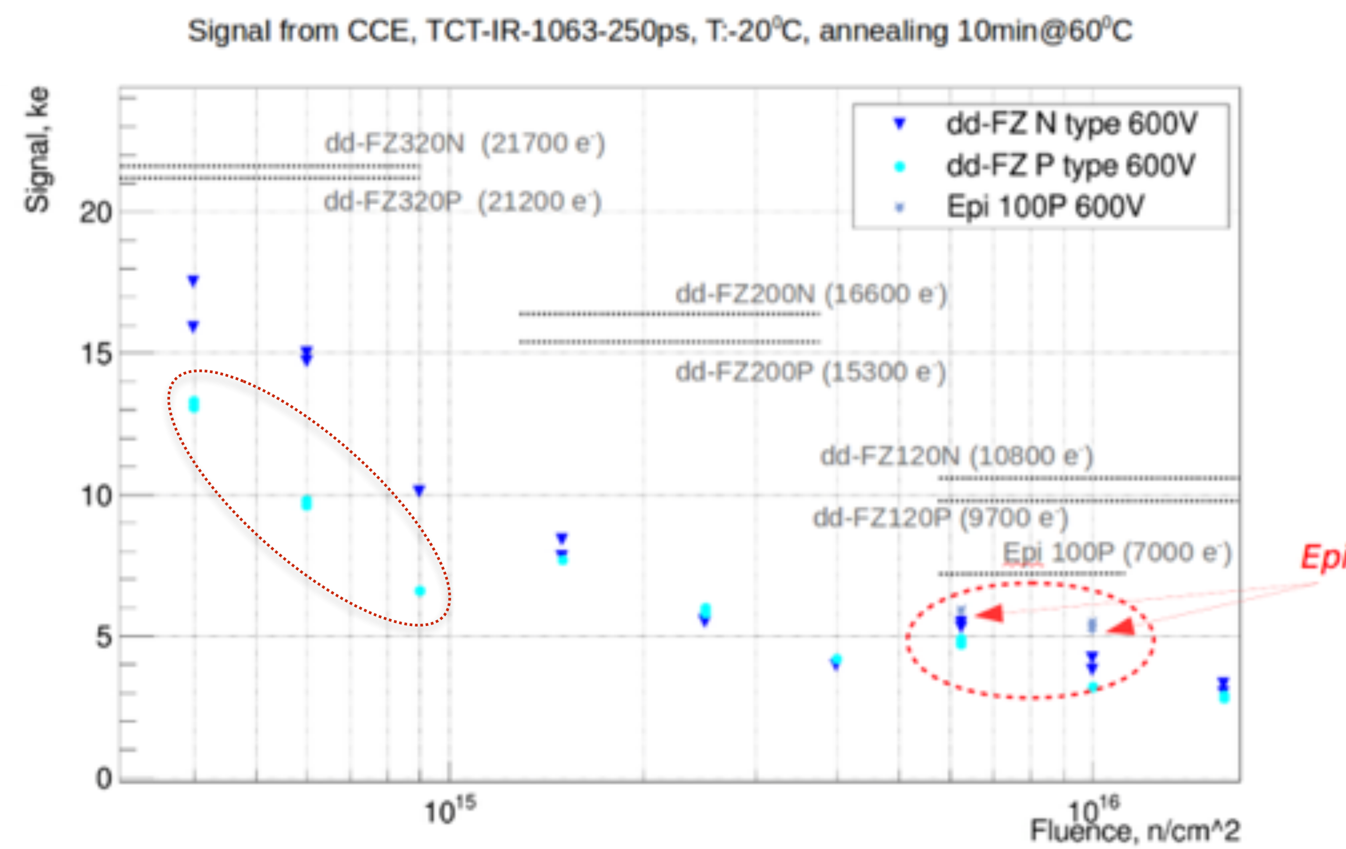
Radiation Hardness Results

-20°C and annealing of 10min@60°C

dd-FZ



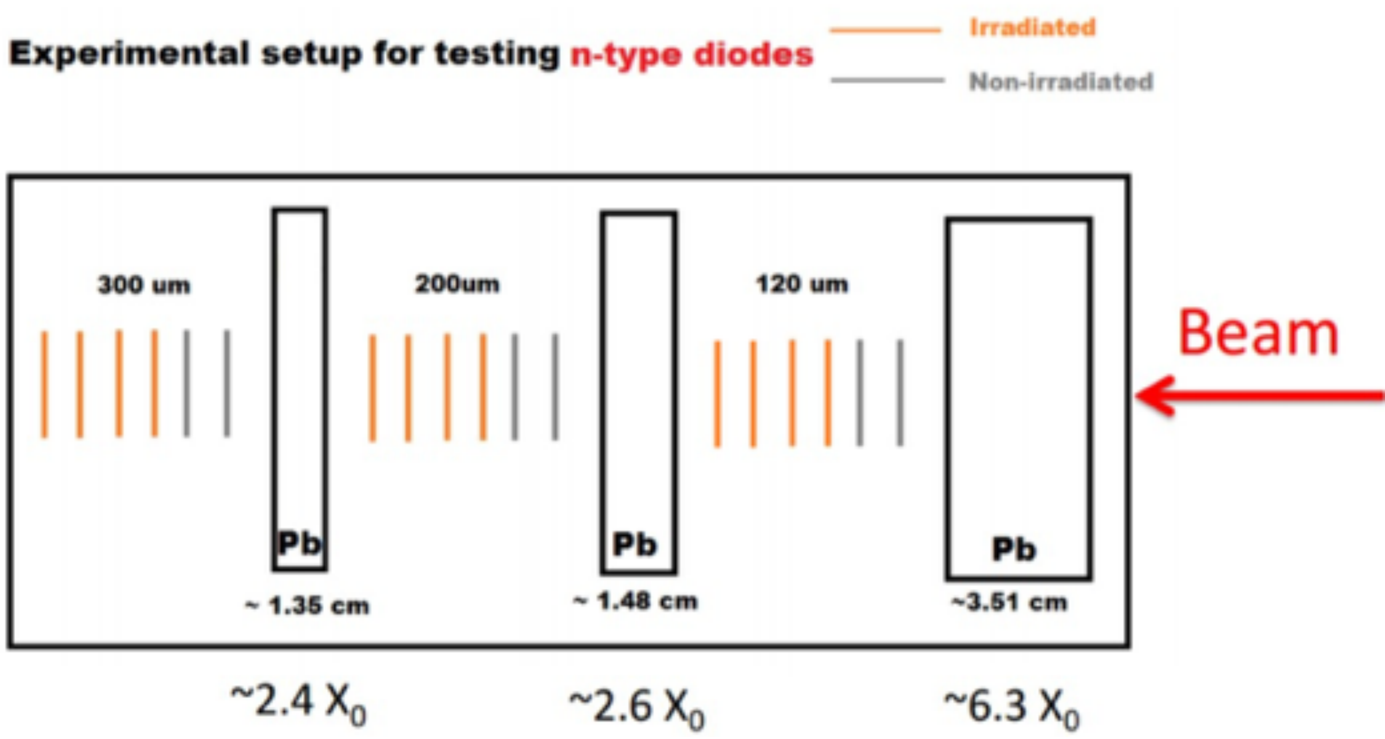
Signal injected with IR laser, confirmed with ^{90}Sr



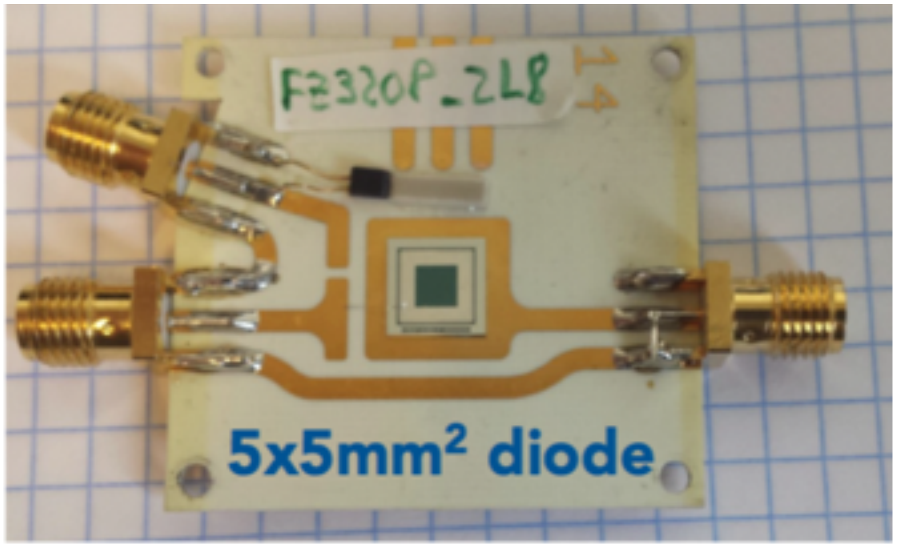
- Leakage current normalized by the volume of the diode is proportional to the fluence, even at high fluences
- The alpha measured at 800V is equal to the value measured during the CMS tracker upgrade with proton irradiation, 5.3x10-17 A/cm3 in both cases (scaled to +20C) and consistent with Moll's thesis alpha value
- P type dd-FZ diodes of 320um thickness showed significantly lower signals than N type diodes (under investigation), while similar for other thicknesses
- Signals from Epi (100um) diodes are larger after radiation than from dd-FZ (120um) diodes

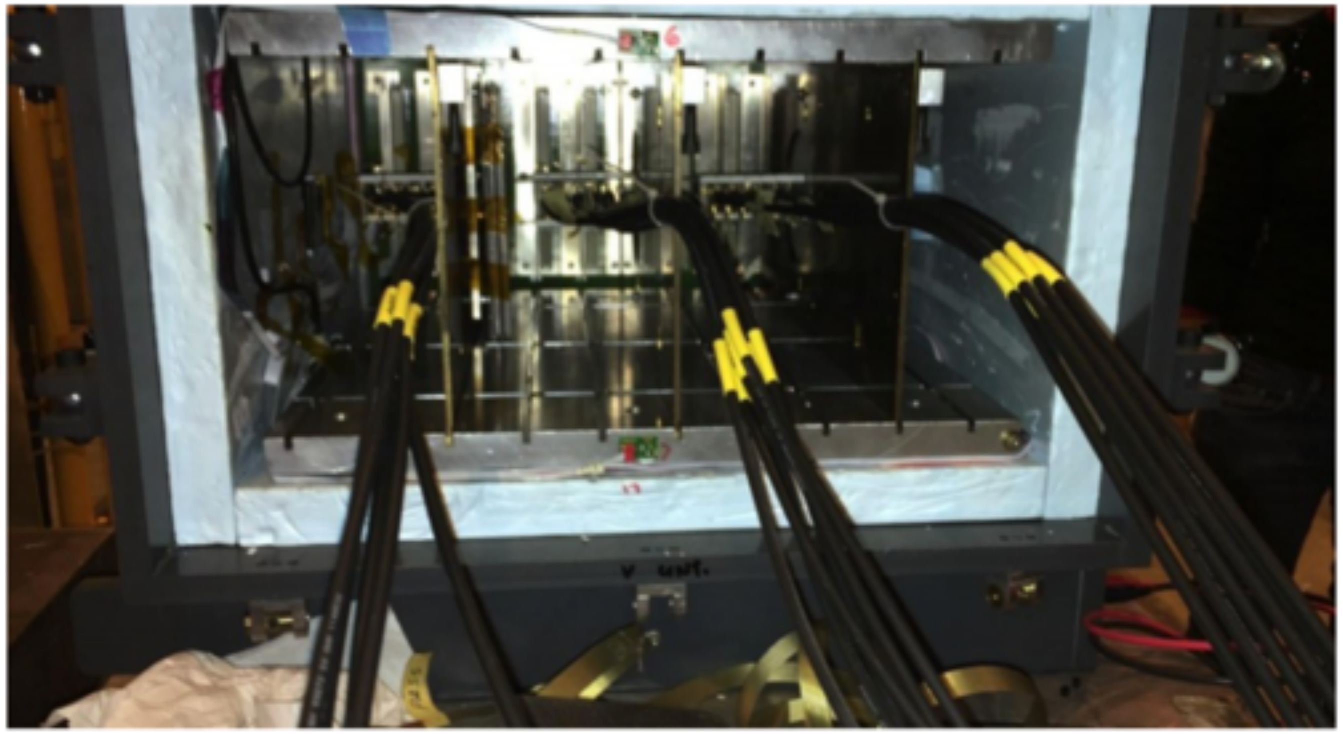
Timing Studies of Diodes at CERN

- **Goal: to measure intrinsic timing capabilities of silicon detectors for EM showers**
- **Study time resolution as a function of signal amplitude, active thickness and fluence**
- **Used Cividec amplifiers and Caen V1742 fast (5GHz) digitizer with >500MHz bandwidth**



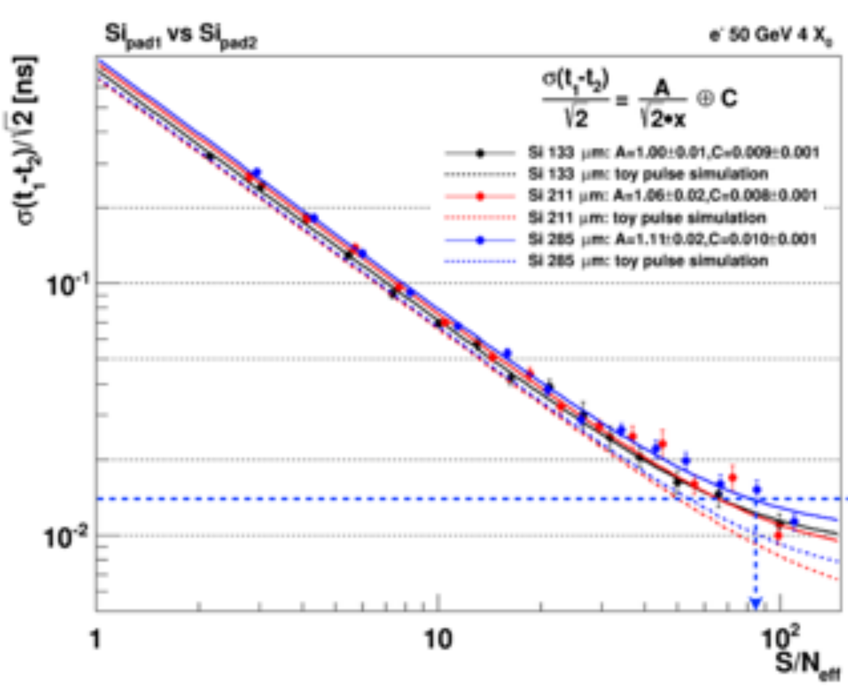
Cold box (-25^{0}C)

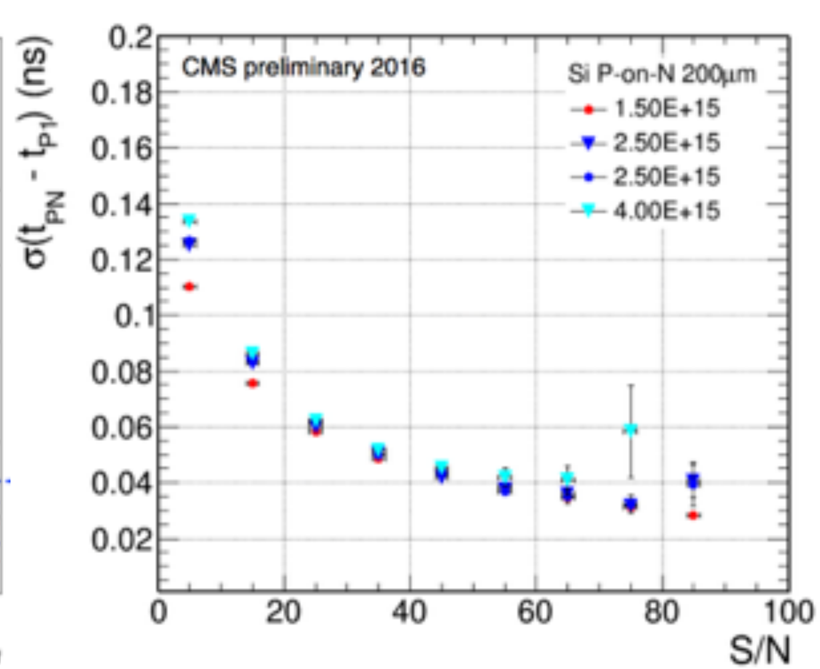


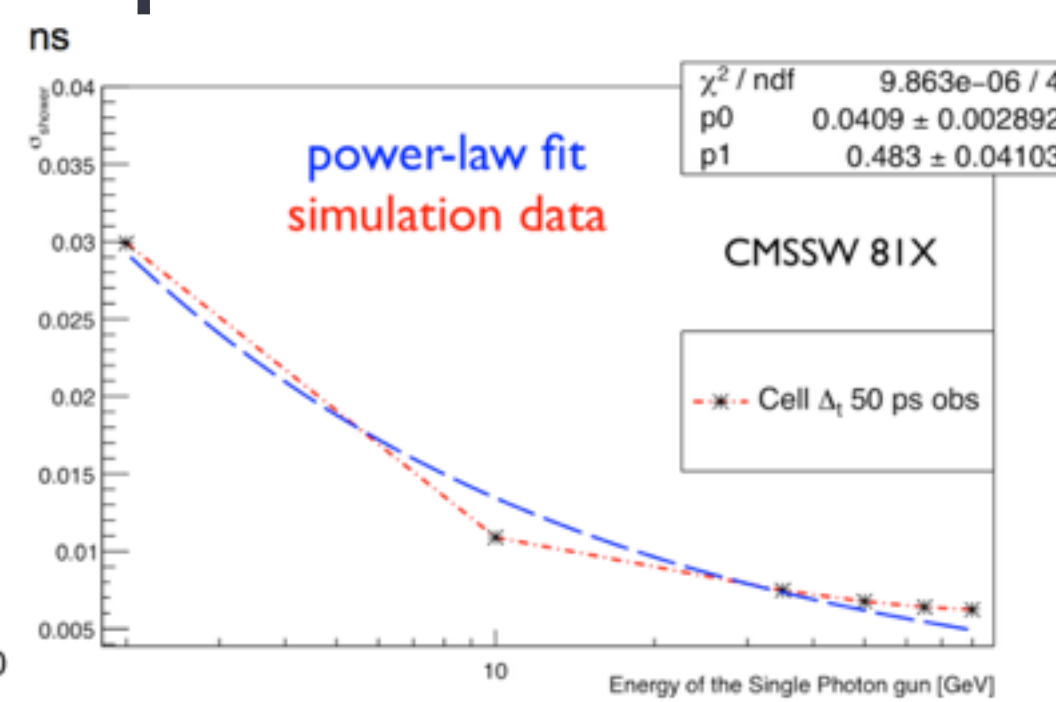


Timing Results

- **Time resolution is measured by comparing time of signal arrival from two Si diodes, event by event**
- **Time resolution is determined by S/N**
  - Dependence on sensor thickness is via S/N
  - Dependence on fluence is also via S/N
- **Timing resolution is < 20ps for S/N > 50**
- **Application of timing capabilities of silicon sensors may resolve showers in time and help mitigate pile-up at HL-LHC**
- **~10ps resolution for EM shower with 50ps cell resolution**

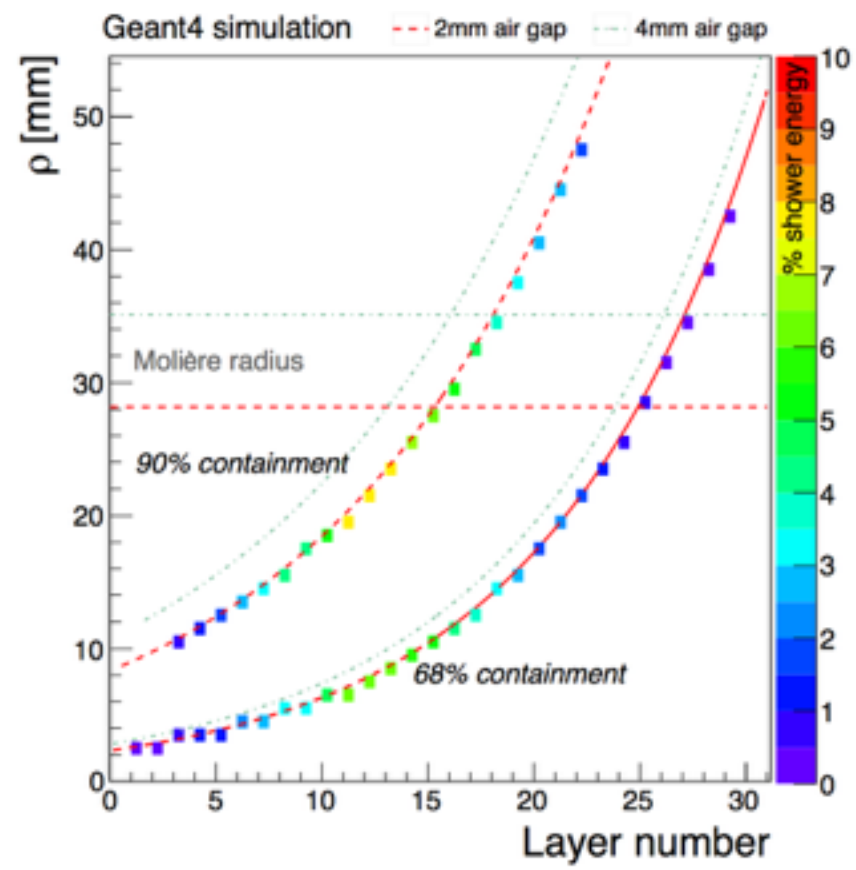


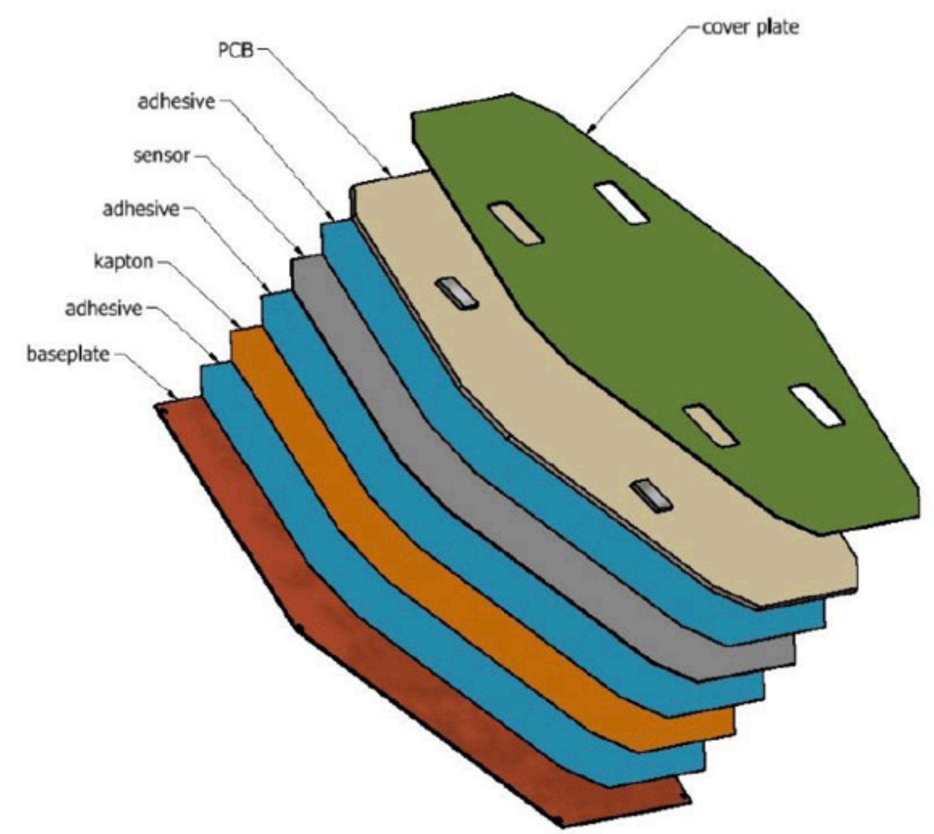




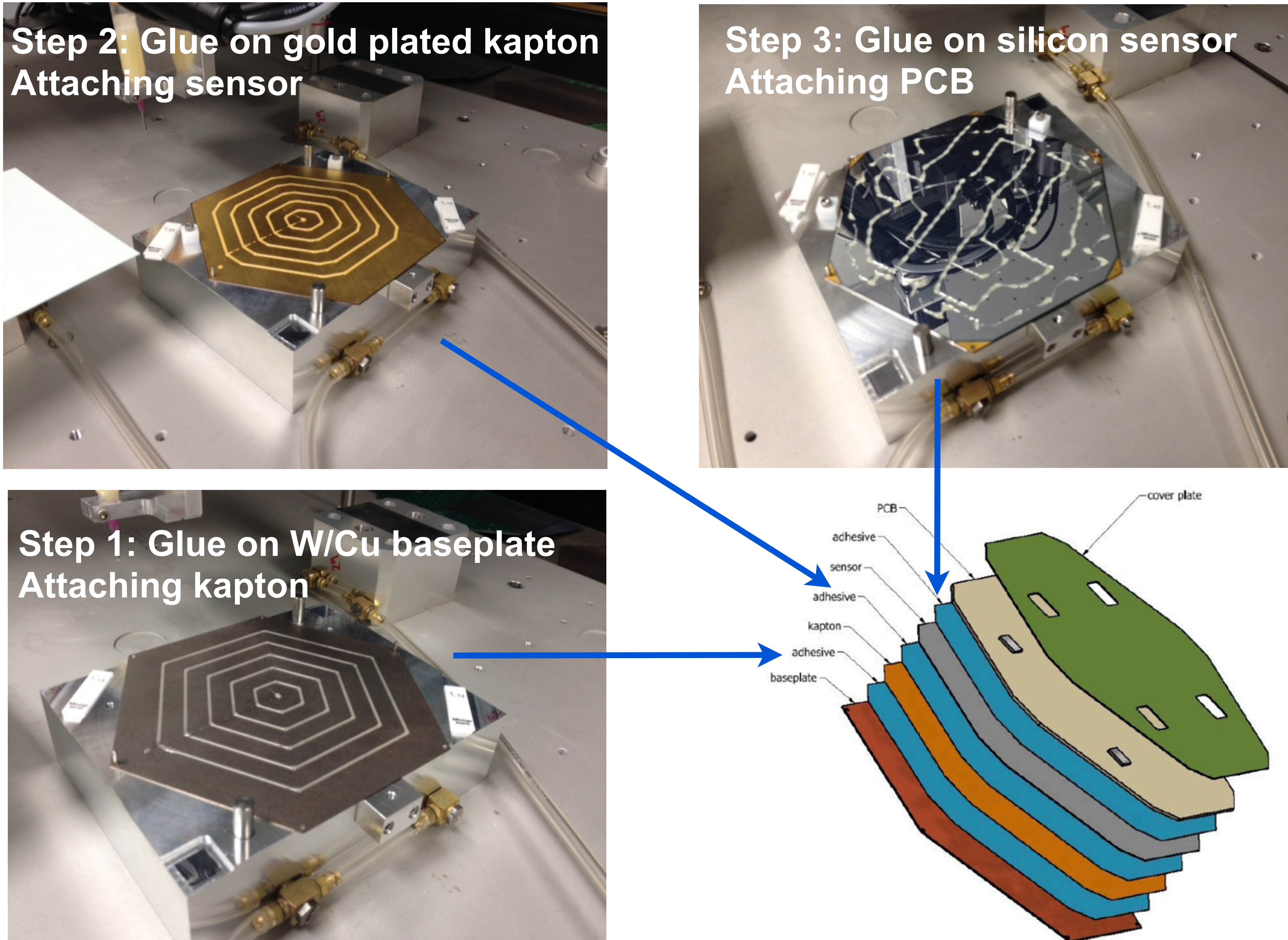
Module Design and Construction

- **The electromagnetic part of HGCal requires compact construction to keep shower size small**
- **Module design is being optimized**
  - to obtain low profile
    - requires as thin as possible electronics design
  - wire-bonding sensor cells to PCB requires
    - meeting tight gluing tolerances to ensure the PCB is flat, horizontal (~100um) and well supported by the glue
    - good alignment (~100um) of sensor and PCB layers
    - may require deep access wire-bonding machine (~1mm deep)



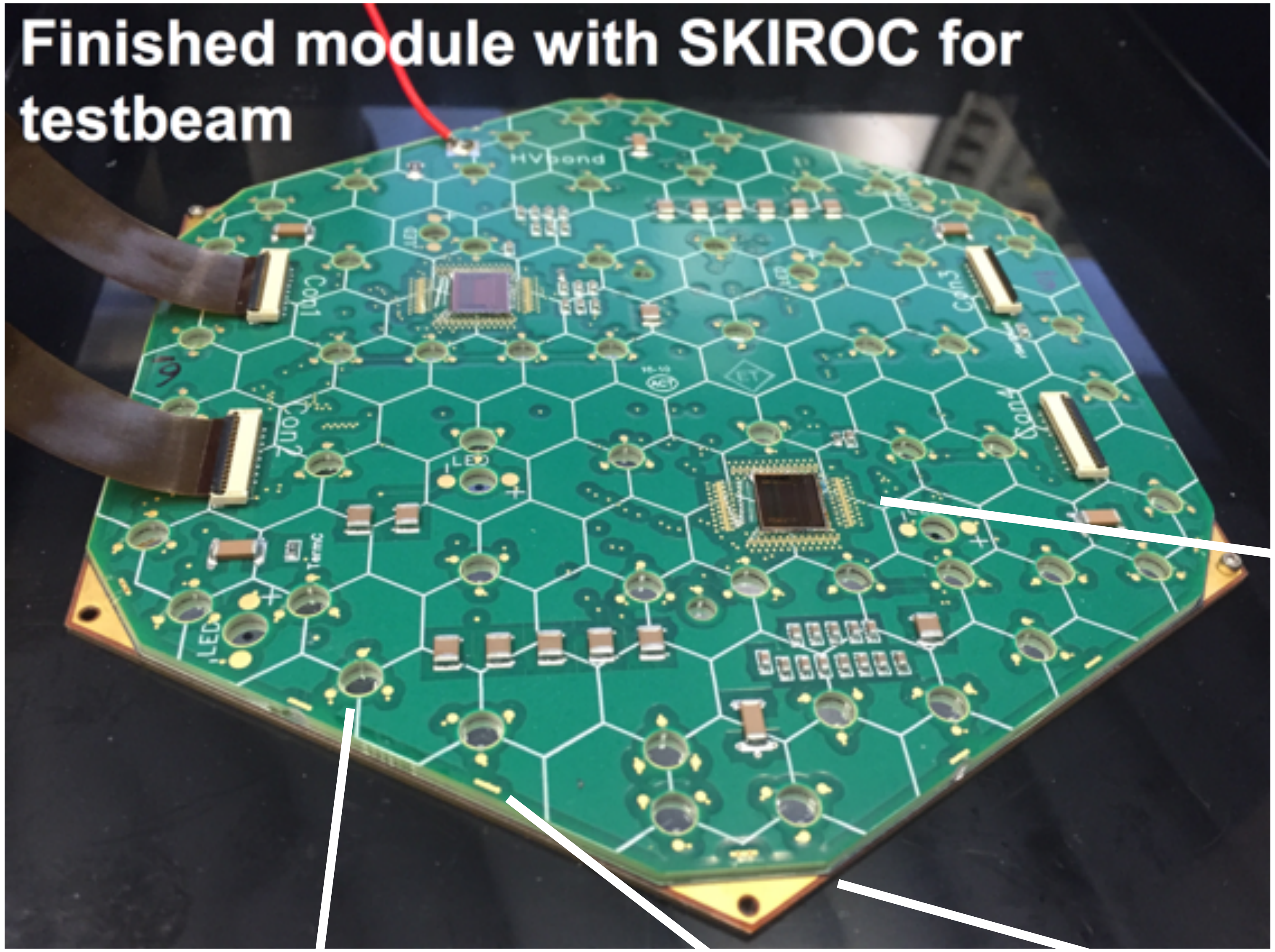


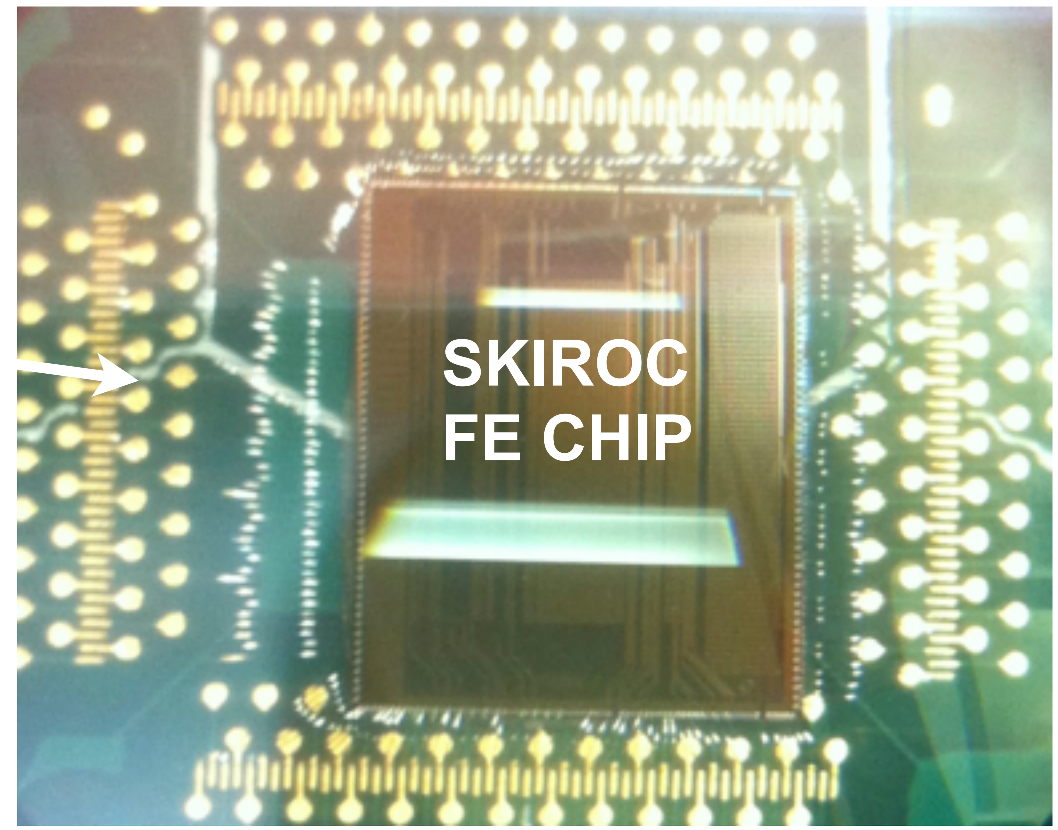
Module Assembly

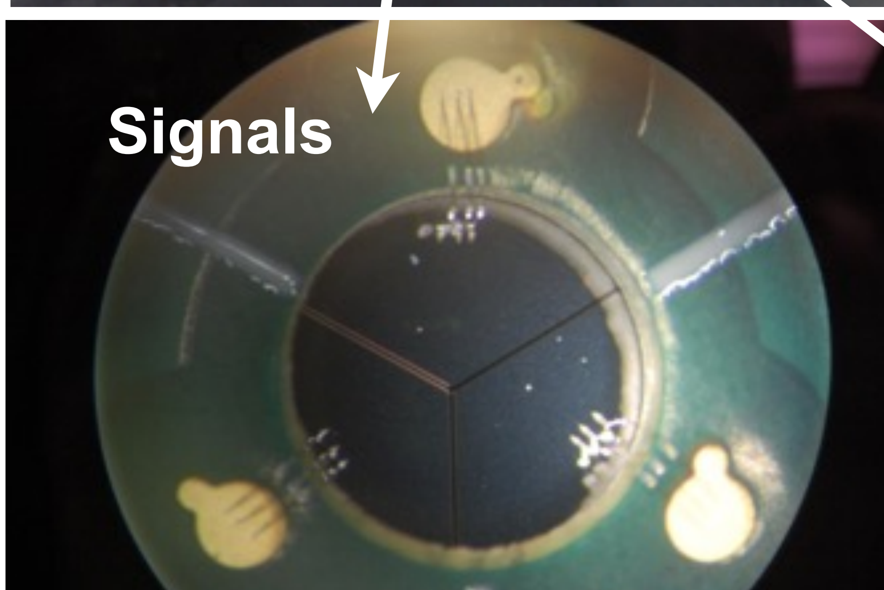


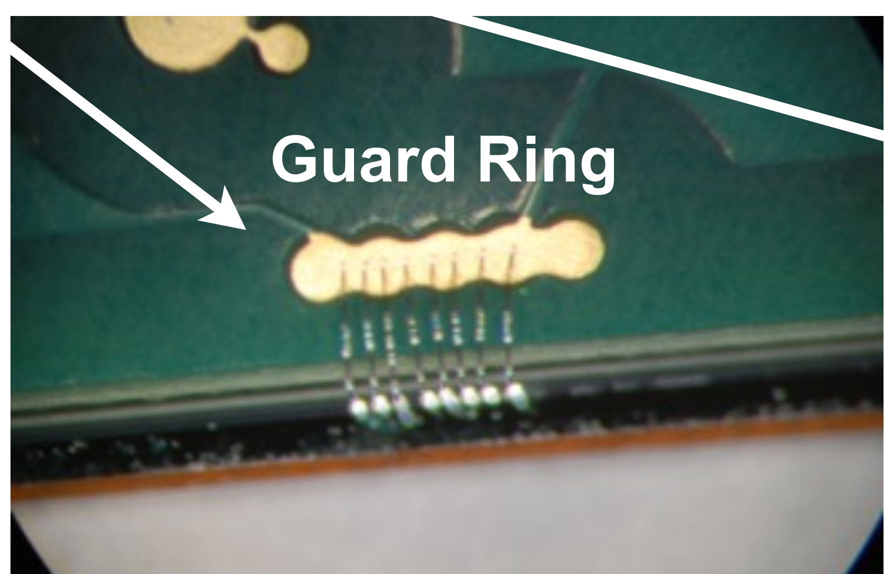
Wire Bonding

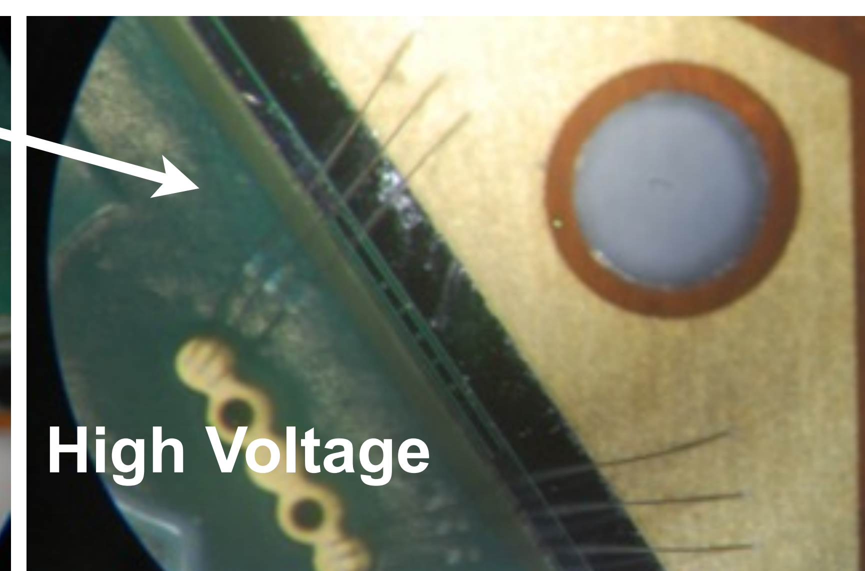
- ~ 700 wire bonds on a single module!





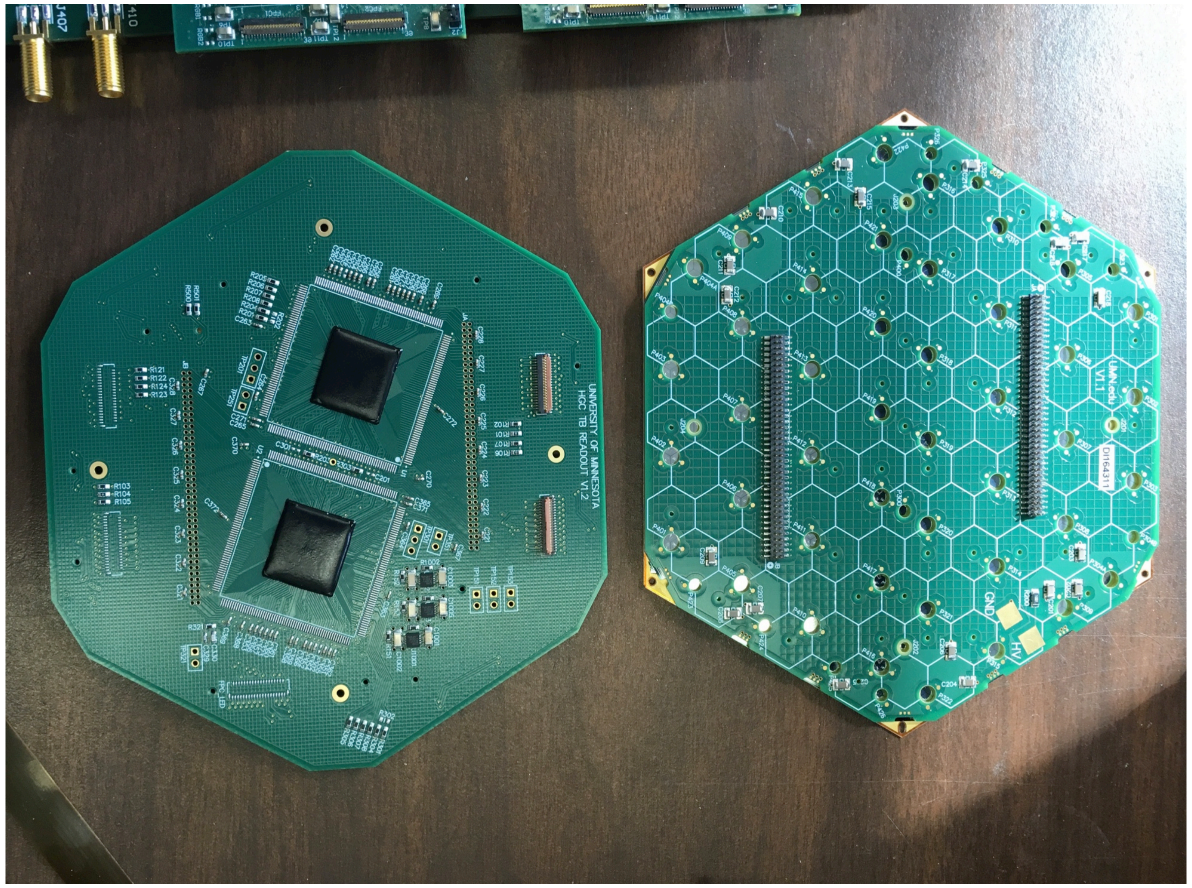


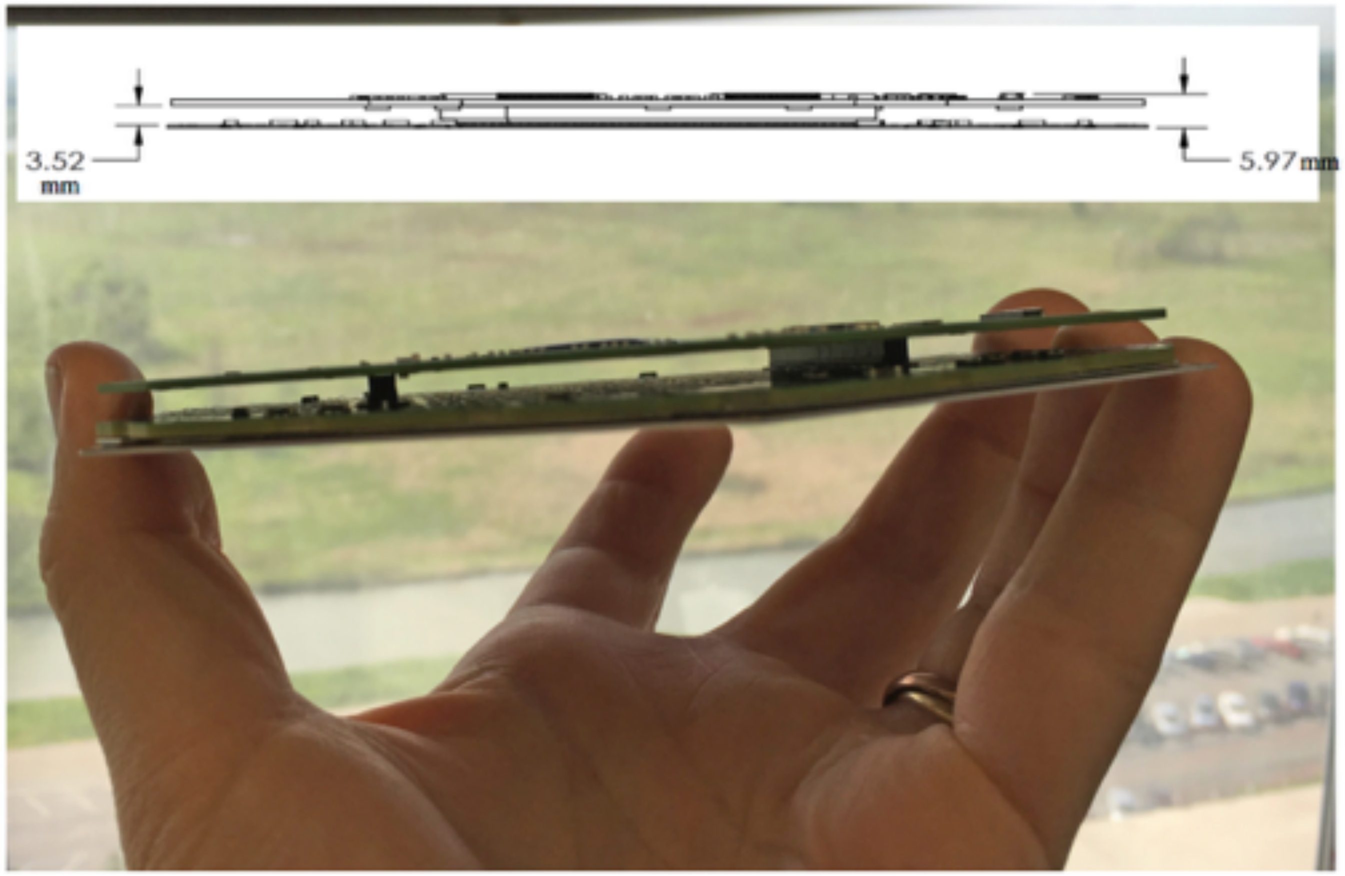




Double-layer Module Prototype

- **In parallel, a double-layer module structure has been explored**
  - bottom layer is a passive PCB connecting silicon pads to a connector
  - top layer carries all electronics, SKIROC chips, etc…
  - allows replacement of electronics and reuse of the sensors during R&D
  - Successfully operated in test beams





Automated Assembly of Modules

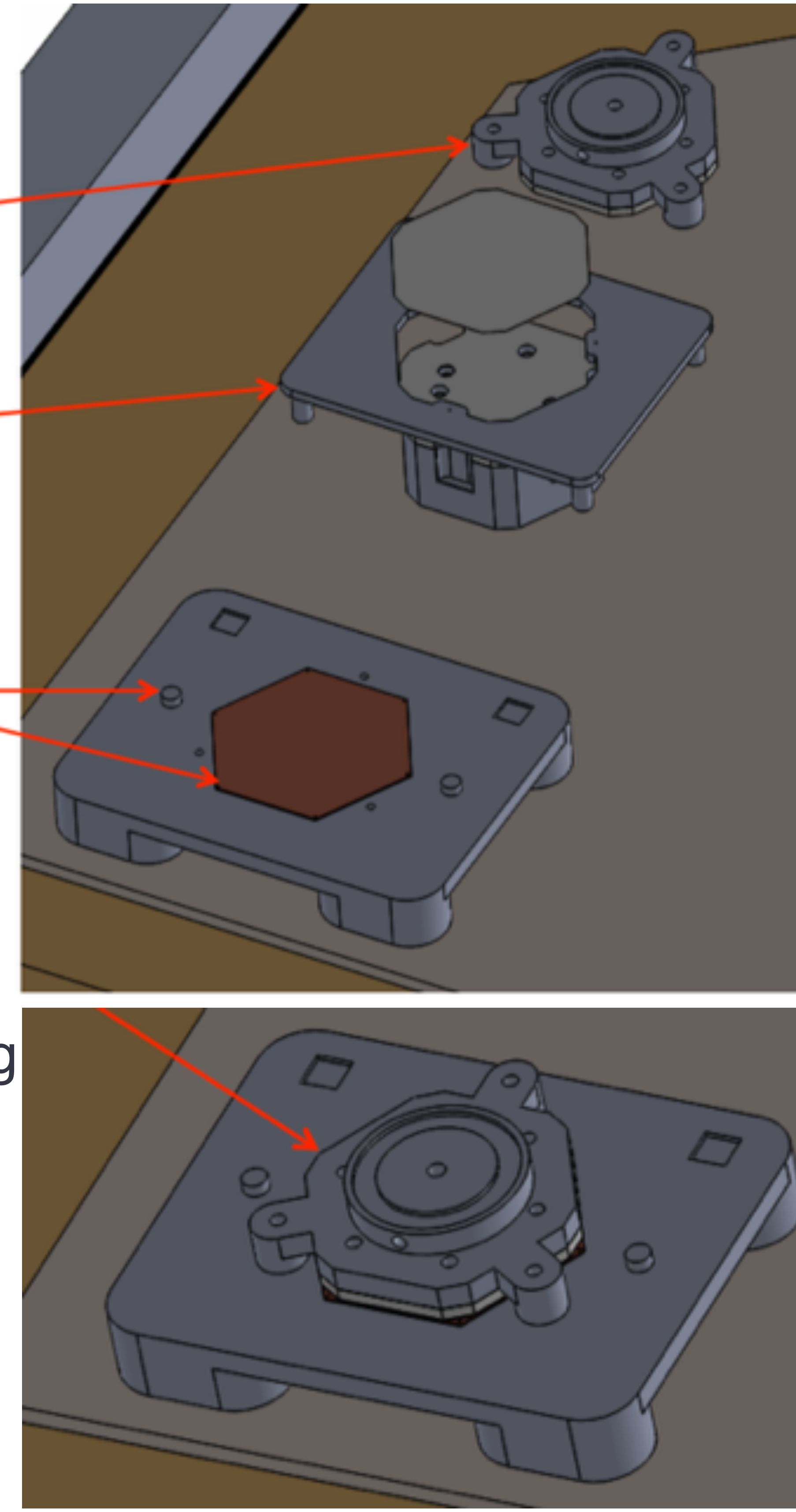
- **Setting up Gantry machine for automated assembly of modules**
- **Reproducible results**
- **High rate and volume of assembly**
- **Will be tested for the production of the test beam prototype calorimeter**

Clamping tool

Sensor holding tray

Baseplate on carrier tray

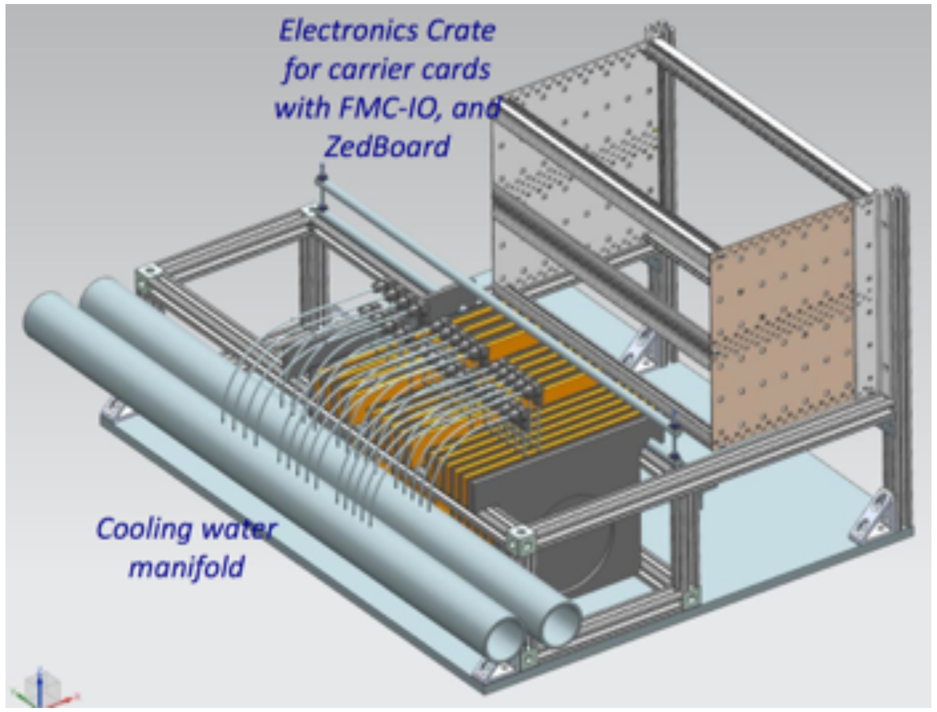
Assembled module cures under clamping tool



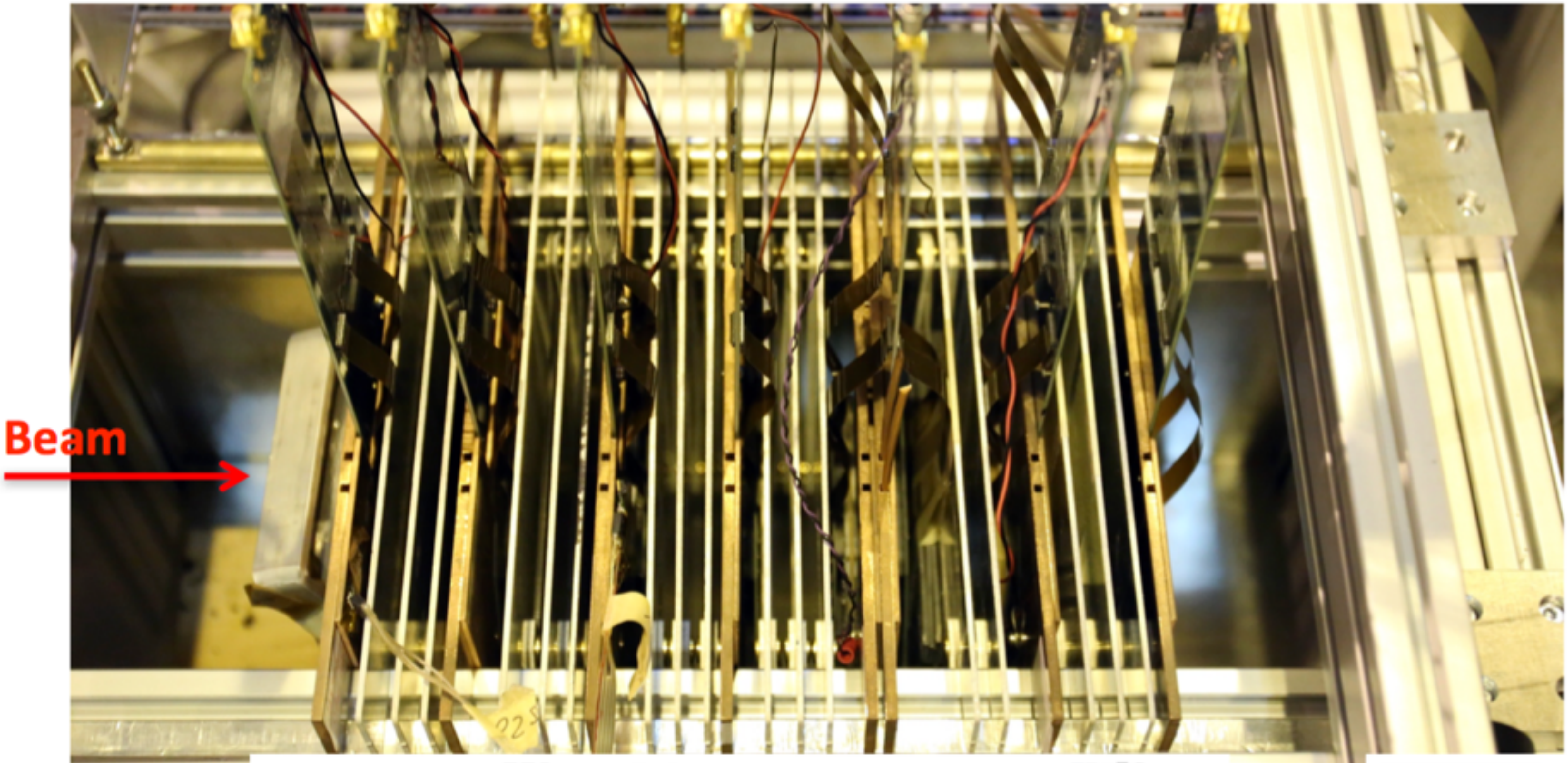
Overview of Beam Tests

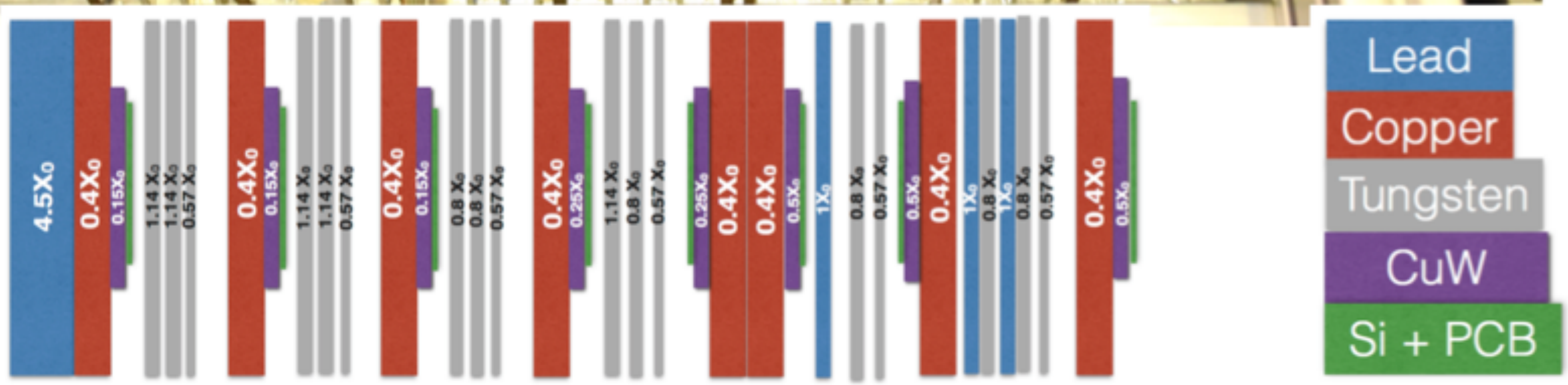
- **Goals**
  - verify functionality of design with a full depth but narrow calorimeter prototype
  - performance studies: signal to noise, timing, energy and position resolutions
- **Several beam tests at FNAL and CERN**
  - FNAL: 120GeV protons, 4-32GeV electrons/pions
  - CERN: 125GeV pions, 20-250 GeV electrons
- **Each layer contains 1 sensor mounted on a copper cooling plate**
  - 6”, 200um active thickness, p-on-n, 1.1cm2 cell size
- **Hanging file design for mechanical structure**
  - Flexible insertion of absorbers and modules on cooling plates

Laboratory	Layers	Rad length	Date
FNAL	1	6	March 2016
FNAL	4	12	May 2016
FNAL	16	15	July 2016
CERN	8	27	Aug 2016



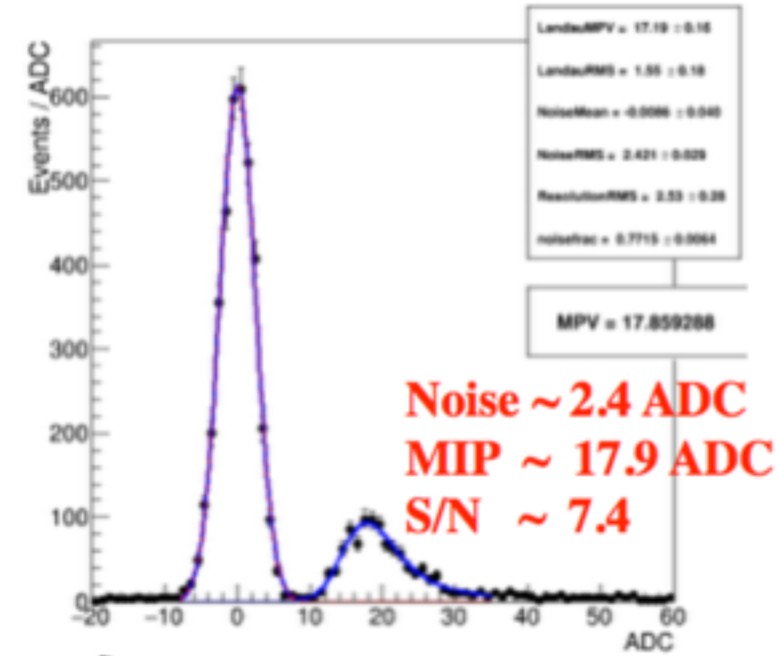
Cern Test Beam (27 X_0 with 8 Layers)

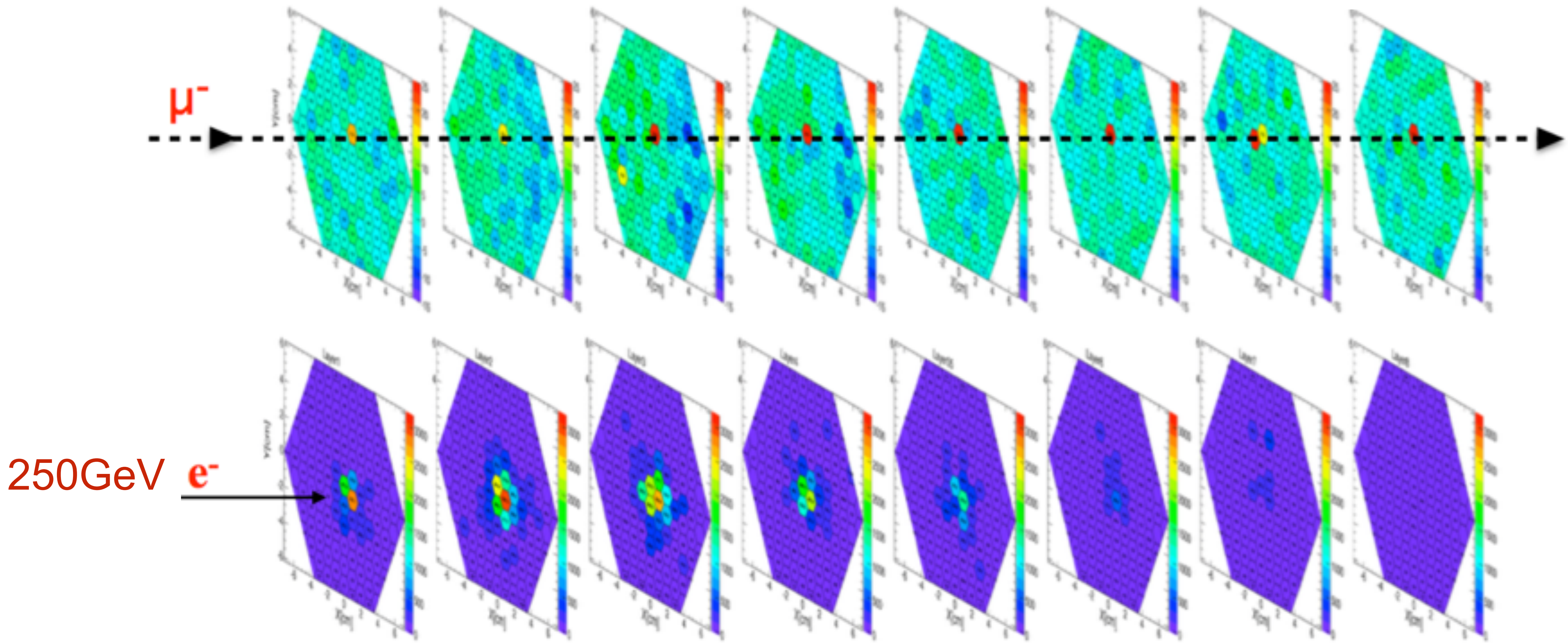




Calibration and Event Displays

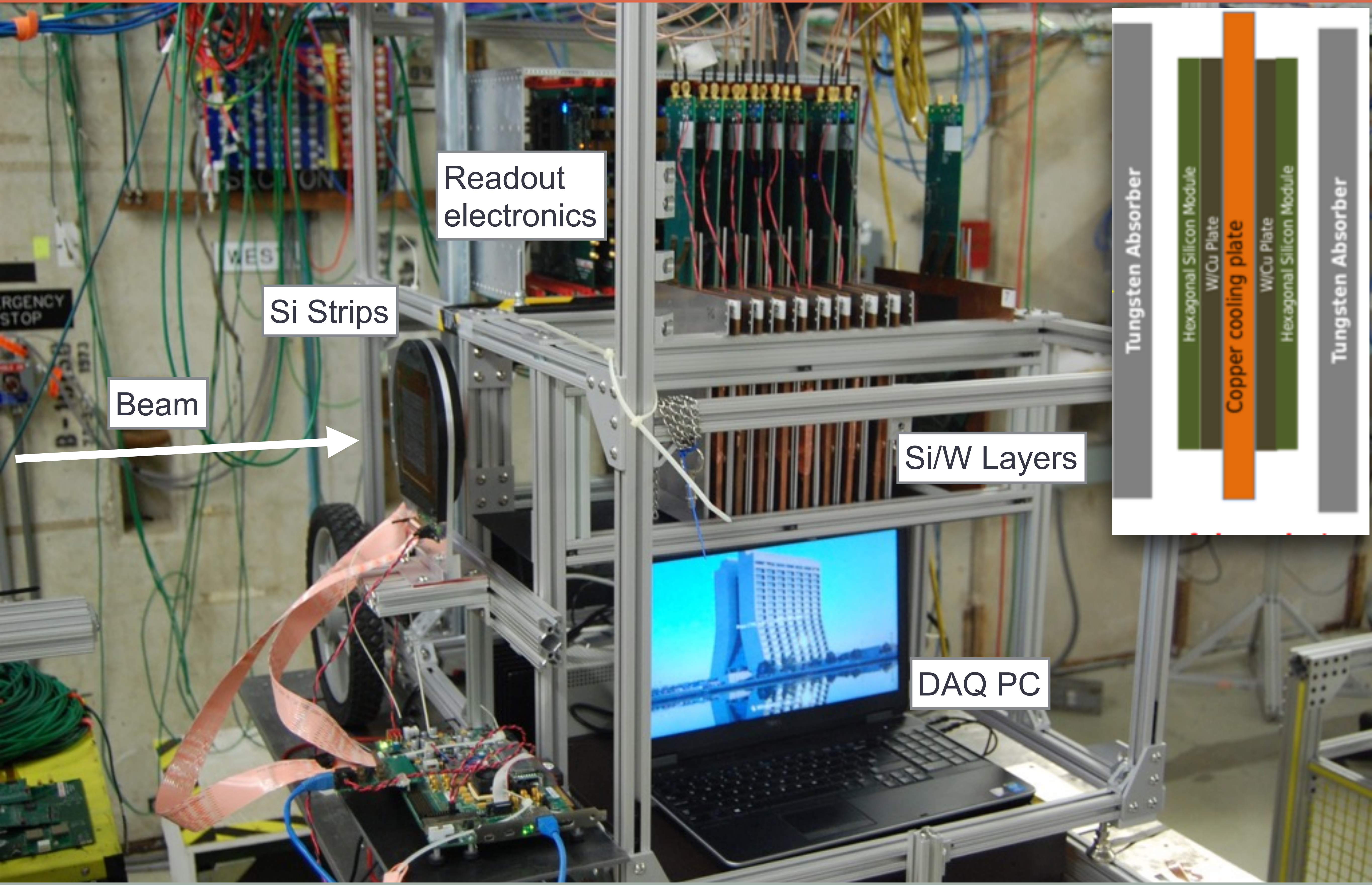
- **Muon beam used to calibrate sensors**
  - After pedestal and coherent noise subtraction distribution of ADC counts is fit with a Landau distribution convoluted with a Gaussian
  - 1 MIP ~ 17.9 ADC
- **Detailed analyses of data ongoing**





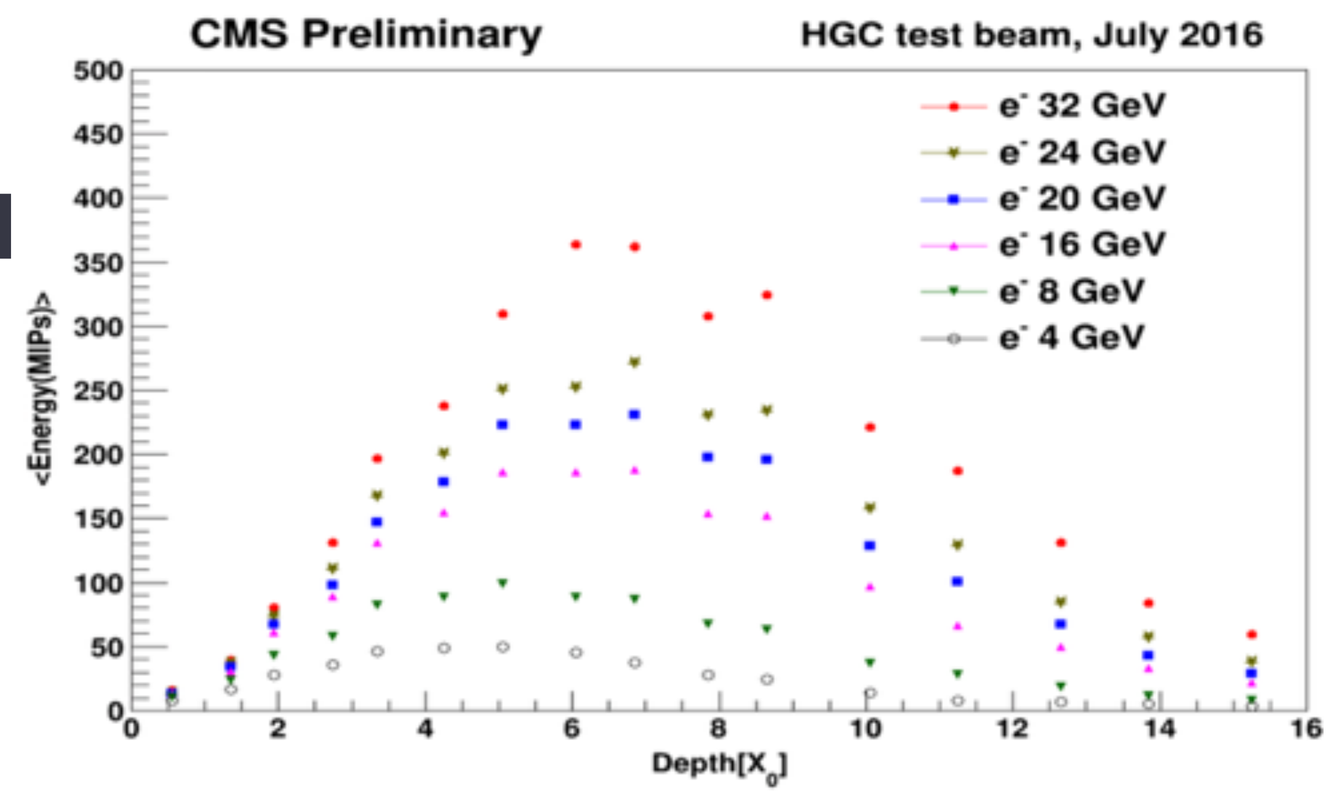
L1 : 5.1X_0 L2 : 8.5X_0 L3 : 11.9X_0 L4 : 14.7X_0 L5 : 17.2X_0 L6 : 18.7X_0 L7 : 21.1X_0 L8 : 27.07X_0

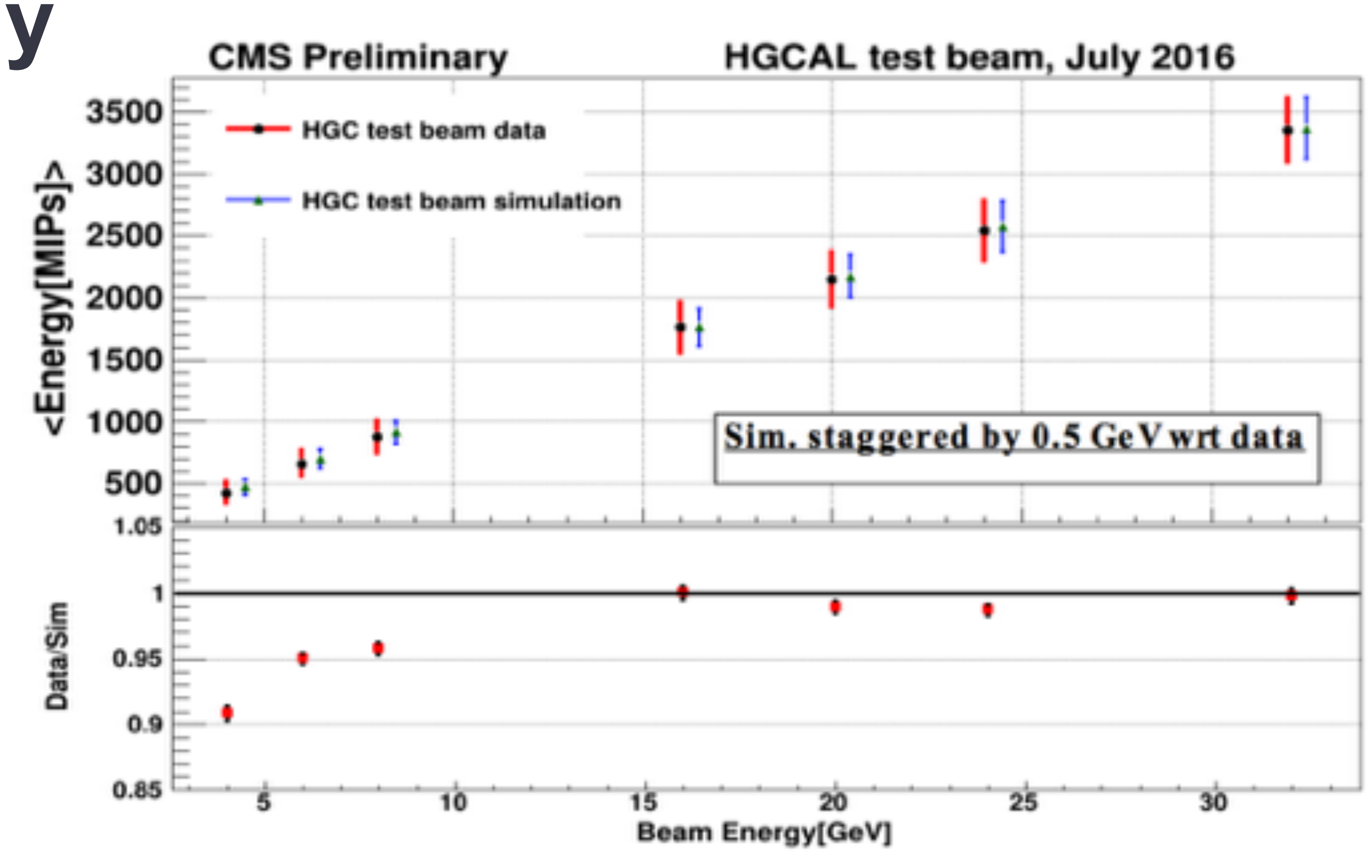
Fermilab Test Beam (15 X_0 with 16 Layers)



Energy Depositions and MC Comparisons

- **All layers have been calibrated**
- **Pedestals and noise subtracted**
- **Top plot shows energy deposited in each layer**
  - Shower max moves to higher depth with increasing electron beam energy, as expected
- **Bottom plot shows total energy deposited in all layers as a function of e⁻ beam energy**
  - Dependence is linear
  - Compared to Geant 4 simulation
  - Good agreement (~5%) observed





Summary

- **CMS is preparing for a High Granularity Endcap calorimeter largely based on silicon sensors, (600m^2 and 6M channels)**
- **First prototype HGCal sensors have been fabricated and show excellent quality and expected performance**
  - comprehensive suite of studies is planned and well underway
- **Radiation studies of silicon diodes show good radiation hardness for entire lifetime of HL-LHC (3000fb-1)**
- **Good intrinsic timing resolution (<20ps at high enough S/N) of silicon diodes has been measured. This can help mitigate the effect of pileup and in localizing the primary vertex of the event of interest.**
- **Construction of prototype modules has been successfully demonstrated and work started on automated assembly**
- **Successfully constructed and operated a 16 layer EE prototype in the test beam**

Additional Material

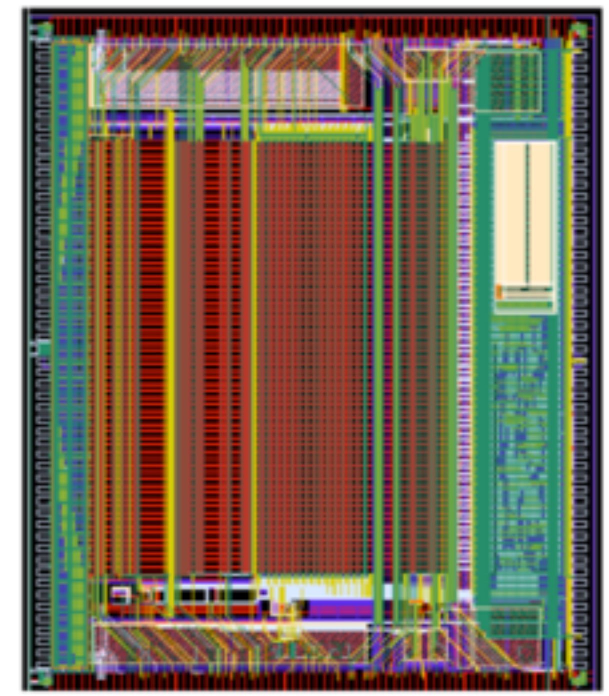
Strategy for FE Electronics

1) Modify existing CALICE chip to include most of the required functionalities

Exercise functionalities such as ToT, cross calibration ADC-ToT, fast timing…
Allows study of FE printed circuit board and module assembly
Test beams 2016-2017

Ωmega

SKIROC2 -> SKIROC2-CMS 0.35 μm AMS (non radhard)
faster shaper 25ns instead of 200 ns
sampling @ 40 MHz, depth 300 ns
ToT
TDC for ToA, 20 ps binning, 50 ps jitter
Received late June, under test (see next presentation)



2) Submit Test Vehicles in 130 nm

TV1 *received* mid-September: analogue architecture, baseline + variants
TV2 to be submitted before end 2016: 8 channels, analogue+ADC+ToT+ Trigger sums

3) Submit first "complete" ASIC June 2017

(some digital functionalities may still be incomplete)

4) Two more iterations foreseen in the overall planning

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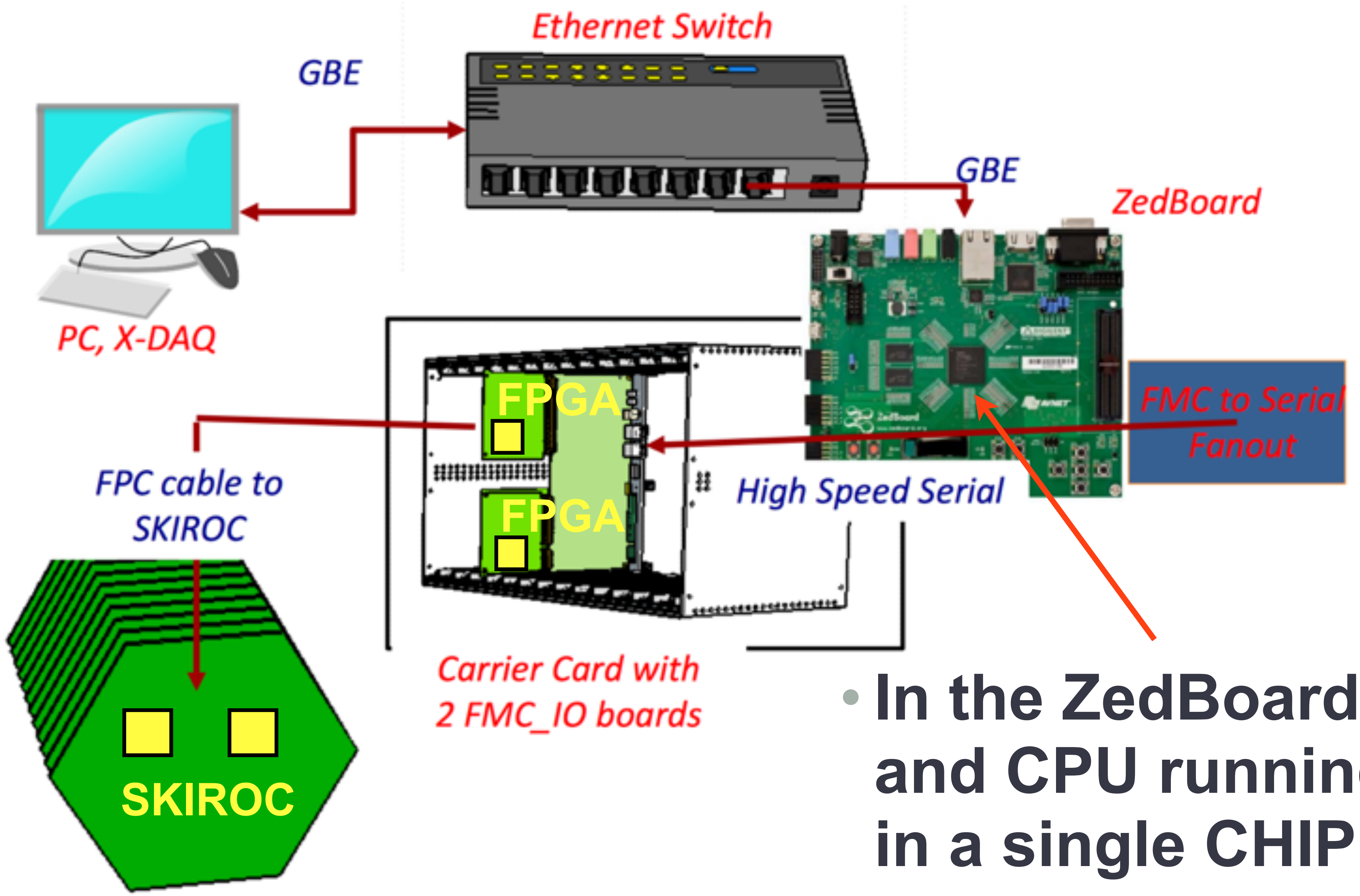
Test Beam DAQ



- **In the ZedBoard: FPGA and CPU running Linux in a single CHIP**
- **Allows easy transfer of data from FPGAs to Computers**