# Triggering at the HL-LHC:

## The Main Challenges for ATLAS and CMS

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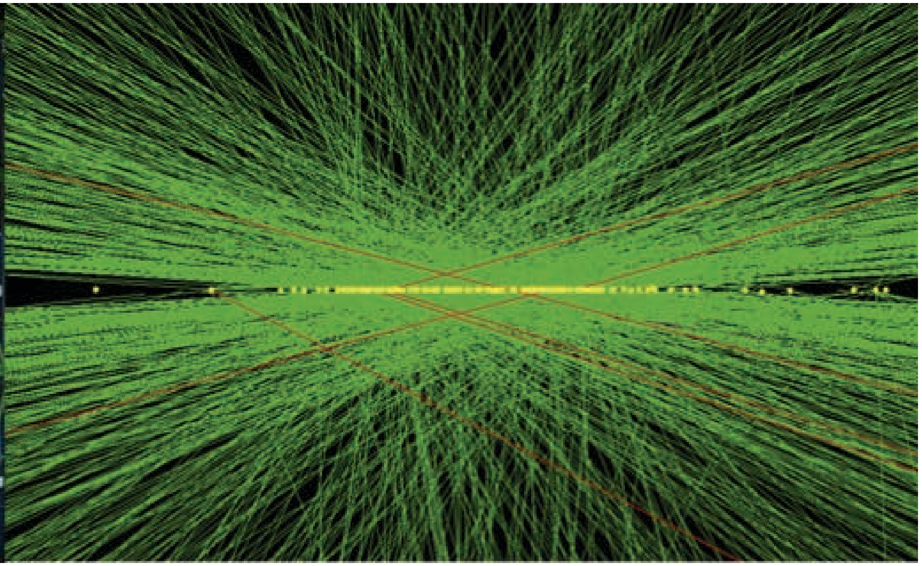
8th INFIERI Workshop

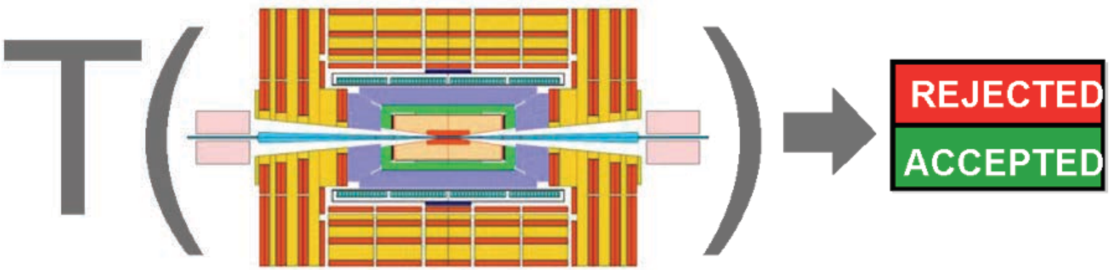
Fermilab, October 18, 2016



# Triggering

- Task: inspect detector information and provide a first decision on whether to keep the event or throw it out

The trigger is a function of :



Event data & Apparatus
Physics channels & Parameters

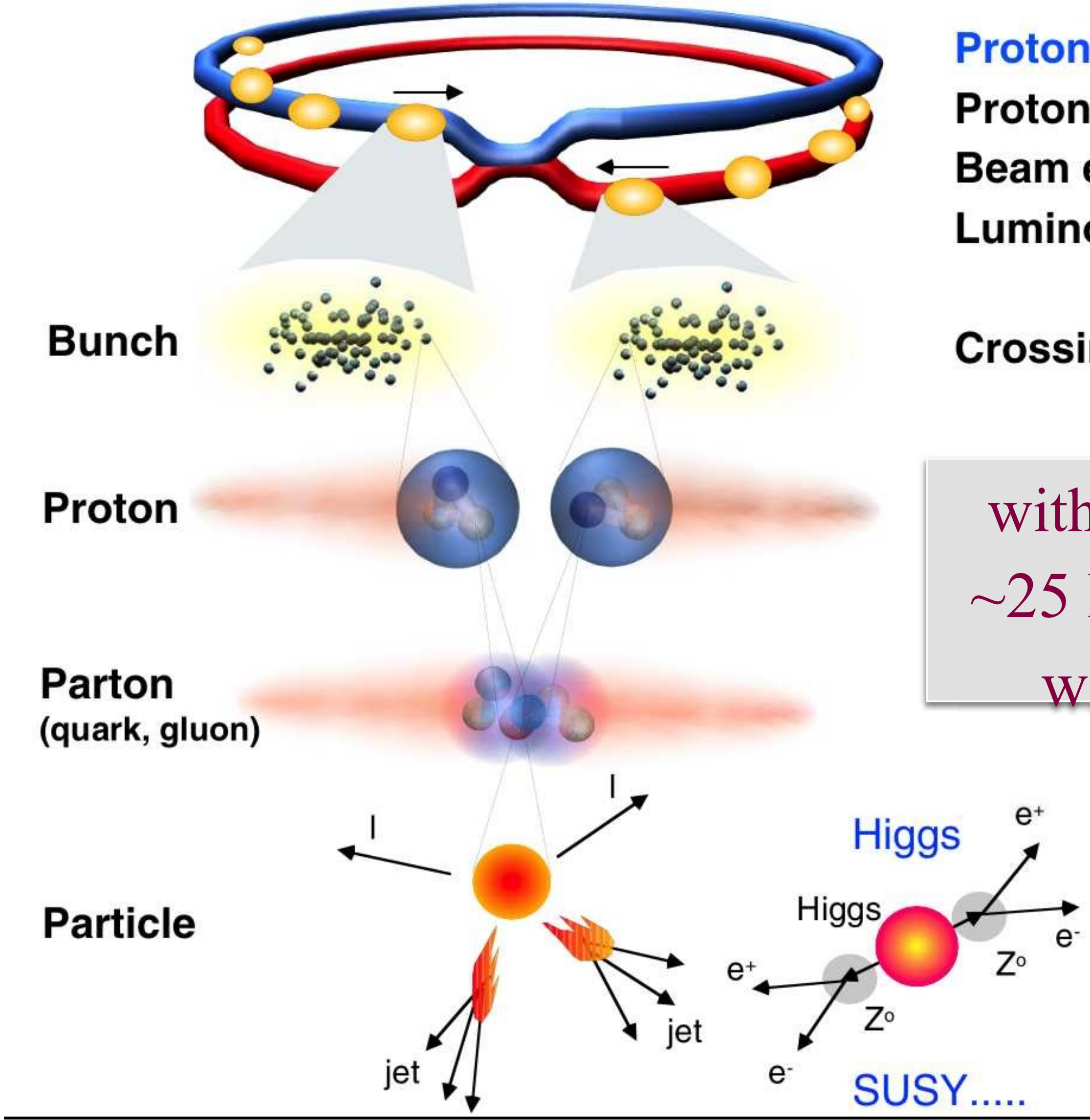
- Detector data not (all) promptly available
- Selection function highly complex

⇒T(...) is evaluated by successive approximations, the

TRIGGER LEVELS

(possibly with zero dead time)

# LHC Overview



| | |
|---|---|
| **Proton-Proton** | **2835 bunch/beam** |
| **Protons/bunch** | **$10^{11}$** |
| **Beam energy** | **7 TeV ($7 \times 10^{12}$ eV)** |
| **Luminosity** | **$10^{34}$ cm$^{-2}$ s$^{-1}$** |
| **Crossing rate** | **40 MHz** |

with every bunch crossing
~25 Minimum Bias events
with ~2000 particles
produced

**Selection of 1 in**
**10,000,000,000,000**

# LHC Physics – Trigger Challenge

Low ≅ 40 GeV

## Electroweak Symmetry Breaking Scale

- Higgs discovery and higgs sector characterization

Low $P_T$ $\gamma$, e, $\mu$

- Quark, lepton Yukawa couplings to higgs

Low $P_T$ B, $\tau$ jets

## New physics at TeV scale to stabilize higgs sector

- Spectroscopy of new resonances (SUSY or otherwise)

Multiple low $P_T$ objects

- Find dark matter candidate

Missing $E_T$

## Multi-TeV scale physics (loop effects)

- Indirect effects on flavor physics (mixing, FCNC, etc.)
  - $B_s$ mixing and rare B decays

~ Dedicated triggers using displaced vertices

- Lepton flavor violation
  - Rare Z and higgs decays

Low $P_T$ leptons

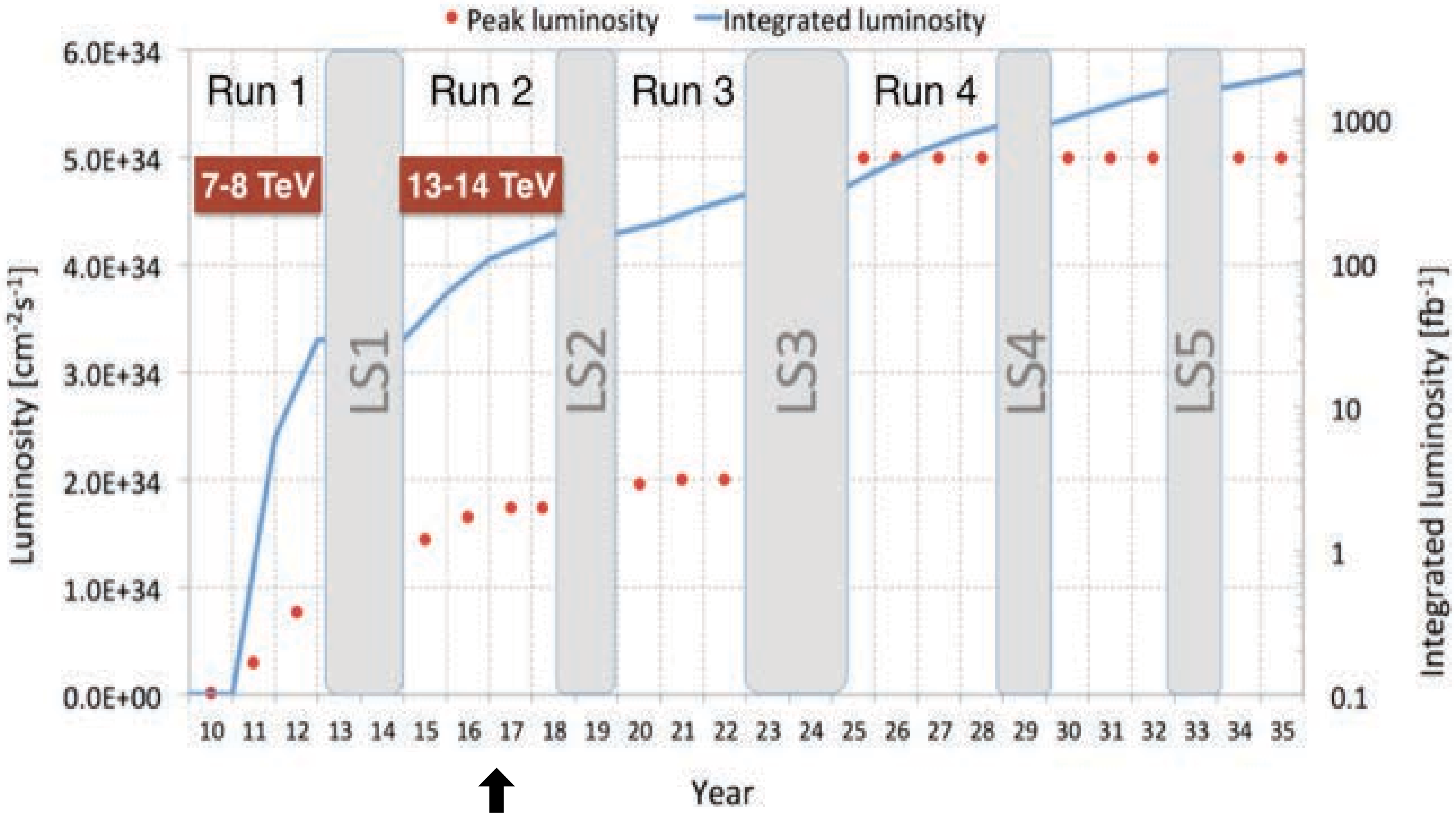
## Planck scale physics

- Large extra dimensions to bring it closer to experiment
- New heavy bosons
- Blackhole production

High $P_T$ leptons and photons

Multi particle and jet events

# The LHC Plan

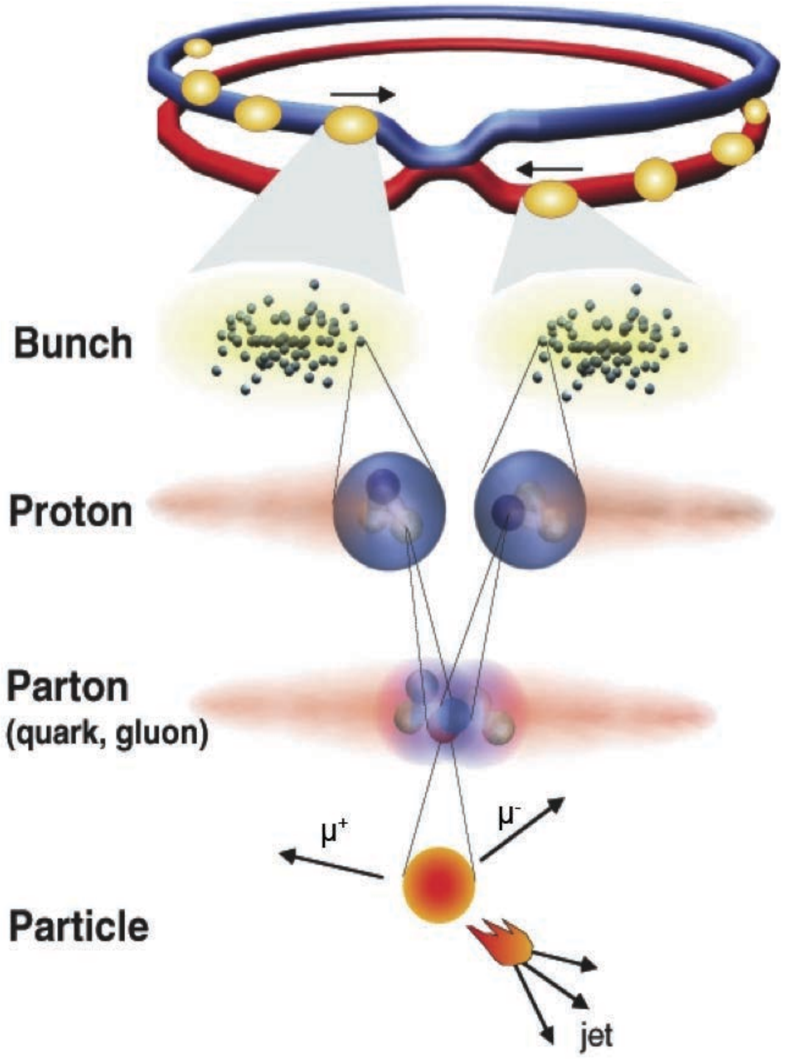


⬆

You are here!

# LHC Run I Parameters

| | Design | 2010 | 2011 | 2012 |
|---|---|---|---|---|
| ***Beam Energy (TeV)*** | ***7*** | ***3.5*** | ***3.5*** | ***4*** |
| Bunches/Beam | 2808 | 368 | 1380 | 1380 |
| ***Proton/Bunch ($10^{11}$)*** | ***1.15*** | ***1.3*** | ***1.5*** | ***1.7*** |
| Peak Lumi. ($10^{32}$ cm$^{-2}$ s$^{-1}$) | 100 | 2 | 30 | 76 |
| ***Integrated Lumi. (fb$^{-1}$)*** | ***100/yr*** | ***0.036*** | ***6*** | ***20*** |
| Pile-Up | 23 | ~1 | 10 | 20 |
| Bunch Spacing | 25 ns | 50 ns | 50 ns | 50 ns |

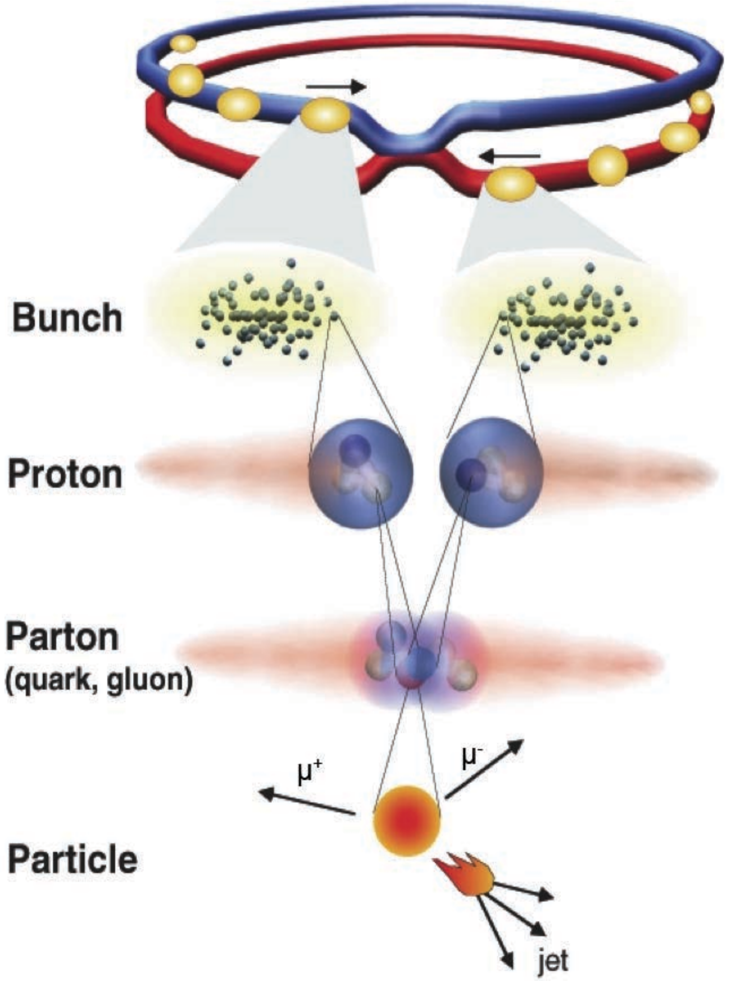


**Pile-Up** – the number of proton interactions occurring during each

# LHC Run II Parameters

| | Design | 2015 | 2016 | 2017/8 (*) |
|---|---|---|---|---|
| Beam Energy (TeV) | ***7*** | ***6.5*** | ***6.5*** | ***6.5/7*** |
| Bunches/Beam | 2808 | 2244 | 2748 | 2808 |
| Proton/Bunch ($10^{11}$) | ***1.15*** | ***1.2*** | ***1.2*** | ***1.2*** |
| Peak Lumi. ($10^{32}$ cm$^{-2}$ s$^{-1}$) | 100 | 51 | 100(*) | 100 |
| Integrated Lumi. (fb$^{-1}$) | ***100/yr*** | ***4*** | ***30(*)*** | ***70(*)*** |
| Pile-Up | 23 | <20 | 40 | 40 |
| Bunch Spacing | 25 ns | 50/25 ns | 25 ns | 25 ns |

**Pile-Up** – the number of proton interactions occurring during each



*expected value

# LHC Physics & Event Rates

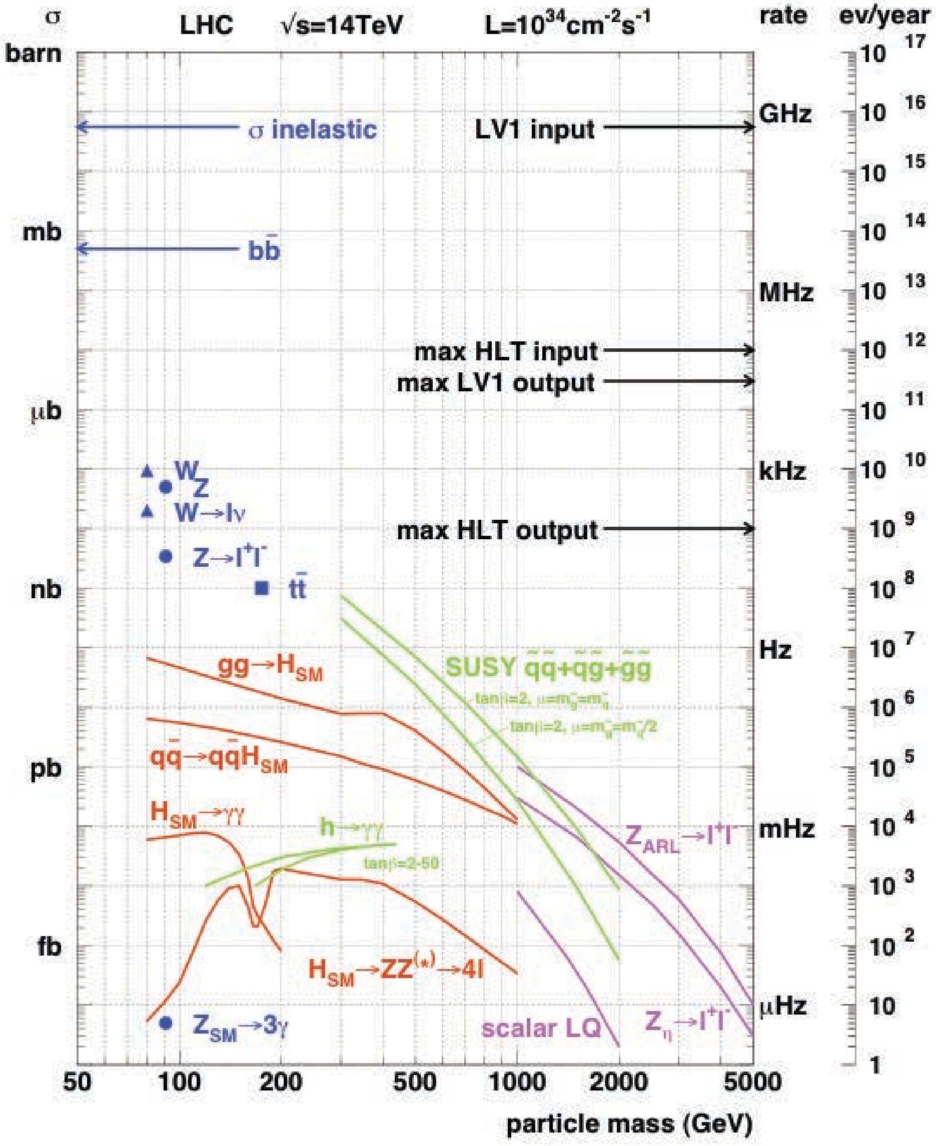
**At design *L* = $10^{34}$cm$^{-2}$s$^{-1}$**

- **23 pp events/25 ns xing**
  - ~ 1 GHz input rate
  - "Good" events contain ~ 20 bkg. events
- **1 kHz W events**
- **10 Hz top events**
- **< $10^4$ detectable Higgs decays/year**

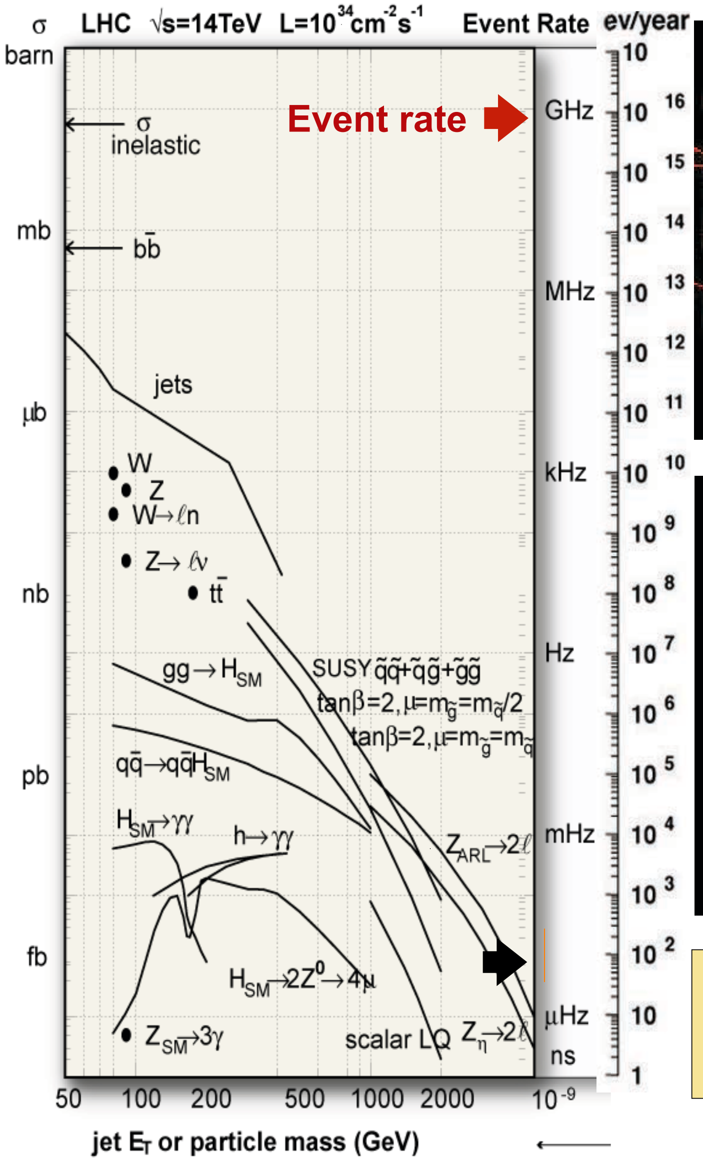
**Can store ~ 1 kHz events**

**Select in stages**

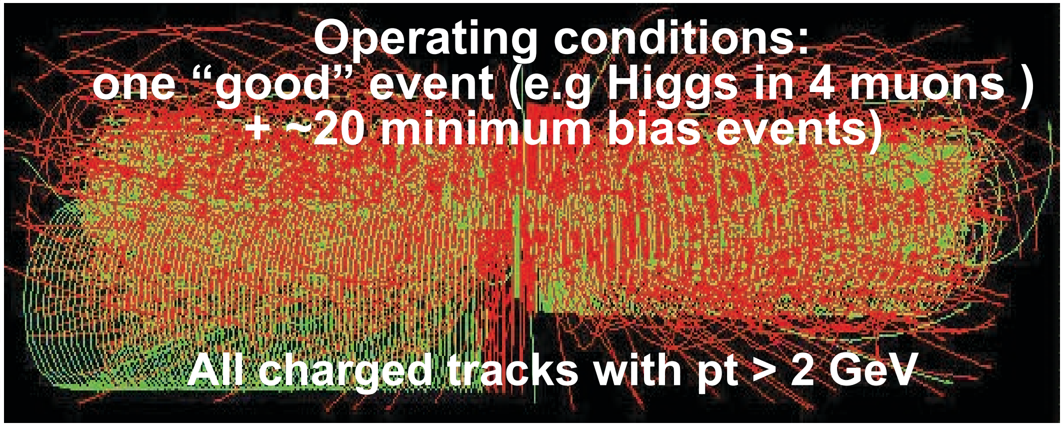
- **Level-1 Triggers**
  - 1 GHz to 100 kHz
- **High Level Triggers**
  - 100 kHz to 1 kHz



# Collisions (p-p) at LHC

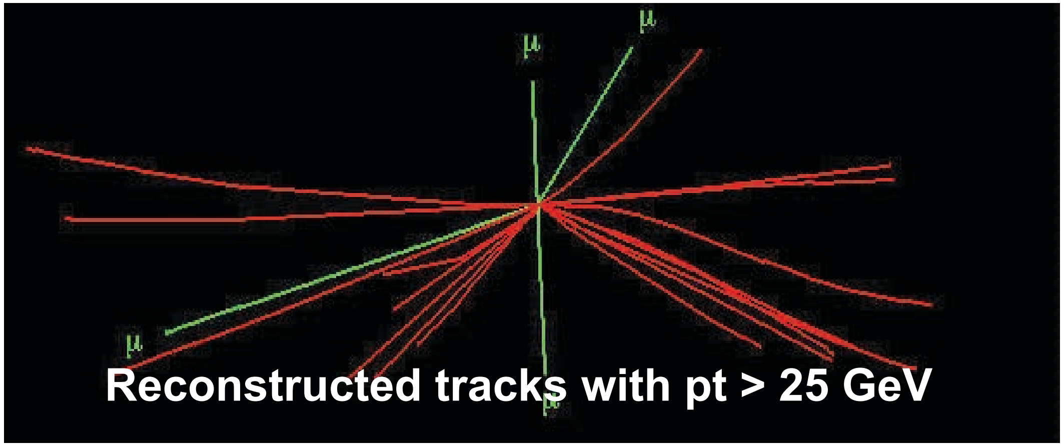


**Event rate**



**Operating conditions:**
**one "good" event (e.g Higgs in 4 muons )**
**+ ~20 minimum bias events)**

**All charged tracks with pt > 2 GeV**

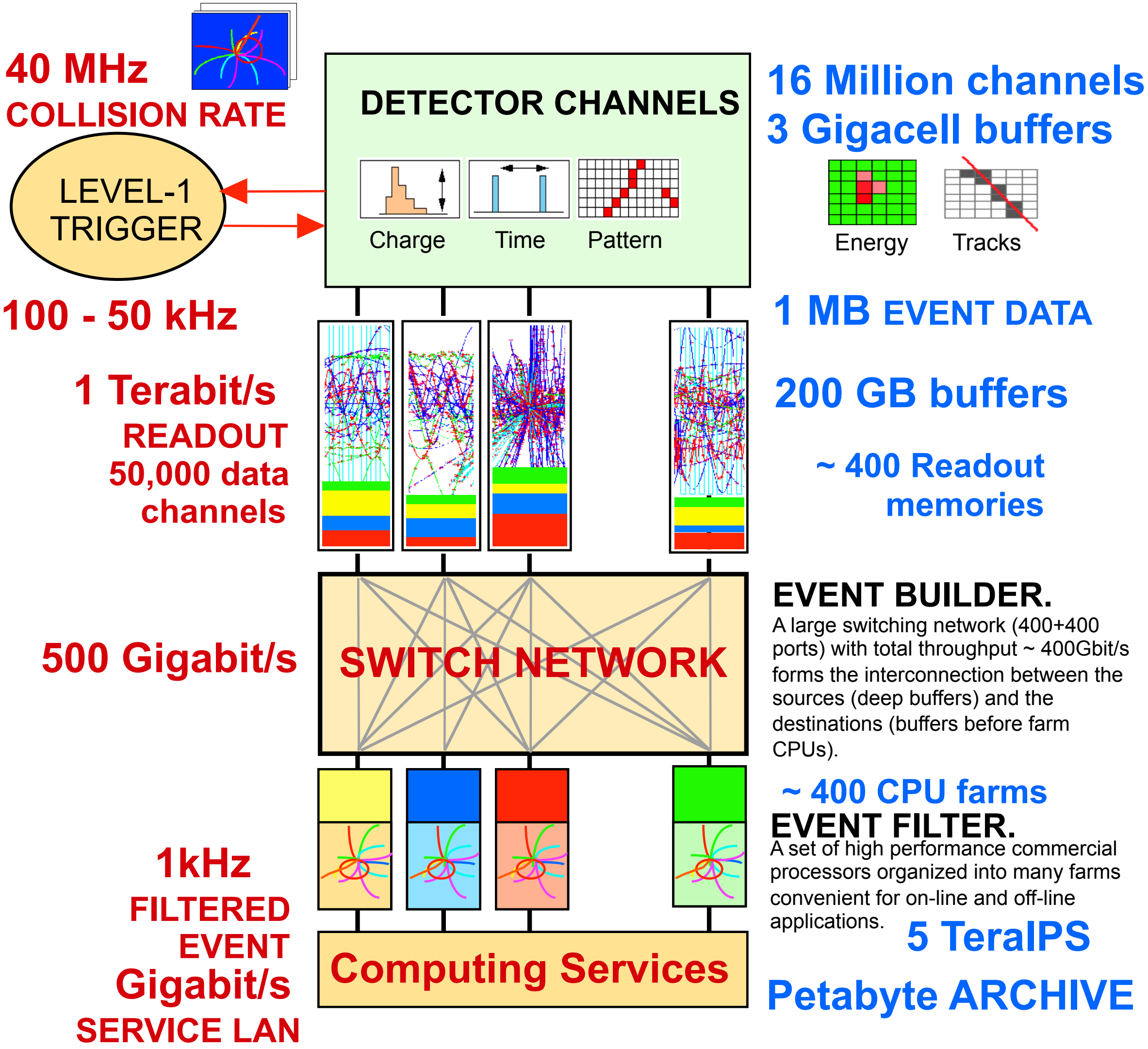


**Reconstructed tracks with pt > 25 GeV**

**Event size: ~1 MByte**

**Processing Power: ~X TFlop**

# LHC Trigger & DAQ Challenges



**40 MHz**
**COLLISION RATE**

LEVEL-1
TRIGGER

**100 - 50 kHz**

**1 Terabit/s**
**READOUT**
**50,000 data channels**

**500 Gigabit/s**

**1kHz**
**FILTERED EVENT**

**Gigabit/s**
**SERVICE LAN**

**DETECTOR CHANNELS**

**SWITCH NETWORK**

**Computing Services**

**16 Million channels**
**3 Gigacell buffers**

**1 MB EVENT DATA**

**200 GB buffers**

**~ 400 Readout memories**

**EVENT BUILDER.**
A large switching network (400+400 ports) with total throughput ~ 400Gbit/s forms the interconnection between the sources (deep buffers) and the destinations (buffers before farm CPUs).

**~ 400 CPU farms**

**EVENT FILTER.**
A set of high performance commercial processors organized into many farms convenient for on-line and off-line applications.

**5 TeraIPS**

**Petabyte ARCHIVE**

## Challenges:

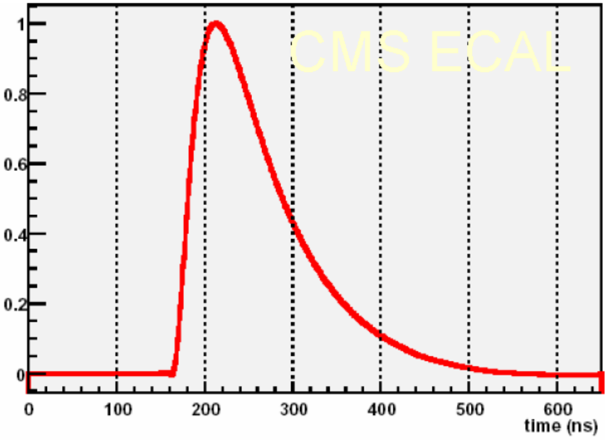
**1 GHz of Input Interactions**

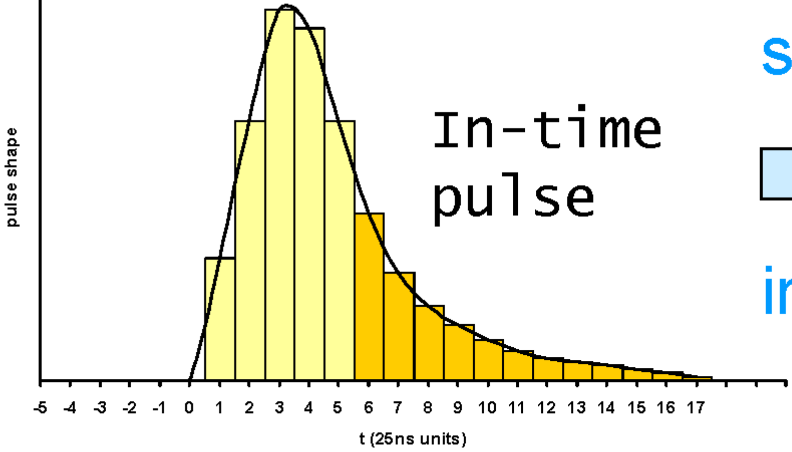
**Beam-crossing every 25 ns with ~ 23 interactions produces over 1 MB of data**

**Archival Storage up to 1 kHz of 1 MB events**

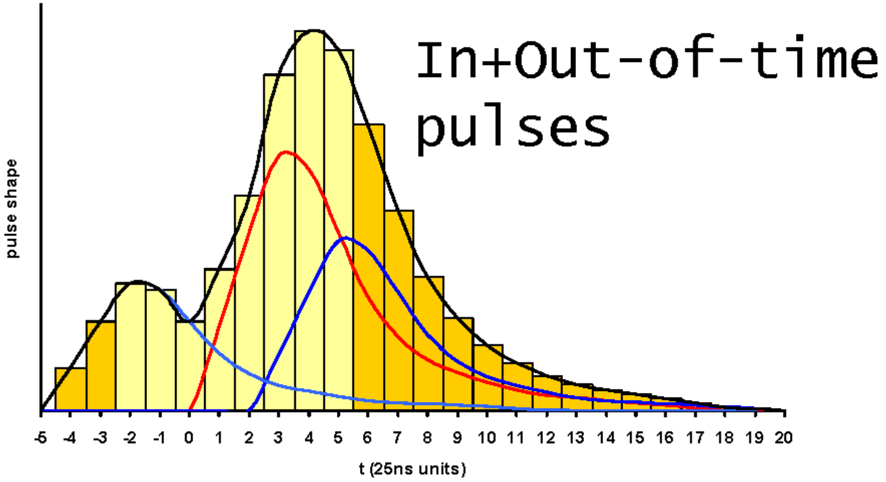
# Challenges: Pile-up

- “In-time” pile-up: particles from the same crossing but from a different pp interaction
- Long detector response/pulse shapes:
  - “Out-of-time” pile-up: left-over signals from interactions in previous crossings
  - Need “bunch-crossing identification”



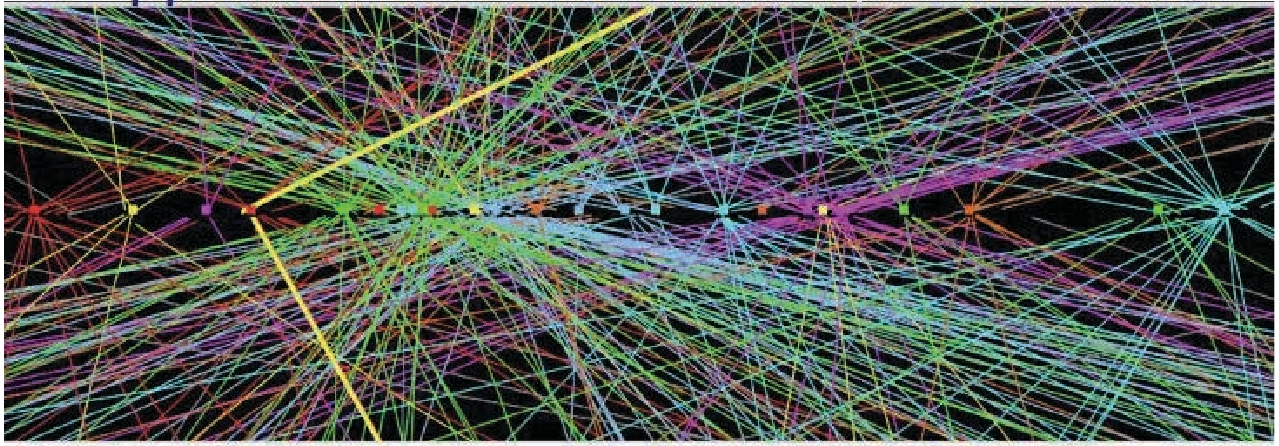


super–
impose

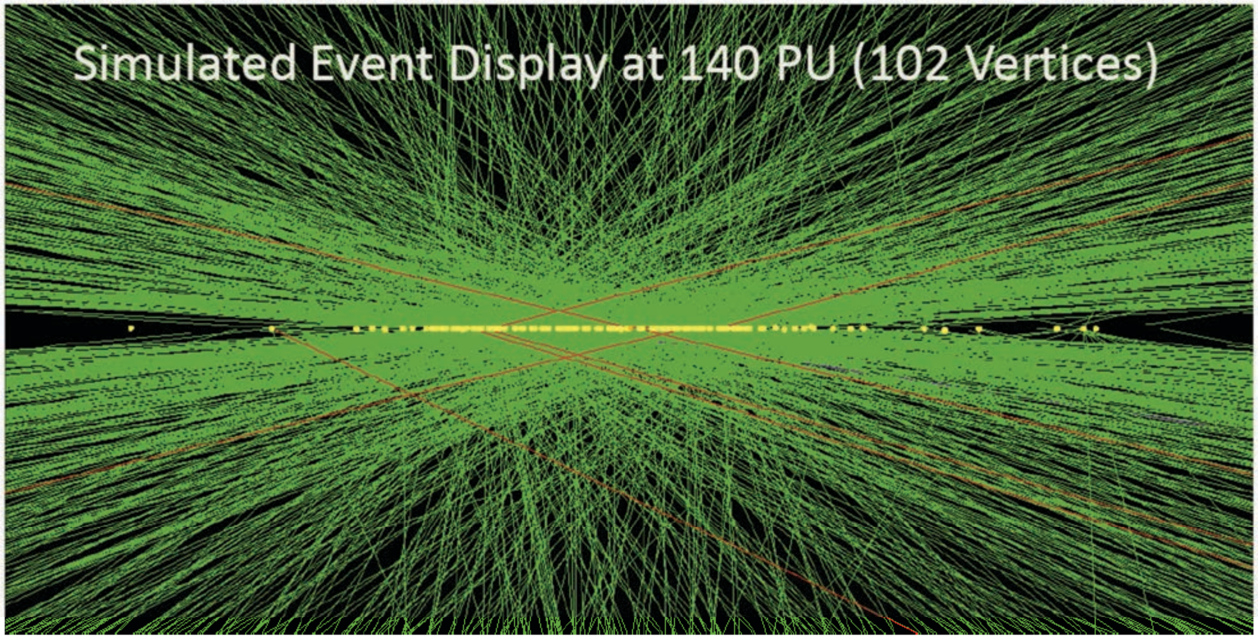


# PileUp: major trigger problem

Z→μμ event from 2012 data with 25 vertices



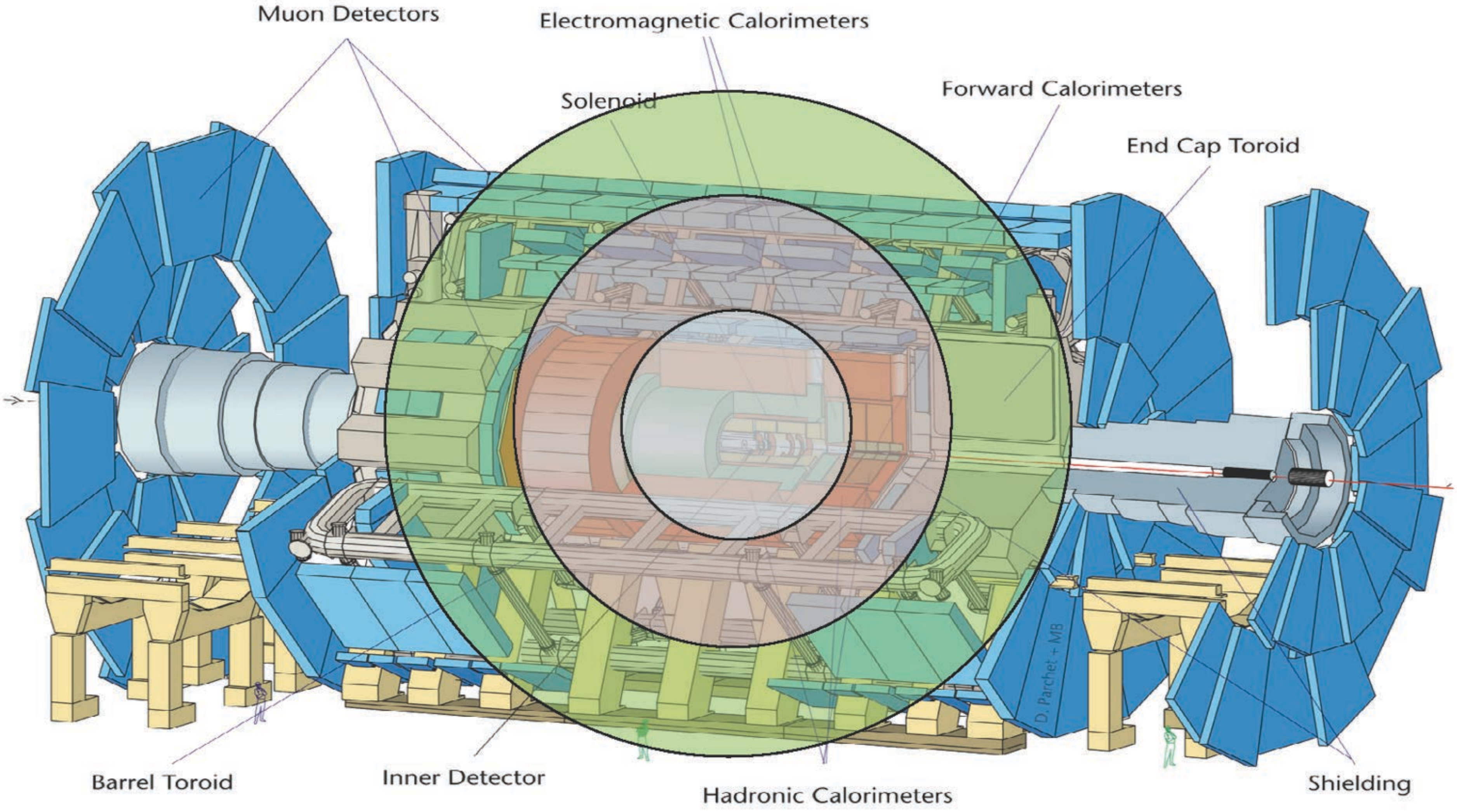
Now



High
Luminosity
LHC: 2025

# Challenges: Time of Flight

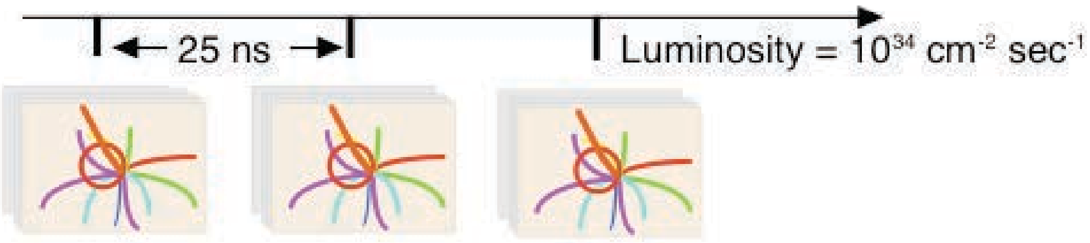
**c = 30 cm/ns → in 25 ns, s = 7.5 m**

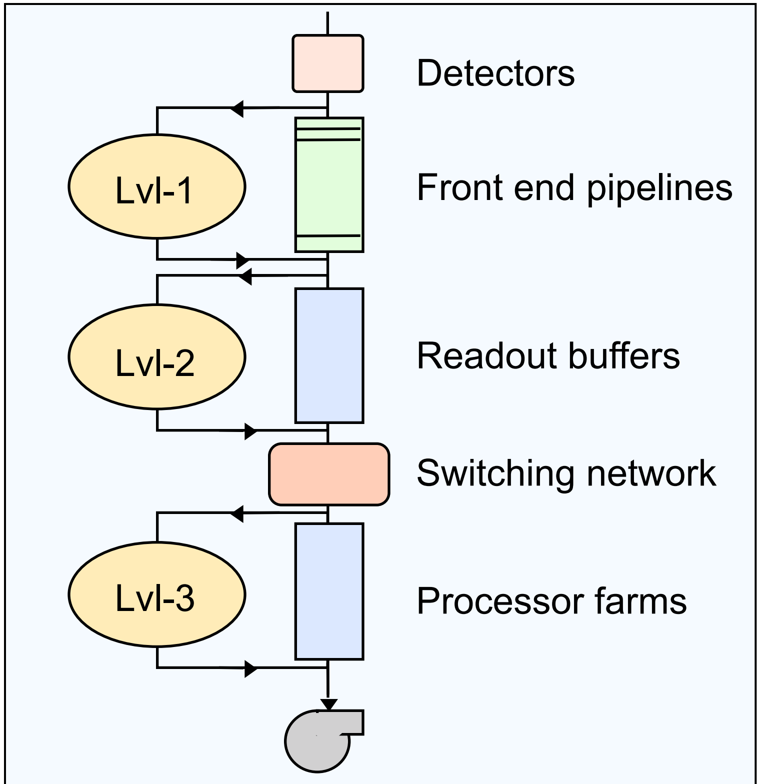


# ATLAS & CMS
# Trigger & Readout Structure

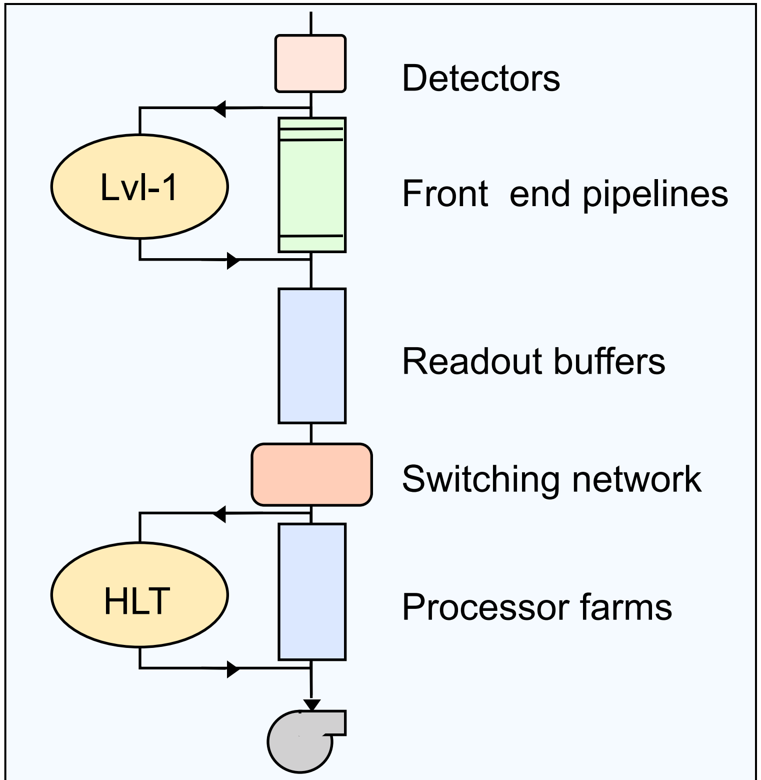
$\approx$ 30 Collisions/25ns
( $10^9$ event/sec )

$10^7$ channels
( $10^{16}$ bit/sec)


25 ns
Luminosity = $10^{34}$ cm$^{-2}$ sec$^{-1}$


Detectors
Lvl-1
Front end pipelines
Lvl-2
Readout buffers
Switching network
Lvl-3
Processor farms

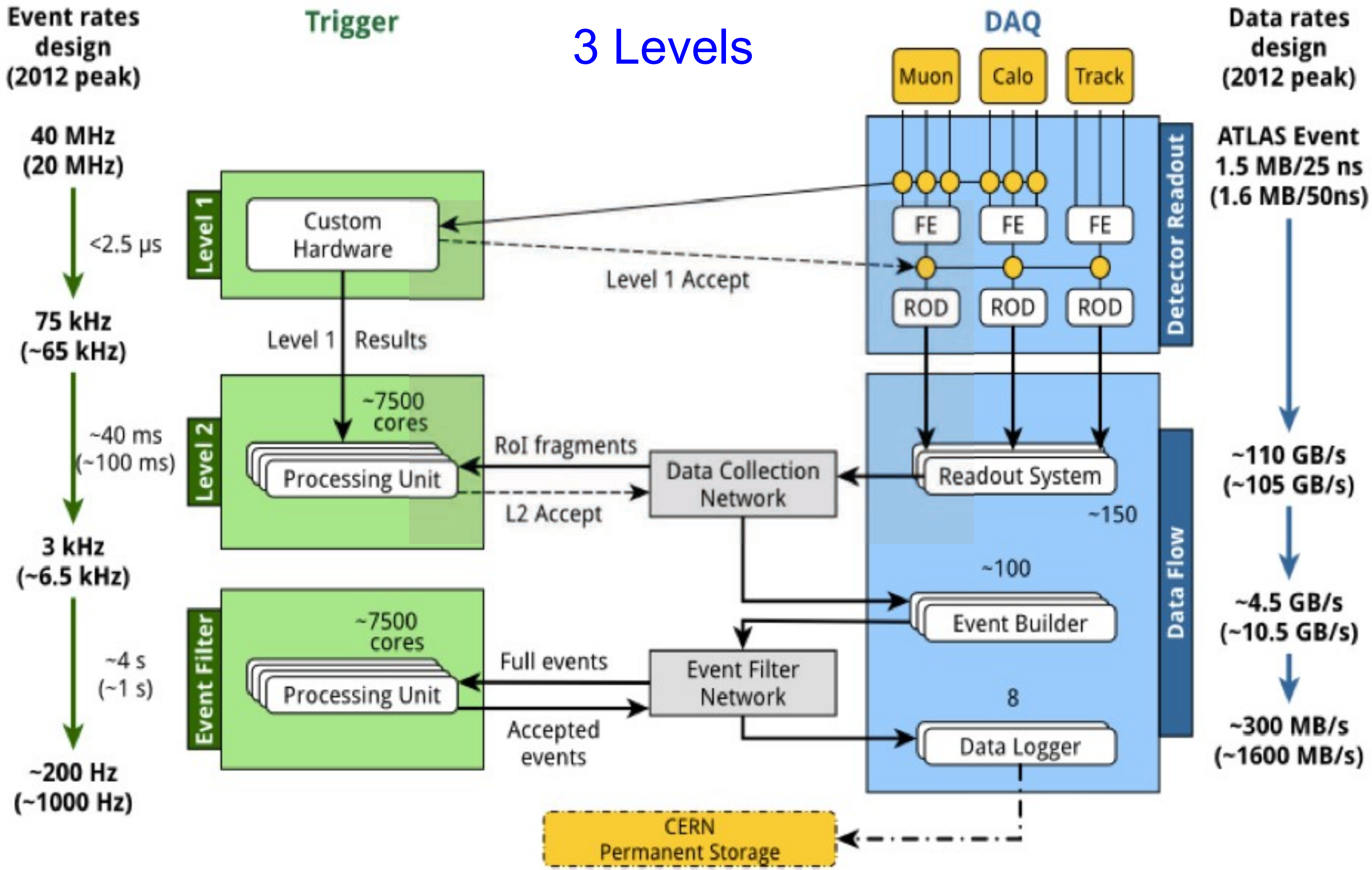
Run 1 ATLAS: 3 physical levels


Detectors
Lvl-1
Front end pipelines
Readout buffers
Switching network
HLT
Processor farms

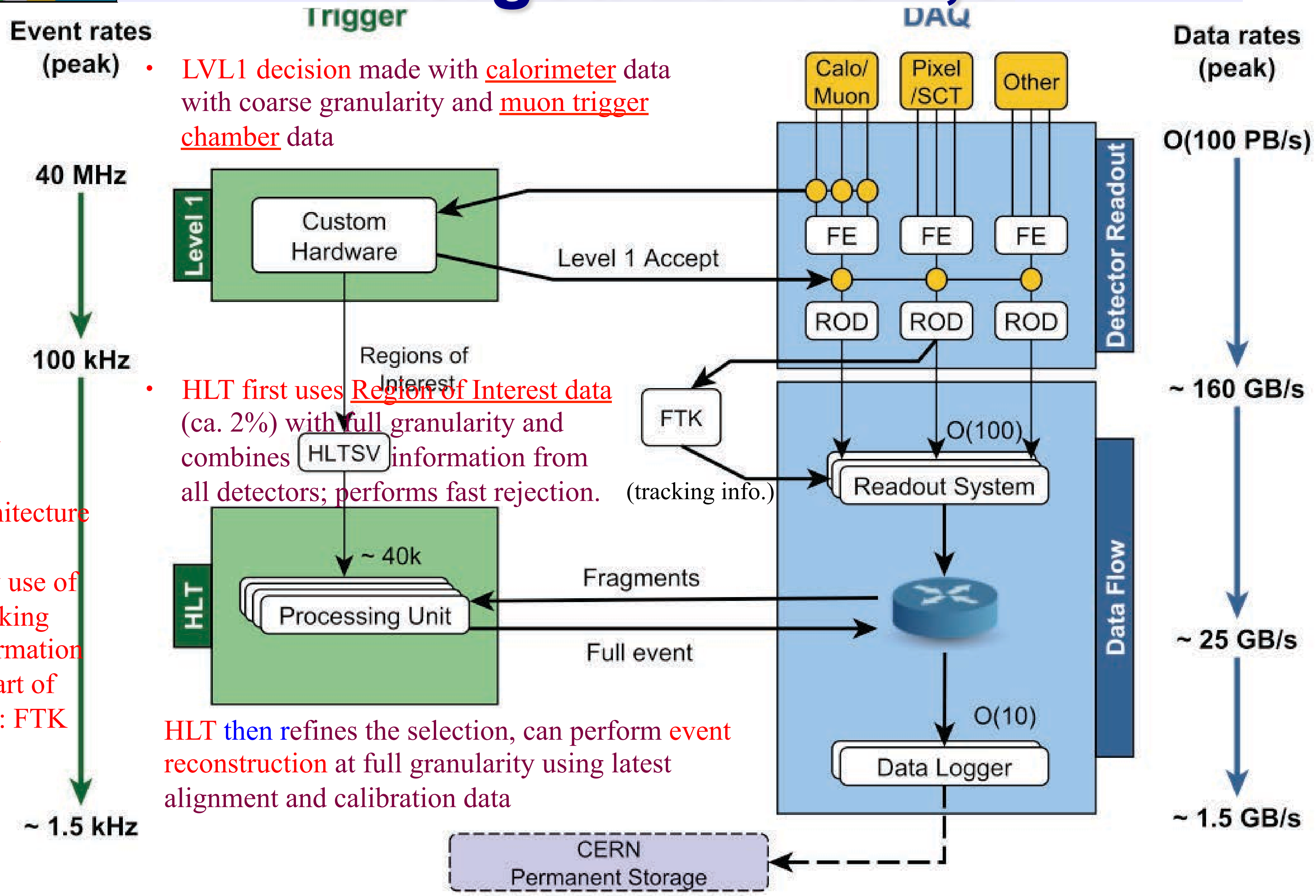
CMS: 2 physical levels

# ATLAS Run 1 Trigger & DAQ

3 Levels



# ATLAS Run 2 Trigger & DAQ: Merged Levels 2,3



- LVL1 decision made with calorimeter data with coarse granularity and muon trigger chamber data

- HLT first uses Region of Interest data (ca. 2%) with full granularity and combines information from all detectors; performs fast rejection.

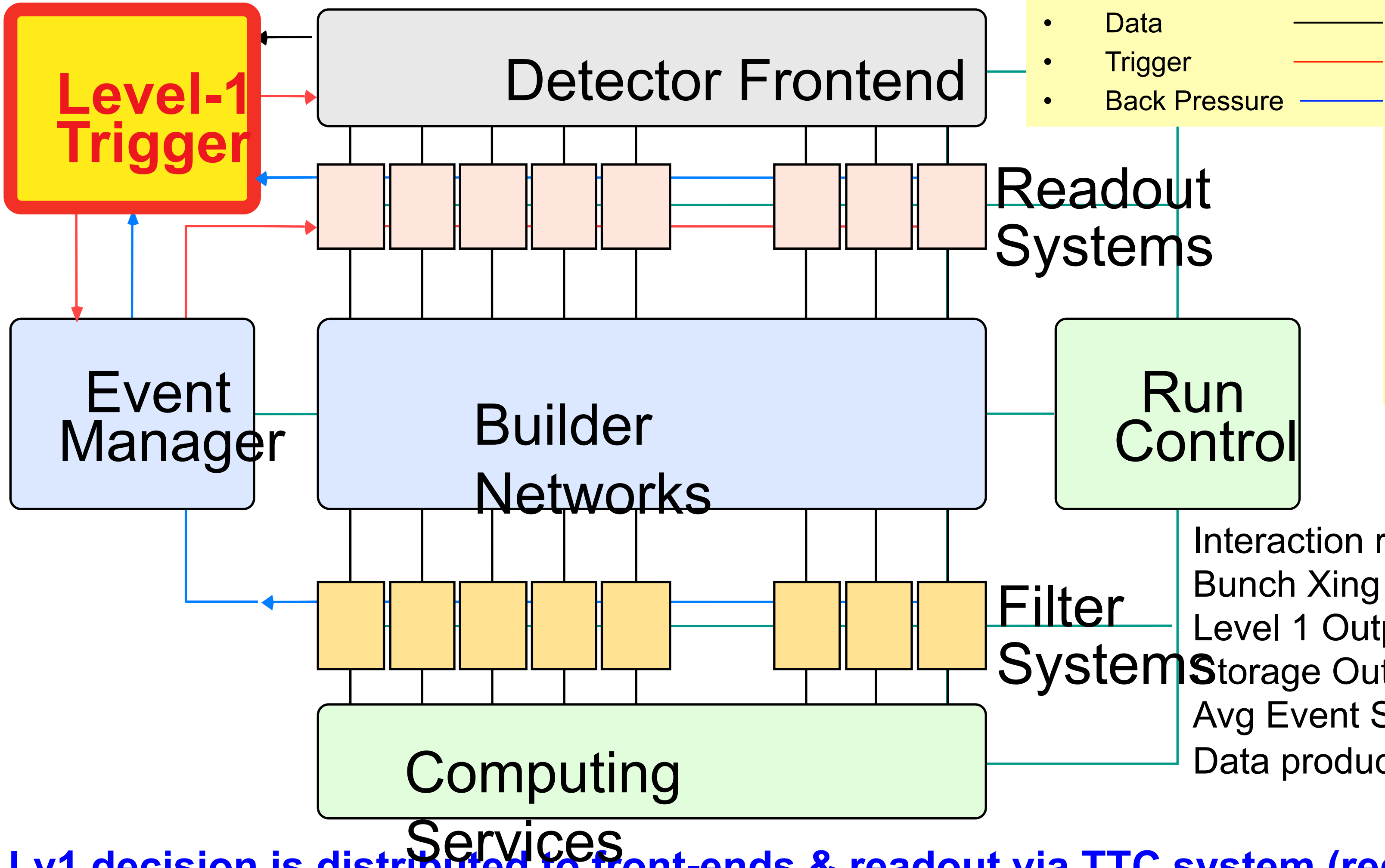
(tracking info.)

New HLT Architecture

New use of Tracking Information at start of HLT: FTK

HLT then refines the selection, can perform event reconstruction at full granularity using latest alignment and calibration data

# CMS Run 1,2 Trigger & DAQ: 2 Levels



**The Lv1-Accept decision causes the readout system to respond with backpressure information.**

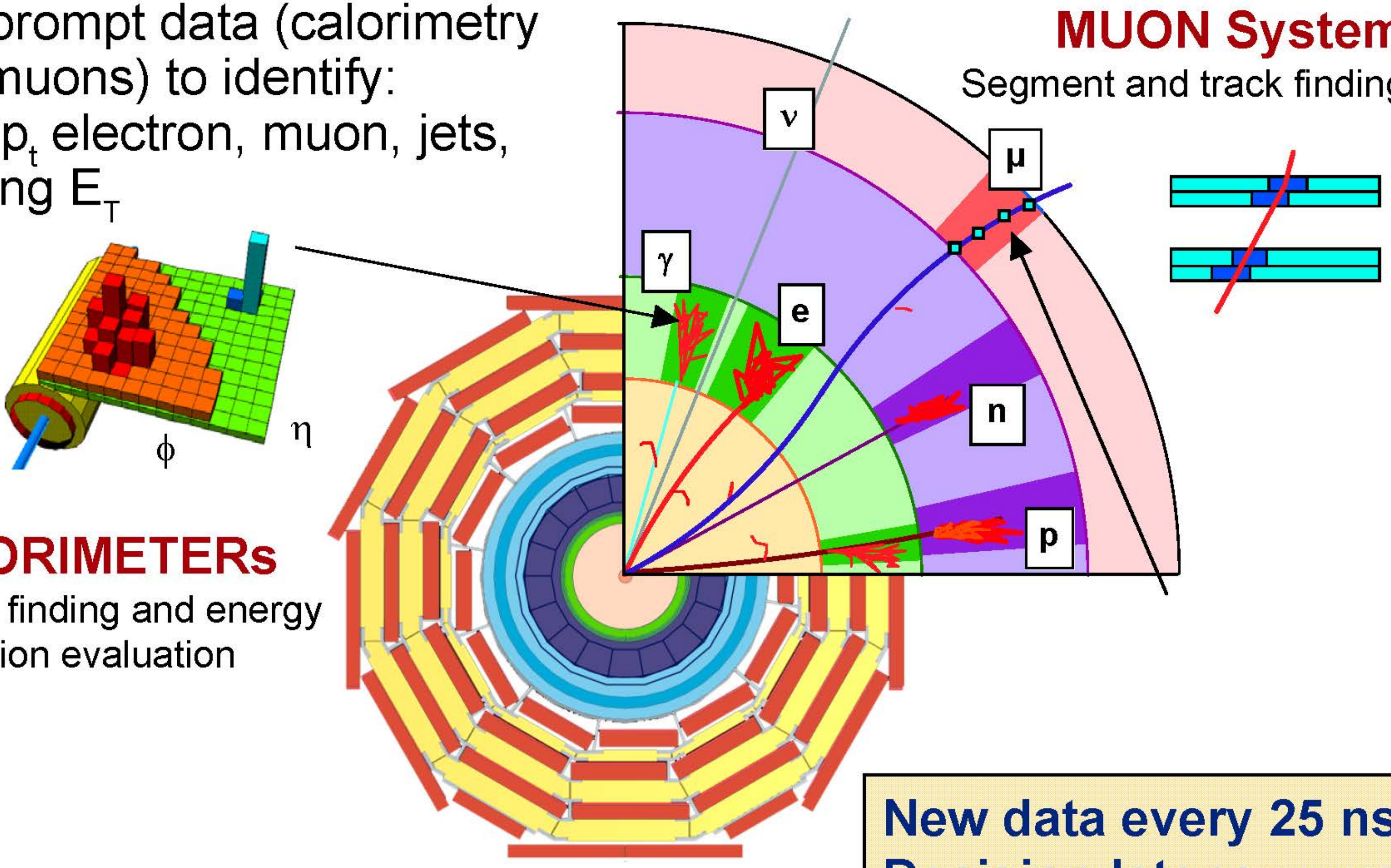
Interaction rate: 1 GHz
Bunch Xing rate: 40 MHz
Level 1 Output: 100 kHz
Storage Output: ~ 400 Hz
Avg Event Size: ~ 0.5 MB
Data production ~ 1 TB/day

**Lv1 decision is distributed to front-ends & readout via TTC system (red).**

**Readout buffers designed to accommodate Poisson fluctuations from 100 kHz Lv1 trigger rate.**

# Present ATLAS & CMS Level 1 Trigger Data

Use prompt data (calorimetry and muons) to identify:
High $p_t$ electron, muon, jets, missing $E_T$



**MUON System**

Segment and track finding

**CALORIMETERs**

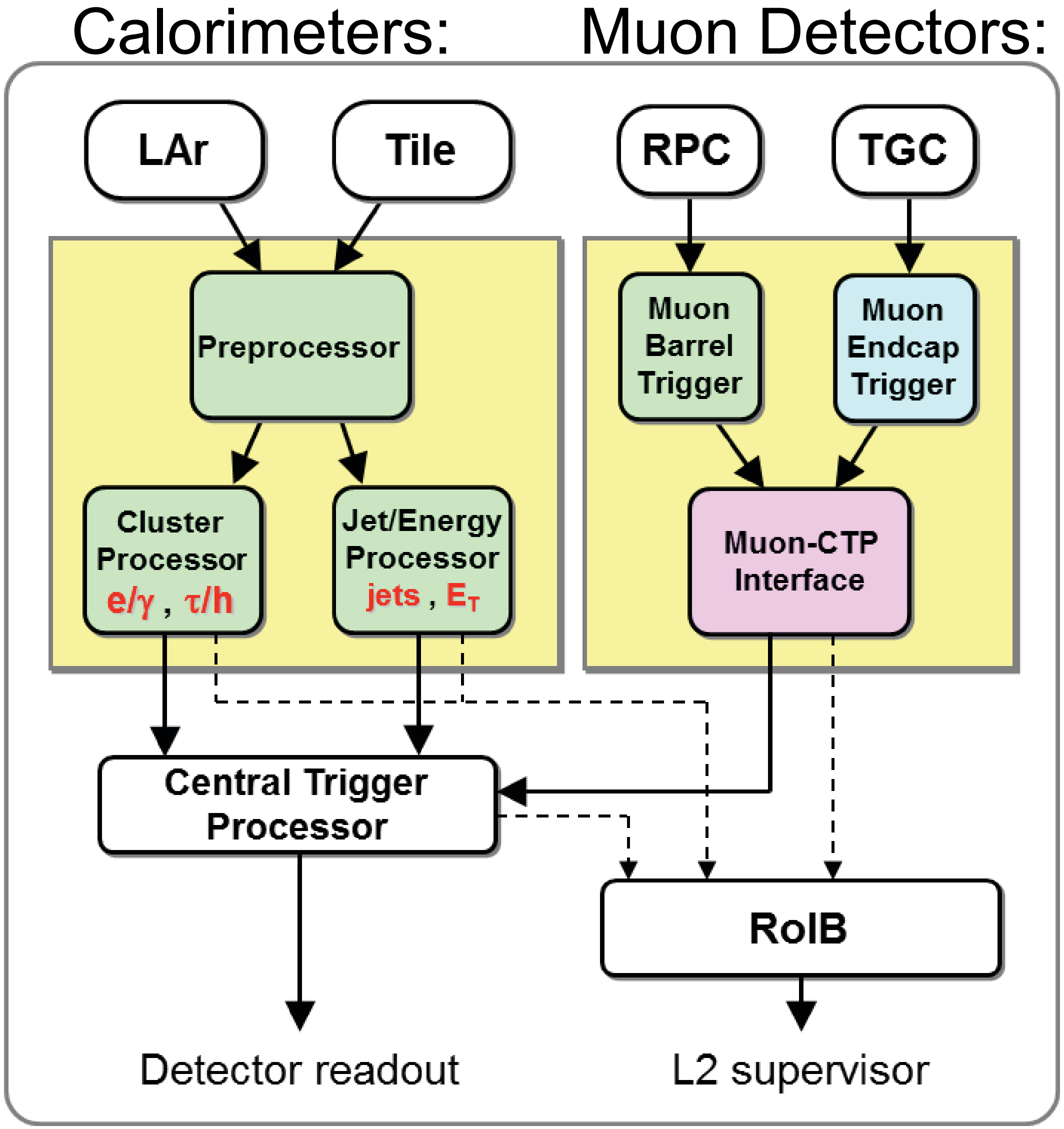
Cluster finding and energy deposition evaluation

**New data every 25 ns**
**Decision latency ~ μs**

# Run 1 ATLAS L1 Trigger

Process reduced granularity data from calorimeter and muon detectors

- Trigger decision based on object multiplicities
- Generate L1A and send via TTC distribution to detector front-ends to initiate readout
- Maximum round-trip latency 2.5 us
  - ➢ Data stores in on-detector pipelines
- Identify regions-of-interest (RoI) to seed L2 trigger
- Custom built electronics
- Synchronous, pipelined processing system operating at the bunch crossing rate



# ATLAS Run 1 RoI Mechanism

**LVL1 triggers on high $p_T$ objects**

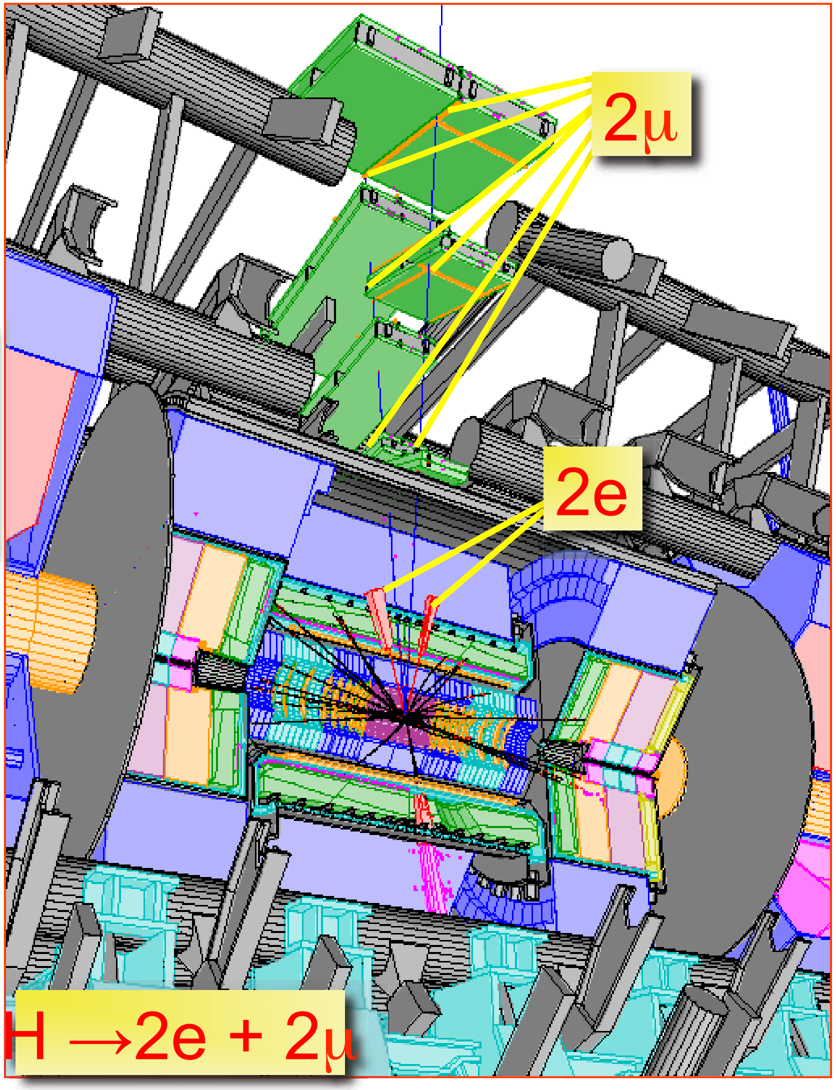
- **Calorimeter cells and muon chambers to find e/γ/τ-jet-μ candidates above thresholds**

LVL2 uses Regions of Interest as identified by Level-1

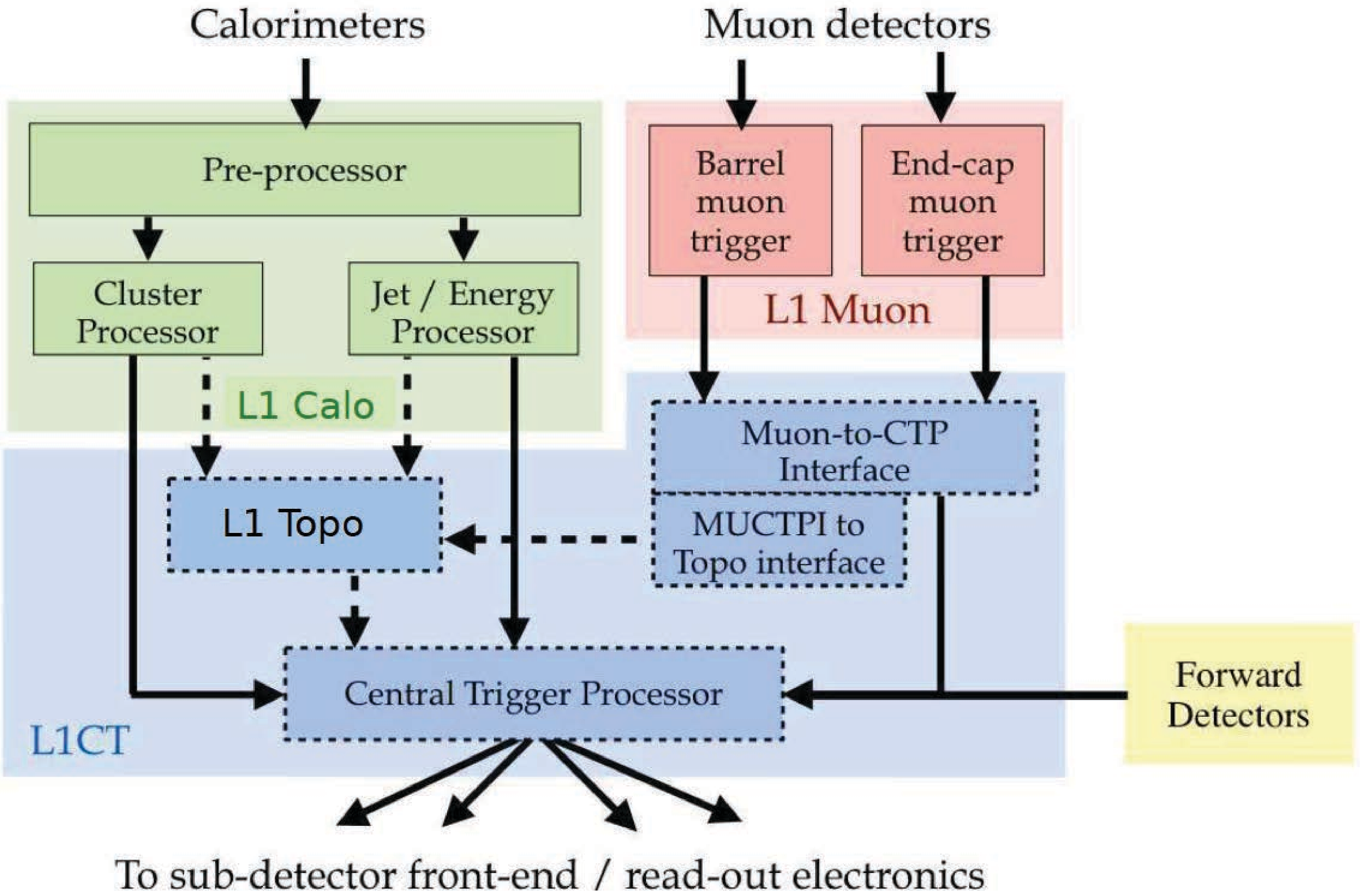
- Local data reconstruction, analysis

The total amount of RoI data is minimal

- ~2% of the Level-1 throughput but it has to be extracted from the rest at 75 kHz



# ATLAS Run 2 L1 Trigger



Calorimeters

Muon detectors

Pre-processor

Cluster Processor

Jet / Energy Processor

L1 Calo

Barrel muon trigger

End-cap muon trigger

L1 Muon

Muon-to-CTP Interface

MUCTPI to Topo interface

L1 Topo

Central Trigger Processor

Forward Detectors

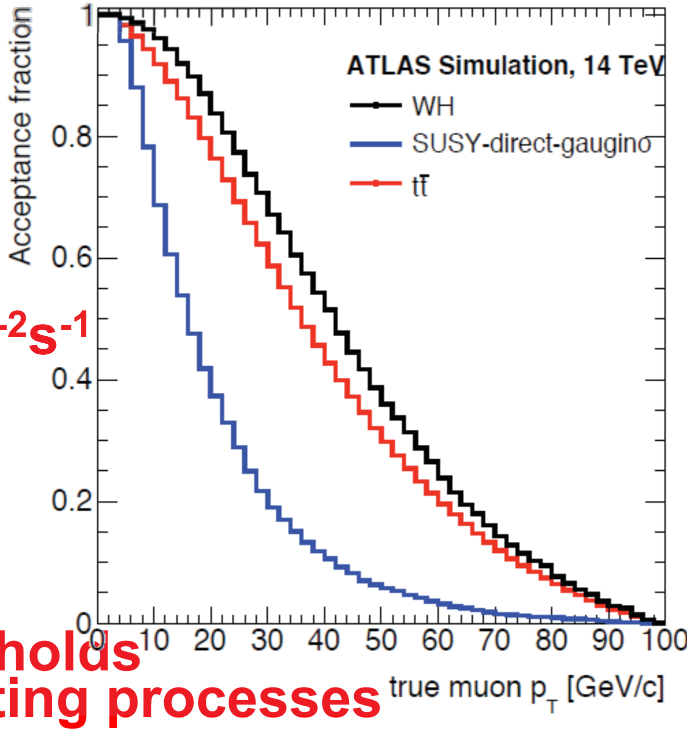
L1CT

To sub-detector front-end / read-out electronics

# ATLAS, CMS Trigger HL-LHC Upgrades

**Maintain current physics sensitivity at HL-LHC challenging for trigger**

- ➢ EWK, top (and Higgs) scale physics remain critical for HL-LHC
- ➢ Cannot fit same “interesting” physics events in trigger at 13-14 TeV, $5\times10^{34}$ cm$^{-2}$s$^{-1}$



- Increasing $p_T$ thresholds reduces signal efficiency
  - ➢ Trigger on lepton daughters from H→ZZ at $p_T$ ~ 10-20 GeV
  - ➢ Very easy to reach the worst case: thresholds increase beyond energy scale of interesting processes
- Backgrounds from HL-LHC pileup further reduces the ability to trigger on rare decay products
  - ➢ Leptons, photons no longer appear isolated and are lost in QCD backgrounds
  - ➢ Increased hadronic activity from pileup impacts jet $p_T$ and MET measurements

# ATLAS,CMS @ HL-LHC

An introductory Summary

## ATLAS*:

- ➢Divide L1 Trigger into L0, L1 of latency 6, 30 μsec, rate ≤ 1 MHz, ≤ 400 kHz, HLT output rate of 5-10 kHz
  - Calorimeter readout at 40 MHz w/backend waveform processing (140 Tbps)
- ➢L0 uses Cal. & μ Triggers, which generate track trigger seeds
- ➢L1 uses Track Trigger and more fine-grained calorimeter trigger information.

## CMS:

- ➢L1 Trigger latency: 12.5 μsec
- ➢L1 Trigger rate: 500 kHz (PU=140), 750 kHz (PU=200)
- ➢L1 uses Track Trigger, finer granularity μ & calo. Triggers
- ➢HLT output rate of 5 kHz (PU=140), 7.5 kHz (PU=200)

# ATLAS & CMS Triggered vs. Triggerless Architectures

## 1 MHz (Triggered) - planned:

- **Network:**
  - 1 MHz with ~5 MB: aggregate ~40 Tbps
  - Links: Event Builder-cDAQ: ~ 500 links of 100 Gbps
  - Switch: almost possible today, for 2022 no problem
- **HLT computing:**
  - General purpose computing: 10(rate)x3(PU)x1.5(energy)x200kHS6 (CMS)
    - **Factor ~50 wrt today maybe for ~same costs**
  - Specialized computing (GPU or else): Possible

## 40 MHz (Triggerless) – not planned:

- **Network:**
  - 40 MHz with ~5 MB: aggregate ~2000 Tbps
  - Event Builder Links: ~2,500 links of 400 Gbps
  - Switch: has to grow by factor ~25 in < 10 years, difficult
- **Front End Electronics**
  - Readout Cables: Copper Tracker! – Show Stopper
- **HLT computing:**
  - General purpose computing: 400(rate) x3(PU)x1.5(energy)x200kHS6 (CMS)
    - **Factor ~2000 wrt today, but too pessimistic since events easier to reject w/o L1**
    - **This factor looks impossible with realistic budget**
  - Specialized computing (GPU or …)
    - **Could possibly provide this …**

# ATLAS & CMS L1 Tracking Trigger

## Reduces Leptonic Trigger Rate

- Validate calorimeter or muon trigger object, e.g. discriminating electrons from hadronic ($\pi^0 \rightarrow \gamma\gamma$) backgrounds in jets
- Addition of precise tracks to improve precision on $p_T$ measurement, sharpening thresholds in muon trigger
- Degree of isolation of $e$, $\gamma$, $\mu$ or $\tau$ candidate
- Requires calorimeter trigger trigger at the finest granularity to reduce electron trigger rate

## Other Triggers

- Primary z-vertex location within 30 cm luminous region derived from projecting tracks found in trigger layers,
- Provide discrimination against pileup events in multiple object triggers, e.g. in lepton plus jet triggers.

# HL-LHC L1 Track Trigger Architectures:

**"Self - seeded" path (CMS Tracker Approach – runs at 40 MHz):**

- **L1 tracking trigger data calculated stand-alone, combined with calorimeter & muon trigger data regionally with finer granularity than presently employed.**
- **After regional correlation stage, physics objects made from tracking, calorimeter & muon regional trigger data transmitted to Global Trigger.**

**"RoI - based" path (ATLAS Tracker Approach):**

- **L1 calorimeter & muon triggers produce a "Level-0" or L0 "pre-trigger" after latency of present L1 trigger, with request for tracking info at ≤ 1 MHz. Request only goes to regions of tracker where candidate was found. Reduces data transmitted from tracker to L1 trigger logic by ≤ 40 (40 MHz to ≤ 1 MHz) times probability of a tracker region to be found with candidates, which could be < 10%, (e.g. 100 kHz, ~ speed of ATLAS FTK – *seeds HLT*)**
- **Tracker sends out info. for these regions only & this data is combined in L1 correlation logic, resulting in L1A combining track, muon & calo. info..**

**"HLT Usage" (both ATLAS & CMS):**

- **L1 Track trigger info, along with rest of information provided to L1 is used at very first stage of HLT processing. Provides track information to HLT algorithms very quickly without having to unpack & process large volume of tracker information through CPU-intensive algorithms. Helps limit the need for significant additional processor power in HLT computer farm.**

# ATLAS HL-LHC TriDAQ

Level-0 Muon & Calo used to make initial fast rejection and identify Regions of Interest

- 1 MHz accept rate, trigger latency 6 μs,minimum detector latency 10 μs

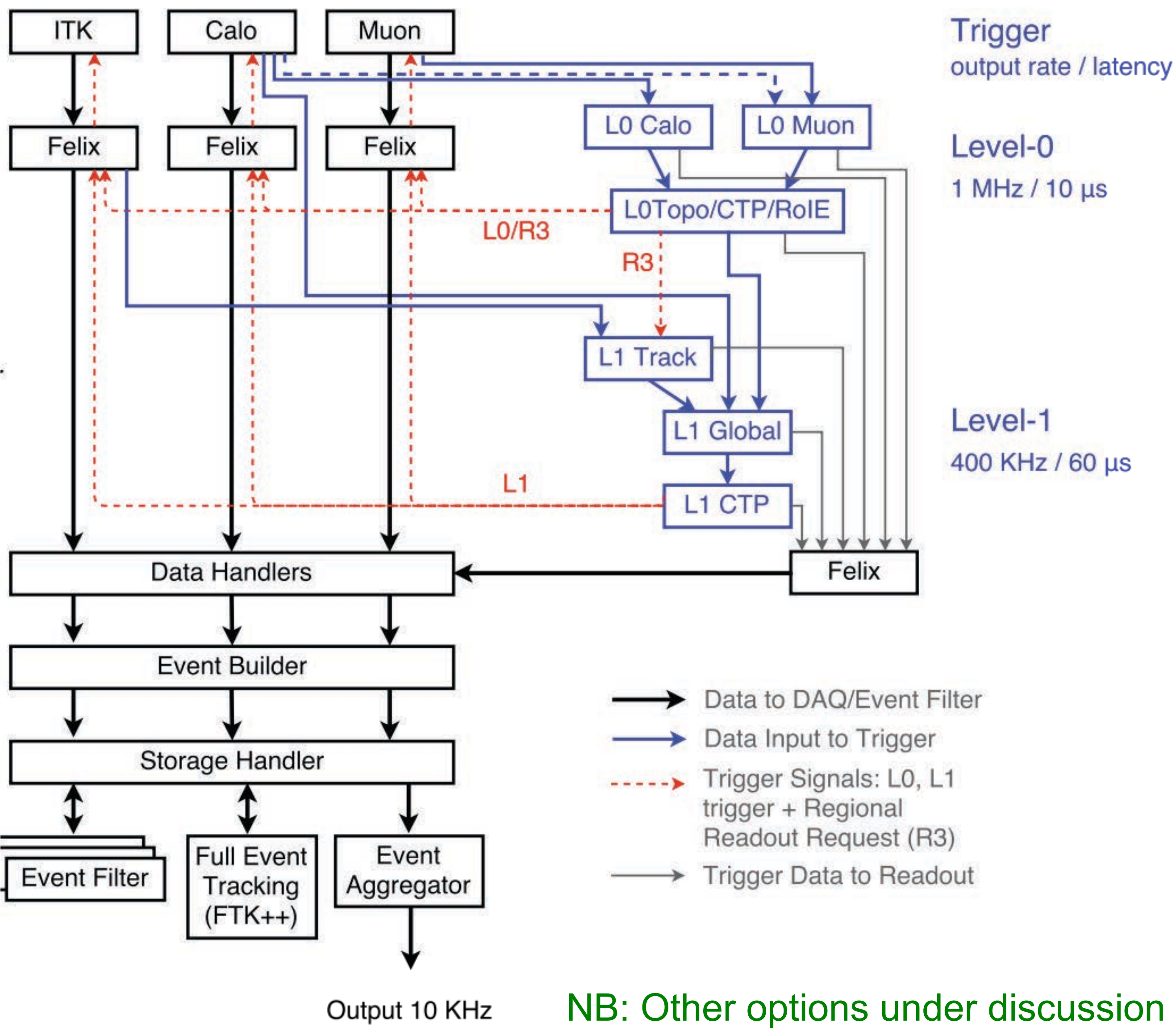
Level-1 hardware track trigger and high resolution calo data provide further rejection

L1Track and L0Calo/ L0Muon feed to L1Global processor

- 400 kHz accept rate, trigger latency 30 μs, minimum detector latency 60 μs

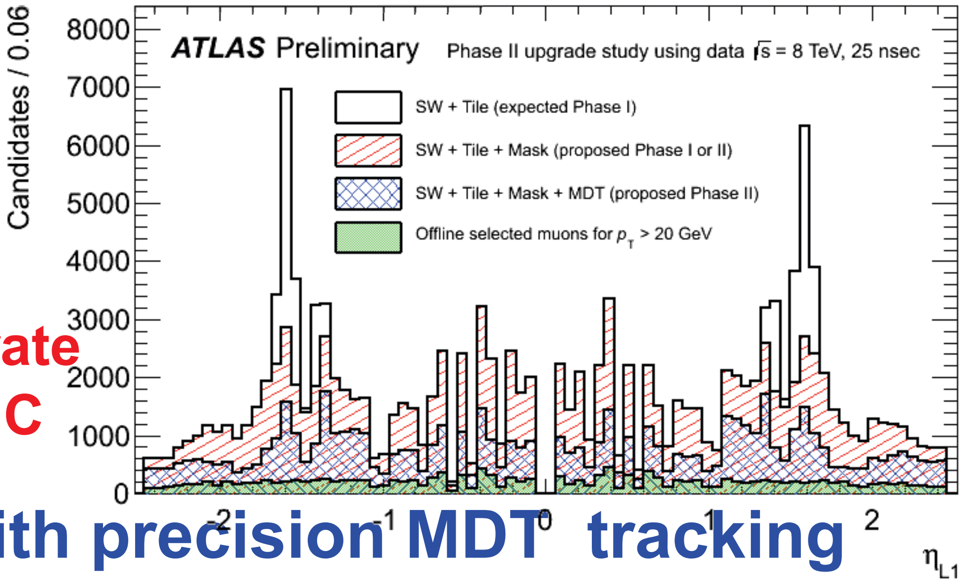
Event Filter (commodity farm + HW tracking) delivers a factor 40 reduction down to output rate of 10 kHz

- FTK++ full event track processor down to $p_T$ > 1 GeV at 100 kHz



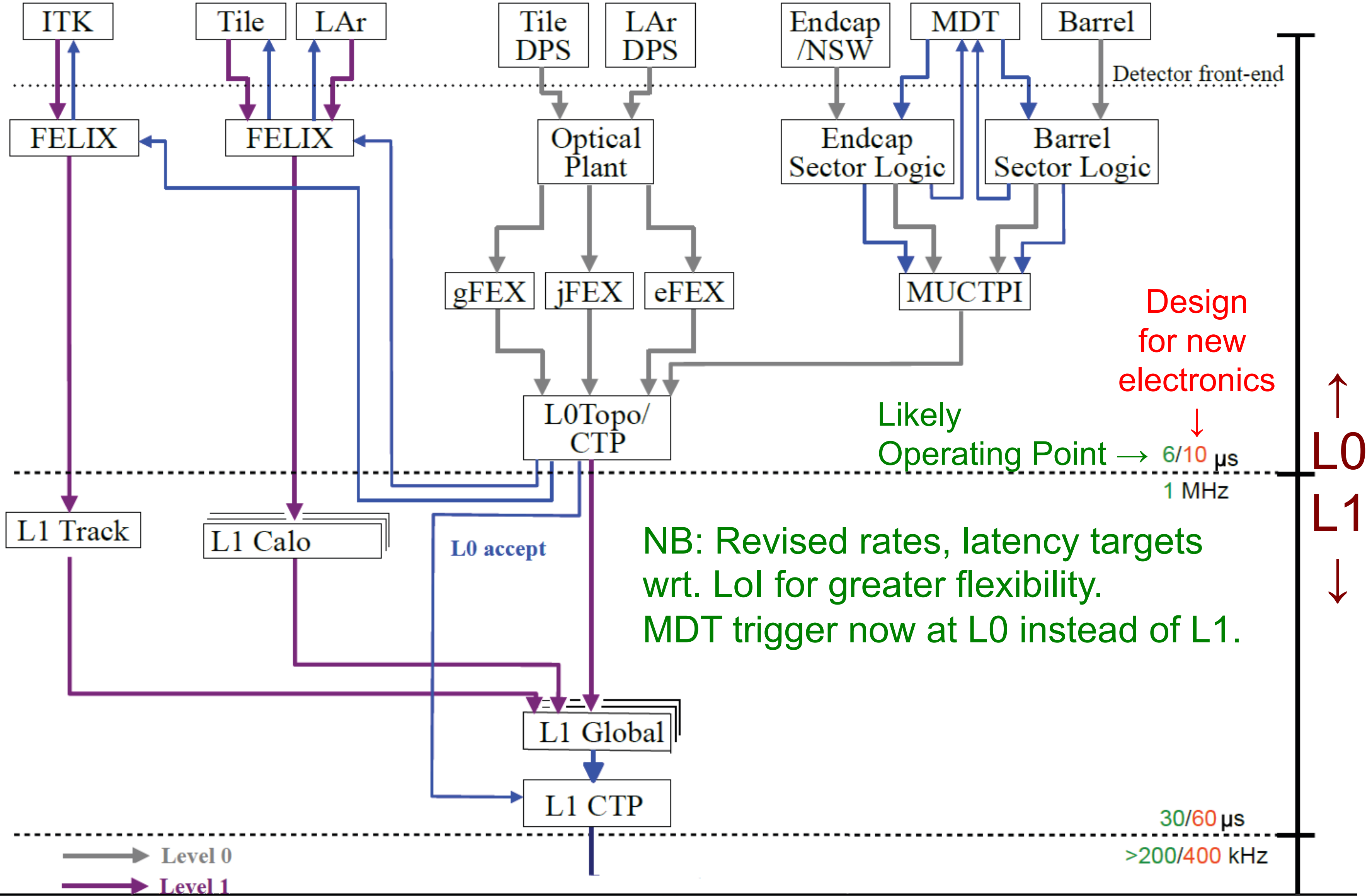
NB: Other options under discussion

# ATLAS Upg. Trig. Components



- **L0 Calorimeter trigger is same as L1Calo in Run 2**
  - Now with digital input from hadronic calorimeter as well
- **New L0 Muon electronics**
  - To deal with higher latency/rate
  - Will replace coincidence ASIC with more flexible FPGA
- **Augment L0 Muon trigger with precision MDT tracking**
  - Estimated to give factor 2 rejection across η
- **L0 Central trigger and topology trigger to be replaced**
  - Need to provide Regions-of-Interest to L1
- **L1 Track trigger in RoIs from L0 triggers**
  - Details to follow
- **New full(?) granularity L1 calorimeter trigger**
  - Architecture and possible algorithms under study

# ATLAS HL-LHC L0/1 Trigger



NB: Revised rates, latency targets wrt. LoI for greater flexibility.
MDT trigger now at L0 instead of L1.

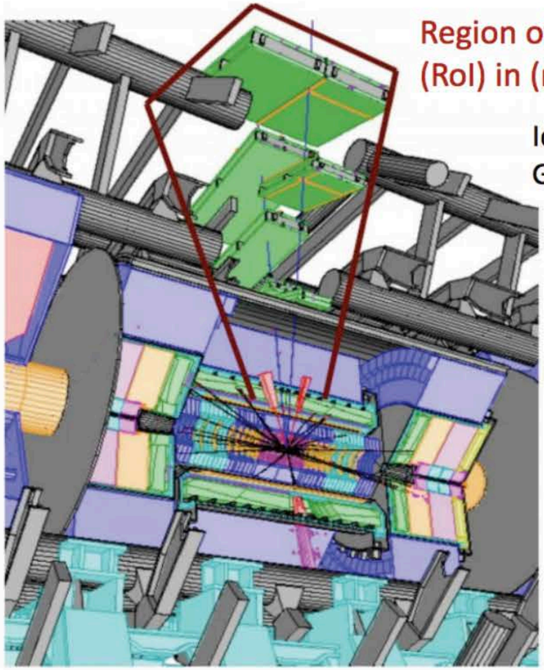
# ATLAS HL-LHC L0 Trigger

## L0 Trigger Components:

L0 Calo:
- Existing Phase-1 L1Calo trigger system becomes L0Calo trigger for HL-LHC
- FEX system receives firmware upgrade; largely same hardware as Run 3

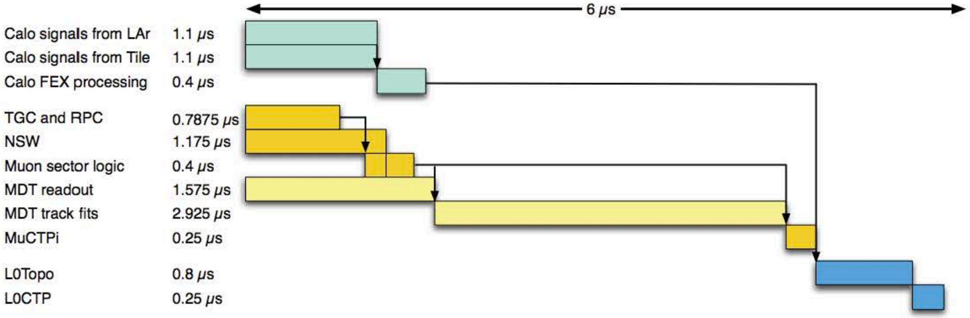
L0 Muon:
- New readout and improved coverage to increase efficiency
- Latency now long enough to use precision MDTs for sharper turn on

L0Topo/Central Trigger Processor/RoIEngine
- Receives trigger objects from L0Calo and L0Muon
- Performs complex trigger selections (invariant mass, missing transverse energy, etc.)
- On L0-Accept, the RoIEngine calculates the Regional Readout Requests to send back to the detectors
- RoIs cover at most 10% of detector => 100 kHz equivalent rate for readout



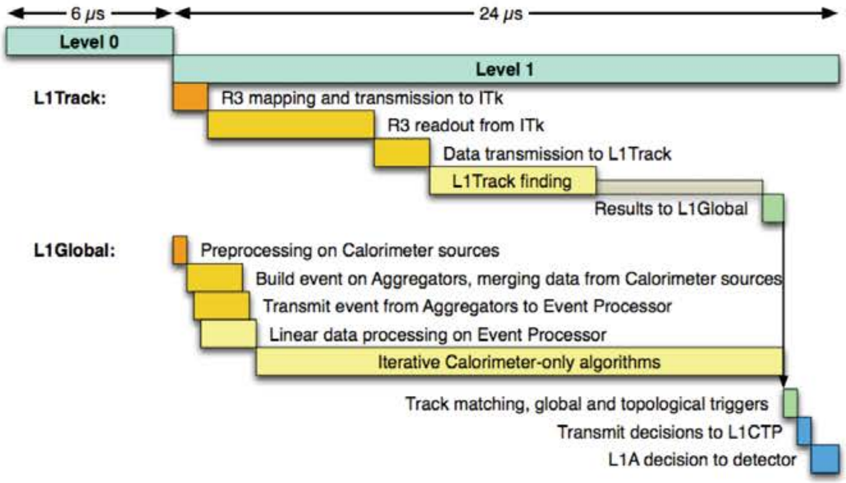
Region of Interest (RoI) in (η,φ)

Identified at L0
Guide L1, EF



- Wade Fisher, MSU, CPAD16

# ATLAS L1 Track Trigger



6 μs

24 μs

Level 0

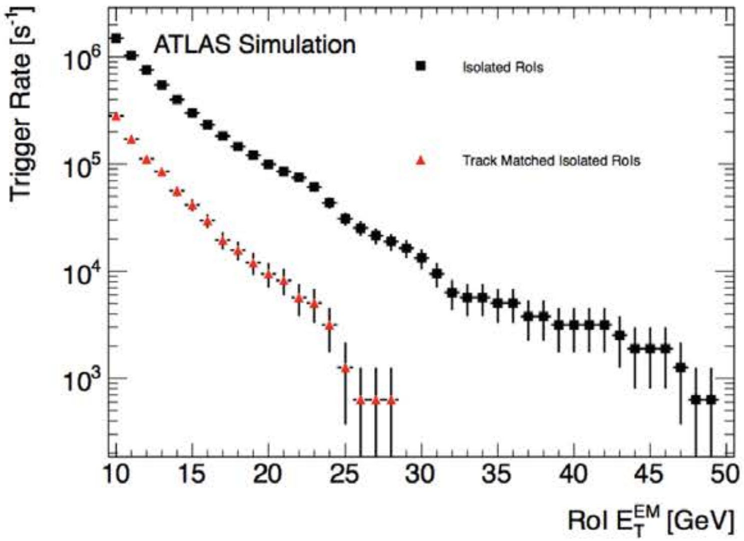
Level 1

**L1Track:**

- R3 mapping and transmission to ITk
- R3 readout from ITk
- Data transmission to L1Track
- L1Track finding
- Results to L1Global

**L1Global:**

- Preprocessing on Calorimeter sources
- Build event on Aggregators, merging data from Calorimeter sources
- Transmit event from Aggregators to Event Processor
- Linear data processing on Event Processor
- Iterative Calorimeter-only algorithms
- Track matching, global and topological triggers
- Transmit decisions to L1CTP
- L1A decision to detector



Level-1 Track Trigger receives ITk data from regions around RoIs contributing to L0-Accept

- Finds tracks in those regions above 4 GeV pT cut
- Quasi-offline resolution, reconstruction efficiency at least 95% for offline tracks
- Rejection factor of 5 for single lepton triggers, pileup track resolution < ~10 mm

Regional readout of 10% ITk in ~6 μs

- Strip front-end readout chips with double-buffer capability
- Full pixel readout at 1 MHz

FTK next-gen associative memory chip and track-fit on FPGA

- 500k track patterns per AM chip at 200 MHz
- 4 fit/ns on modern FPGA

\- Wade Fisher, MSU, CPAD16

# ATLAS Upgrade L1T Latency, Performance

## Latency:

- **~24μs from L0A to L1A:**
  - ~6μs for regional (R3) data readout
  - ~12-15μs for L1Track pattern recognition
  - ~3-6μs for cable times, Global L1 processing, decision
  - Accepts consecutive 25 ns beam crossings w/o gaps (now 5)

## Performance

- **Emphasis on high signal efficiency**
  - Target signal efficiency = ~95% or above
- **No need for very high rate reduction to go from 1MHz to a few hundred kHz**
  - Target background rejection = ~5

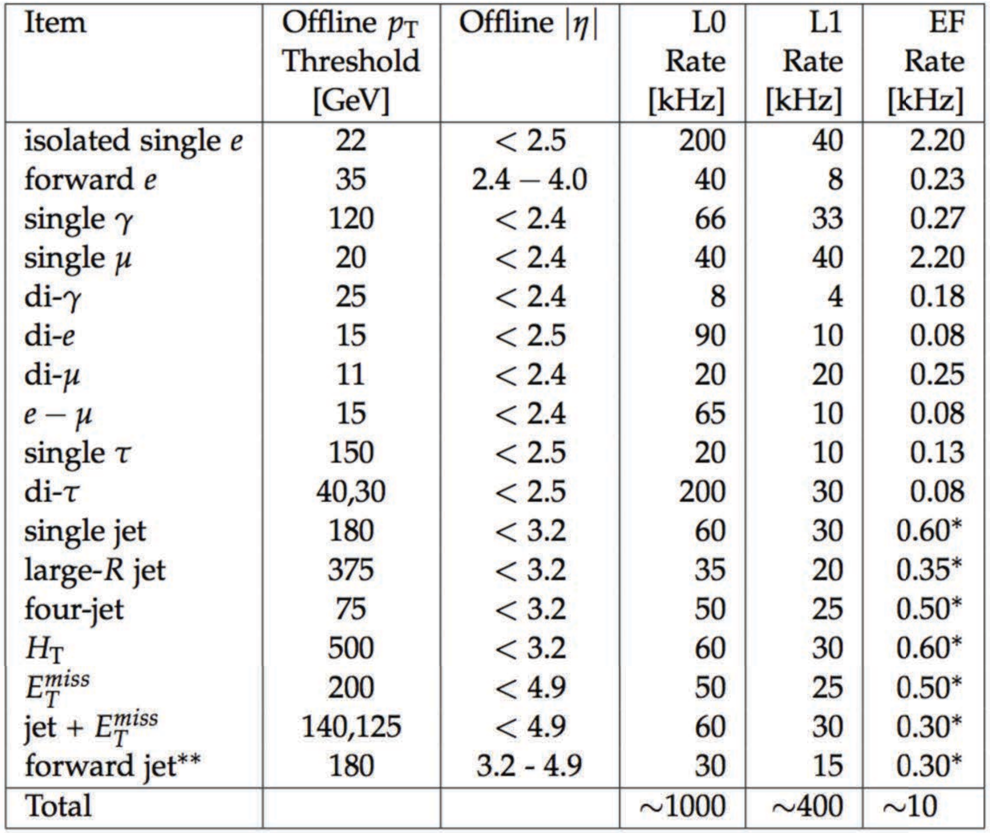
# ATLAS Trigger Strategy

Reduction in two hardware level system at Level-1 mainly using tracks from L1Track

Lower rate triggers for multiple low-pT leptons, taus, jets and missing transverse energy

- e.g. single electron 200 kHz Level-0, 40 kHz Level-1, 2.2 kHz output
- also improvements from individual cell information for calorimeter at Level-1

In single level system Level-0 rates feed directly into Event Filter



| Item | Offline $p_T$ Threshold [GeV] | Offline $\|\eta\|$ | L0 Rate [kHz] | L1 Rate [kHz] | EF Rate [kHz] |
|---|---|---|---|---|---|
| isolated single $e$ | 22 | $< 2.5$ | 200 | 40 | 2.20 |
| forward $e$ | 35 | $2.4 - 4.0$ | 40 | 8 | 0.23 |
| single $\gamma$ | 120 | $< 2.4$ | 66 | 33 | 0.27 |
| single $\mu$ | 20 | $< 2.4$ | 40 | 40 | 2.20 |
| di-$\gamma$ | 25 | $< 2.4$ | 8 | 4 | 0.18 |
| di-$e$ | 15 | $< 2.5$ | 90 | 10 | 0.08 |
| di-$\mu$ | 11 | $< 2.4$ | 20 | 20 | 0.25 |
| $e - \mu$ | 15 | $< 2.4$ | 65 | 10 | 0.08 |
| single $\tau$ | 150 | $< 2.5$ | 20 | 10 | 0.13 |
| di-$\tau$ | 40,30 | $< 2.5$ | 200 | 30 | 0.08 |
| single jet | 180 | $< 3.2$ | 60 | 30 | 0.60* |
| large-$R$ jet | 375 | $< 3.2$ | 35 | 20 | 0.35* |
| four-jet | 75 | $< 3.2$ | 50 | 25 | 0.50* |
| $H_T$ | 500 | $< 3.2$ | 60 | 30 | 0.60* |
| $E_T^{miss}$ | 200 | $< 4.9$ | 50 | 25 | 0.50* |
| jet + $E_T^{miss}$ | 140,125 | $< 4.9$ | 60 | 30 | 0.30* |
| forward jet** | 180 | 3.2 - 4.9 | 30 | 15 | 0.30* |
| Total | | | $\sim$1000 | $\sim$400 | $\sim$10 |

- Wade Fisher, MSU, CPAD16

# CMS HL-LHC Trigger Scenario

## L1 Accept rate up to 750 kHz

- Plan for L1A rate up to 500 kHz @ 140 PU and 750 kHz @ 200 PU
- Driven by keeping acceptance consistent with Run 1 and Phase 1 Upgrade
- Includes acceptance of consecutive 25 ns beam crossings
- Limited by pixel readout, impacts on DAQ readout, EVB, & HLT CPU

## Tracking Trigger

- Driven by keeping acceptance consistent with Run 1 and Phase 1 Upgrade
- Leptons: $P_T$ cut & isolation, Jets: Vertex
- Improves $E_T$ sums and enables Track MET

## New L1 Trigger (Calorimeter, Muon, Global) to incorporate Track Trigger

- Finer calorimeter cluster trigger, muon & calorimeter seeds for track match
- Also incorporate additional muon chambers for $|\eta| > 1.5$ (e.g. GEMs)

## Latency of 12.5 μsec

- Driven by Tracking Trigger and logic to incorporate it.
- Limit from complications for outer tracker readout

## HLT Output Rate up to 7.5 kHz

- Plan for 5 kHz @ 140 PU and 7.5 kHz @ 200 PU
- Limit from Computing (e.g. cost), no limit from DAQ
- Same reduction of L1 rate (~100) as present

# CMS HL-LHC L1 Trig. Components

## Calorimeter Trigger

- Process individual readout granularity cells for optimal matching to track trigger
- Data processed by input Layer 1 and then final Layer 2 providing the output. Similar to Phase 1 upgrade calorimeter trigger, essentially scaled to higher number of channels involved.

## Endcap Muon Trigger

- Covering |η| from 1.6 to 2.5: rebuilt to incorporate additional chambers in endcap and to provide input to the tracking correlator.

## Overlap & Barrel Muon Triggers

- Modifications of existing muon triggers covering the barrel and overlap regions to provide input to tracking correlator.

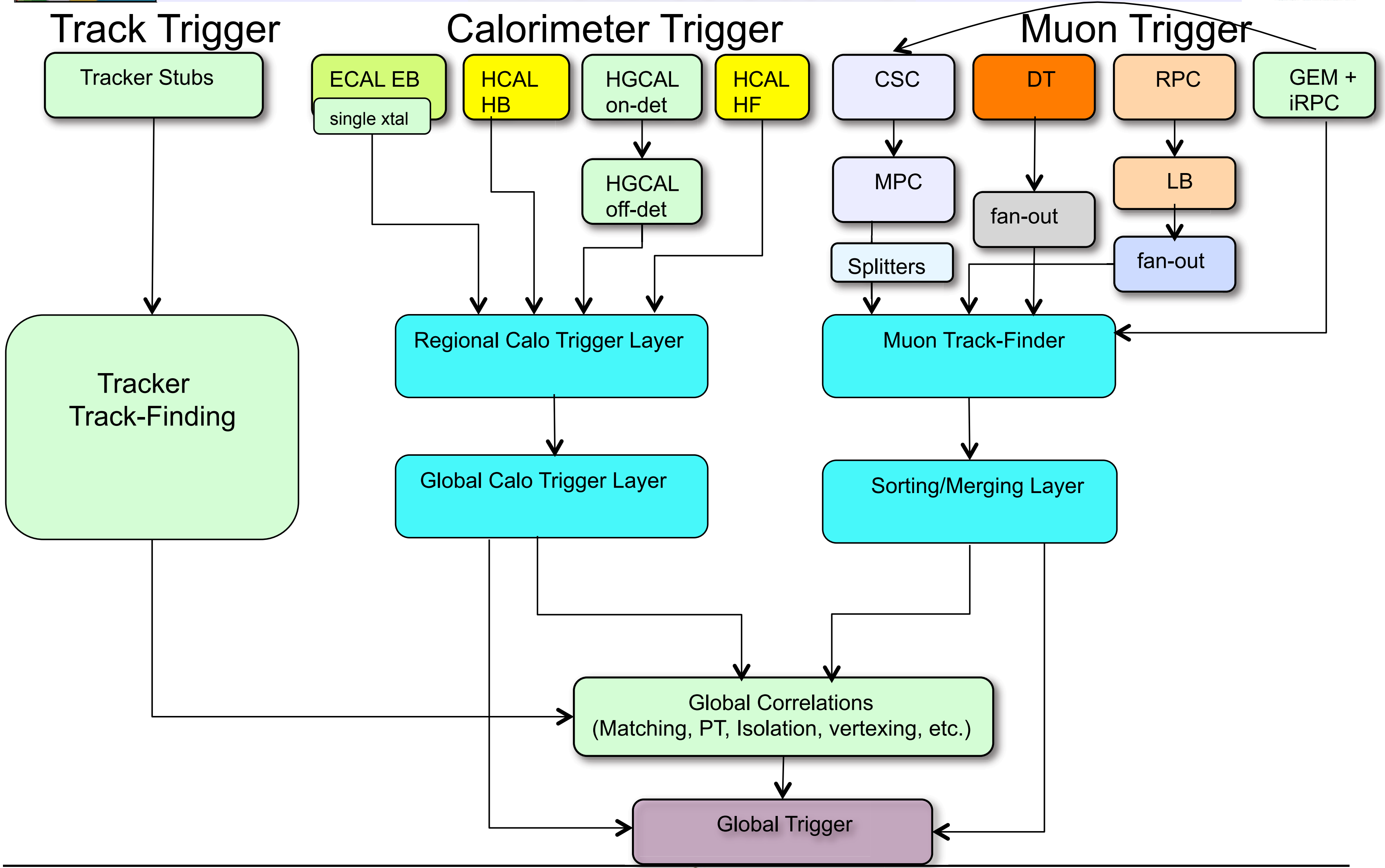
## Track Trigger Correlator

- L1 Track Finding is contained within the Tracker, with L1 Trigger performing correlation of produced track with muon and calorimeter trigger information.
- Logic is based on adaptation of Particle Flow ideas to L1 Trigger.
- Input trigger data is processed by an input Layer 1 and then final Layer 2 providing output to Global trigger

## Global Trigger

- Process more information than Phase 1 upgrade from many more objects with additional Tracking Trigger load. Design scales by ratio of data volume from Phase 1 upgrade.

# CMS HL-LHC L1 Trigger Architecture



Track Trigger

Calorimeter Trigger

Muon Trigger

Tracker Stubs

ECAL EB

single xtal

HCAL HB

HGCAL on-det

HCAL HF

CSC

DT

RPC

GEM + iRPC

HGCAL off-det

MPC

fan-out

LB

Splitters

fan-out

Tracker Track-Finding

Regional Calo Trigger Layer

Muon Track-Finder

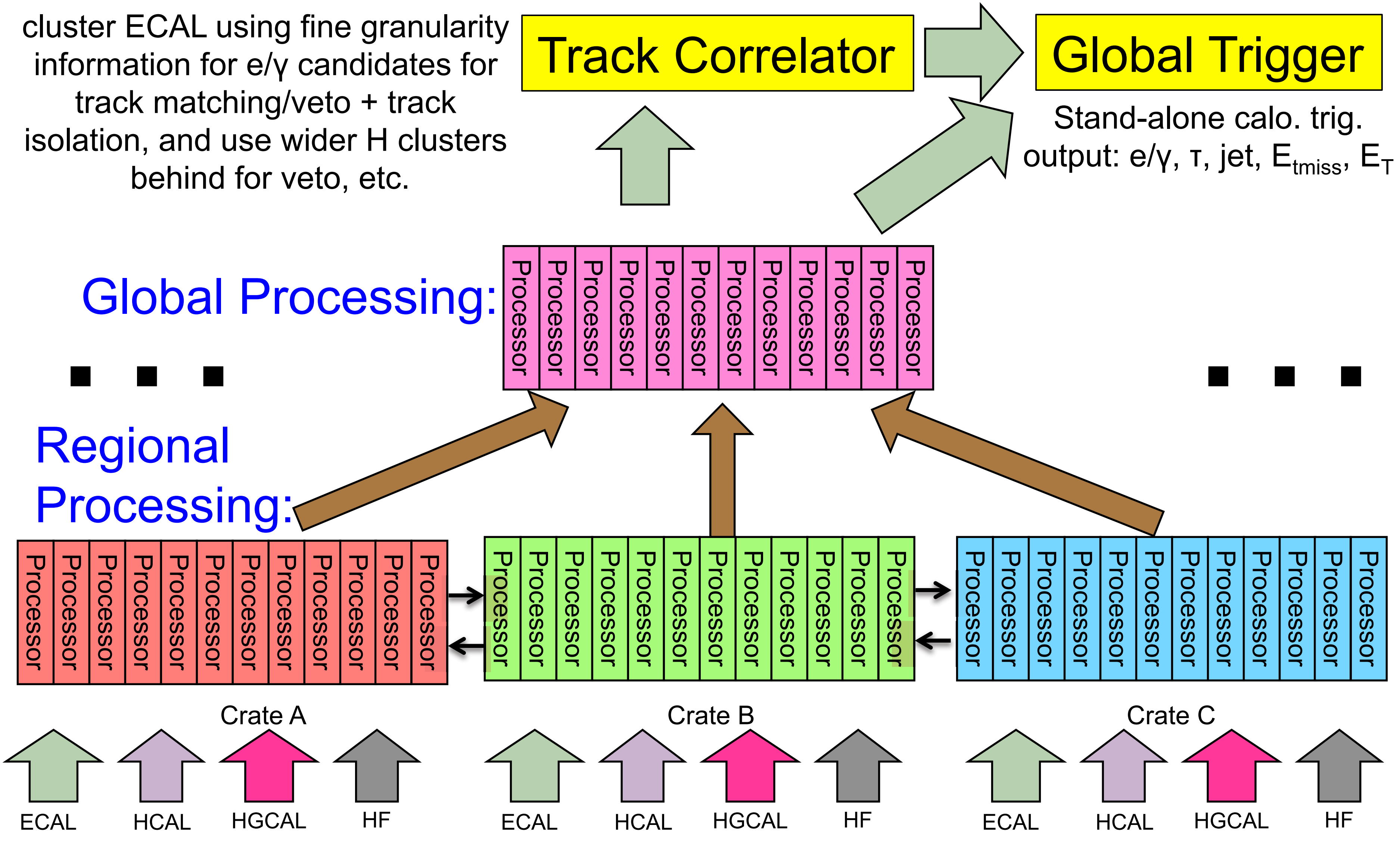
Global Calo Trigger Layer

Sorting/Merging Layer

Global Correlations
(Matching, PT, Isolation, vertexing, etc.)

Global Trigger

# Model for HL-LHC L1 Cal. Trigger



cluster ECAL using fine granularity information for e/γ candidates for track matching/veto + track isolation, and use wider H clusters behind for veto, etc.

Track Correlator

Global Trigger

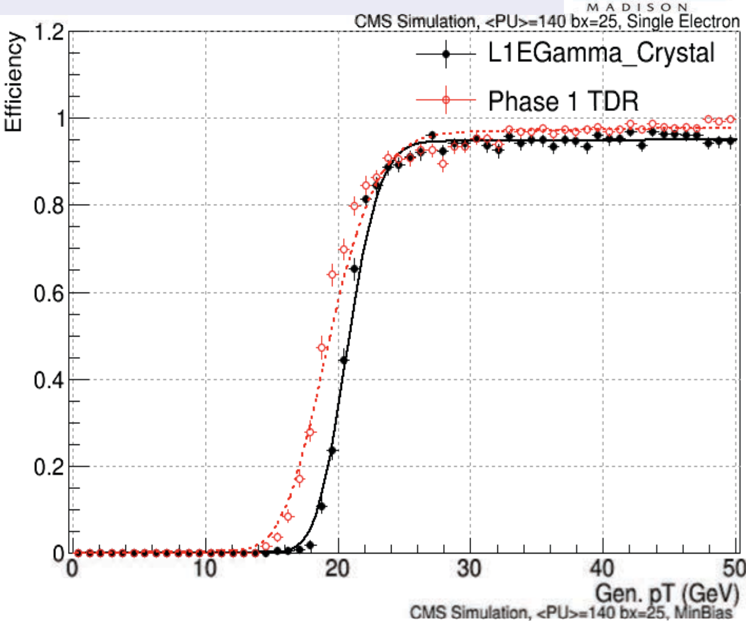
Stand-alone calo. trig. output: e/γ, τ, jet, $E_{tmiss}$, $E_T$

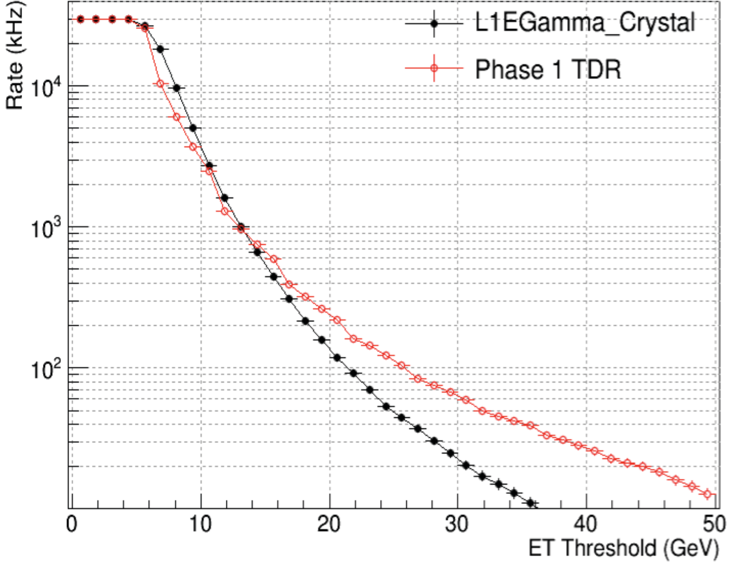
Global Processing:

Regional Processing:

# L1 Calo Trigger HL-LHC

- ECAL Barrel: process individual crystal energies instead of present 5x5 crystal towers
  - $\eta \times \phi$ = .0875×.0875 → .0175×.0175
- HCAL Barrel: keeps .0875×.0875
- HGCAL: produce energy information on ~ same scale (.0175×.0175) as Barrel ECAL.
- Improvement in stand-alone electron trigger efficiency + rate example from Barrel →
- Also provides higher resolution for matching to tracks: ΔR < 0.006
  - See later slide



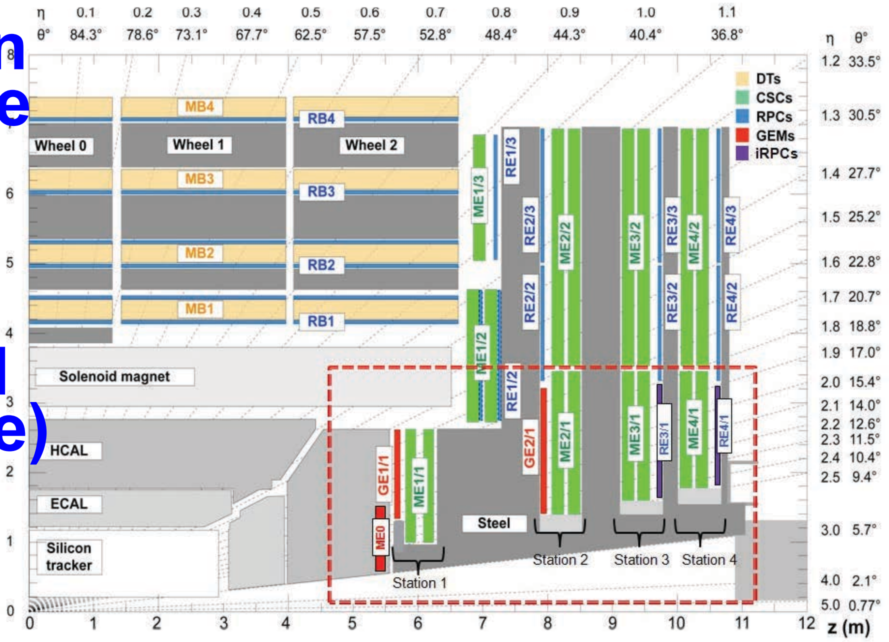


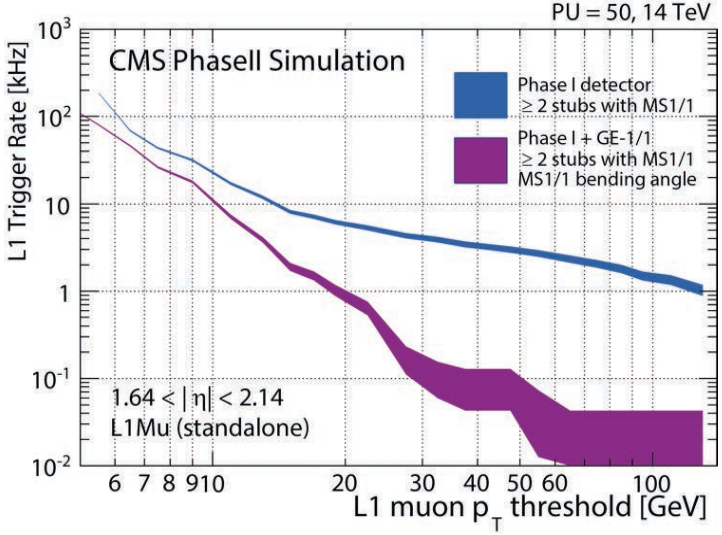
# HL-LHC Muon Trigger

**New detectors in forward region to add redundancy and enhance trigger**

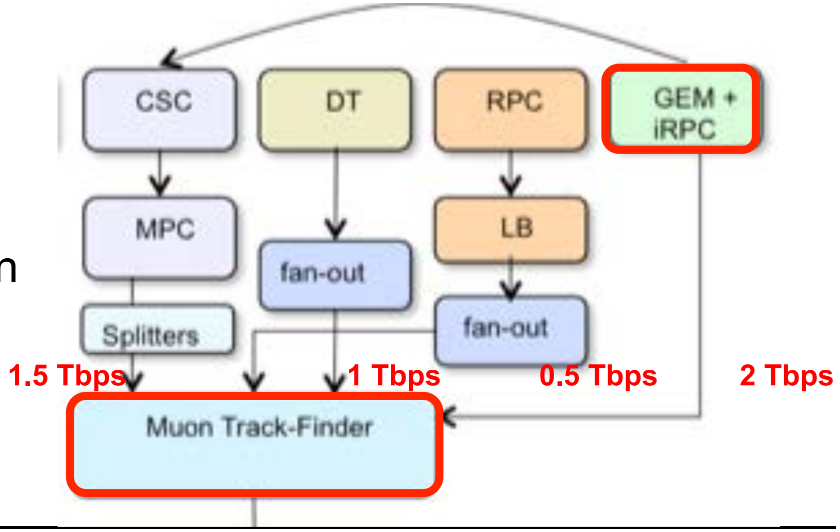
- GEM in ME0, GE1/1, GE2/1
- Improved RPC in outer layers

**Additional inputs and improved angular information (bend angle) for track-finding for better efficiency and rate rejection in stand-alone muon trigger.**





Rate only in GE1/1 region



CSC

DT

RPC

GEM + iRPC

MPC

fan-out

LB

fan-out

Splitters

1.5 Tbps

1 Tbps

0.5 Tbps

2 Tbps

Muon Track-Finder

# HL-LHC L1 Tracking Trigger

## Require:

- **Highest possible efficiency over all η for isolated high $P_T$ tracks**
- **Good efficiency for tracks in jets for vertex identification**
- **$P_T$ > 2-3 GeV (small difference within this range)**
  - Expect ~ 115 charged tracks with $P_T > 2$ GeV at PU = 140
  - Design for 350 tracks per bunch crossing
- **Z vertex position resolution ~ 1 mm**

## Use:

- **Charged Lepton ID**
- **Improve $P_T$ resolution of muons**
- **Determine isolation of leptons and photons**
- **Determine vertex of charged leptons and jet objects**
- **Determine primary vertex and MET from L1 Tracks from this vertex**

## Pixel Trigger Option

- **Under consideration for now, but need a strong physics case**
- **Challenging to meet 12.5 μsec latency**

# HL-LHC L1 Track Trigger Use

## Reduces Leptonic Trigger Rate

- Validate calorimeter or muon trigger object, e.g. discriminating electrons from hadronic ($\pi^0 \rightarrow \gamma\gamma$) backgrounds in jets
- Addition of precise tracks to improve precision on $p_T$ measurement, sharpening thresholds in muon trigger
- Degree of isolation of $e$, $\gamma$, $\mu$ or $\tau$ candidate
- Requires calorimeter trigger trigger at the finest granularity to reduce electron trigger rate

## Other Triggers

- Primary z-vertex location within 30 cm luminous region derived from projecting tracks found in trigger layers,
- Provide discrimination against pileup events in multiple object triggers, e.g. in lepton plus jet triggers.

# L1 Track Trigger Design

## Self-seeded Level-1 Track Trigger

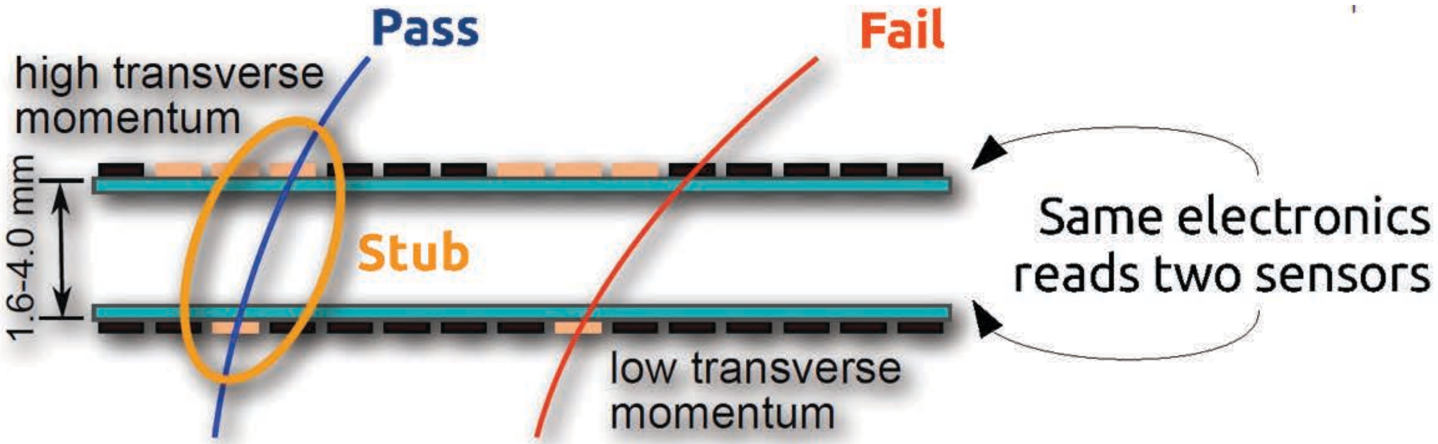
- Relies on local $p_T$ reconstruction
- Reconstructs tracks with $p_T > 2$ GeV
- Identifies z-vertex location with ~ 1 mm precision
  - Similar to average vertex separation at PU ~ 140.

## $p_T$ modules provide $p_T$ discrimination through hit correlations between closely spaced sensors

- Correlate pairs of clusters consistent w/track > 2 GeV
- In minimum bias events, ~ 95% of tracks have $p_T <$ 2GeV

Example: CMS Track Trigger design finds stubs with $p_T \gtrsim 2$:

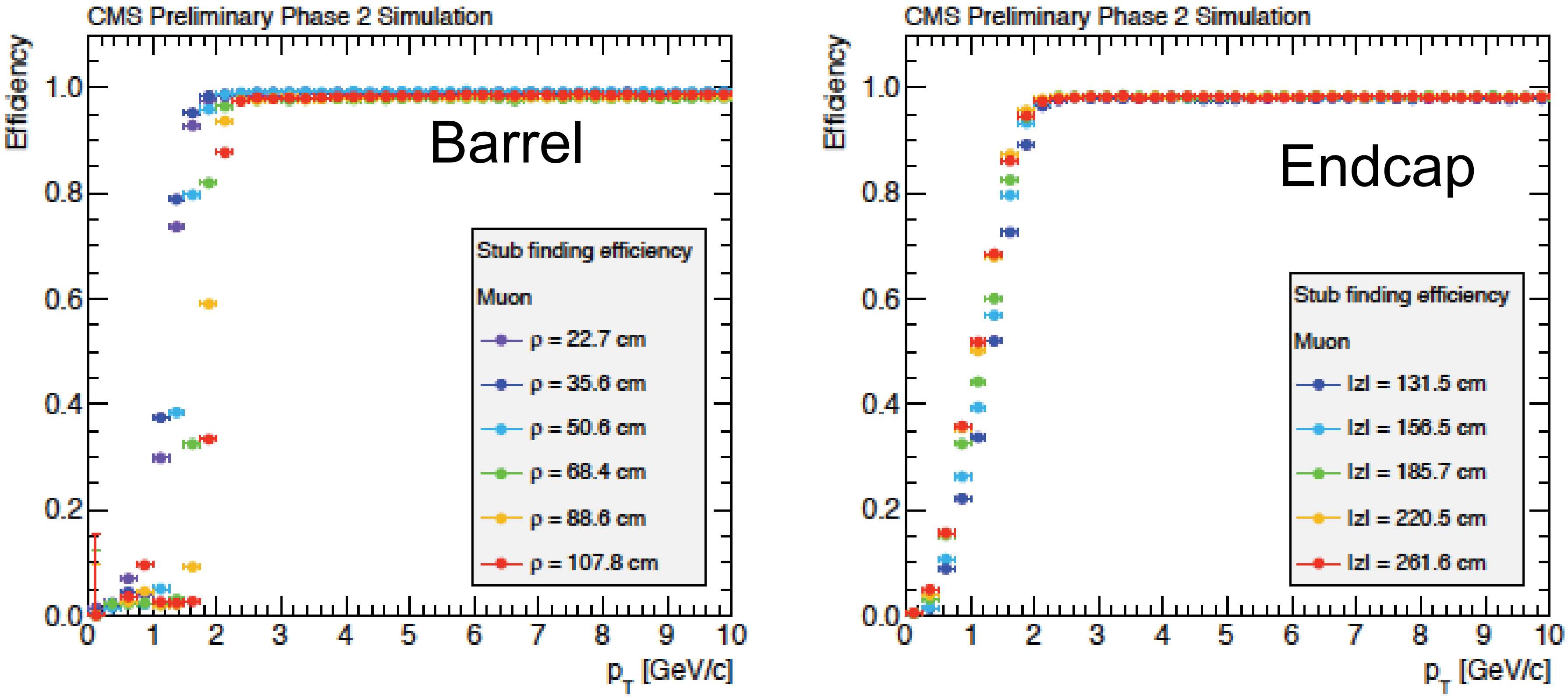
*Thanks to CMS 3.8 T magnetic field!*



# Track Stub Finding

**Push" design: all stubs forwarded to Track-finder**

**Stub efficiency vs. $p_T$ for various layers and disks:**



1 BX = 25ns

# Track-Finding

“Push” design, not region of interest

- Input: Expect ~10K stubs/BX @ PU~140, of which 5-10% belong to tracks with $P_T$>2 GeV
- Output: ~100 bits/track → several Tbps to track correlators
- Latency: ~5 μs allocated

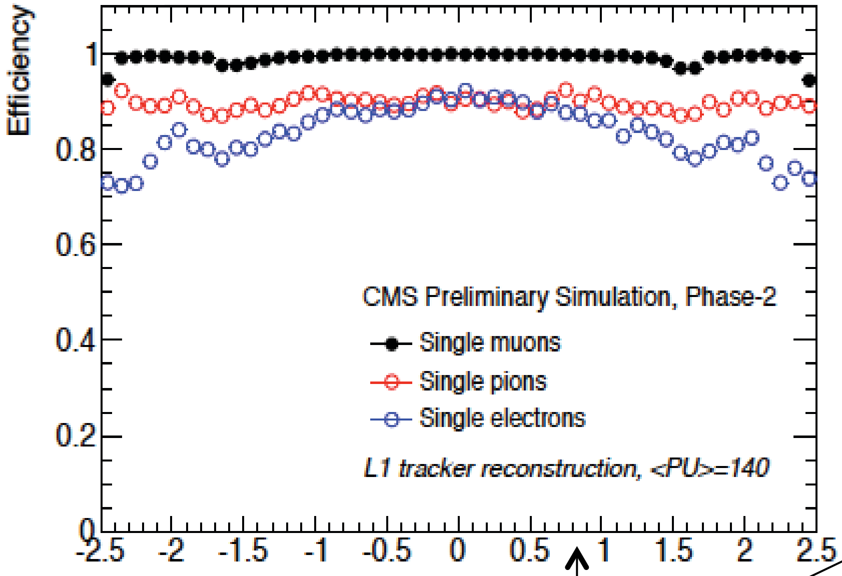
Multiple approaches under consideration to find tracks, examples:

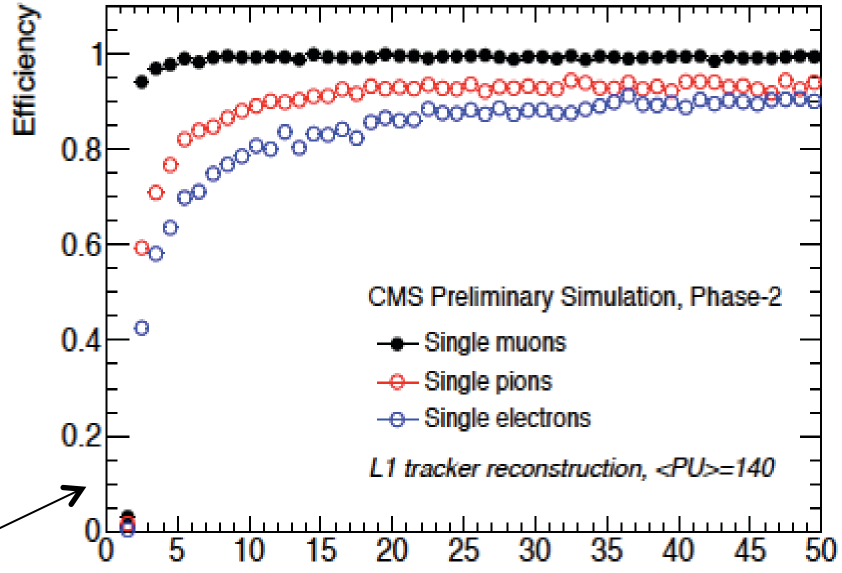
- Pattern-based: Track patterns stored in Associative Memory chips
  - Target implementation in custom ASICs (Associative Memories, e.g. VIPRAM) to store large number of patterns (~100M overall)
- “Tracklet” approach: Track building from stubs with pair-wise layer extrapolations
  - Target implementation in FPGAs
- More details in Tracking Parallel Session

Generally implemented with time-multiplexing of the input data (round-robin of event data to processors)

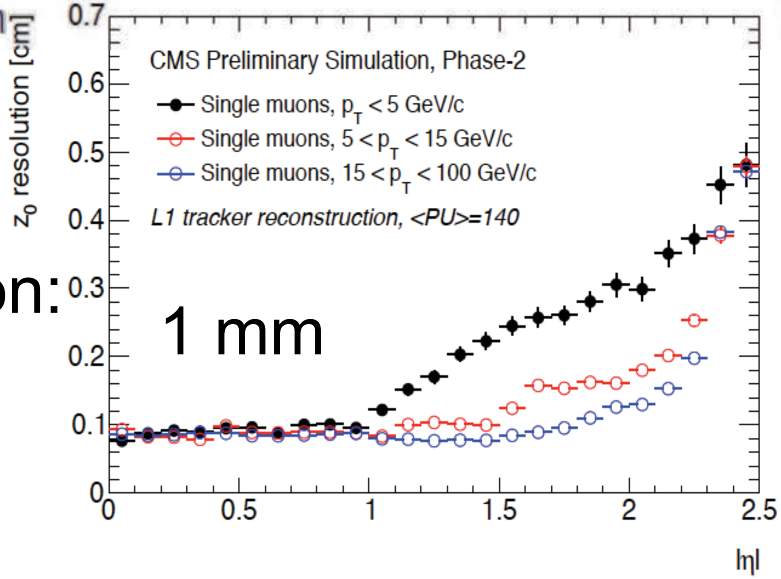
All followed by a (generally FPGA-based) track-fitting stage to extract track parameters

# Track Trigger Performance



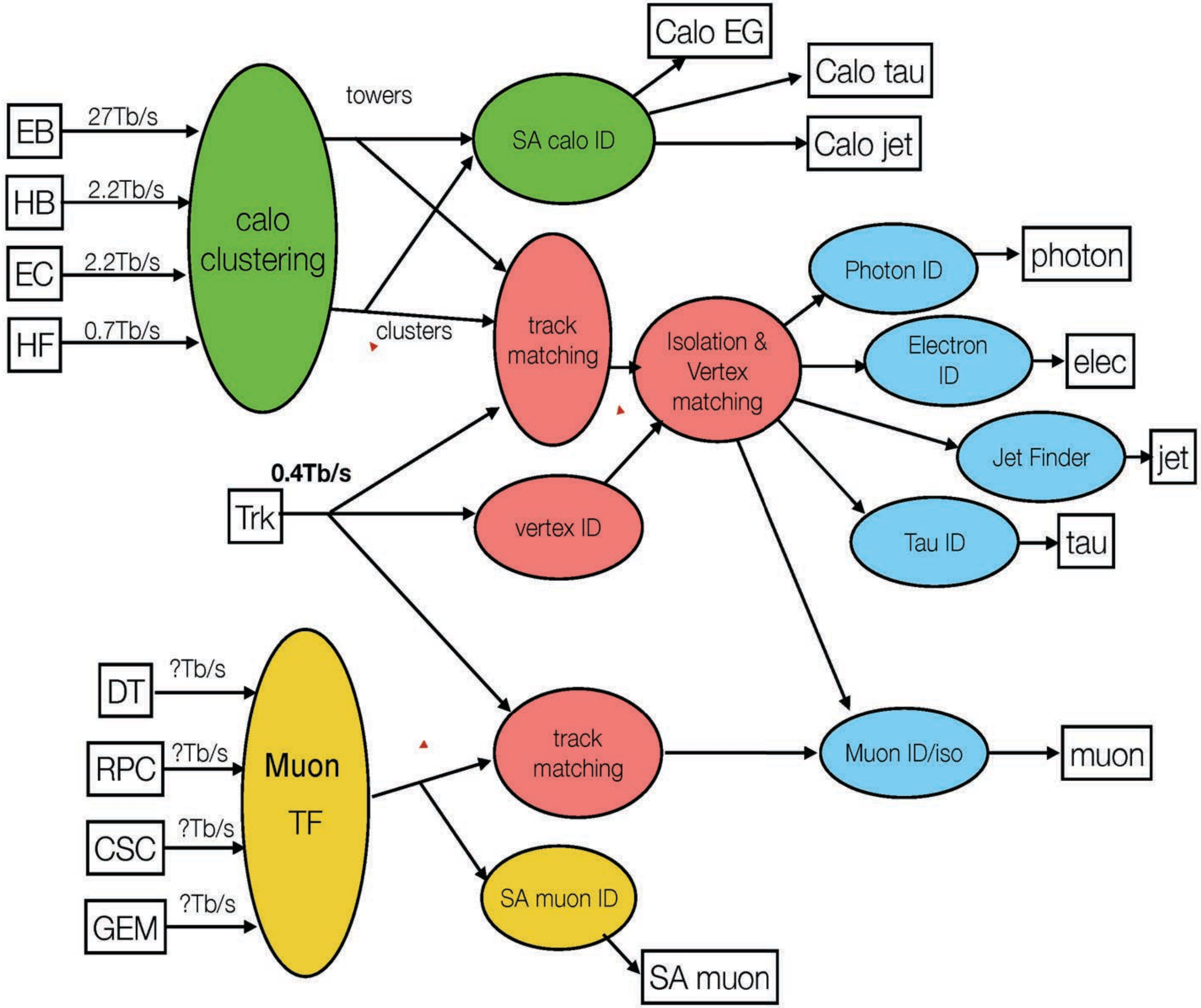


Efficiency curves vs. η & $p_T$ for PU=140



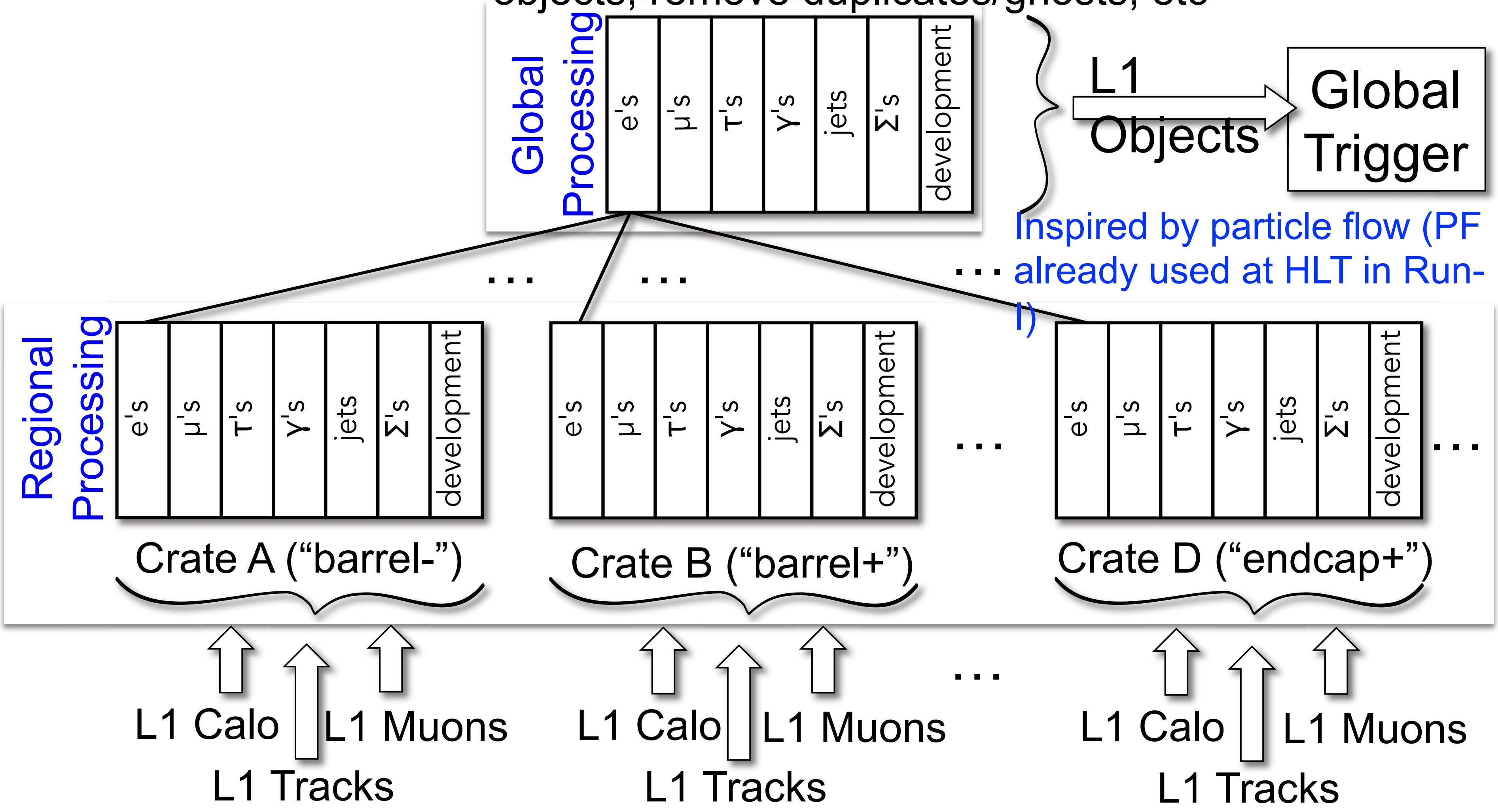
$Z_0$ resolution: 1 mm

# Correlator Conceptual Design



# Model for L1 Correlator Trigger

Calculate global sums (MET, SET, etc), sort objects, remove duplicates/ghosts, etc



Global Processing

e's | μ's | τ's | γ's | jets | Σ's | development

L1 Objects → Global Trigger

Inspired by particle flow (PF already used at HLT in Run-I)

Regional Processing

e's | μ's | τ's | γ's | jets | Σ's | development

Crate A (“barrel-”)

Crate B (“barrel+”)

Crate D (“endcap+”)

…

L1 Calo

L1 Tracks

L1 Muons

# CMS HL-LHC L1 Trigger Latency
## (preliminary estimate)

- **Estimate L1 Track Trigger result available 5 μs after interaction occurred.**
  - ➢ **L1 Track trigger is a "push" system, not region of interest**
- **Regional processing (Correlation Logic) involves (+2.5 μs ⇒ 7.5 μs) :**
  - ➢ **Preprocessing + distribution of L1 Cal, Mu, Track Trigger Primitives – 0.5 μs**
  - ➢ **Using tracks to find primary vertex – 0.5 μs**
  - ➢ **Associating tracks with the primary vertex – 0.5 μs**

    **In parallel with**

    ↕
  - ➢ **Associating tracks with calorimeter objects**
  - ➢ **Associating tracks with and fitting tracks with muon tracks**

    **0.5 μs**
  - ➢ **Calculating track-correlated L1-objects + their characteristics – 1.0 μs**
  - ➢ **Using tracks to calculate isolation of cal. and muon objects – 0.5 μs.**

    **2.0 μs**
- **Global processing involves +(1 μs ⇒ 8.5 μs):**
  - ➢ **Global sums, kinematic calculations, correlations between trigger objects, trigger decision logic (incl. trigger rules)**
- **Propagation back to detector front ends (+1 μs ⇒ 9.5 μs)**
  - ➢ **38 bx in present system (0.95 μs)**
- **Safety Factor of 30% ⇒ 12.5 μs**
  - ➢ **NB: Original Trig. TDR Latency: 127 bx, Run 1: 157 bx (+ 0.8 μs), req'd: 168 bx**
    - Run 2 Latency now up to 164 bx.
- **Set 12.5 μs as minimum design latency**
  - ➢ **Once 6 μs exceeded, 12.5 μs is the next point where consequences**

# L1 Menu Studies

**Goal: maintain overall physics performance + acceptance of L1 Trigger Upgrade TDR (e.g. thresholds near the end of run 1)**

- **Study a sample menu using ~70% of bandwidth**
  - Not included: any prescaled trigger (minbias, triggers with lower thresholds), triggers involving forward calorimeter, MET/MHT, three lepton triggers, other acceptance, diagnostic and calibration triggers.
- **Compensate by increasing found total rate by 30%**

**Benchmark conditions: 140 PU**

- **Use Minbias Sample with PU = 140**
- **Assume bunch spacing at 25 ns: L ~ 5.6 E34**

**Use Tracking Trigger**

- **Assume “perfect” performance**

**High PU Conditions: 200 PU as a check**

- **Use unofficial production of 200 PU events**
- **Assume bunch spacing at 25 ns: L ~ 8 E34**

**Uncertainties: Need Safety factor of at least 1.5**

- **Simulation uncertainty**
- **Readout underachievement**
- **Realistic Tracking Trigger performance**

# L1 Trigger Menu at 140 PU with L1 Tracking Trigger

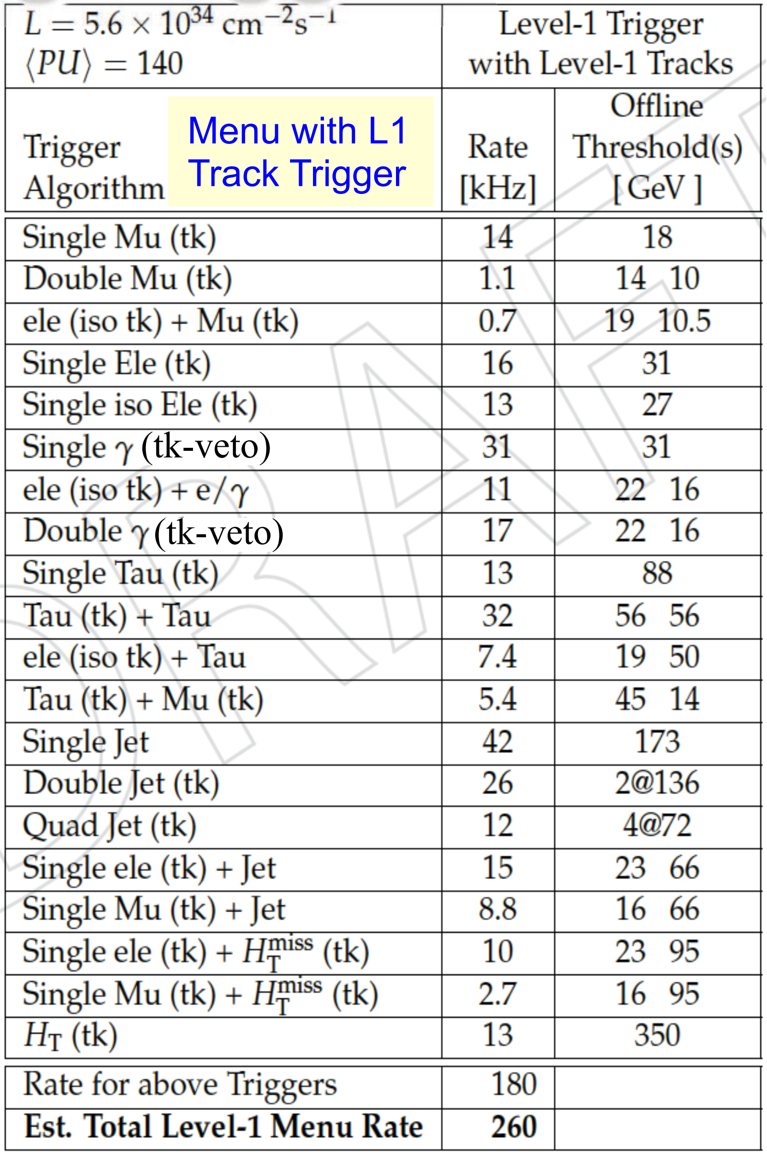
## Menu w/o Tracking Trigger produces a total rate of 1.5 MHz at 140 PU

- ➢ Tracking trigger provides factor of 5.5 reduction to 260 kHz →
- ➢ w/ 1.5 safety factor: 390 kHz
- ➢ Use 500 kHz as benchmark

## Menu w/Tracking Trigger produces total rate of 500 kHz at 200 PU

- ➢ w/ 1.5 safety factor: 750 kHz
- ➢ w/o track trig., approach 4 MHz!
  - (6 MHz w/safety!)

Warning: this menu is just a sample table only for evaluating bandwidth



Menu with L1 Track Trigger

| $L = 5.6 \times 10^{34}$ cm$^{-2}$s$^{-1}$ $\langle PU \rangle = 140$ | Level-1 Trigger with Level-1 Tracks | |
|---|---|---|
| Trigger Algorithm | Rate [kHz] | Offline Threshold(s) [ GeV ] |
| Single Mu (tk) | 14 | 18 |
| Double Mu (tk) | 1.1 | 14 10 |
| ele (iso tk) + Mu (tk) | 0.7 | 19 10.5 |
| Single Ele (tk) | 16 | 31 |
| Single iso Ele (tk) | 13 | 27 |
| Single $\gamma$ (tk-veto) | 31 | 31 |
| ele (iso tk) + e/$\gamma$ | 11 | 22 16 |
| Double $\gamma$ (tk-veto) | 17 | 22 16 |
| Single Tau (tk) | 13 | 88 |
| Tau (tk) + Tau | 32 | 56 56 |
| ele (iso tk) + Tau | 7.4 | 19 50 |
| Tau (tk) + Mu (tk) | 5.4 | 45 14 |
| Single Jet | 42 | 173 |
| Double Jet (tk) | 26 | 2@136 |
| Quad Jet (tk) | 12 | 4@72 |
| Single ele (tk) + Jet | 15 | 23 66 |
| Single Mu (tk) + Jet | 8.8 | 16 66 |
| Single ele (tk) + $H_T^{miss}$ (tk) | 10 | 23 95 |
| Single Mu (tk) + $H_T^{miss}$ (tk) | 2.7 | 16 95 |
| $H_T$ (tk) | 13 | 350 |
| Rate for above Triggers | 180 | |
| **Est. Total Level-1 Menu Rate** | **260** | |

DRAFT

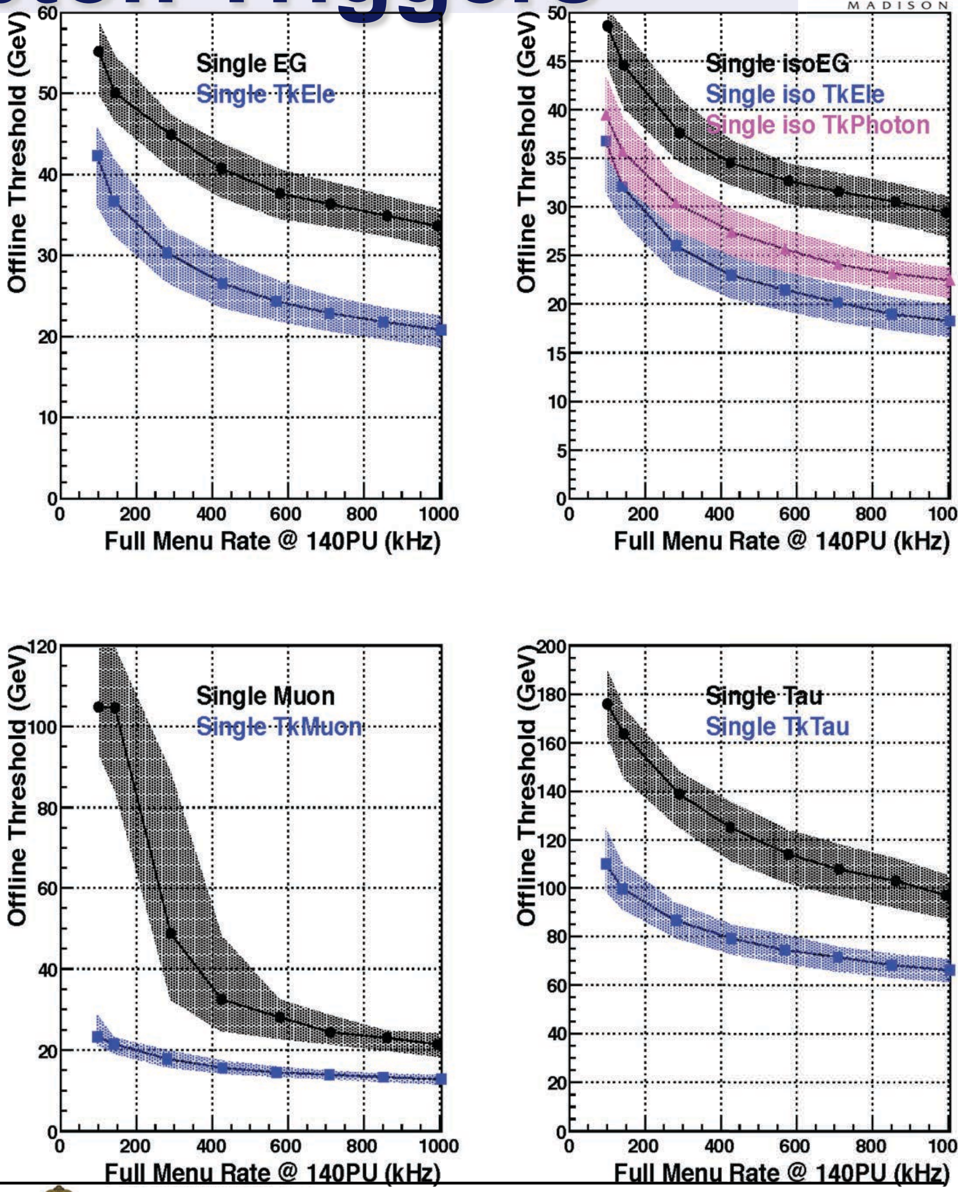
# L1 Thresholds vs. Bandwidth: Single Lepton Triggers

Allocate initial BW for each algorithm in full menu according to BW fractions used in sample menus with and without L1 Tracking

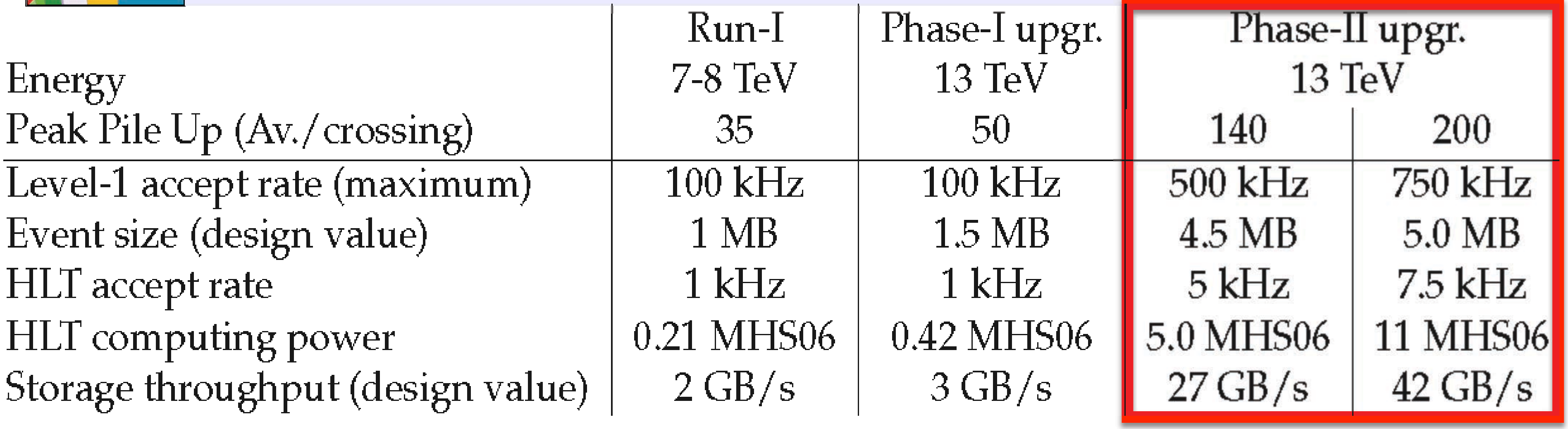
- ➢Determine trigger thresholds necessary to fit assigned rate
- ➢Repeat for a range of total bandwidths

Plots show rates for full menus with and without L1 Tracking @ 140 PU

- ➢No safety factors applied



# CMS HL-LHC HLT & DAQ



| | Run-I | Phase-I upgr. | Phase-II upgr. | |
|---|---|---|---|---|
| Energy | 7-8 TeV | 13 TeV | 13 TeV | |
| Peak Pile Up (Av./crossing) | 35 | 50 | 140 | 200 |
| Level-1 accept rate (maximum) | 100 kHz | 100 kHz | 500 kHz | 750 kHz |
| Event size (design value) | 1 MB | 1.5 MB | 4.5 MB | 5.0 MB |
| HLT accept rate | 1 kHz | 1 kHz | 5 kHz | 7.5 kHz |
| HLT computing power | 0.21 MHS06 | 0.42 MHS06 | 5.0 MHS06 | 11 MHS06 |
| Storage throughput (design value) | 2 GB/s | 3 GB/s | 27 GB/s | 42 GB/s |

**HLT: x24/51 at 500/750 kHz+140/200 PU increased processing power v. Run 1**

- **x 5/7.5 increase in L1 input rate (500 kHz @ PU=140/750 kHz @ PU=200)**
- **x 4/5.7 for increased complexity due to higher PU, x 1.5 for higher energy**
  - Estimated from observed CPU dependence on PU and MC studies
  - x 0.8 mitigation due to prompt access to tracking info. from L1 Track Trigger at HLT
- **Affordable in 2024 assuming extrapolation of ~1 CHF/HS06 in 2024**

**DAQ: For 5 MB events at 750 kHz, total required throughput is 30 Tbps.**

- **Similar event builder and storage as present 800 links x 100 Gbps with 30% eff. will provide 30 Tbps event building throughput**
- **InfiniBand switch today provides 32 Tbps unidirectional bandwidth. Costs of this infrastructure are likely below those of existing system.**

# HL-LHC Trigger R&D Goals

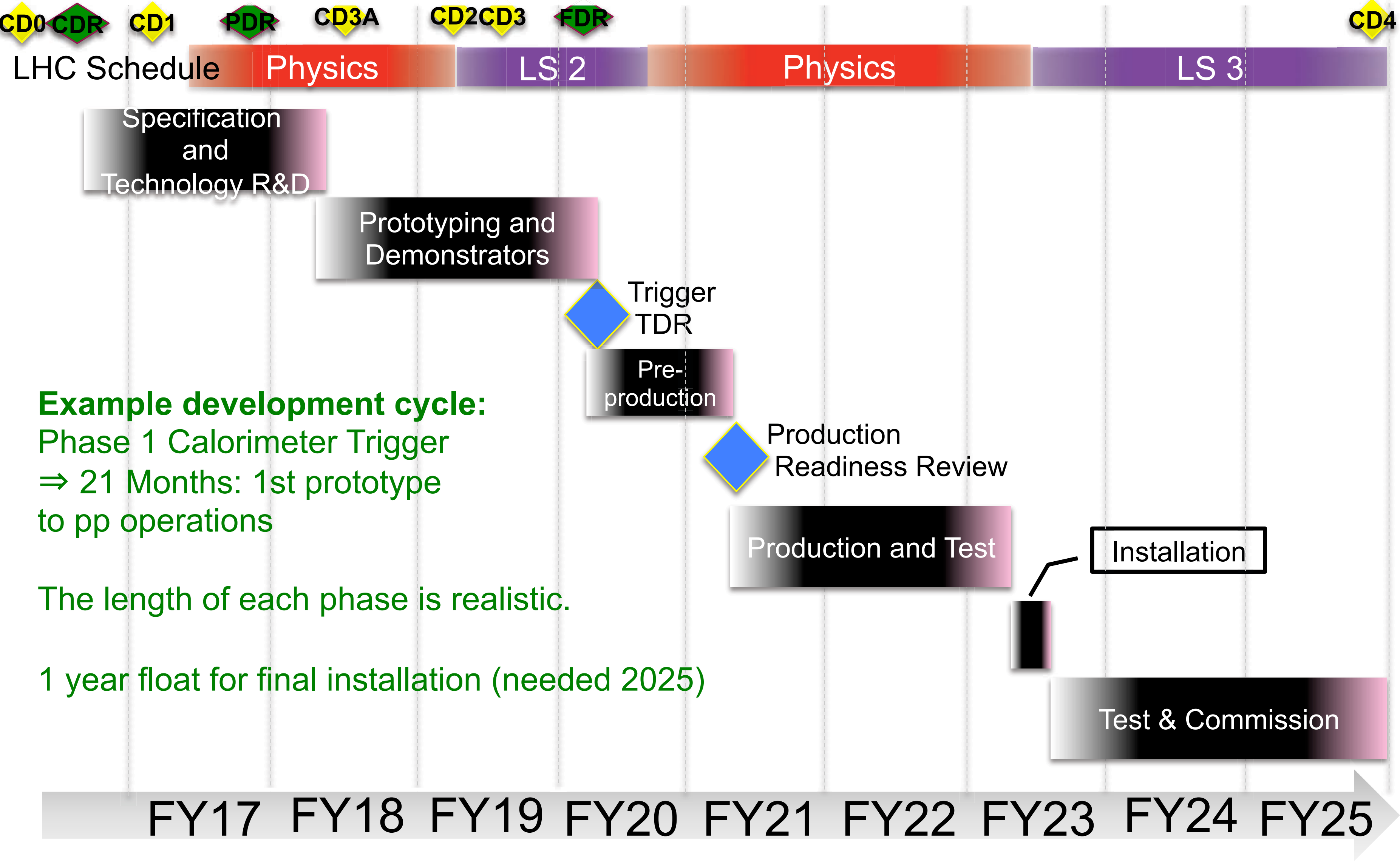
## Challenges:

- **Large increase in trigger input data**
  - e.g. present EB 5x5 trigger towers vs. full xtal granularity – x25 increase, also new HGCal data volume w/ similar granularity
- **Large increase in processing complexity**
  - Tracking information
  - Fine grain calorimeter information
  - Fitting Muon and Tracking data together
  - More complex objects, conditions and algorithms

## Phases:

- **Establish algorithms, techniques and feasibility**
- **Decide on a hardware framework**
- **Build prototypes to test functionality**
- **Build individual parts of the system**
- **Construct demonstrators**
- **Connect to detector prototypes to validate designs**

# Schedule and Milestones



**Example development cycle:**

Phase 1 Calorimeter Trigger

⇒ 21 Months: 1st prototype to pp operations

The length of each phase is realistic.

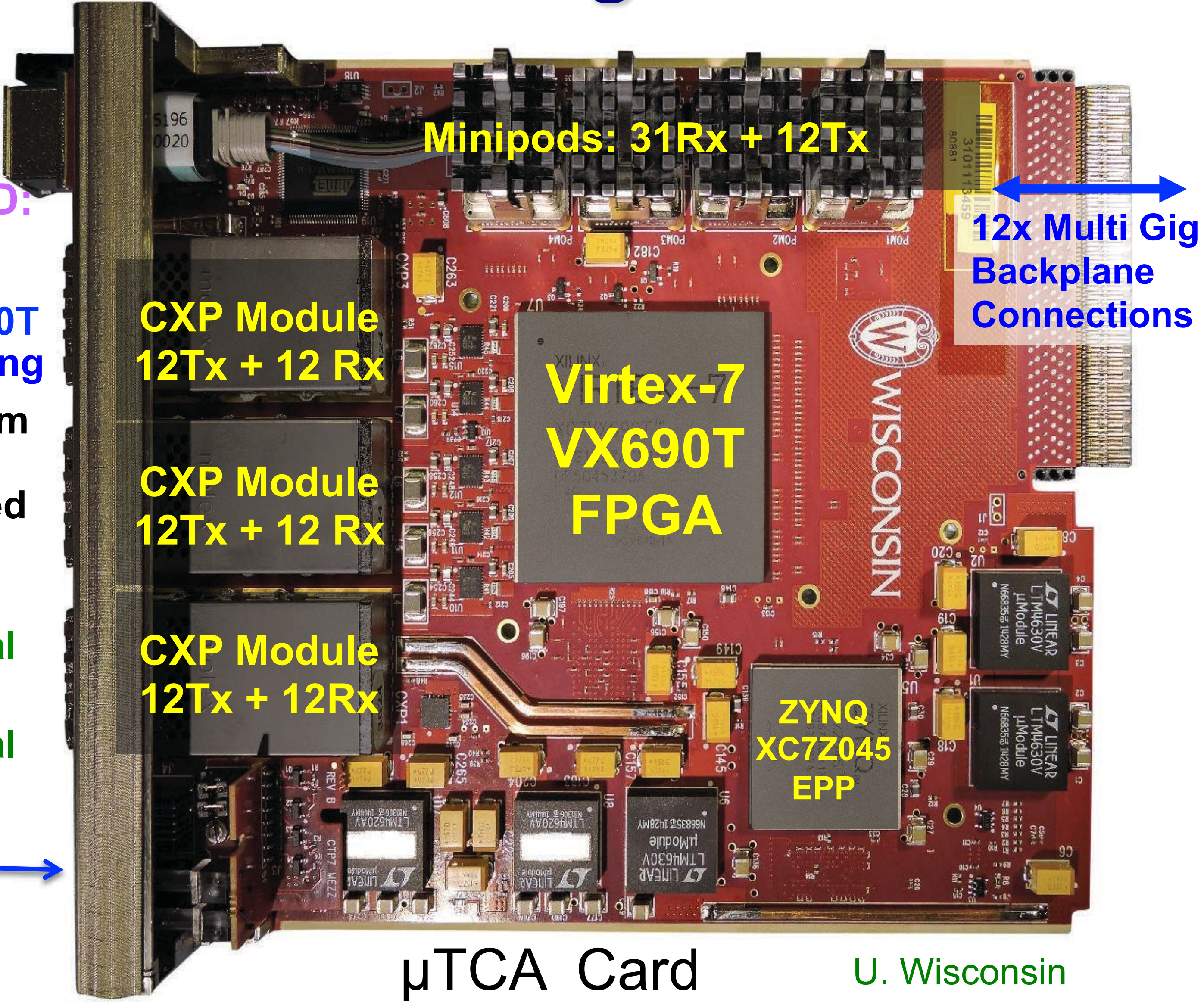
1 year float for final installation (needed 2025)

# Example Starting Point: Phase 1 Cal. Trig. Card

In use for Tracklet Trigger, GEM, EB, Correl, Calo, Muon Trigger HL-LHC R&D:

**CTP7:**

- Xilinx Virtex-7 690T for data processing
- ZYNQ `045 System -on-Chip (SoC) Device (embedded Linux control platform)
- 67 10Gbps optical Input links
- 48 10Gbps optical Output links



µTCA Card

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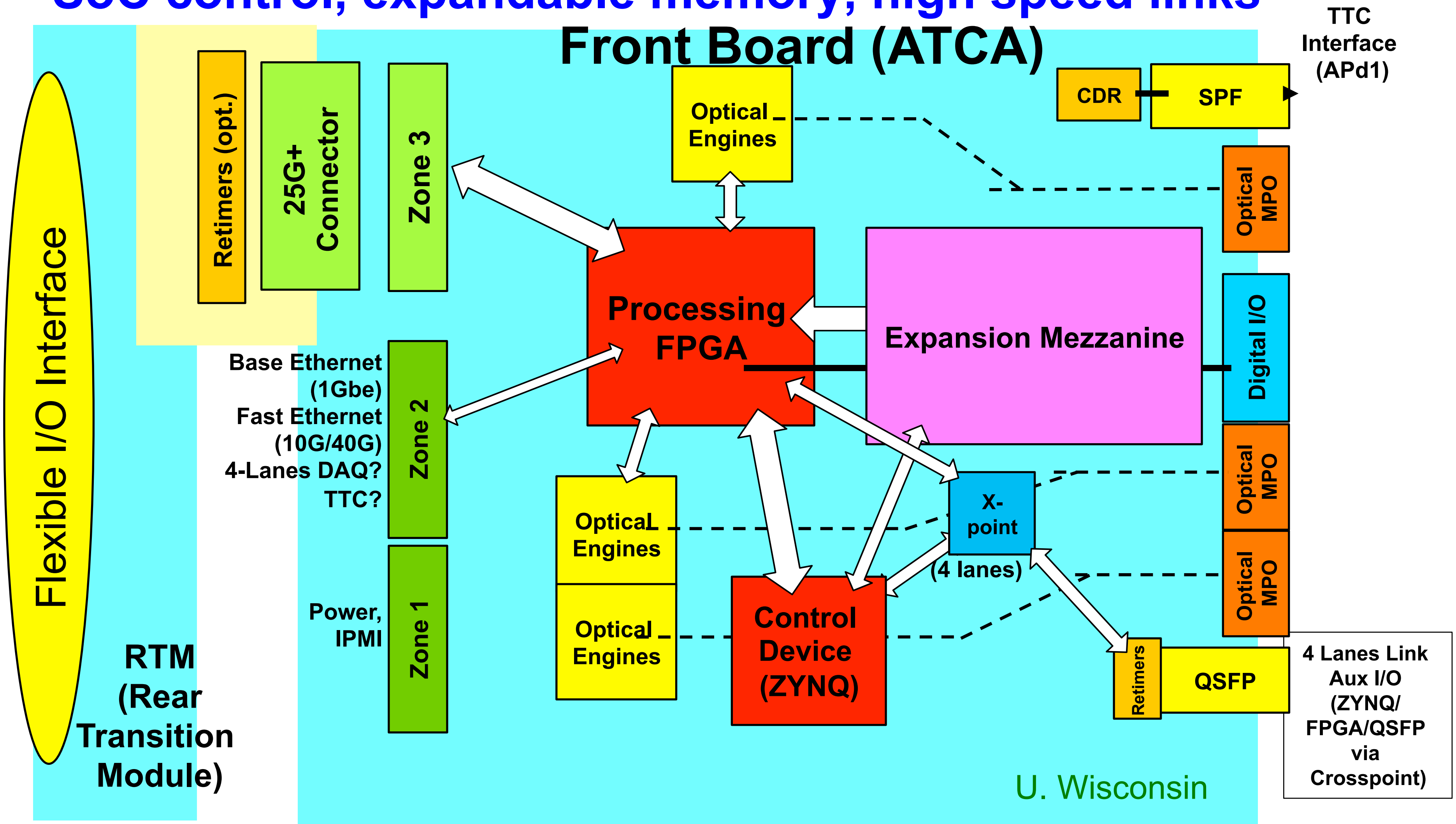
# Example: Hardware Framework R&D: Advanced Processor (APx) Concept

## APx Top level diagram: Ultrascale+ processing ZYNQ SoC control, expandable memory, high speed links



Front Board (ATCA)

Flexible I/O Interface

Retimers (opt.)

25G+ Connector

Zone 3

Zone 2

Zone 1

Base Ethernet (1Gbe)
Fast Ethernet (10G/40G)
4-Lanes DAQ?
TTC?

Power, IPMI

RTM (Rear Transition Module)

Optical Engines

Processing FPGA

Expansion Mezzanine

Optical Engines

Optical Engines

Control Device (ZYNQ)

X-point

(4 lanes)

CDR

SPF

TTC Interface (APd1)

Optical MPO

Digital I/O

Optical MPO

Optical MPO

Retimers

QSFP

4 Lanes Link Aux I/O (ZYNQ/ FPGA/QSFP via Crosspoint)

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# HL-LHC Trigger Technologies (in use/under test with CTP7)

## Embedded Linux

- Functional Linux system (network, file system, shell)
- Low latency access point tightly integrated with workhorse FPGA
- Basic card level infrastructure with very little new code—Ethernet, I2C, USART, GPIO drivers, ssh, file system, etc.—all standard
- Paid for itself in time saved in the first project cycle
  - First CTP7 proto. power-up to integrated operation in CMS pp runs in 21 months

## AXI Architecture

- Industry standard on-chip interconnection scheme for FPGAs
- Straightforward to implement AXI interfaces for registers and memory
- AXI infrastructure bridged into the Virtex-7 ("Chip2Chip" core), a single integrated address space for both devices
- 95% of CTP7 generic infrastructure from ZYNQ hard cores and Library IP catalog, no custom HDL needed—it's in the tools
- Improved status and access to advanced applications
  - Real-time link eye-diagrams for all channels while taking data available online!

## XVC – Embedded Linux Xilinx Virtual Cable (e.g. JTAG)

- Debug Card at P5 via TCP/IP just as if on the bench in the lab

# HL-LHC R&D Technology Examples

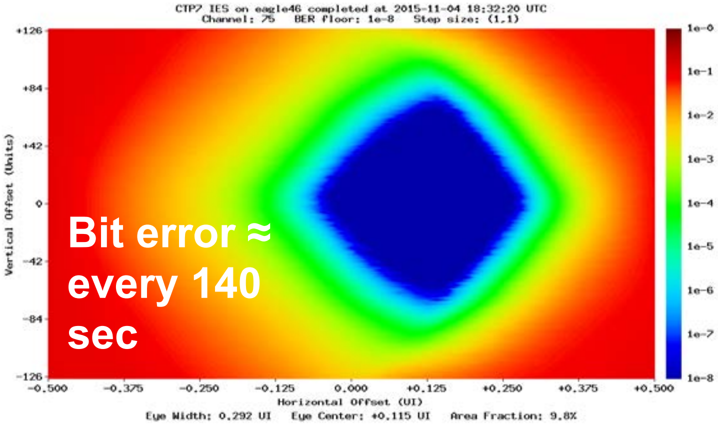
## Link monitoring/tuning using embedded Linux (ZYNQ):

**Monitor individual link performance by running continuous eye-scans while taking data.**

- ➢ Used to predict BER and proactively detect weak links before data transmission errors appear – manage large #'s of links

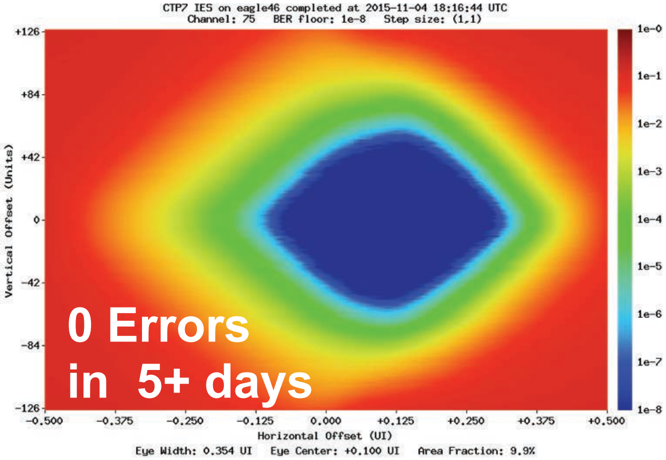
**Automatically and quickly tune parameters to optimize link performance while link is operating**

- ➢ Allows use of higher bandwidth links and moving boards while minimizing performance differences



**Bit error ≈ every 140 sec**

CTP7 using DFE* program on ZYNQ ➔

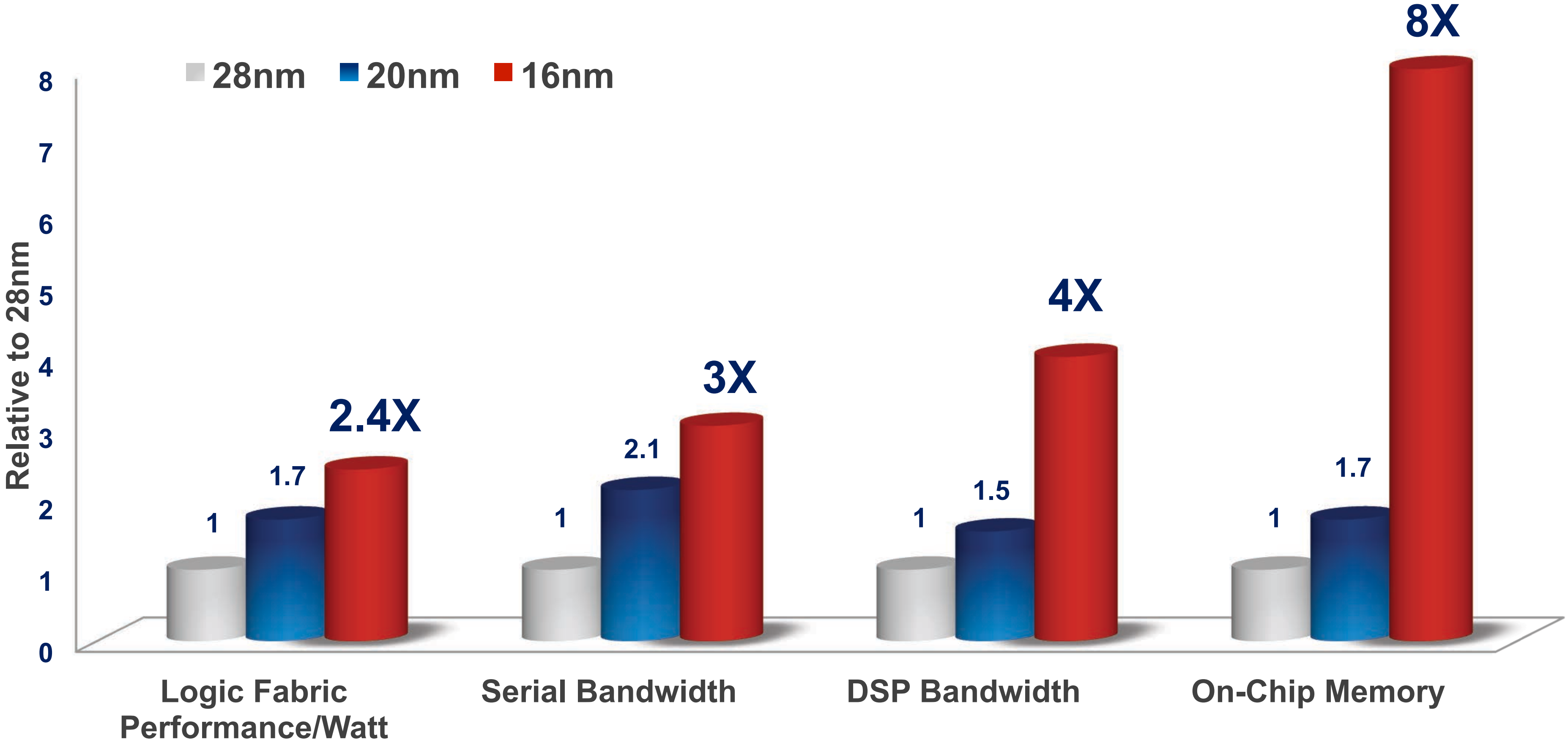


**0 Errors in 5+ days**

*Xilinx DFE = Decision Feedback Equalization plus Cont. Time Linear Equalization

# Tools for Triggers: FPGAs

Example: Xilinx Virtex 7 (28 nm), Ultrascale (20 nm), Ultrascale + (16 nm)

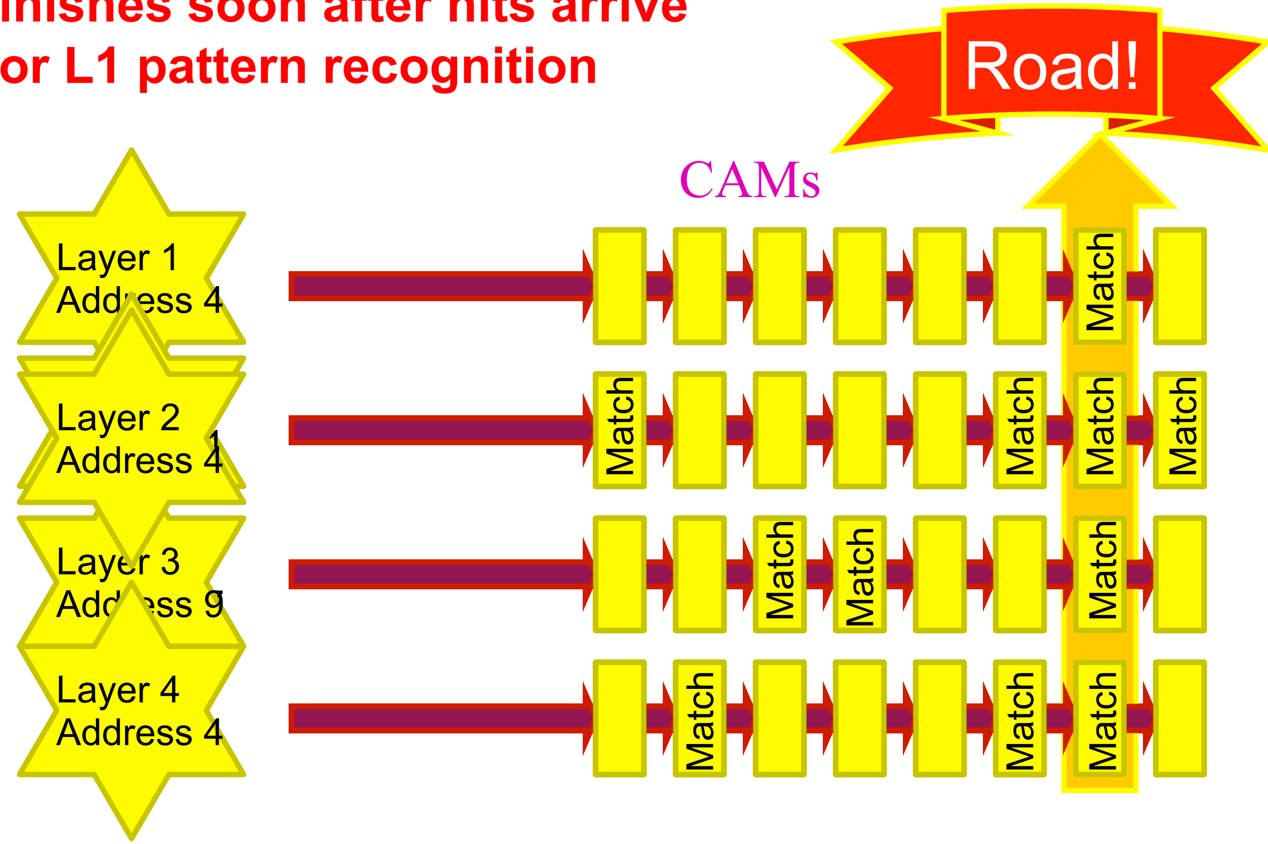


| | | | |
|---|---|---|---|
| Enhanced Fabric with FinFET performance | Up to 128 transceivers at up to 32.75 Gb/s | ~12,000 DSP slices running at ~900 MHz | UltraRAM for SRAM device replacement |

# Tool for Tracking Triggers: Associative Memories

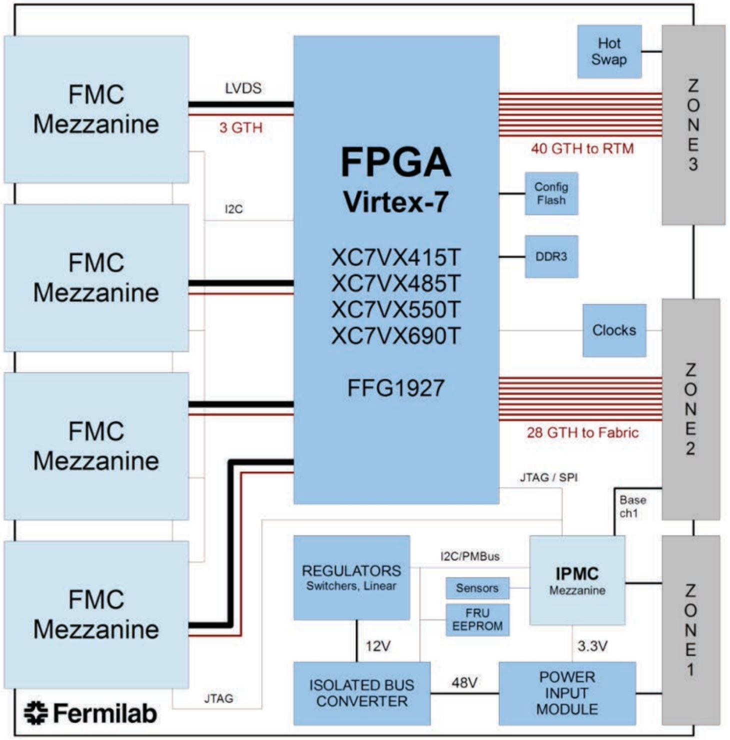
## Pattern Recognition Associative Memory (PRAM)

- **Based on CAM cells to match and majority logic to associate hits in different detector layers to a set of pre-determined hit patterns**
  - Example of FTK planned for ATLAS Level 2 Trigger in Phase 1
- **highly flexible/configurable, much less demand on detector design**
- **Pattern recognition finishes soon after hits arrive**
- **Potential candidate for L1 pattern recognition**
- **However: Latency**
- **Challenges:**
  - Increase pattern density by 2 orders of magnitude
  - Increase speed x 3
  - Same Power
  - Use 3D architecture: Vertically Integrated Pattern Recognition AM - VIPRAM

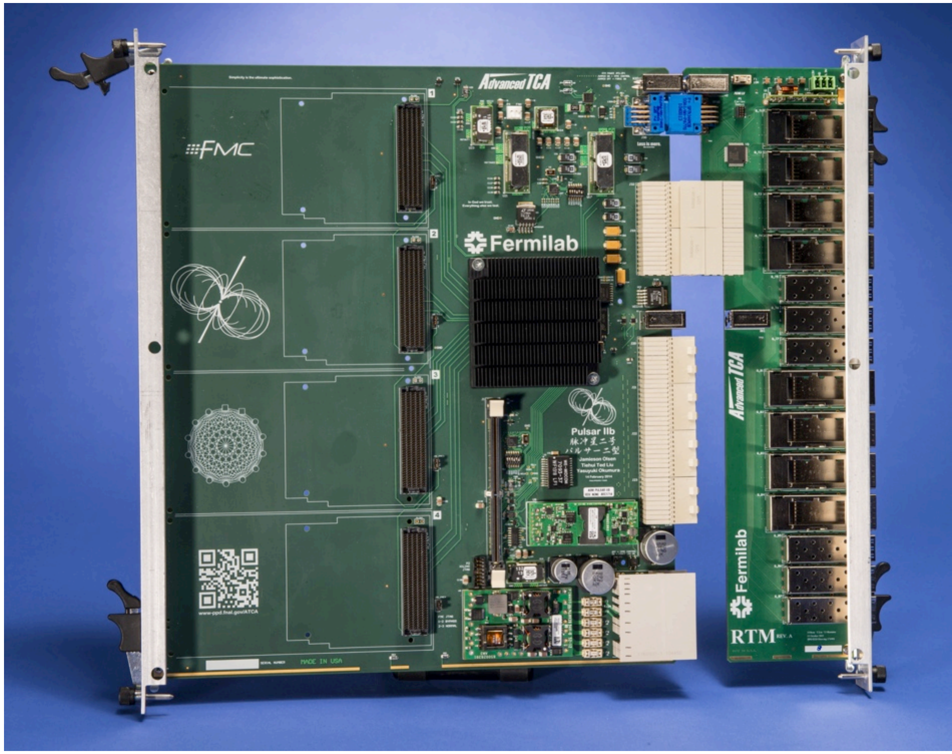


# Tools for Trigger/DAQ: ATCA

- **Advanced Telecommunications Computing Architecture**
- **Example: Pulsar Card (FNAL, UIC, Northwestern) for CMS Track Trigger**
  - **Use FPGAs for low latency**
  - **FPGAs are directly connected to the full mesh fabric channels**
  - **No network switch**
  - **Low overhead serial protocols**
  - **High bandwidth I/O via serial links on Rear Transition Module and mezzanines**



FMC Mezzanine
FMC Mezzanine
FMC Mezzanine
FMC Mezzanine
LVDS
3 GTH
I2C
JTAG
**FPGA**
**Virtex-7**
XC7VX415T
XC7VX485T
XC7VX550T
XC7VX690T
FFG1927
Hot Swap
40 GTH to RTM
Config Flash
DDR3
Clocks
28 GTH to Fabric
JTAG / SPI
Base ch1
ZONE 3
ZONE 2
ZONE 1
REGULATORS Switchers, Linear
I2C/PMBus
Sensors
FRU EEPROM
IPMC Mezzanine
12V
3.3V
ISOLATED BUS CONVERTER
48V
POWER INPUT MODULE
Fermilab

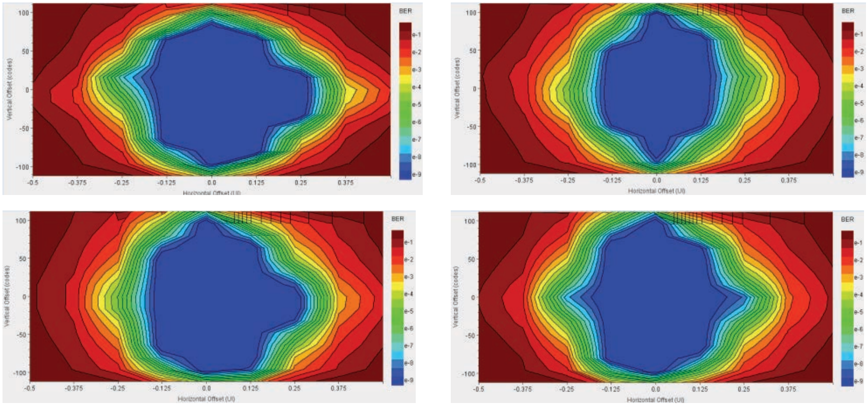


# ATCA Backplane example: Pulsar IIb

**Full shelf tests with all lanes running at 10 Gbps**

- **BER = $2 \times 10^{-16}$**

**Evaluating latest high performance 40G+ full mesh backplanes from ASIS-PRO, COMTEL, and Pentair/Schroff**



Fermilab

# ATLAS & CMS HL-LHC Trigger Summary

## ATLAS Architecture:

- Divide L1 Trigger into L0, L1 of latency 6, 30 μsec, rate ≲ 1 MHz, ≲ 0.4 MHz, HLT output rate of 5 - 10 kHz
- L0 uses Cal. & μ Triggers, which generate track trigger seeds
- L1 uses Track Trigger & more muon detectors & more fine-grained calorimeter trigger information.

## CMS Architecture

- L1 Trigger latency, rate: 12.5 μsec, .5 – .75 MHz (140 – 200 PU)
- L1 uses Track Trigger, finer granularity μ & calo. Triggers
- HLT output rate of 5 – 7.5 kHz (140 – 200 PU)

## Performance:

- Track Trigger reduces L1 Menu rate by ~ 6
- Track Trigger combined with L1A rate maintains overall physics performance + acceptance of L1 Trigger Phase 1 Upgrade (e.g. thresholds near what are running now)

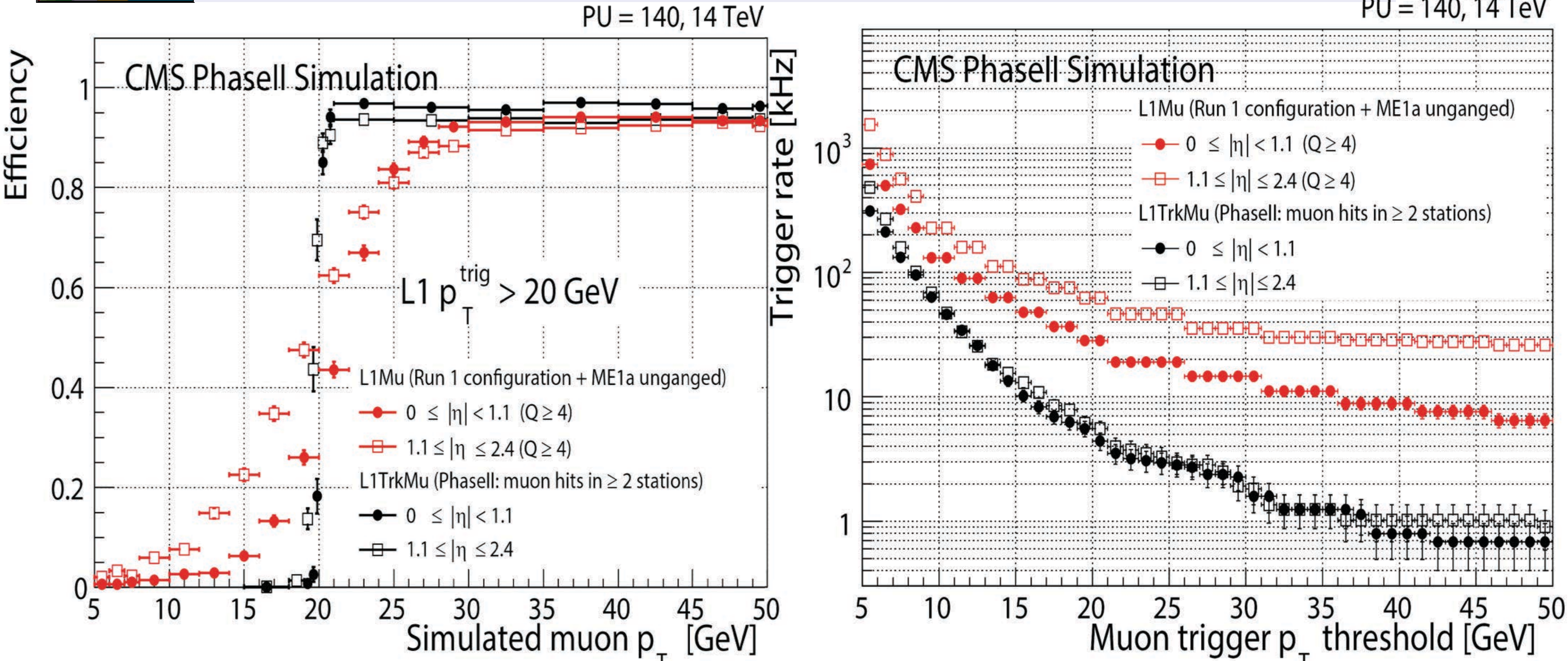
## Schedule:

- R&D Program underway now…important to validate design, techniques & technologies

# Backup

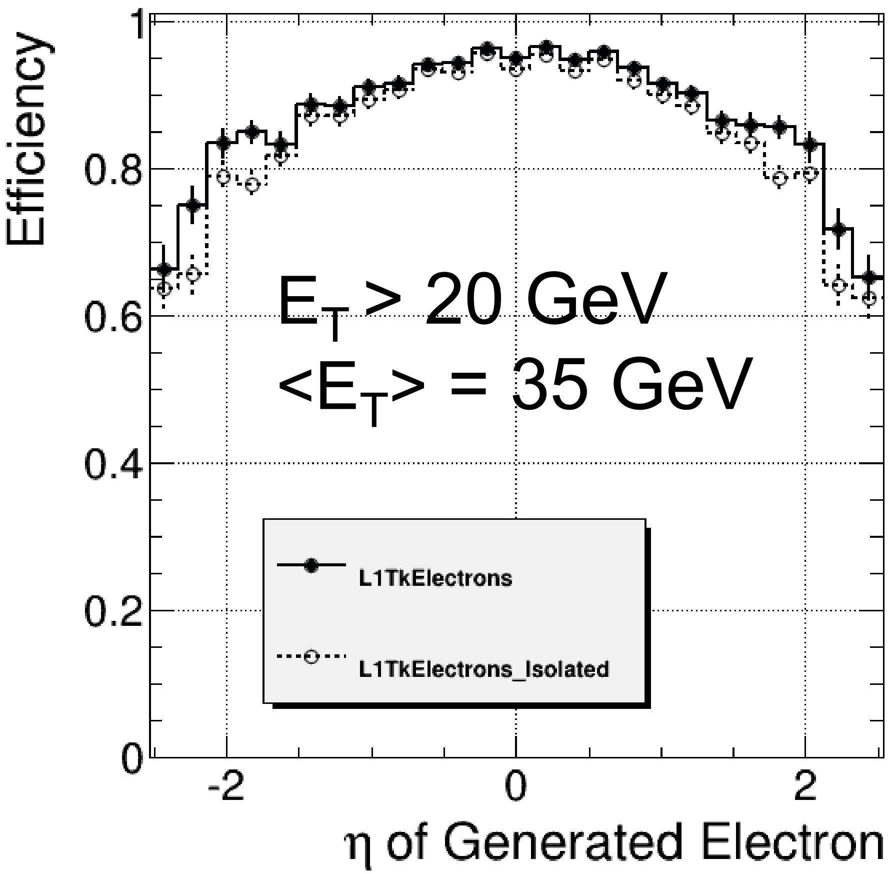
## Slides on Algorithms
## (see Rick Cavanaugh's Talk)

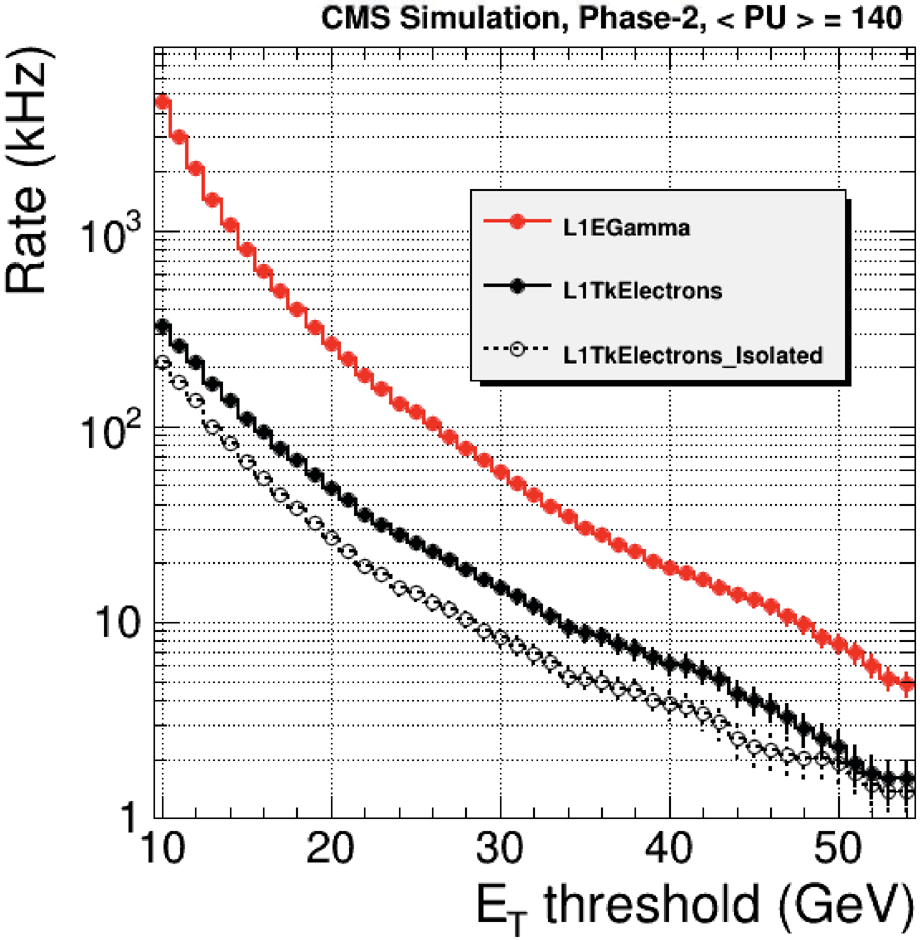
# Track Trig. Correlator: muons



- Stand-alone muon trigger rates flatten above ~30 GeV from mis-assignments of low $p_T$ muons
- Match L1 tracks + L1 muons (inside-out vs outside-in)
- Sharpens turn-on curve, improves efficiency
- For a threshold of ~ 20 GeV, rate of single muon trigger can be reduced by a factor of O(10)

# Track Trig. Correlator: electrons

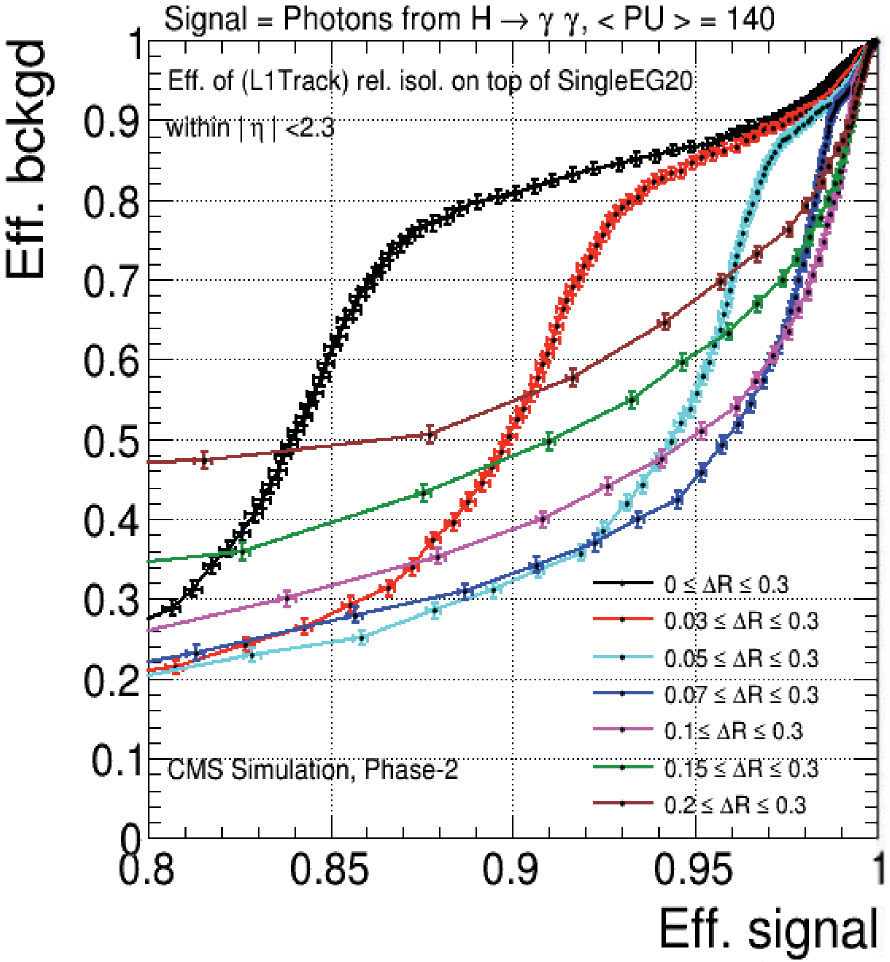


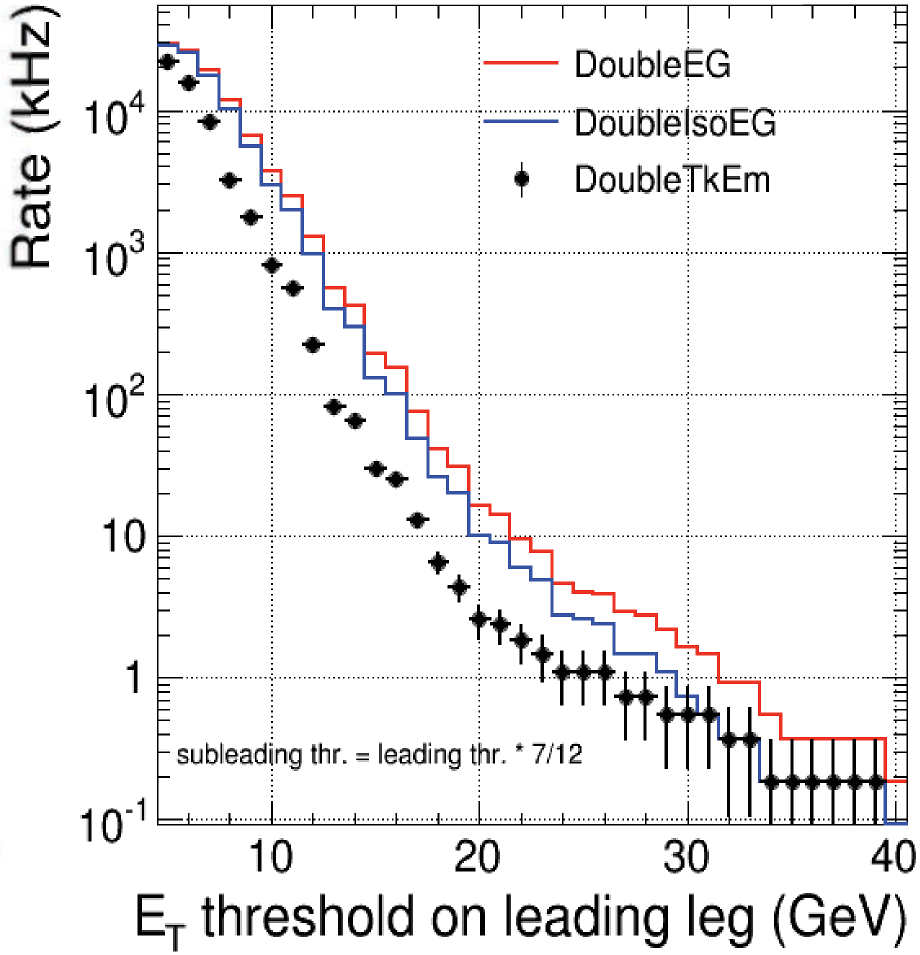


**Efficiency exceeds 90% in central region**

**Match with Track Trigger plus track-based isolation retains good efficiency with rate reduction of O(10)**

# Track Trig. Correlator: photons



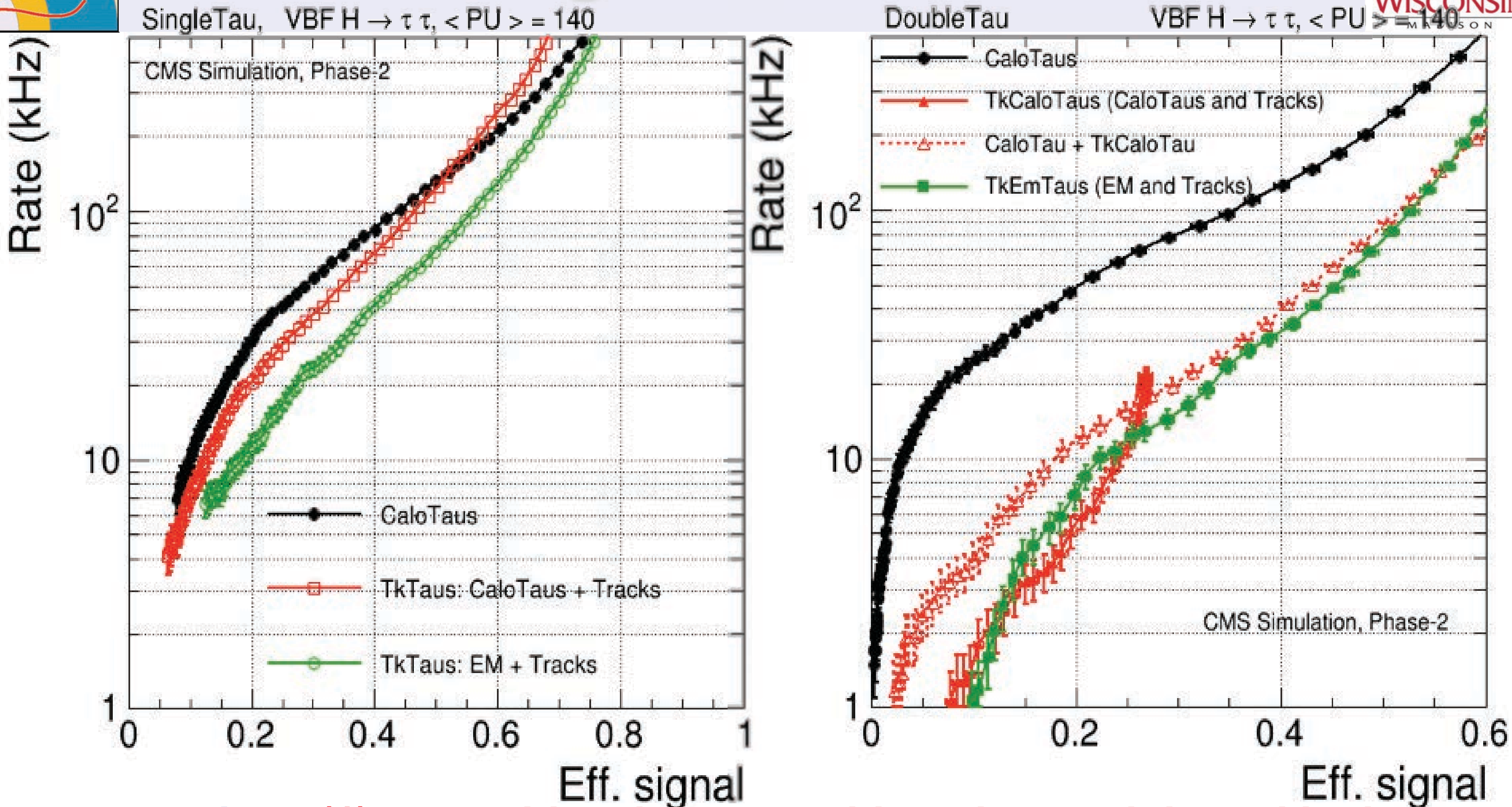


**Track-based isolation excludes tracks from conversions**

**Reduce rate of Single Photon trigger by 2 (3) for an efficiency on H → γγ of 95% (90%)**

**For diphoton thresholds of ~ 18,10 GeV on leading, subleading legs, the rate can be reduced by a factor of > 6**

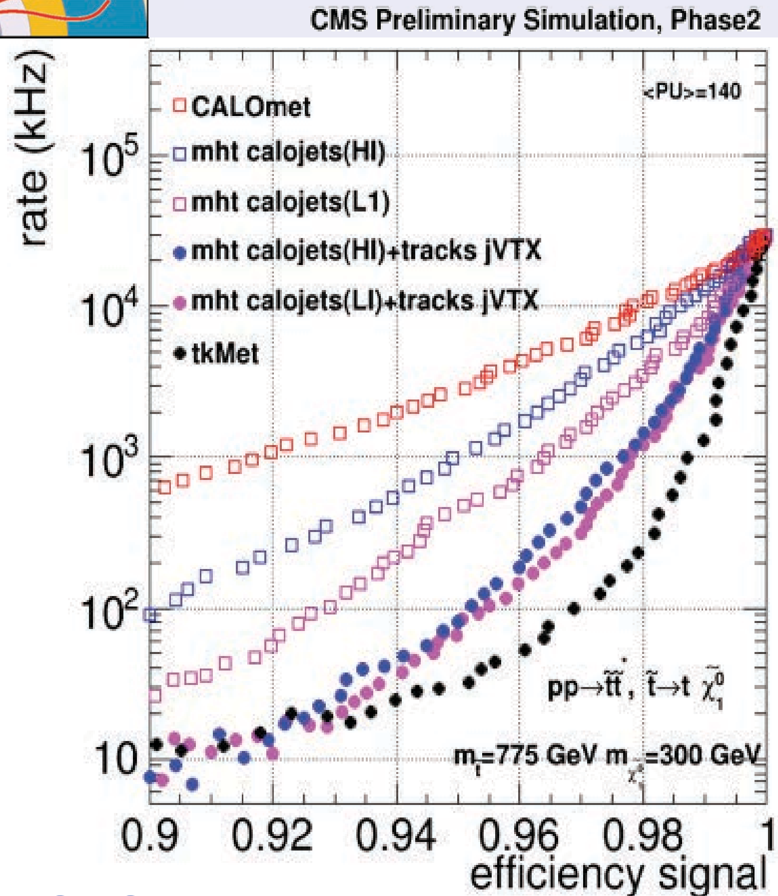
# Track Trig. Correlator: taus

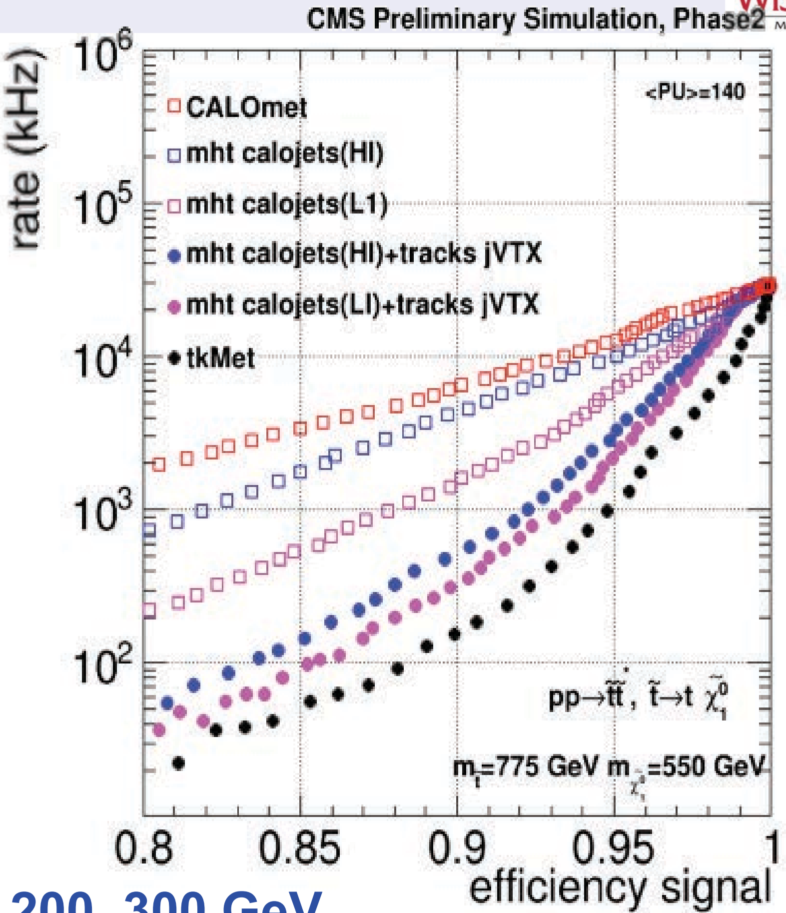


**Two approaches: (1) start with calo. taus, add tracks, track-based isolation or (2) start w/tracks, add crystal L1 EM objects.**

**With either approach can maintain ~ 50 kHz trigger rate with ~ 50% efficiency for VBF H →ττ**

# Track Trig. Correlator: MET, MHT





- Two SUSY scenarios generating MET of 200, 300 GeV
  - Stop pair decays to top and neutralino
- Signal defined to be events with gen. MET > 100 GeV
- MHT plus vertex constraint 95% efficient with few 10's kHz rate
- Track-based MET reduces rate over calo MET by 2 orders of magnitude while maintaining 80-85% efficiency in "Low MET" scenario