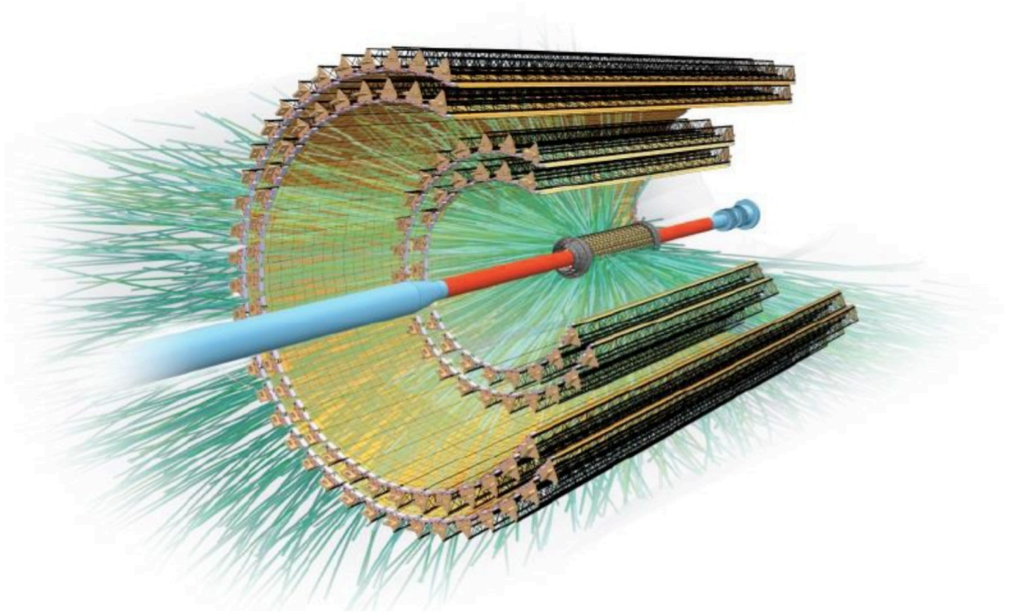
A new generation of MAPS for the ALICE Inner Tracking System



J.W. van Hoorne - CERN

WG11 – Detector Design Meeting

CERN, December 19th, 2016

Outline

1. Introduction
    - Present ALICE detector and upgrade plans
    - Upgrade of the ALICE Inner Tracking System (ITS)

2. ALPIDE
    - Concept
    - Key results

3. Future developments
    - Process modifications for enhanced depletion
    - Silicon-only vertex detector?

4. Summary

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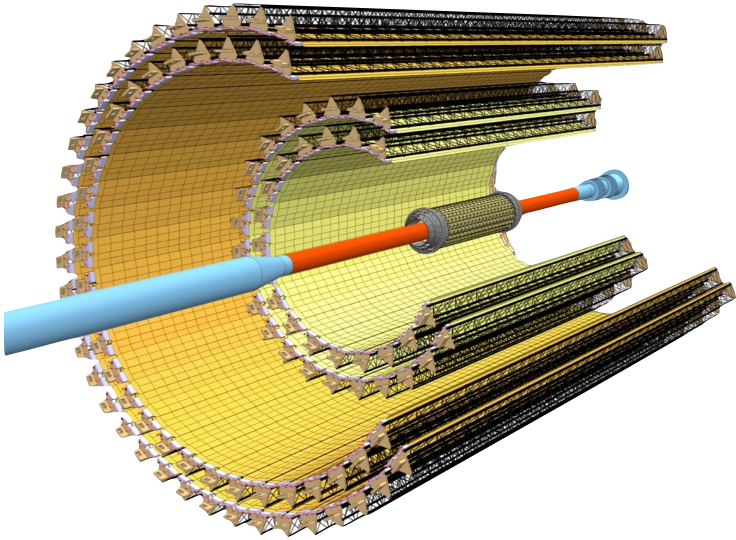
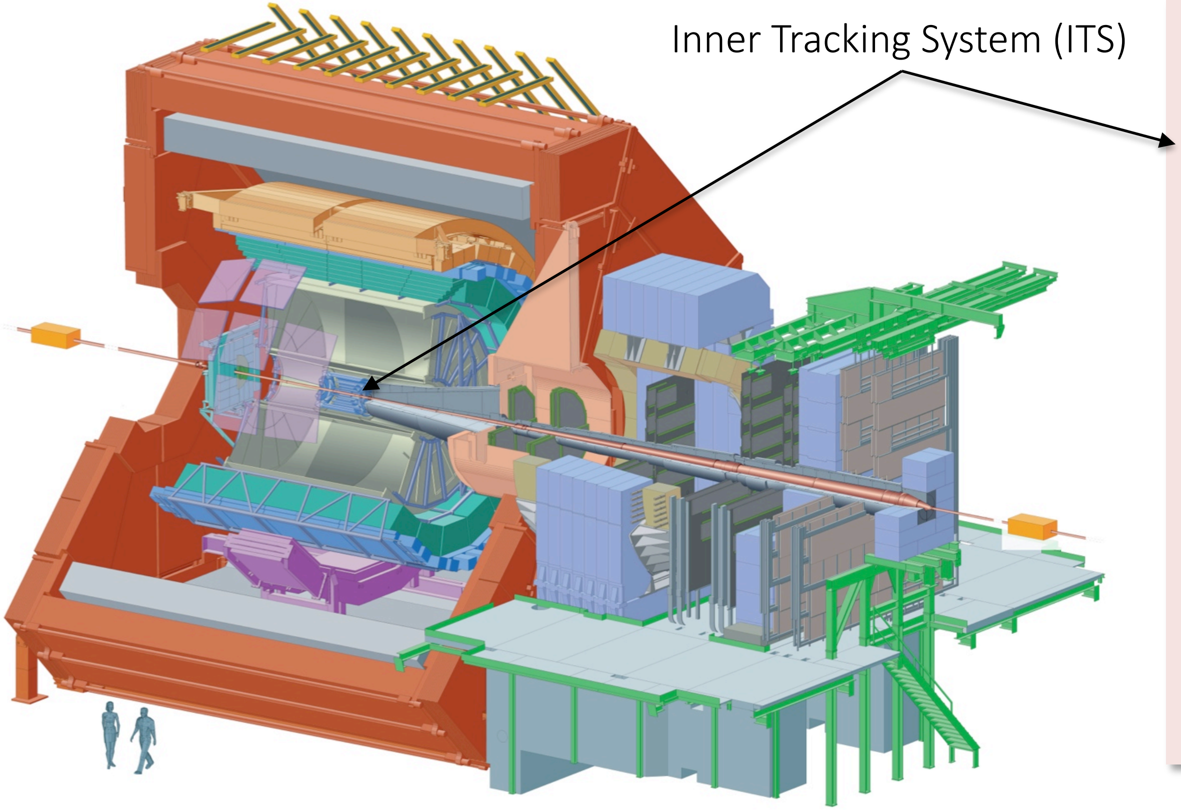


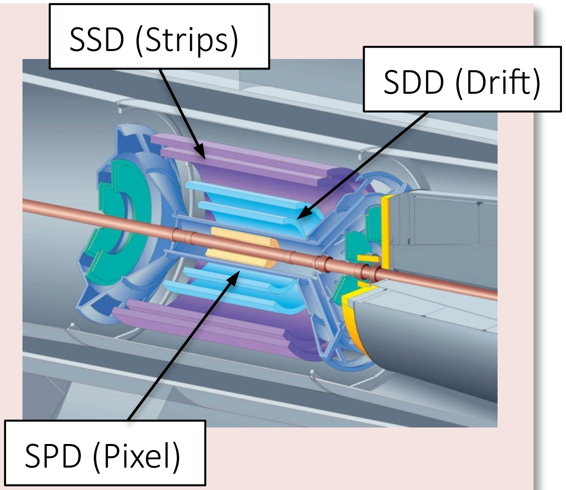
ALICE experiment and upgrade plans

1. Introduction

- ALICE prepares major upgrade of experimental setup in LS2 of LHC in 2019/2020
- Targets:
  - Large sample of recorded events: 10 nb^{-1} Pb-Pb plus pp and p-Pb data -> gain factor 100 in statistics over originally approved program
  - Significant improvement of tracking and vertexing capabilities at low p_T

➔ also present ITS needs to be upgraded!





6 layers:

- 2 layers silicon pixel (SPD)
- 2 layers silicon drift (SDD)
- 2 layers silicon strips (SSD)

ITS upgrade: design objectives

1. Introduction

Improve pointing resolution by a factor ~3 in r-ϕ and ~5 in z at p_T=500MeV/c (~40 µm at p_T = 500 MeV/c)

- reduce beam pipe radius: 29mm → 19mm
- get closer to IP: 39mm → 22mm (innermost layer)
- reduce material budget: ~1.14% x/X_0 → ~0.3% x/X_0 (inner layers)

  → less material → reduce power consumption
- reduce pixel size: 50x425µm^2 → O(30x30µm^2)

Improve tracking efficiency and p_T-resolution at low p_T

- increase granularity: 6 layers → 7 layers, only pixel sensors

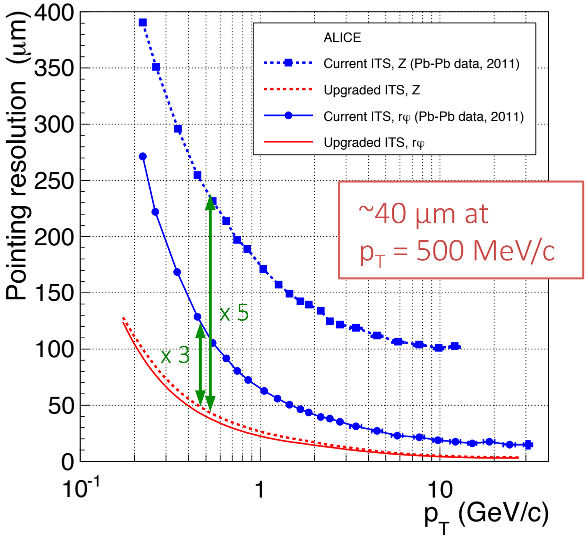
Fast readout

- readout of Pb-Pb at up to 100 kHz (presently 1kHz) and 400kHz for pp

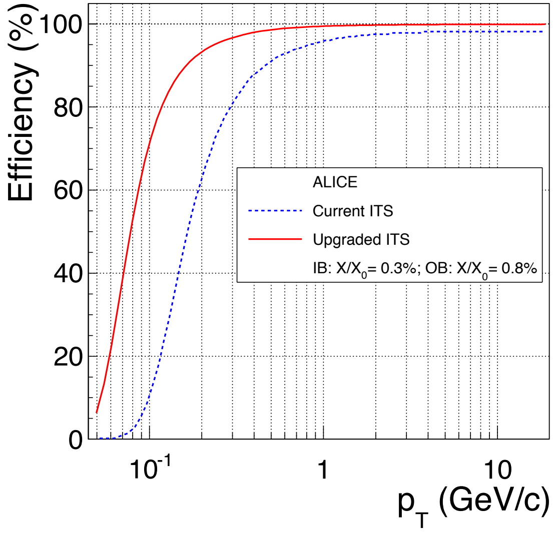
Fast insertion/removal of detector modules

- possibility to replace non-functioning detector modules during yearly shutdown

→ Decision to fully replace present ITS



~40 µm at p_T = 500 MeV/c

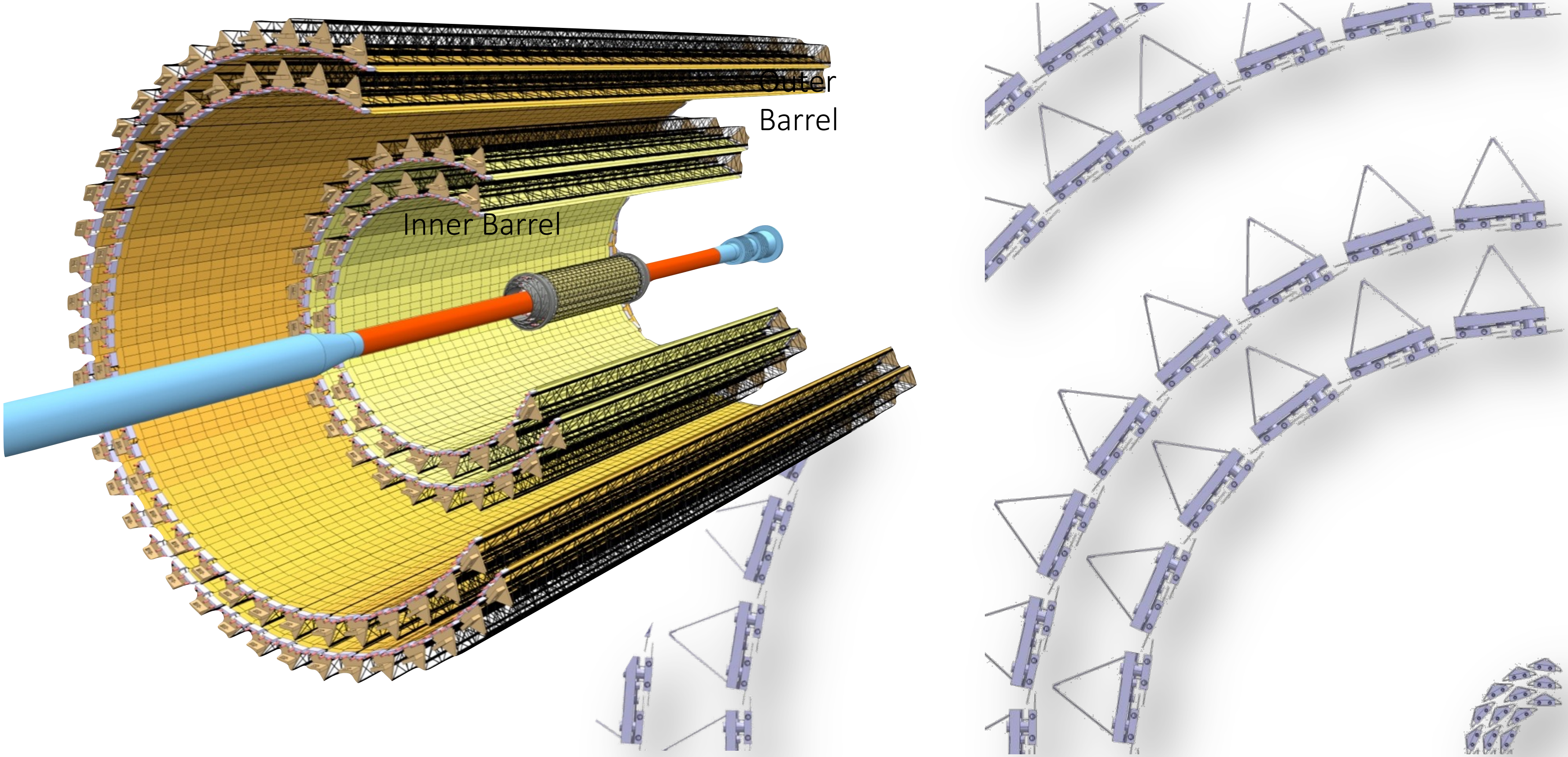


Layout of new ALICE Inner Tracking System

7-layer geometry:

- r-coverage: 23 mm - 400 mm
- η-coverage: |η|≤ 1.22 for tracks from 90% luminous region

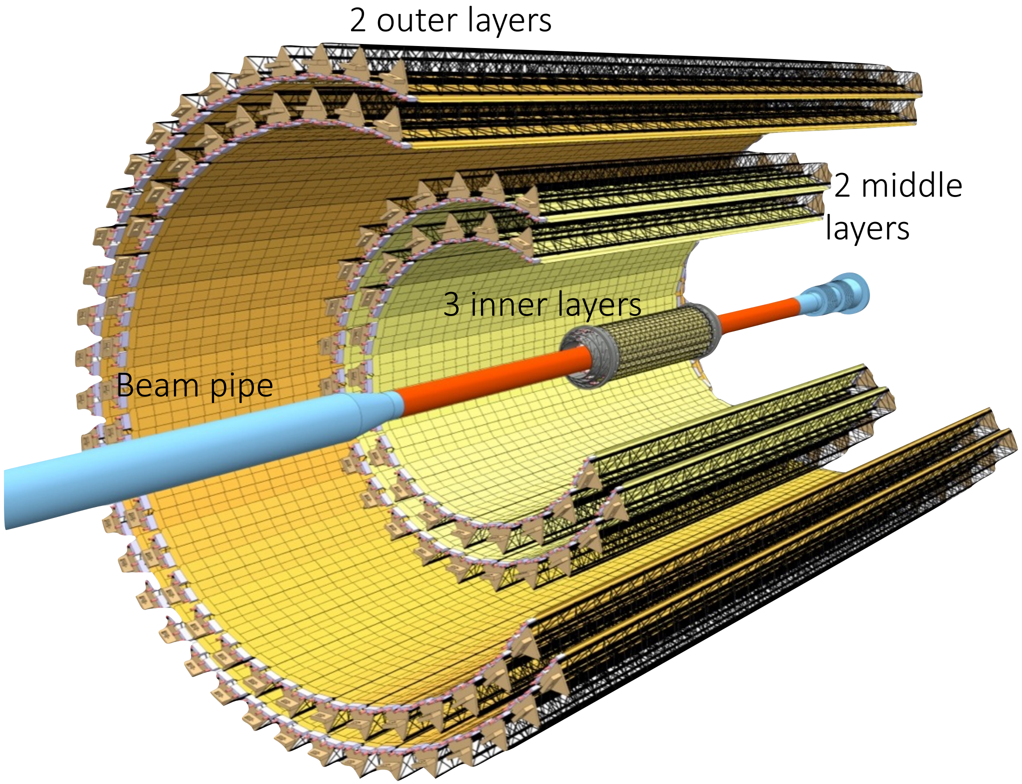
- 3 Inner Barrel layers: 0.3% x/X_0 per layer
- 4 Outer Barrel layers: 1% x/X_0 per layer



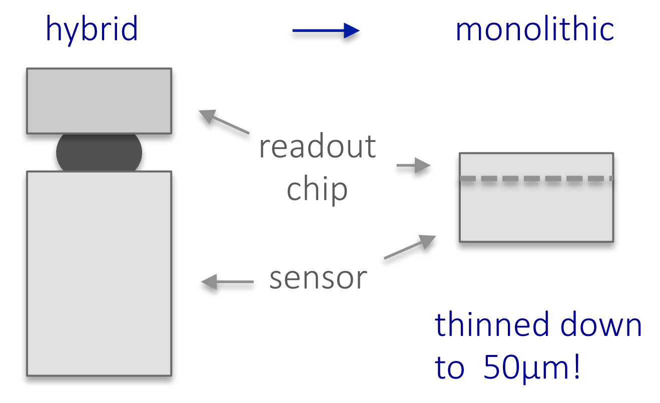
Layer n.	6	5	4	3	2	1	0
N. of staves	48	42	30	24	20	16	12
Stave length	1500 mm		900 mm		290mm		

Layout of new ALICE Inner Tracking System

1. Introduction



Fully equipped with Monolithic Active Pixel Sensors (MAPS)



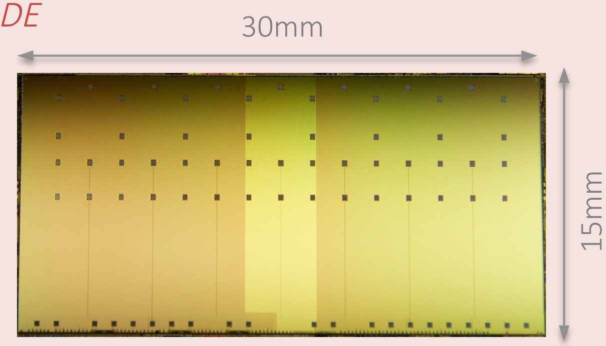
hybrid → monolithic

readout chip

sensor

thinned down to 50µm!

ALPIDE

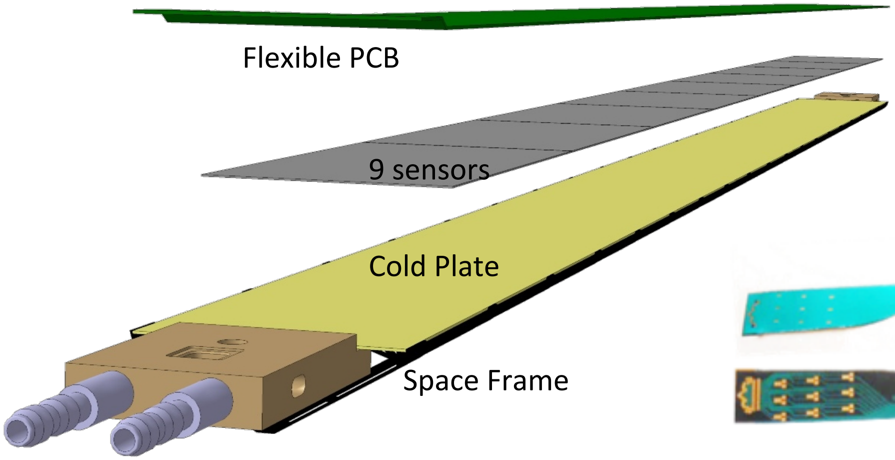


12.5 G-pixel camera:

- binary readout
- ~10 m^2 total area
- ~25000 chips

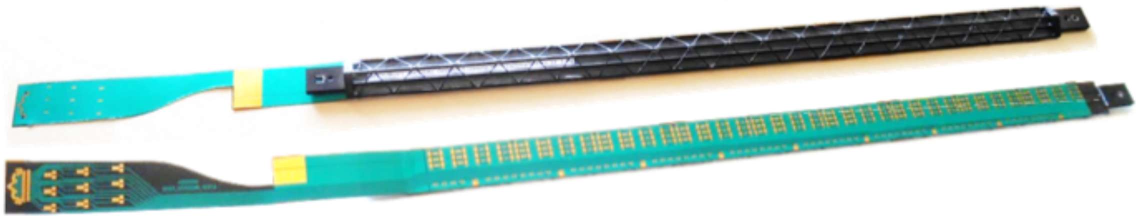
Stave layout

Inner Barrel stave

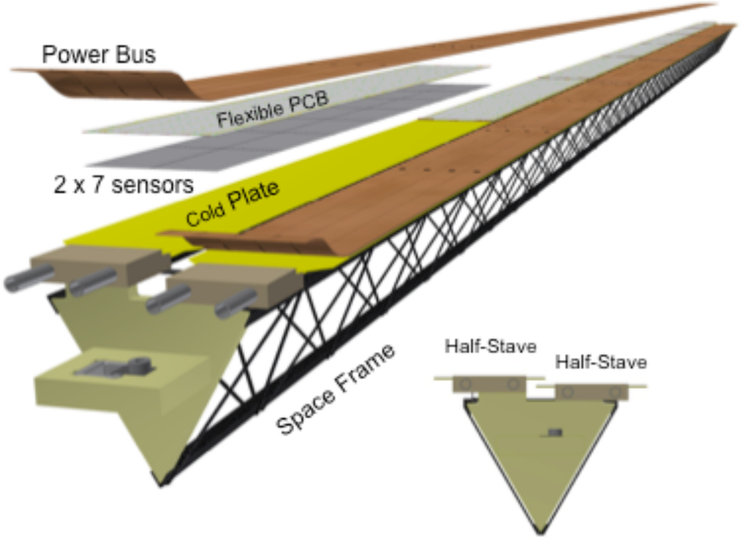


Inner barrel module (x48):

- 9 chips, each read out using 1.2 Gb/s link

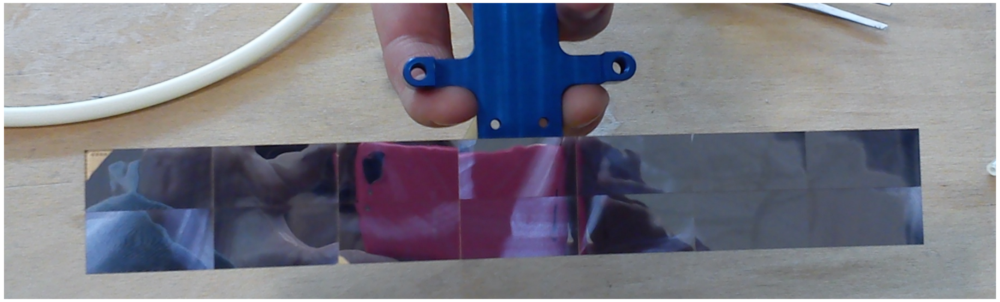


Outer Barrel



Outer barrel module (x1800)

- 2×7 chips (1 master, 6 slaves), locally interconnected, read out using 2×400 Mb/s links

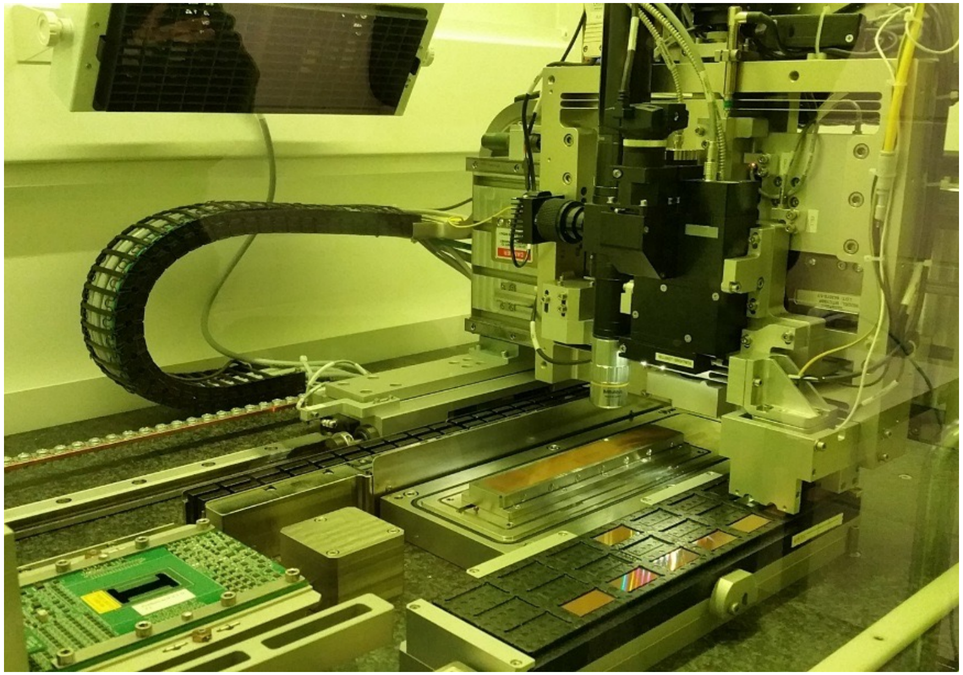


Module assembly

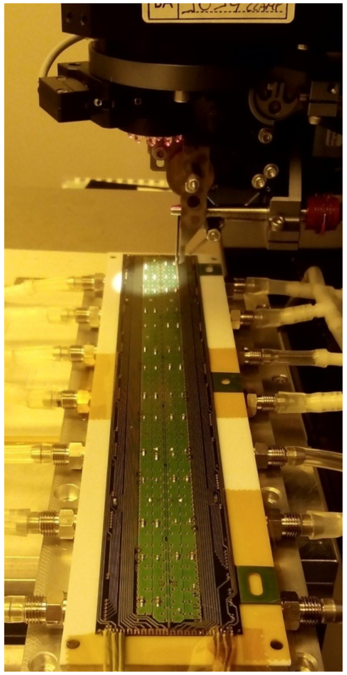
1. Introduction

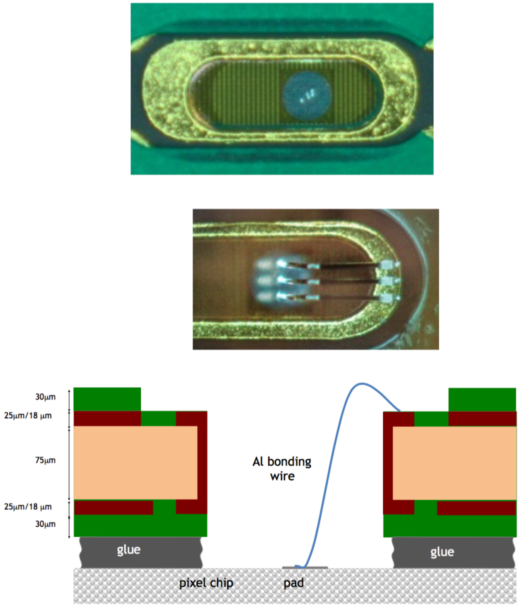
Module (HIC – hybrid integrated circuit): chips glued and wire-bonded to flexible PCB

Chip placement + gluing to flexible PCB



Wire bonding





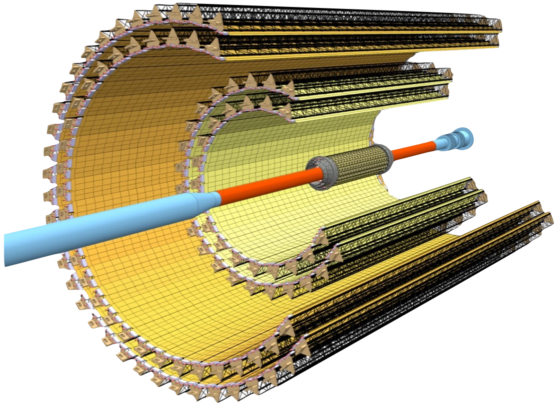
- Placement is handled by automated custom-made machine (distributed to 6 assembly sites worldwide)
- Flexible PCB is glued to chips

- Chips are wire bonded through vias in the FPCB distributed over full chip surface

Detector readout

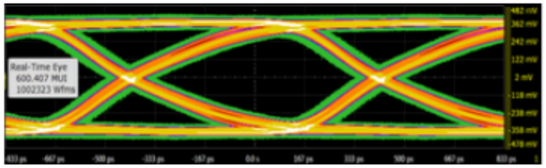
1. Introduction

Detector



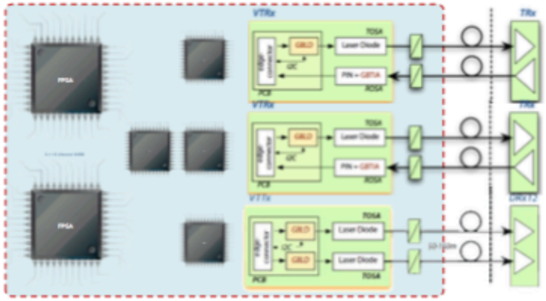
- Readout logic fully integrated into ALPIDE
- ALPIDE can directly drive 5m cables using integrated high-speed transmitters (up to 1.2 Gb/s)
- No further electronics on detector

5m cable



- 1.2 Gb/s (data IB)
- 400 Mb/s (data OB)
- 80 Mb/s (ctrl IB/OB)
- Clock
- Power

Readout units



- Total: 192 Readout Units
- Distribute trigger and control signals
- Interface data links to ALICE DAQ
- Control power supplies of chips

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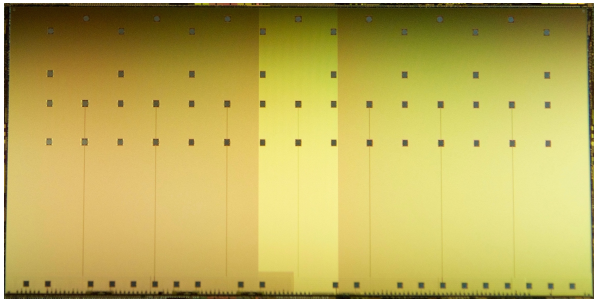


30mm

ALICE ITS pixel chip requirements

2. ALPIDE

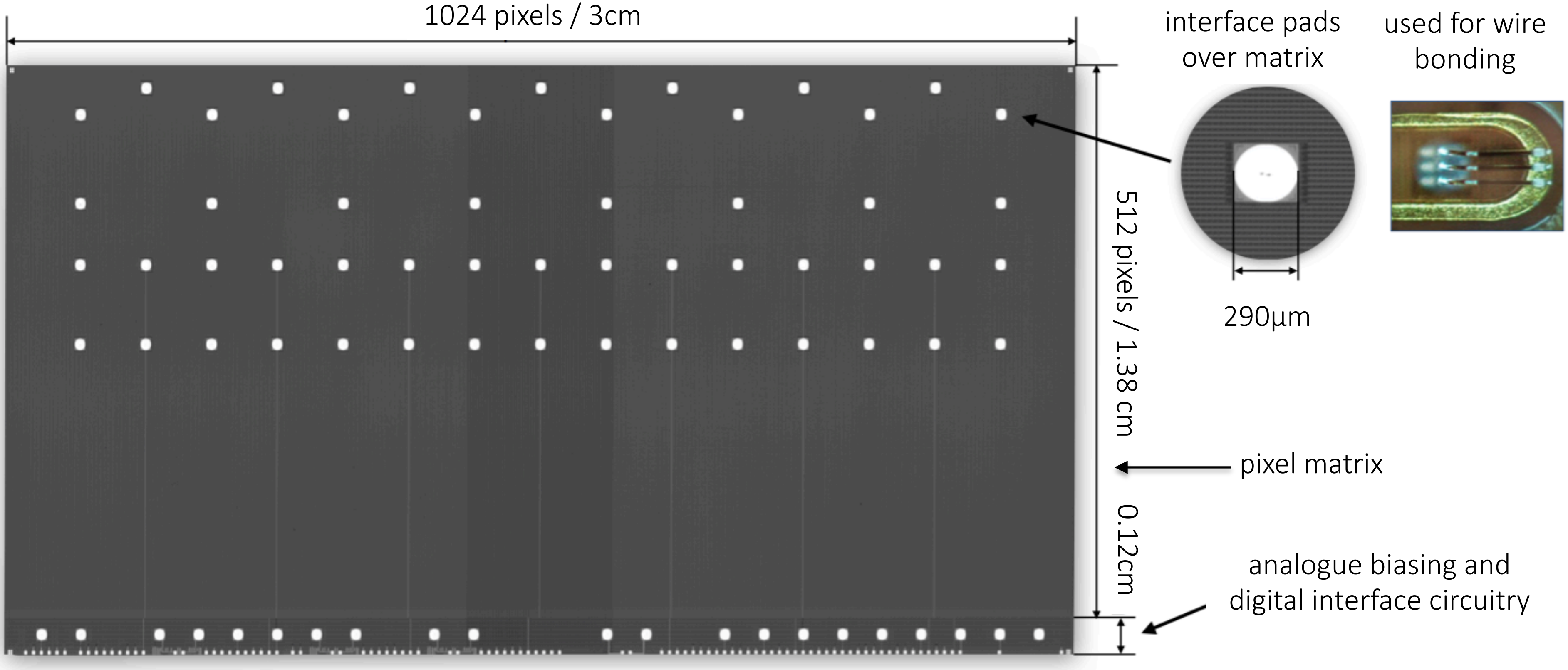
State of the art of monolithic CMOS pixel sensors at start of pixel chip R&D for the ITS upgrade end 2011

Parameter	Inner Barrel	Outer Barrel	Ultimate at STAR
Silicon thickness	50µm		50µm
Spatial resolution	5µm	10µm	~4µm
Chip dimension	15mm x 30mm		22.71mm x 20.24mm
Power density	< 300mW/cm^2	< 100mW/cm^2	150mW/cm^2
Event time resolution	< 30µs		185.6µs
Detection efficiency	> 99%		> 99%
Fake hit rate	< 10^{-5}/event/pixel		< 10^{-4}/event/pixel
NIEL tolerance	1.7x10^{12} 1MeV n_{eq}/cm^2	10^{11} 1MeV n_{eq}/cm^2	3x10^{12} 1MeV n_{eq}/cm^2
TID tolerance	270krad	10krad	150krad

- First large MAPS-based vertex detector: STAR PXL detector at RHIC with Ultimate chip
- Ultimate chip does not fulfill requirement of ITS upgrade -> new development required -> ALPIDE

ALPIDE: floor plan

2. ALPIDE



1024 pixels / 3cm

512 pixels / 1.38 cm

0.12cm

interface pads over matrix

used for wire bonding

290µm

pixel matrix

analogue biasing and digital interface circuitry

Key features:

- Dimension: 30mm x 15mm (1024 x 512 pixels)
- Pixel pitch: 29µm x 27µm
- Ultra low power:~40mW/cm^2 (average over entire chip)
- Global shutter: triggered acquisition (up to 200 kHz Pb-Pb, 1MHz pp) or continuous (progr. integration time: 1µs - ∞)

Key concepts:

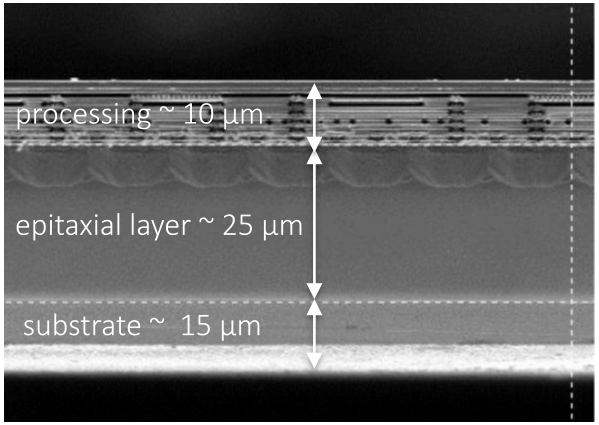
- In-pixel amplification
- In-pixel hit discrimination
- In-pixel 3-level event memory
- In-matrix zero-suppression

ALPIDE: process technology

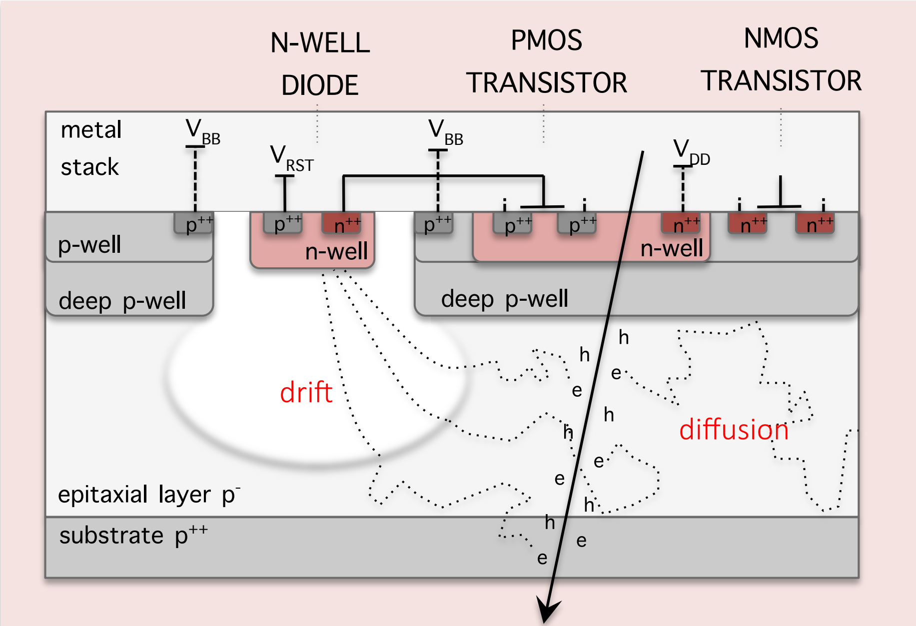
TowerJazz 180nm CMOS imaging sensor process:

- High-resistivity (>1kΩcm) p-type epitaxial layer (18µm-40µm) on p-type substrate (~10Ωcm)
- Deep p-well for full CMOS circuitry within the matrix
- Feature size 180nm and 6 metal layers ➔ dense circuitry

Sensor only partially depleted ➔ application of moderate reverse bias V_{BB} (<6V) possible via the substrate



SEM picture of prototype chip cross-section



Signal from collection diode: ΔV ~ Q/C

- ➢ Increase Q:
  - increase epitaxial layer thickness
  - limit charge sharing and losses
- ➢ Decrease C:
  - optimizing collection diode
  - increase reverse bias

Charge collection time: ~1-50ns

- depending on size of depletion zone

Q/C ratio and sensor design parameters

2. ALPIDE

Sensor performance mainly determined by:

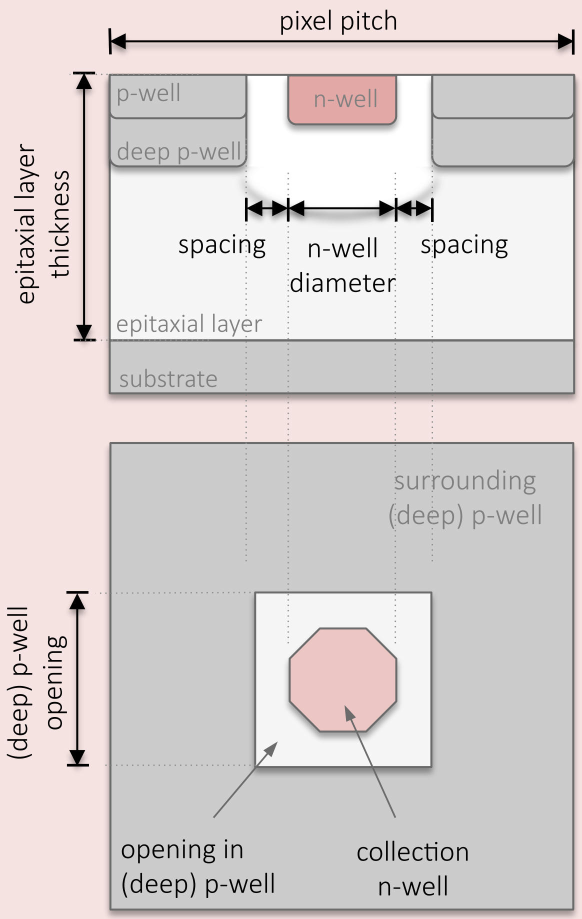
- Pixel pitch
- Collection n-well size
- Spacing between the collection n-well and surrounding(deep) p-well
- Epitaxial layer thickness and resistivity
- Reverse bias voltage V_{BB} on the collection diode

- Sensor optimization studies mainly by small-scale prototypes with analog readout
- During design of ALPIDE, particular focus put on low pixel-input capacitance C
  - ➔ values as low as 2fF achieved (signal of 80mV for 1000e$^-$)

Parameters selected for ALPIDE (29µm x 27µm pixel size):

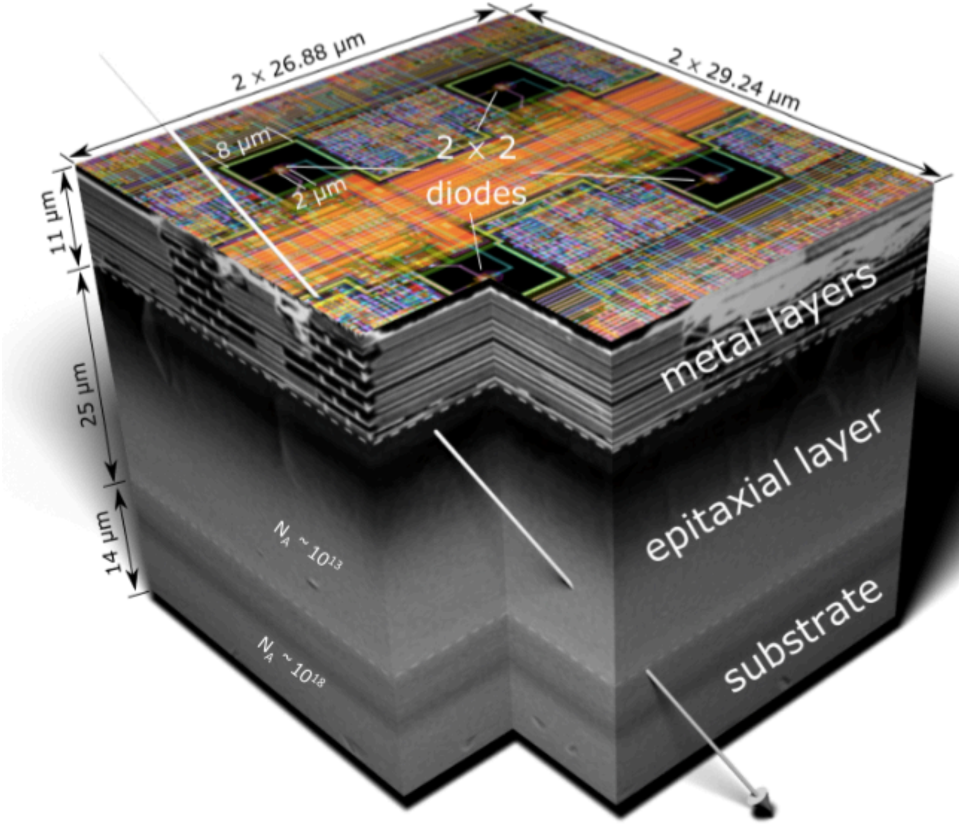
- 25µm epitaxial layer
- 2µm n-well diameter, 3µm spacing
  - ➢ 88% of pixel surface can be used for circuitry

Pixel and collection electrode geometry (not to scale):

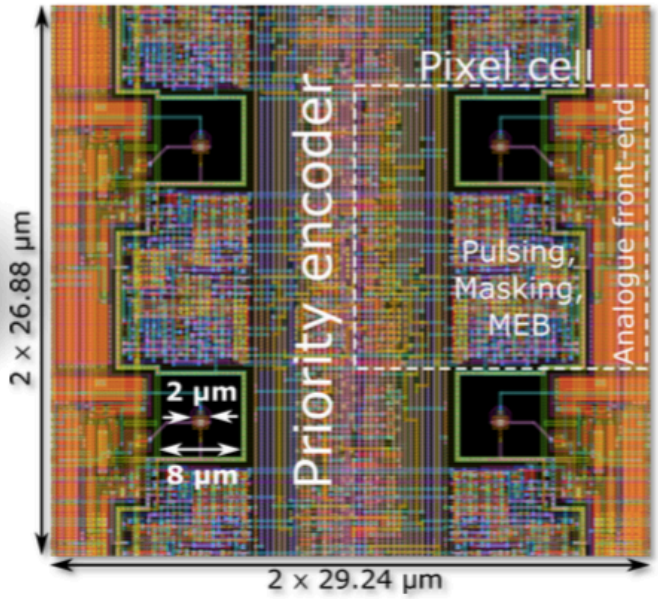


3D and 2D view of 2x2 pixels

2. ALPIDE



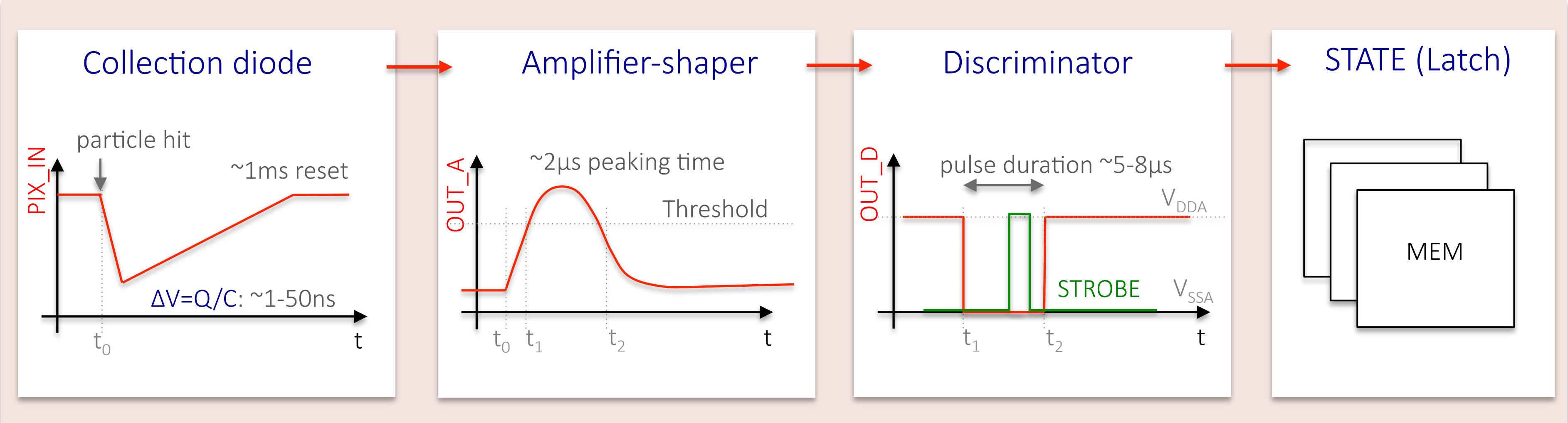
full CMOS circuitry within pixel matrix



ALPIDE in-pixel circuitry

- Front-end: continuously active, power consumption 40nW (9 transistors, full custom)
- Multi-event memory: 3 stages (62 transistors, full-custom)
- Configuration: masking and pulsing registers (31 transistors, full-custom)
- Testing: analog and digital test pulse circuitry (17 transistors, full-custom)
- Matrix read-out: priority encoder, asynchronous, hit-driven

ALPIDE: front-end circuit



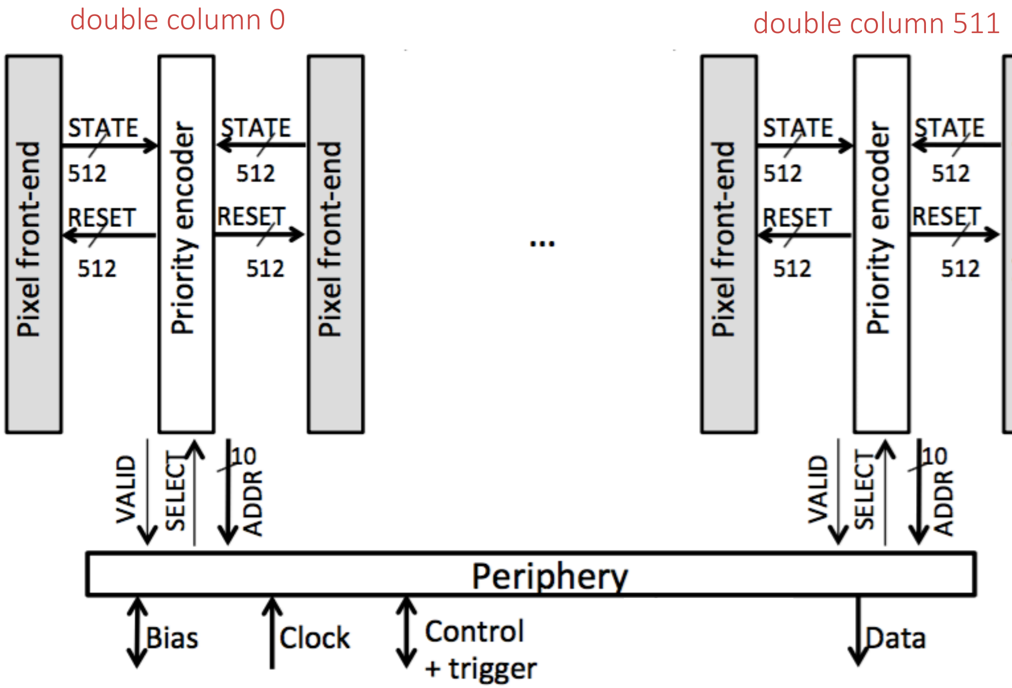
Front-end acts as delay line

Ultra low-power front-end circuit 40nW/pixel

- Sensor and front-end continuously active
- Upon particle hit front-end forms a pulse with peaking time of 2-4µs (<-> time walk)
  - charge collection time < 50ns! -> long pulse duration a choice made for ALICE ITS: functioning as delay line and reduce power consumption (40nW/pixel) <-> material budget
- Threshold is applied to form a binary pulse
  - globally set by front-end bias DACs
- Hit is latched into memory if STROBE is applied during binary pulse
  - Global shutter: triggered (up to 200 kHz Pb-Pb, 1MHz pp) or continuous (progr. integration time: 1µs - ∞)

ALPIDE: readout architecture

2. ALPIDE



Low-power matrix readout ~3mW

Matrix readout by hit-driven asynchronous circuit (priority encoder) in double-columns:

- sequentially provides addresses only of hit pixels ➔ in-matrix zero suppression, fast
- no activity if not hit (no free running clock) ➔ low-power matrix readout (~2mW)

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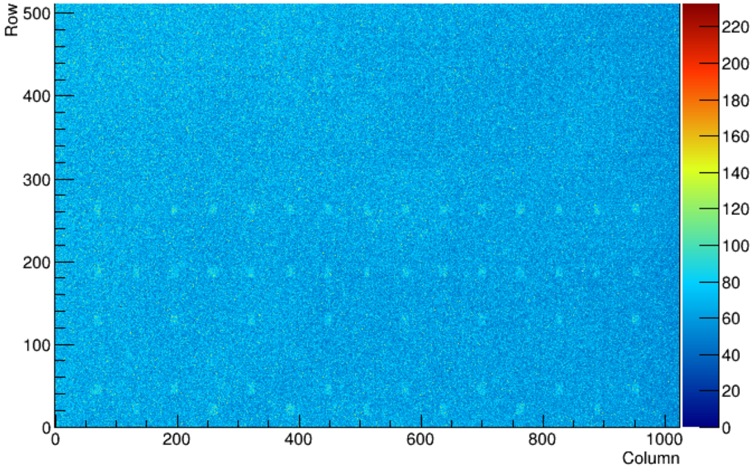
4. Summary

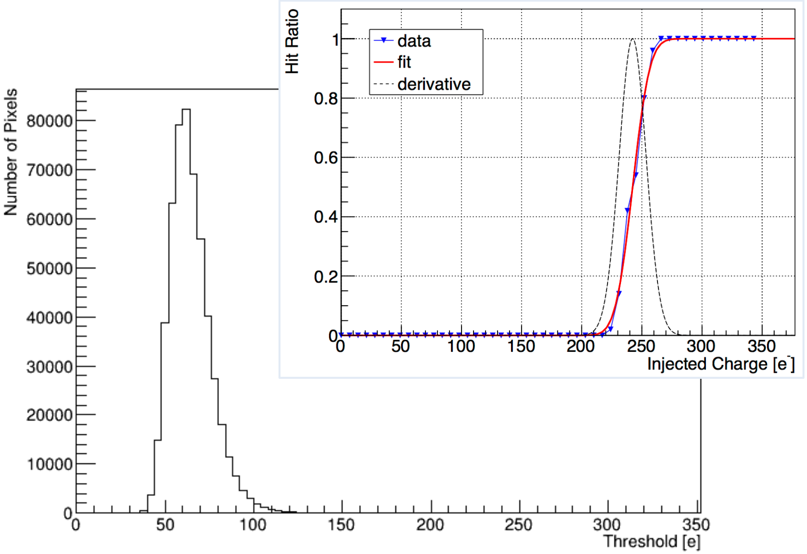
30mm

ALPIDE: Threshold and noise

2. ALPIDE

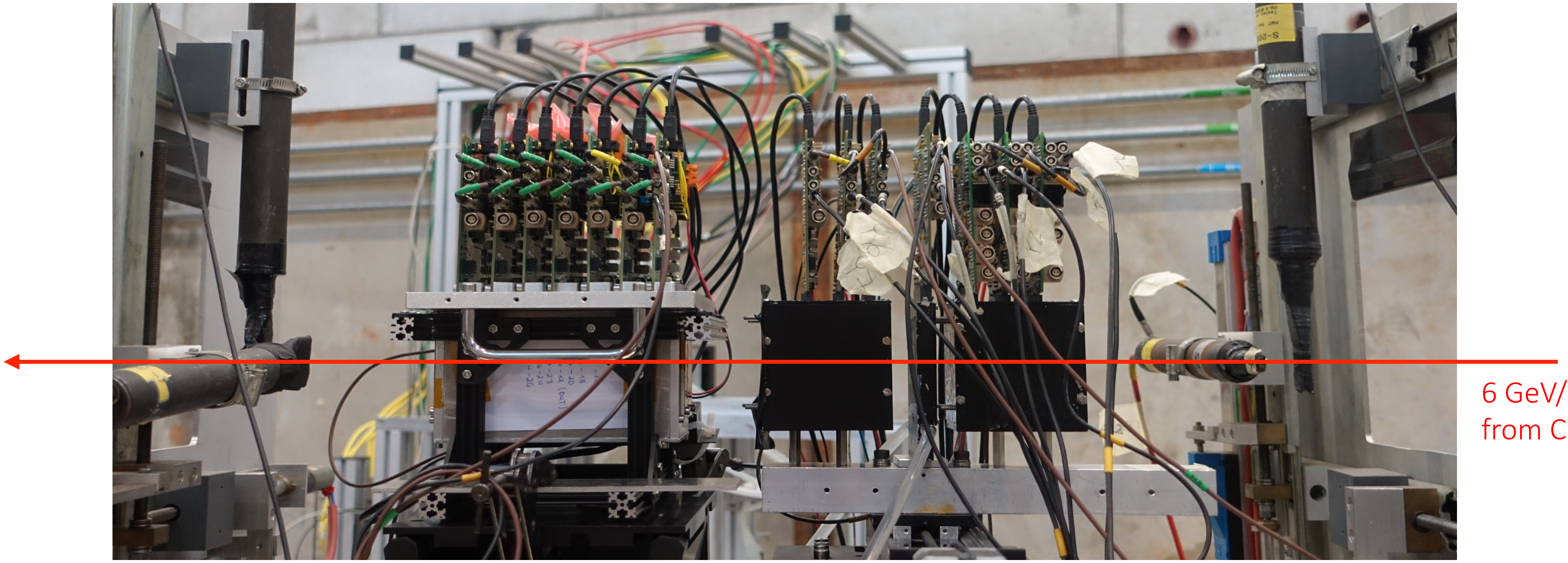
- Threshold globally adjustable via on-chip DACs
- Good threshold uniformity
  - Threshold RMS 10-15% of average threshold
- Very low noise values
  - 5-6e^- without reverse substrate bias, 2-3e^- with
- Large threshold-to-noise ratio
  - Fake-hits due to Gaussian noise extremely rare
- Large operational margin
  - MIPs release in order of 1400e- (MPV) in sensitive layer (Landau fluctuations, charge sharing also to be considered..)





ALPIDE: Test beam

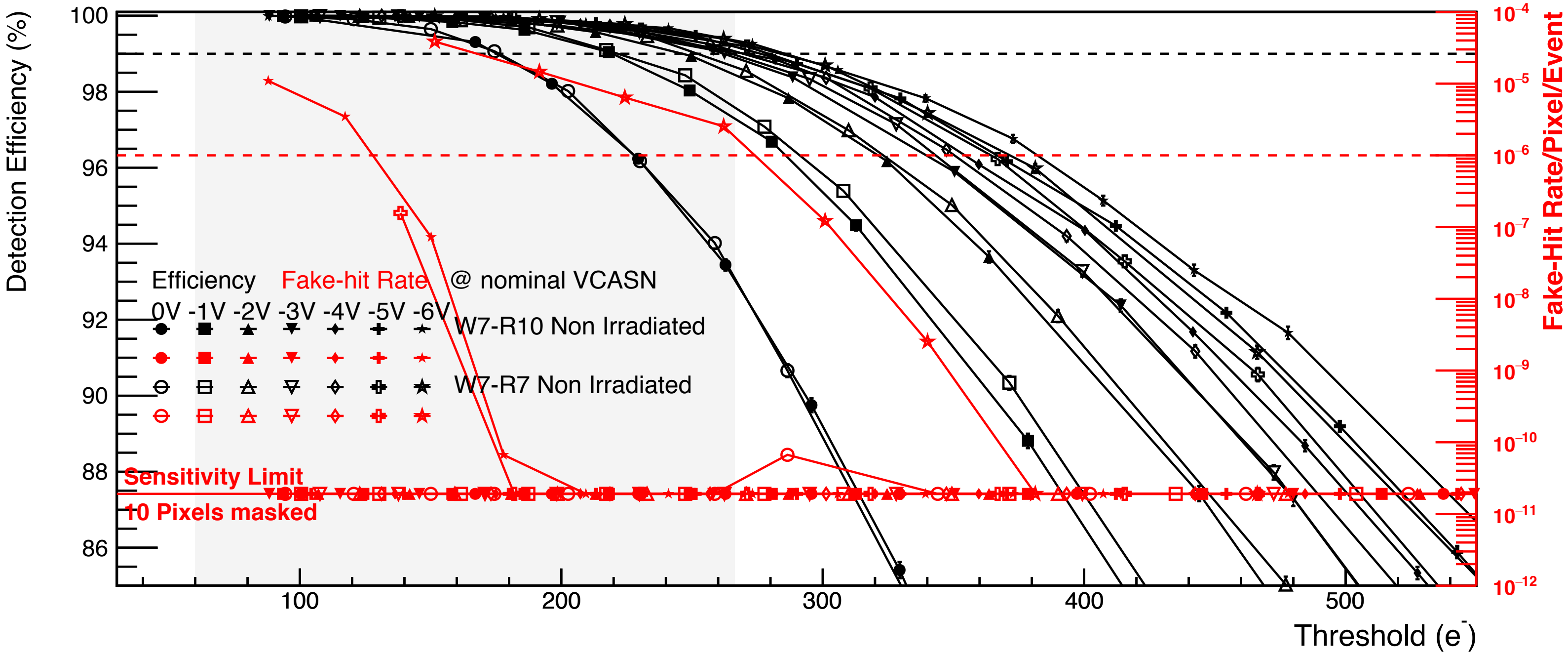
2. ALPIDE



- Test beam performed using ALPIDE telescopes, central chip is treated as device under test (DUT)
- Calculated resolution at DUT around 2-3 µm
- Studied performance in terms of: detection efficiency, position resolution, cluster sizes and shapes
  - plus corresponding lab measurements of fake-hit rate, threshold (s-curve scan)

Reverse substrate bias dependence

Detection efficiency and fake-hit rate

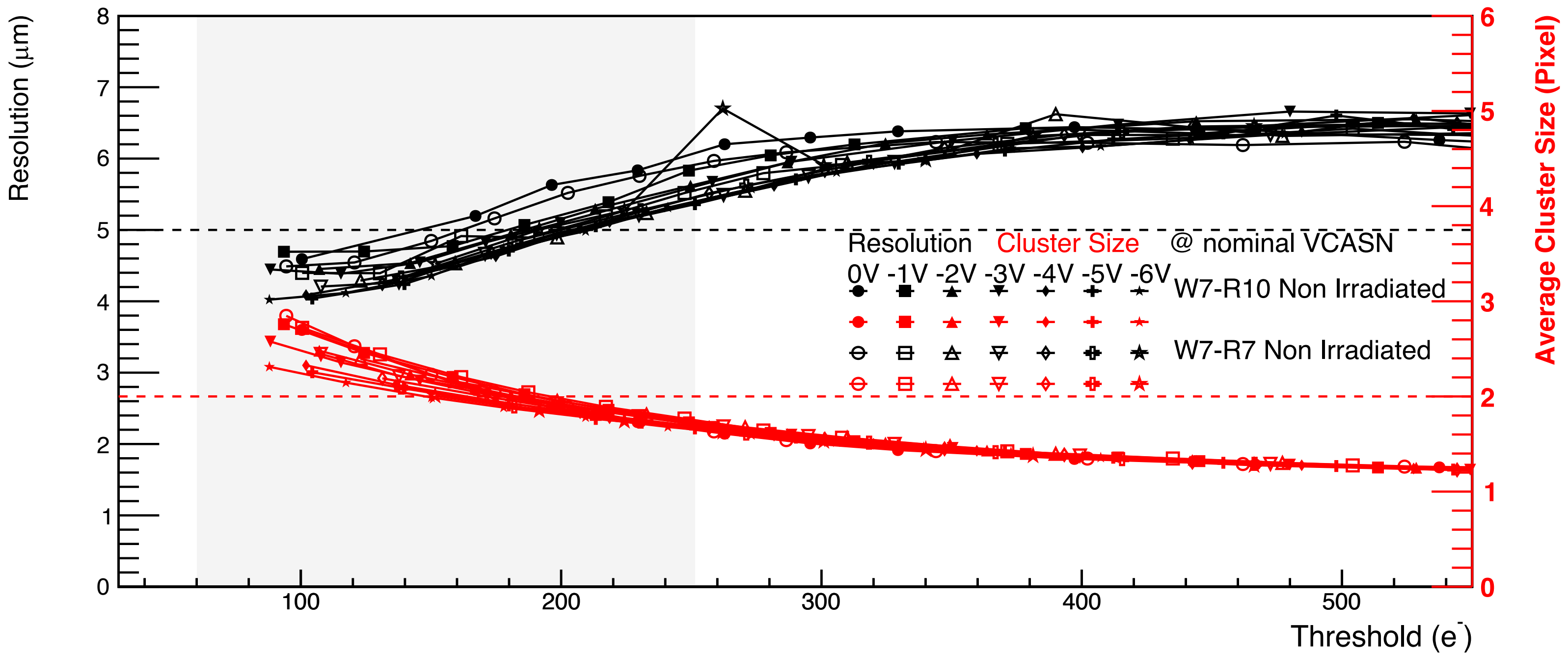


- Detection efficiency stays at 100% - ε over wide range of thresholds
  - Chip-to-chip fluctuations negligible
- Clear ordering: increasing performance with larger reverse substrate bias
  - Most significant improvement from 0V to -1V
- Extremely low fake-hit rate
  - Below measurement limit of 10^{-11}/pixel/event after masking 10 pixels (1/50 000), only increased for -6V

Reverse substrate bias dependence

2. ALPIDE

Position resolution and cluster size

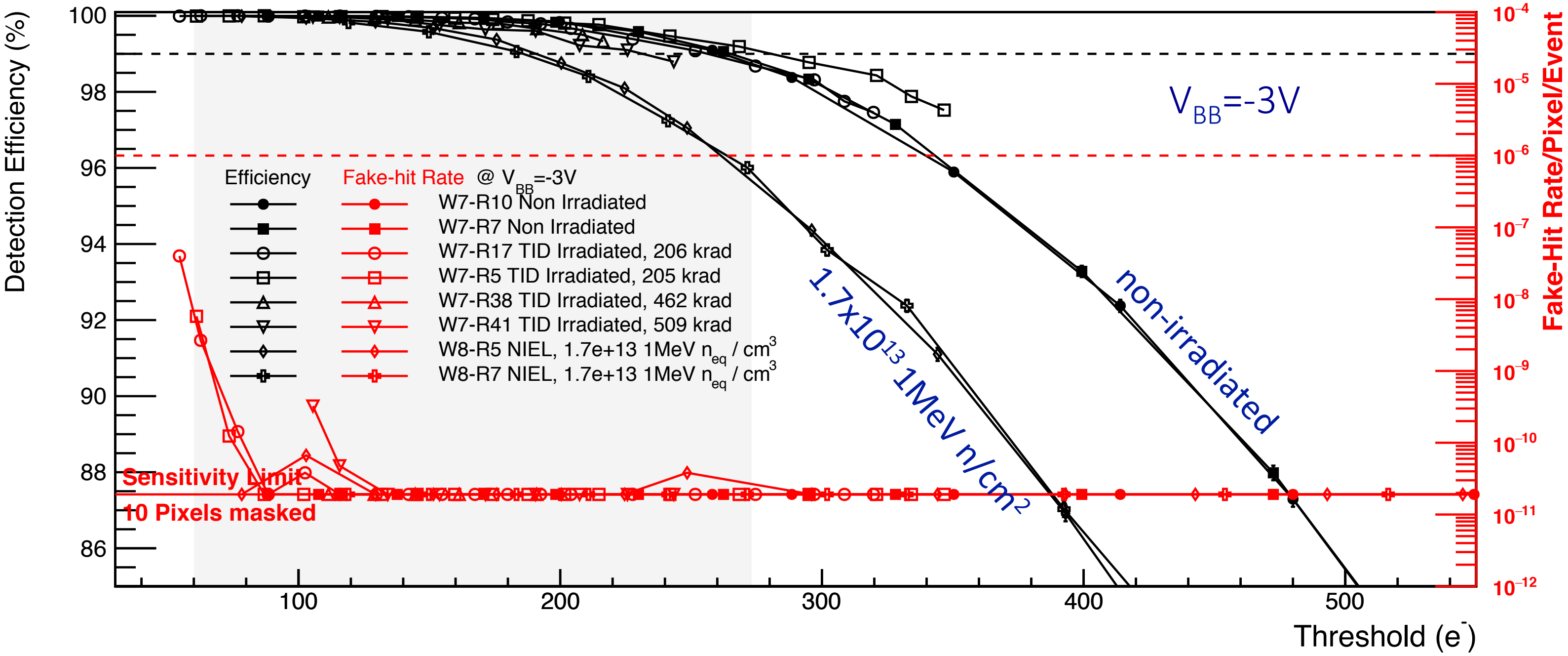


- Average cluster sizes vary between 1 and 3 pixels (for MIPs)
- Position resolution around desired 5µm in threshold range with detection efficiency > 99%
  - Biggest improvement from 0V to -1V
  - Little dependence on reverse substrate bias from -2V to -6V

NIEL irradiation

2. ALPIDE

Detection efficiency and fake-hit rate

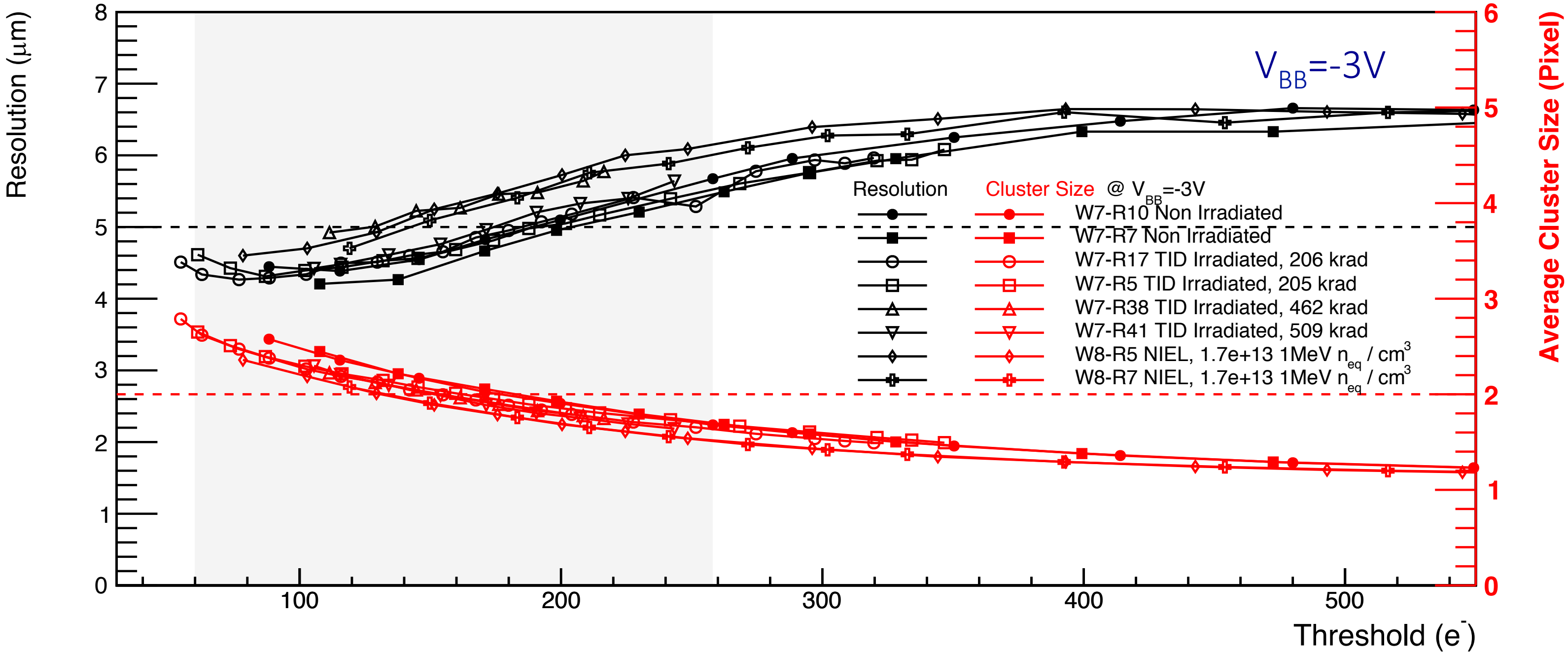


- Sufficient operational margin after 1.7x10^{13} 1MeV n/cm^2 (10 times life time dose of upgraded ITS)

NIEL irradiation

2. ALPIDE

Position resolution and cluster size



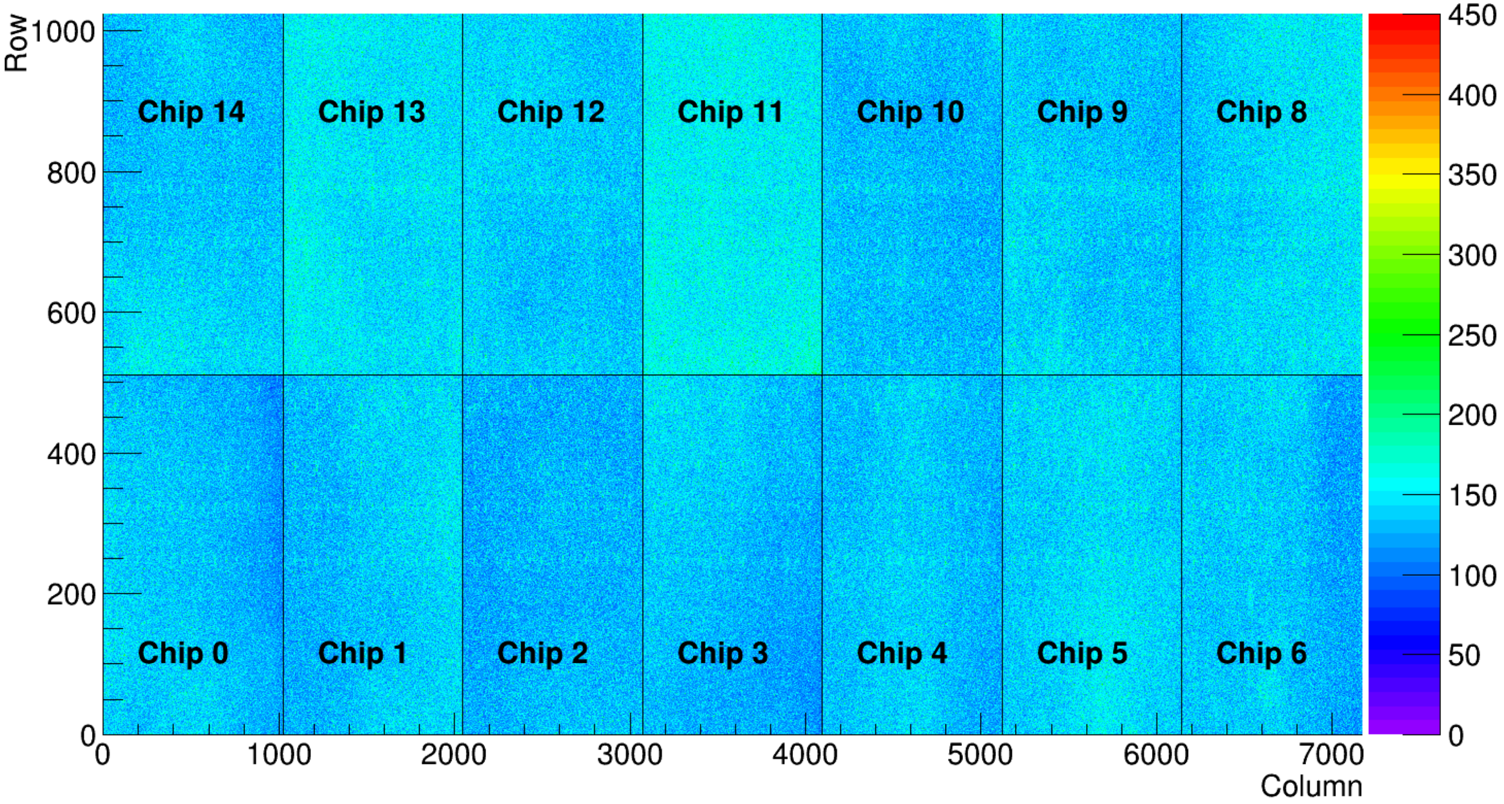
- Cluster sizes and position resolution slightly reduced after 1.7×10^{13} 1MeV n/cm^2 (10 times life time dose of upgraded ITS)
  - Resolution remains around desired 5μm in threshold range with detection efficiency > 99%

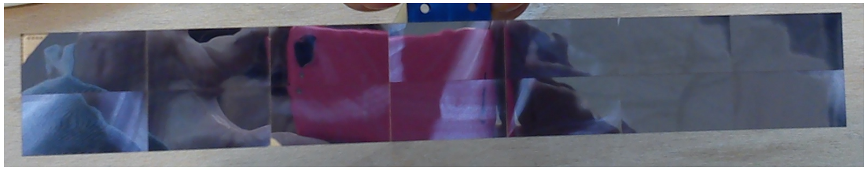
ALPIDE in module assemblies

2. ALPIDE

Example: threshold scan at nominal setting on OB module (HIC – hybrid integrated circuit)

-



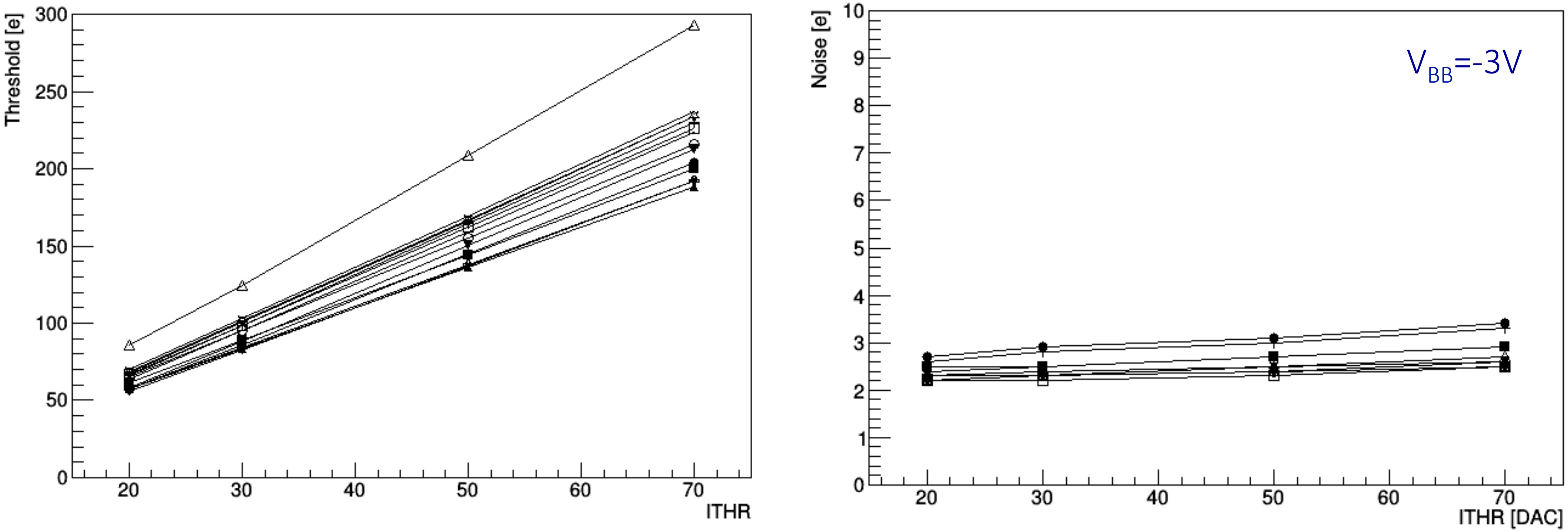


14 ALPIDE chips connected to flexible PCB

ALPIDE in module assemblies

2. ALPIDE

Example: threshold vs ITHR DAC setting for all 14 chips on OB module



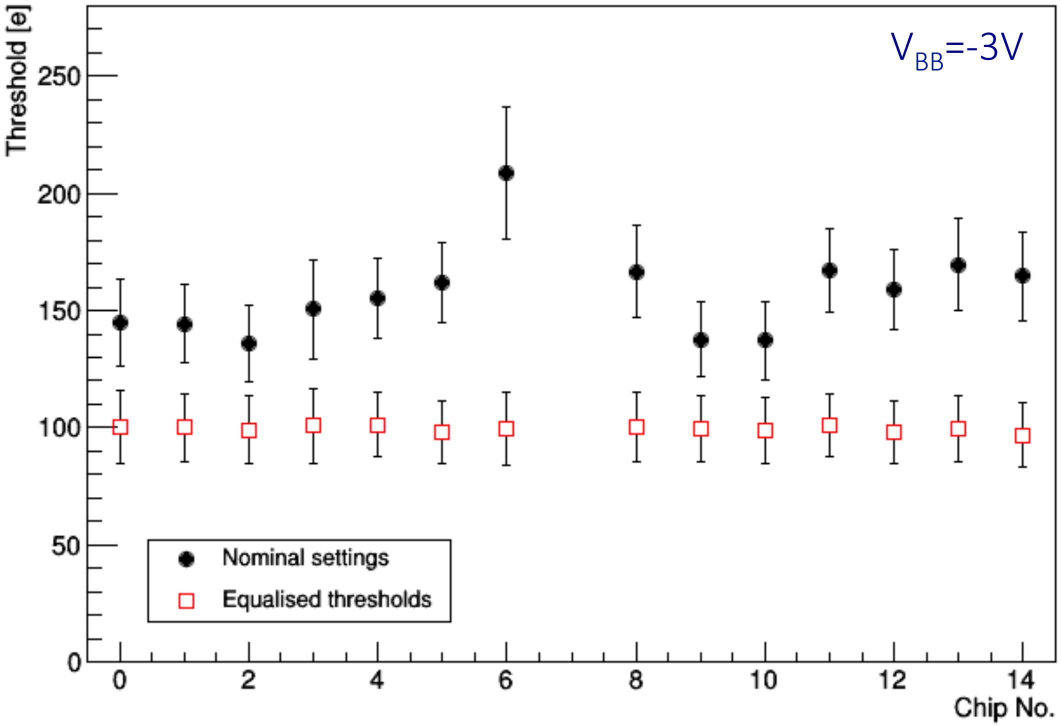
Behavior comparable to single chips

- Threshold RMS 10% - 15% of average threshold
- Noise 2-3e^-

ALPIDE in module assemblies

2. ALPIDE

Threshold equalization



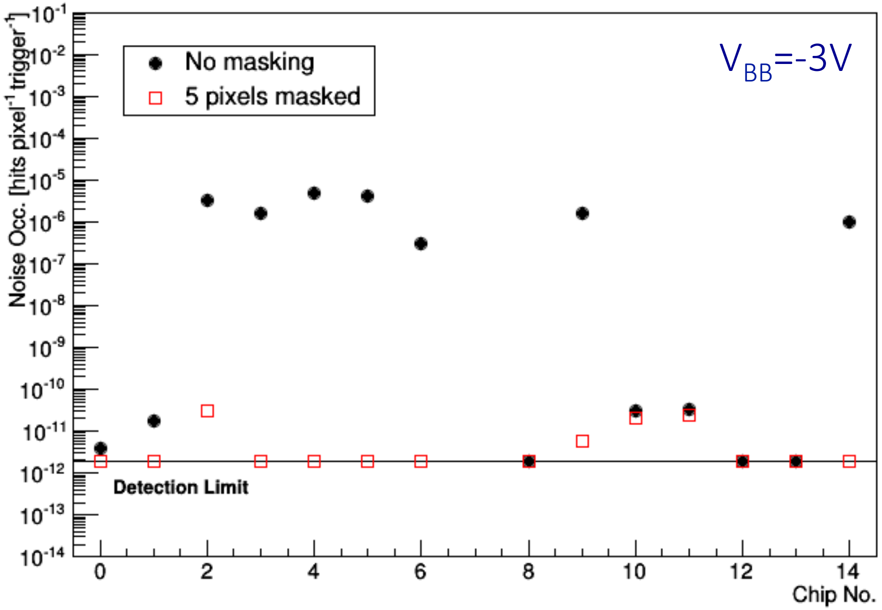
- Tuned thresholds
  - Use ITHR DAC to equalize thresholds between chips
  - Here: OB module at nominal settings and tuned to 100 e^-
    ITHR settings determined from linear fit to threshold-vs-ITHR curves

ALPIDE in module assemblies

2. ALPIDE

Fake-hit rate from data taking with random triggers (OB module)

- Fake-hit rate in OB HIC for all 14 chips without masking and with masking 5 pixels per chip (1 / 100000)
- -3V reverse substrate bias, low threshold (ITHR = 20, threshold 50 – 70 e$^-$)



Behavior comparable to single chips

- Fake-hit rate < 10^{-10} with 5 masked pixels (1/100 000)

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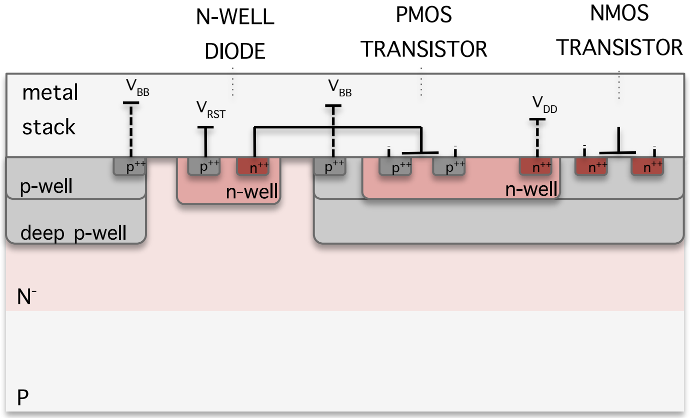


Development monolithic CMOS pixel sensors

3. Future developments

State of the art of monolithic CMOS pixel sensors at start of pixel chip R&D for the ITS upgrade end 2011

ALPIDE development,
First application at LHC

Parameter	Ultimate at STAR	ALPIDE
Silicon thickness	50µm	50µm
Spatial resolution	~4µm	~5µm
Power density	150mW/cm^2	< 40mW/cm^2
Event time resolution	185.6µs	~2µs
Detection efficiency	> 99%	> 99%
Fake hit rate	< 10^{-4}/event/pixel	<<< 10^{-6}/event/pixel
NIEL radiation tolerance	3x10^{12} 1MeV n_{eq}/cm^2	>1.7x10^{13} 1MeV n_{eq}/cm^2

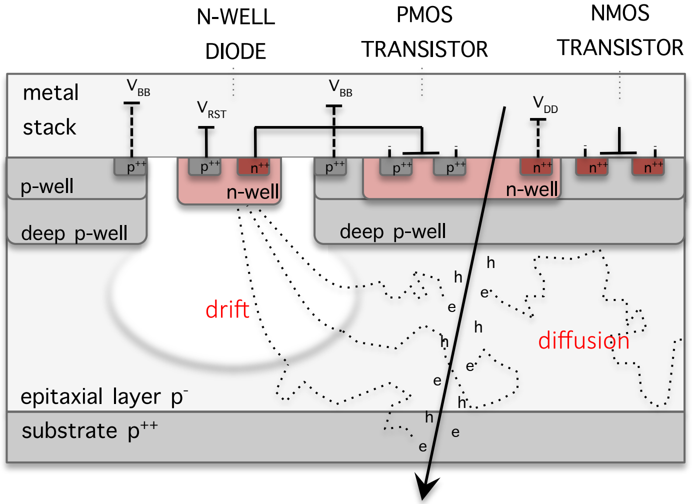
Application of monolithic CMOS pixel sensors in more demanding environments?

- ALPIDE fulfills or surpasses pixel-chip requirements of the ALICE ITS upgrade
- ALPIDE development represents significant advancement regarding power density, fake-hit rate, readout speed, and radiation hardness
- Application of monolithic CMOS pixel sensors in more demanding environments requires increased radiation tolerance and better timing resolution required

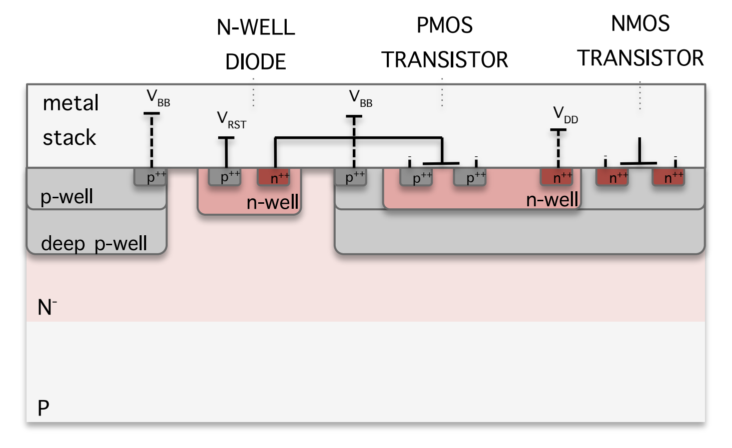
Process modification for enhanced depletion

3. Future developments

Standard TowerJazz CIS process



Recent process modification (CERN –TJ):



- Developed in collaboration with foundry to achieve enhanced (full?) depletion, while retaining extremely low input capacitances
- Planar deep N^- - P junction
- Does not require significant circuit or layout changes ➔ same design can be fabricated in both std and mod process
- Prototypes processed using pALPIDE-2 mask set
- Note: not used for ALICE ITS upgrade

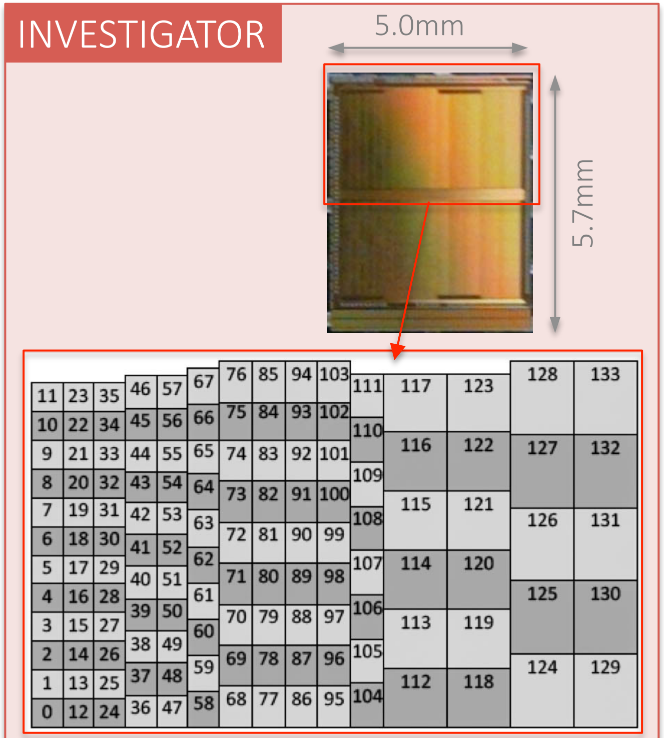
Test chip: INVESTIGATOR

3. Future developments

- INVESTIGATOR: dedicated test chip developed within ALPIDE R&D phase, designed for systematic studies on influence of design parameters on sensor characteristics
- Consists of 134 matrices of 8x8 pixels ("mini-matrices", MM)
    - Various pixel sizes (20x20µm^2 to 50x50µm^2) and collection electrode designs (n-well size, spacing)
- Each of the mini-matrices can be selected and connected to a set of 64 output buffers (~10ns rise time)
    - All 64 pixels of a mini-matrix can be read out in parallel, allowing for continuous parallel signal sampling
    - Possibility of measuring evolution of a cluster, i.e. charge collection time in each pixel
    - Dedicated 64-channel readout system developed, sampling at 65MHz

✓ Chips produced on different wafers with epi-layer thickness between 18µm and 30µm, and in different process variants (std, mod)

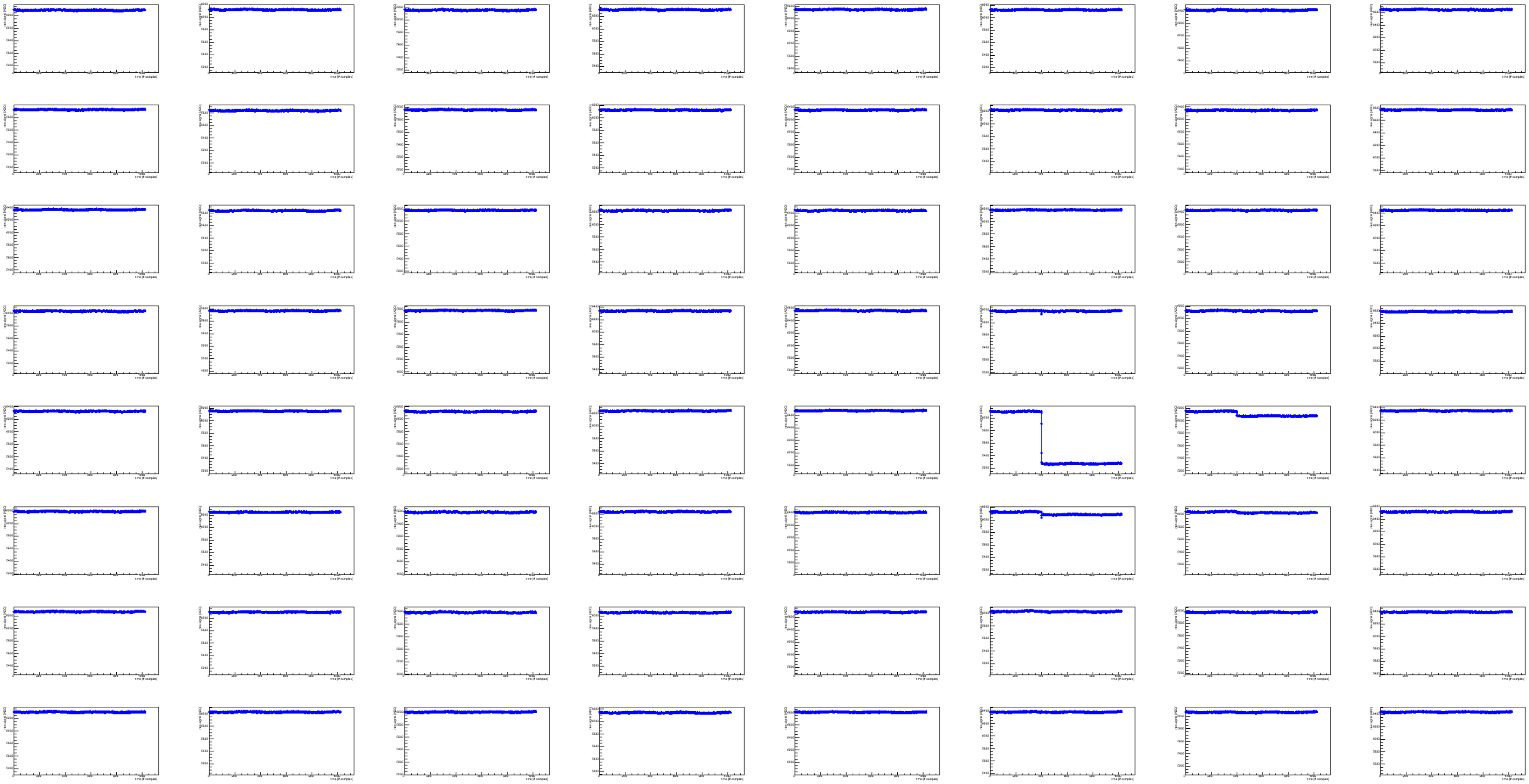
- ✓ Samples tested up to 10^{15} 1MeV n_{eq}/cm^2 and 1Mrad



MM address	Pixel pitch [µm]	Number of MM (per pitch)
0 - 35	20	36
36 - 57	22	22
58 - 67	25	10
68 - 103	28	36
104 - 111	30	8
112 – 123	40	12
123 - 134	50	10

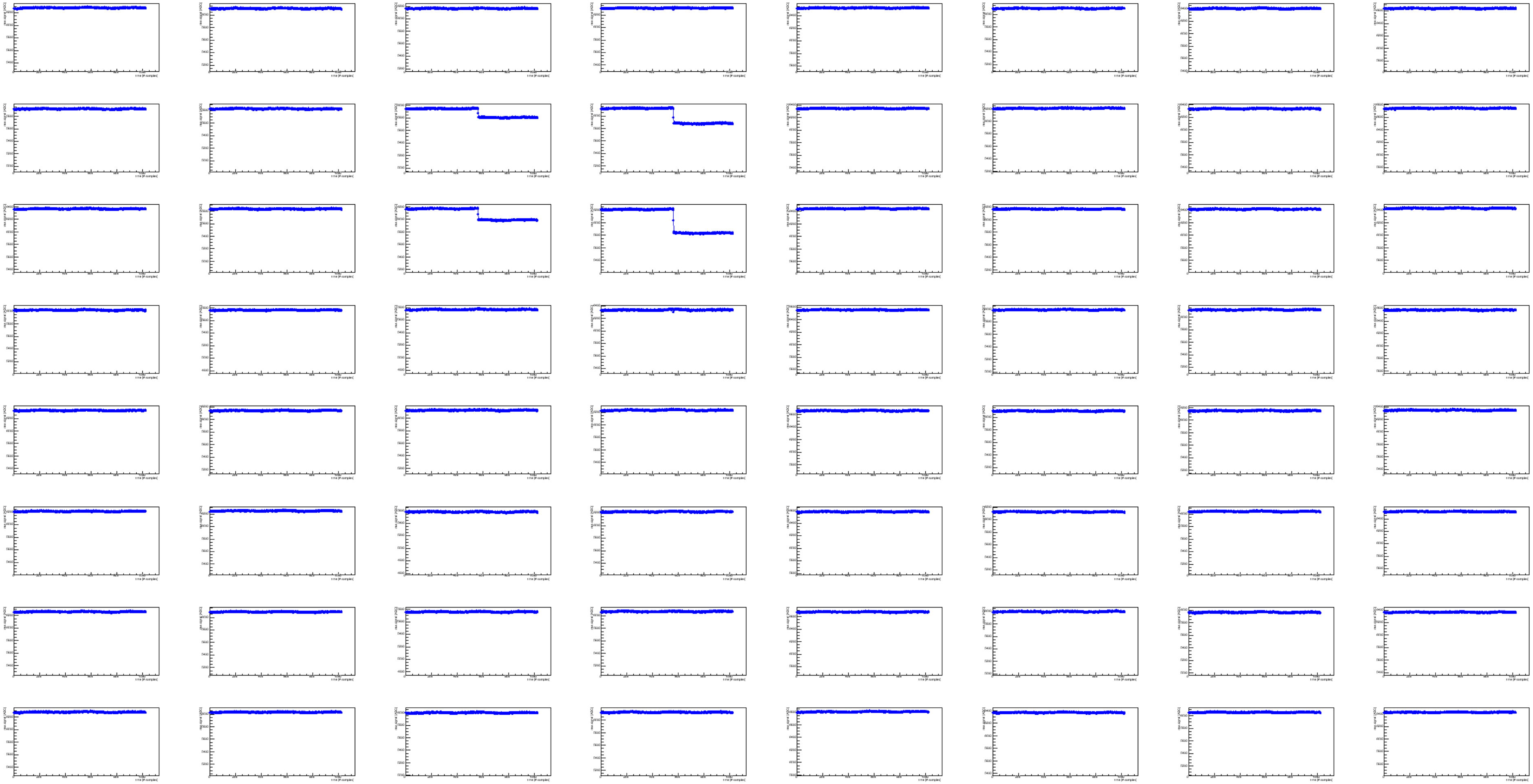
INVESTIGATOR – waveform-event display for all 64 pixels

3. Future developments



INVESTIGATOR – waveform-event display for all 64 pixels

3. Future developments



Charge-collection time

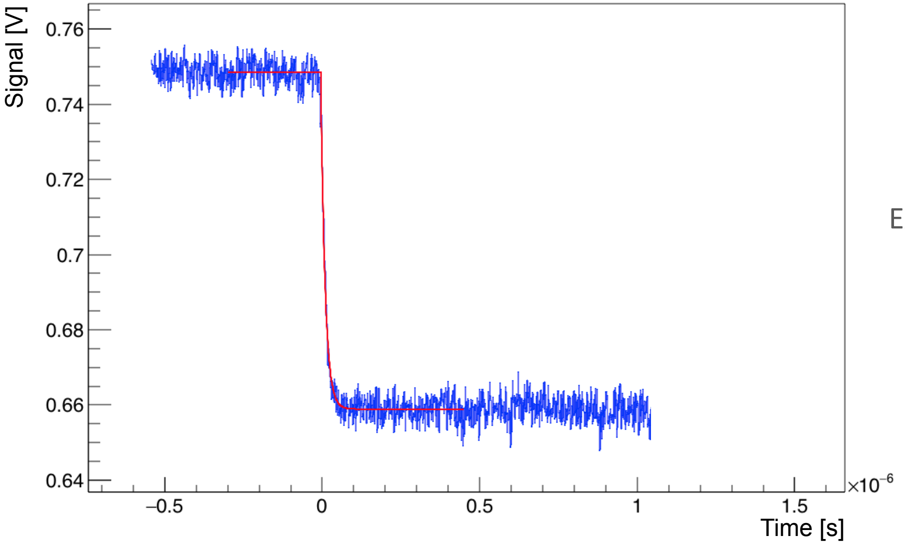
3. Future developments

- Precise charge-collection time measurements performed using differential probe and fast scope on single pixel

- Fit of waveforms with function:

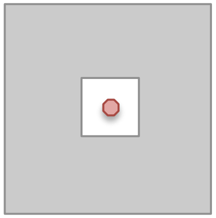
$$t \le t_0 \qquad f = a + m \cdot (t - t_0)$$

$$t > t_0 \qquad f = a + m \cdot (t - t_0) - b \cdot \left(e^{-\frac{t - t_0}{\tau}} - 1\right)$$



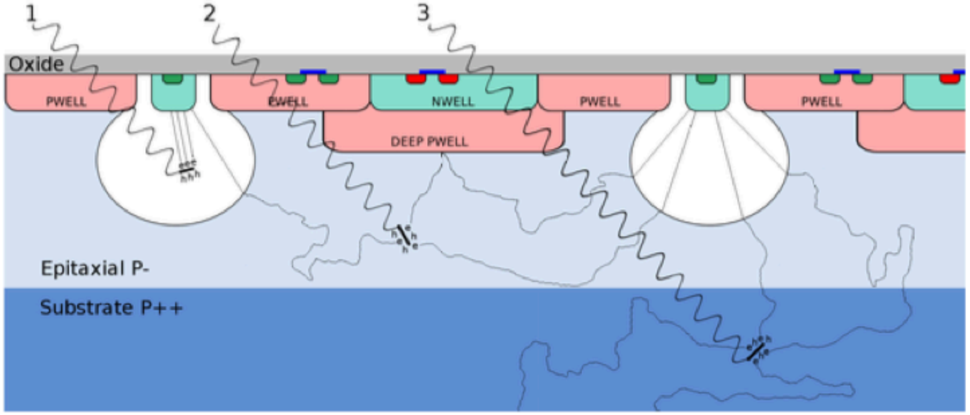
Example waveform and fit

- ALPIDE-like pixel studied: 28µm pitch, 2um n-well diameter, 3µm spacing, 25µm epi
- Measurements performed with ^{55}Fe



Charge-collection time measurements with X-Rays

3. Future developments

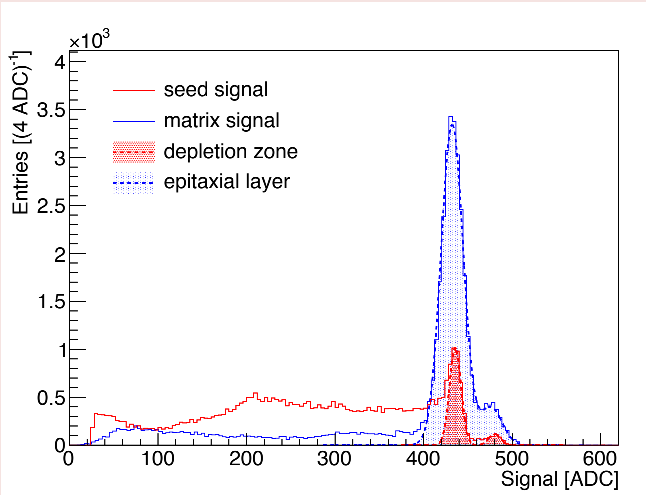


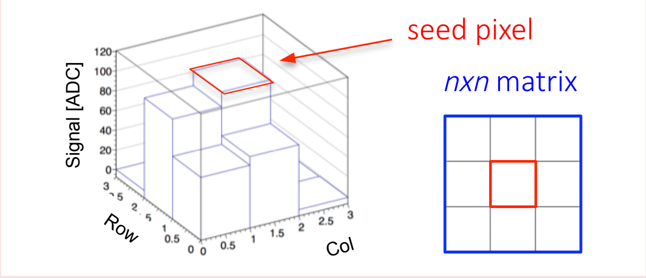
^{55}Fe: two X-Ray emission modes:

1. K-α: 5.9keV (1640e/h in Si), relative frequency: 89.5%
   attenuation length in Si: 29µm
2. K-β: 6.5keV (1800e/h in Si), relative frequency: 10.5%
   attenuation length in Si: 37µm

For X-Ray absorption in sensor fabricated with the std process three cases can be defined:

1. Absorption in depletion volume: charge collected by drift, no charge sharing, single pixel clusters
   - Events of this case populate the calibration (K-α) peak in signal histogram
   - Charge collection time expected to be ≈ 1ns
2. Absorption in epitaxial layer: charge partially collected by diffusion and then drift, charge sharing between pixels depending on position of X-Ray absorption
   - Charge collection time expected to be dependent on distance of the X-Ray absorption from a depletion volume, and longer than for events of case 1
3. Absorption in substrate:
   - contribution depending on depth of X-Ray absorption position within substrate, and charge carrier lifetime within substrate

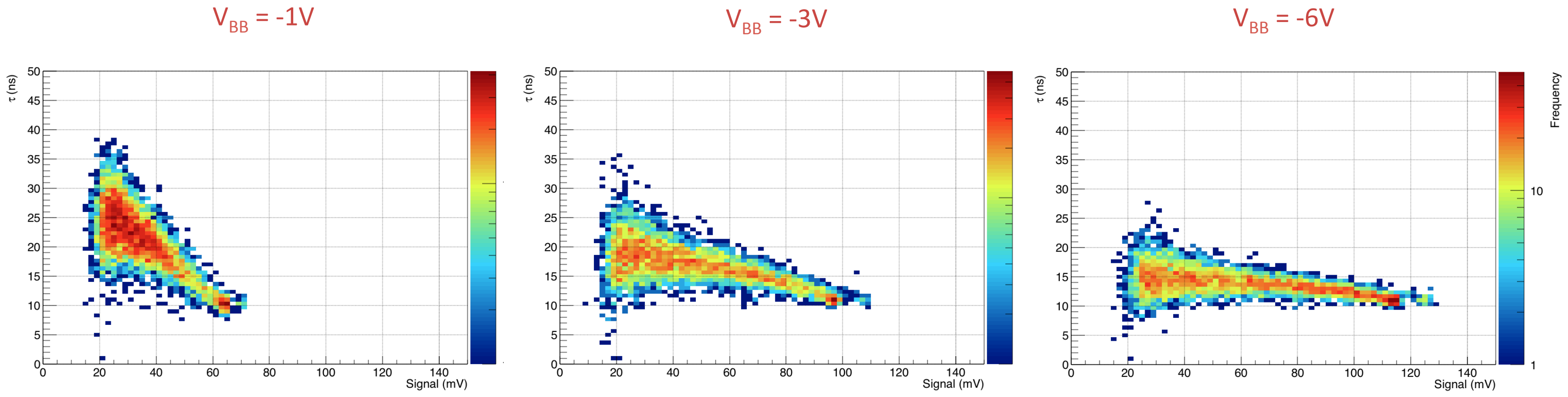




Charge-collection time - Standard process

3. Future developments

MM75: 28µm pitch, 2um n-well diameter, 3µm spacing, 25µm epi



V_{BB} = -1V

V_{BB} = -3V

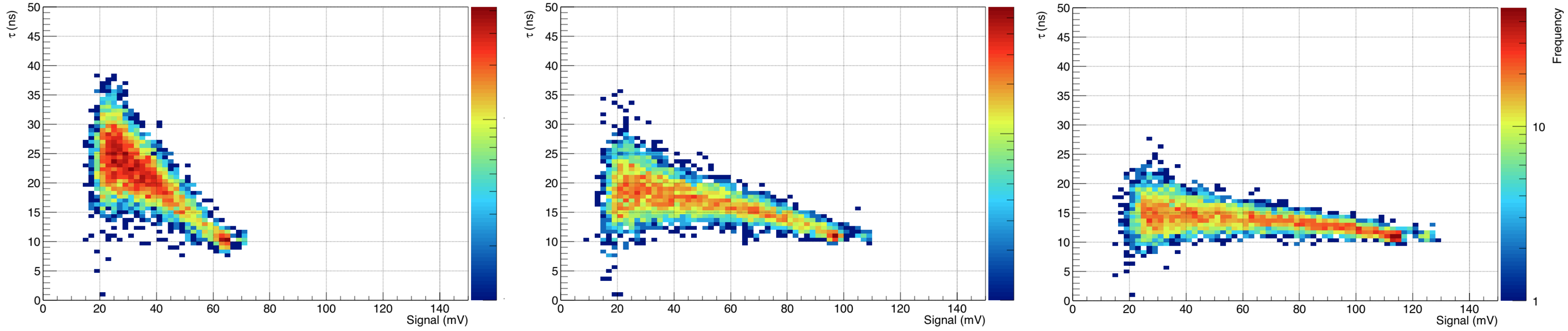
V_{BB} = -6V

Charge-collection time - Standard process

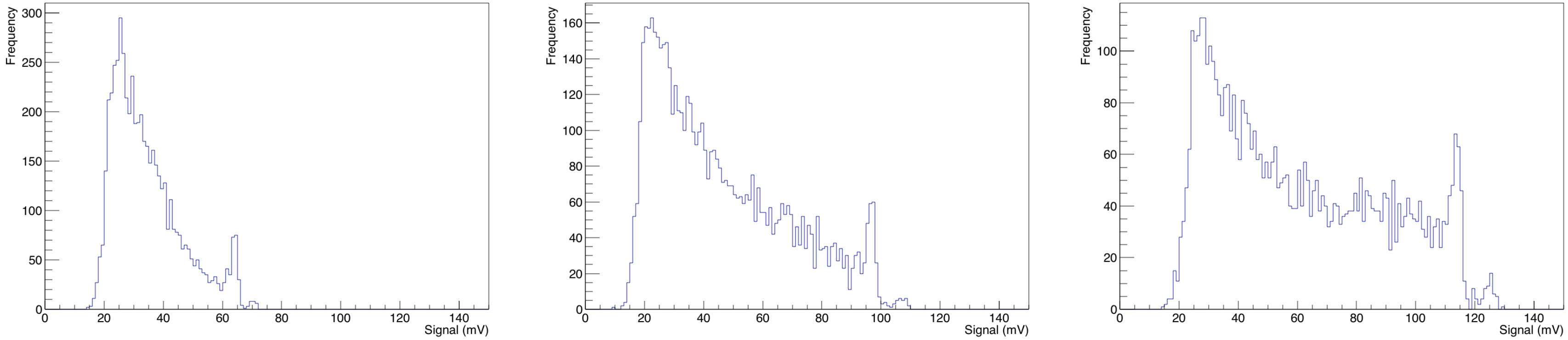
3. Future developments

MM75: 28µm pitch, 2um n-well diameter, 3µm spacing, 25µm epi

V_{BB} = -1V V_{BB} = -3V V_{BB} = -6V



Signal:

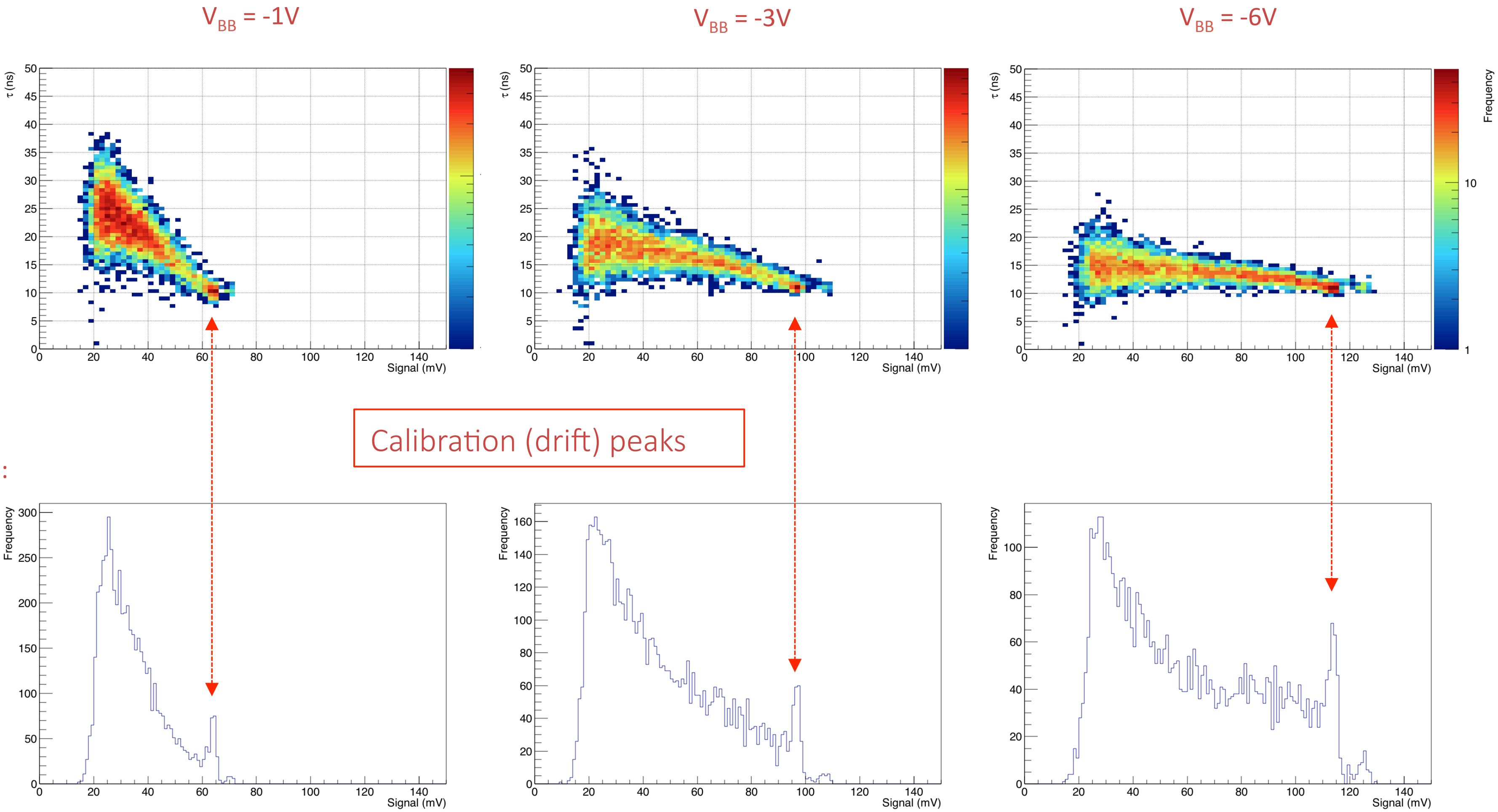


Charge-collection time - Standard process

3. Future developments

MM75: 28µm pitch, 2um n-well diameter, 3µm spacing, 25µm epi

Signal:



V_{BB} = -1V

V_{BB} = -3V

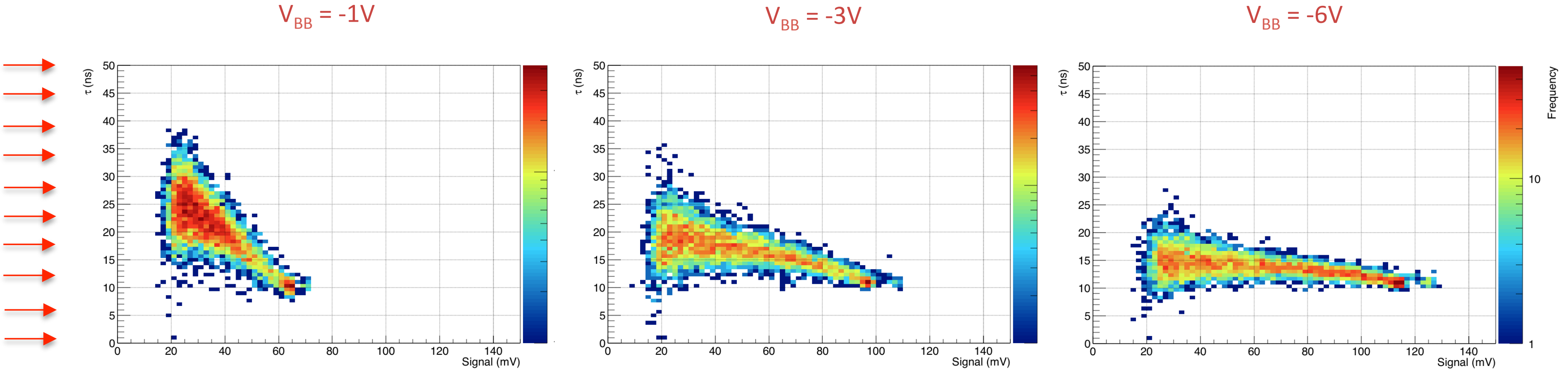
V_{BB} = -6V

Calibration (drift) peaks

Charge-collection time - Standard process

3. Future developments

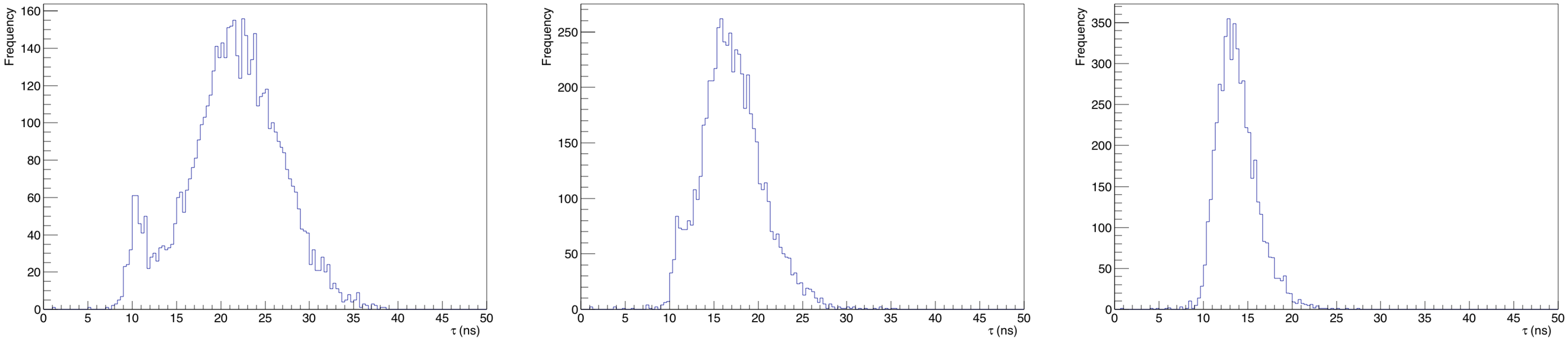
MM75: 28µm pitch, 2um n-well diameter, 3µm spacing, 25µm epi


V_{BB} = -1V

V_{BB} = -3V

V_{BB} = -6V

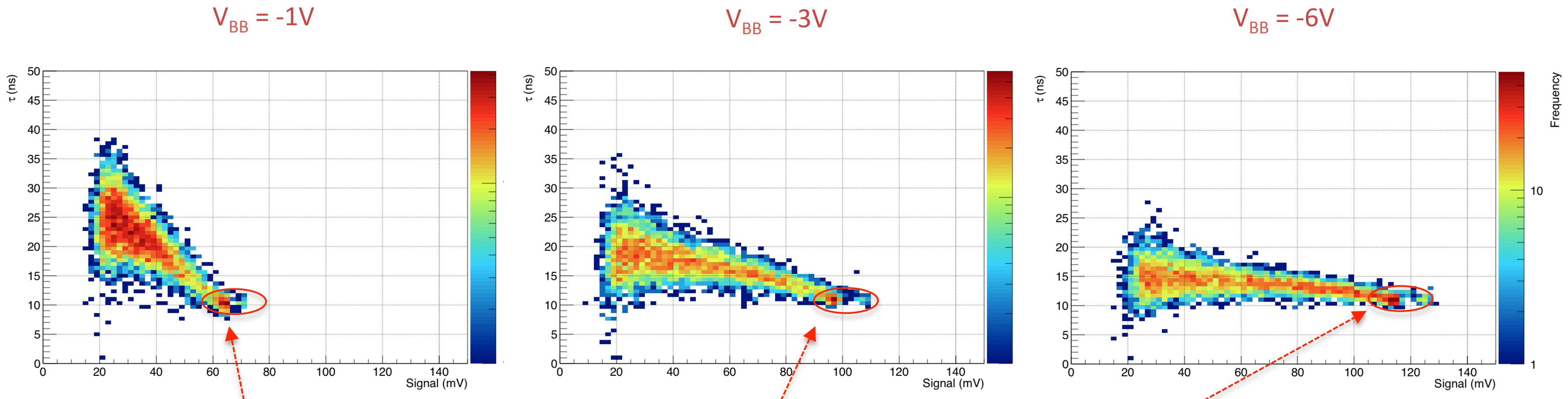
Rise time (τ):



Charge-collection time - Standard process

3. Future developments

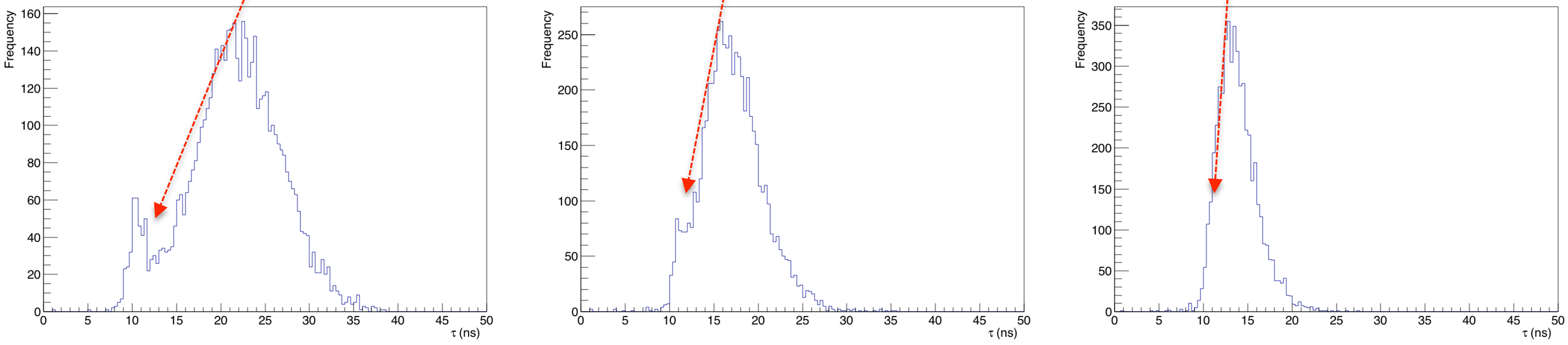
MM75: 28µm pitch, 2um n-well diameter, 3µm spacing, 25µm epi


V_{BB} = -1V
V_{BB} = -3V
V_{BB} = -6V

Calibration (drift) peak: no charge sharing, signal collected by drift (in <= 1ns)

- Rise time about equal for all all values of $V_{BB,}$ moreover about equal to buffer rise time
- Drift peak clearly visible in low-V_{BB} rise time histograms, for larger V_{BB} it overlaps with diffusion-drift peak

Rise time (τ):



Charge-collection time - Standard process

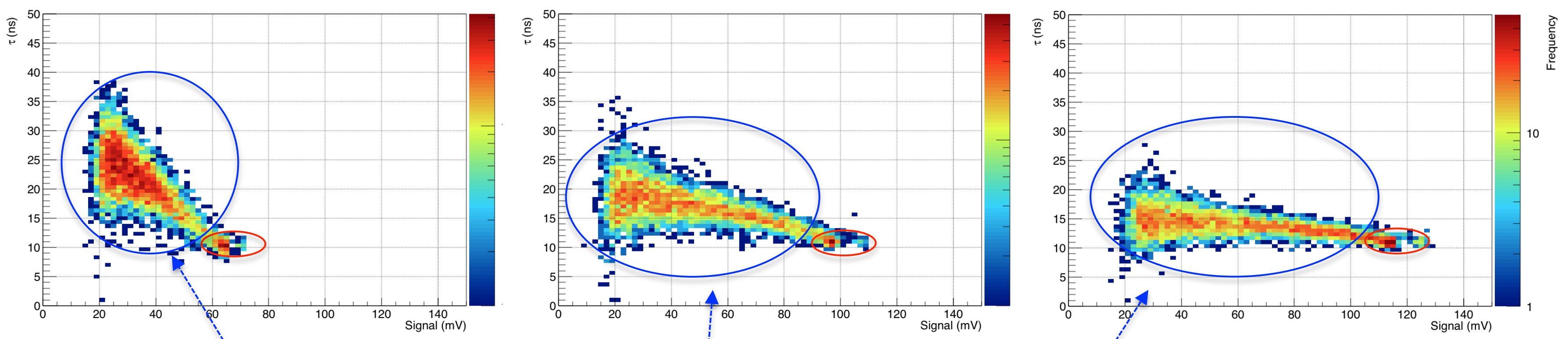
3. Future developments

MM75: 28µm pitch, 2um n-well diameter, 3µm spacing, 25µm epi

V_{BB} = -1V

V_{BB} = -3V

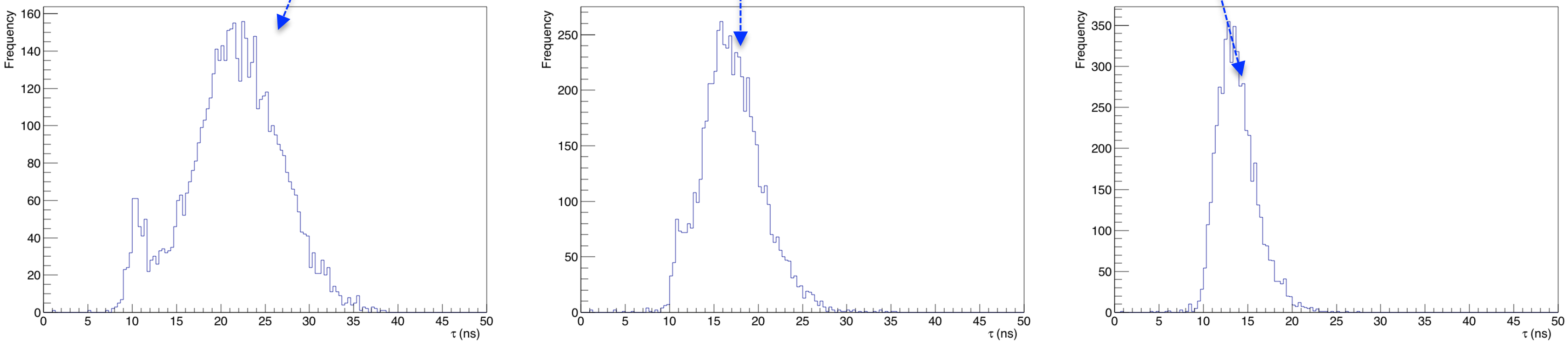
V_{BB} = -6V



Charge sharing – signal collected partly by diffusion and then drift

- Larger rise times with decreasing signal clearly visible in low-V_{BB} measurements
- Less clear in high-V_{BB} measurements (larger depletion volumes)

Rise time (τ):



Charge-collection time - Modified process

3. Future developments

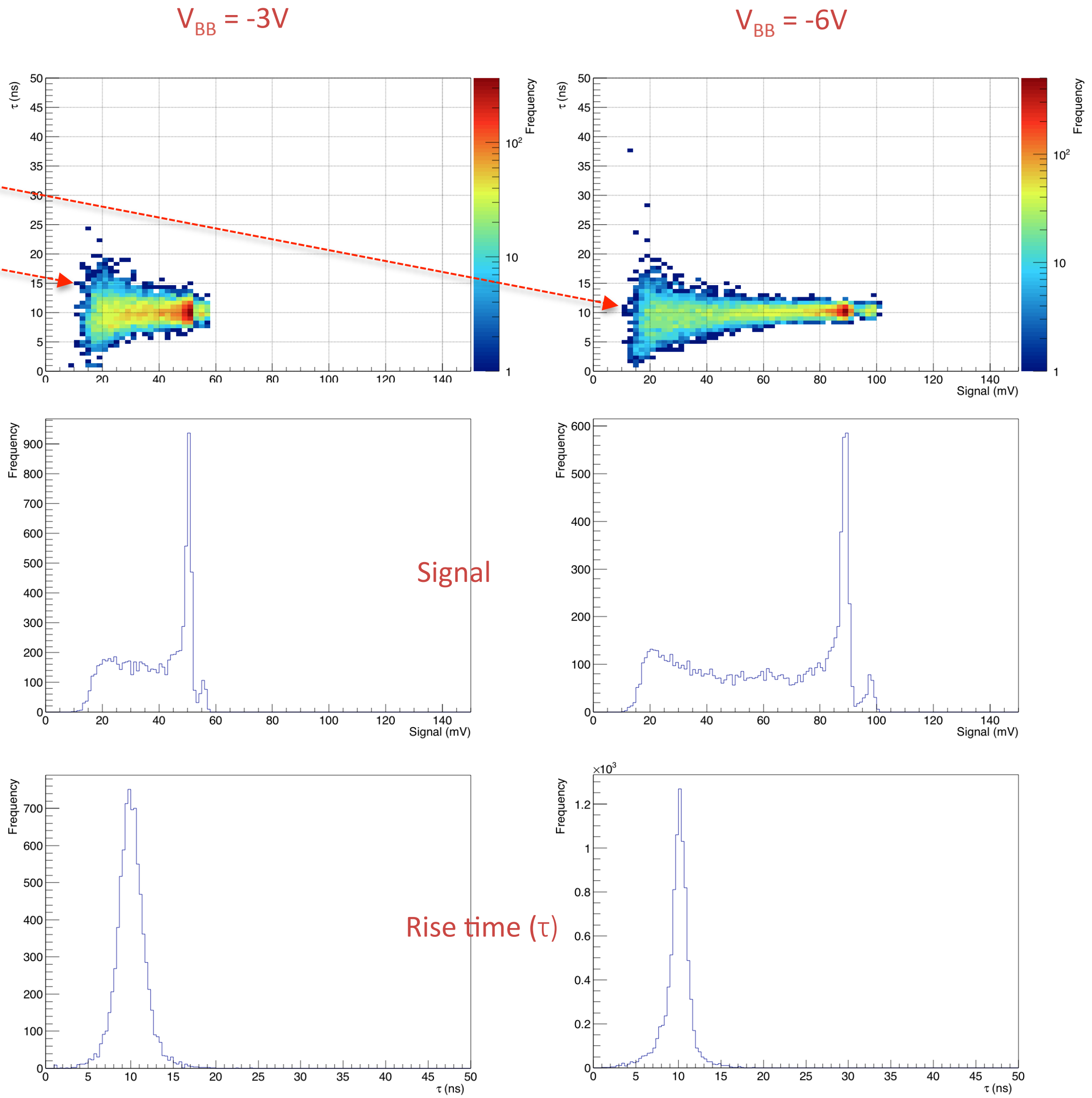
MM75: 28µm pitch, 2um n-well diameter, 3µm spacing, 25µm epi

- For modified process, otherwise same pixel (geometry) no change in rise time between events with or without charge sharing

  ➔ charge collected purely by drift

- No change in signal rise times between -3V and -6V V_{BB}, only in signal (capacitance C)

- Signal rise time about equal to the one for drift peak in the std process



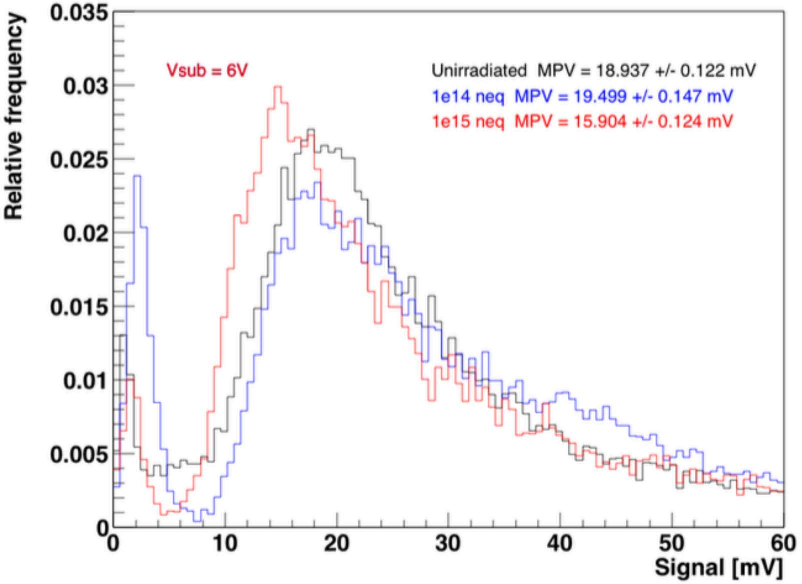
Charge-collection and signal rise time at up to 1x10^{15} 1MeV n$_{eq}$/cm^{2}

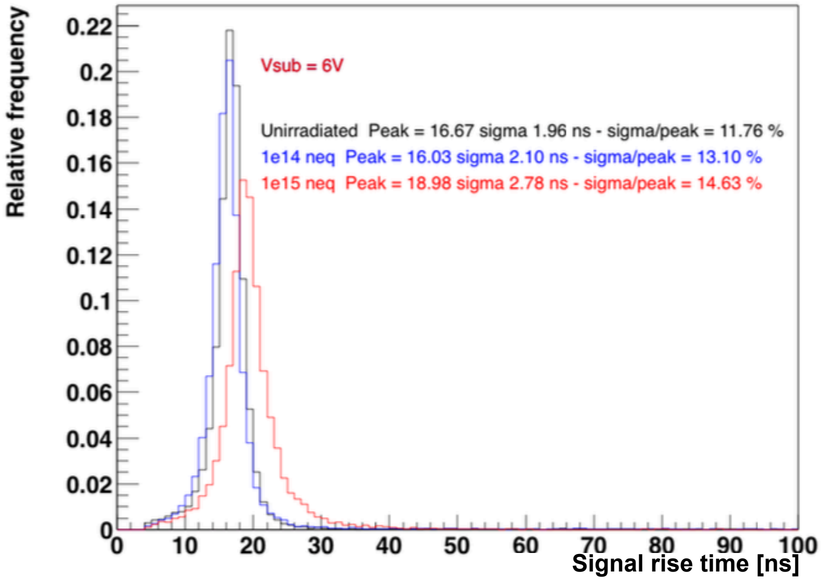
3. Future developments

^{90}Sr measurements on modified-process samples (different setup, different pixel w.r.t. before)

- Non-irradiated
- 1x10^{14} 1MeV n$_{eq}$/cm^{2} (NIEL) and 100krad (TID)
- 1x10^{15} 1MeV n$_{eq}$/cm^{2} (NIEL) and 1Mrad (TID)

MM129: 50µm pitch, 3um n-well diameter, 18.5µm spacing, 25µm epi





Courtesy of H. Pernegger, C. Riegel et al. (ATLAS)

- Little change to signal after irradiation, signal well separated from noise
  - Note: standard process no longer working after 1x10^{15} 1MeV n$_{eq}$/cm^{2}
- Recent test beam measurements show no change of efficiency after 1x10^{15} 1MeV n$_{eq}$/cm^{2}

Outline

1. Introduction
   - Present ALICE detector and upgrade plans
   - Upgrade of the ALICE Inner Tracking System (ITS)

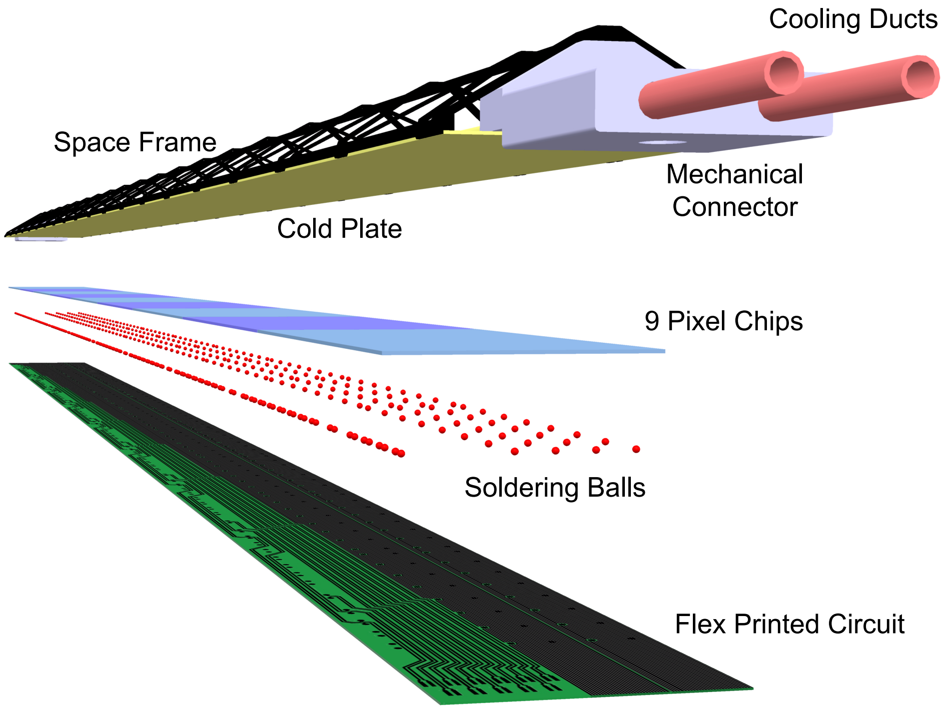
2. ALPIDE
   - Concept
   - Key results

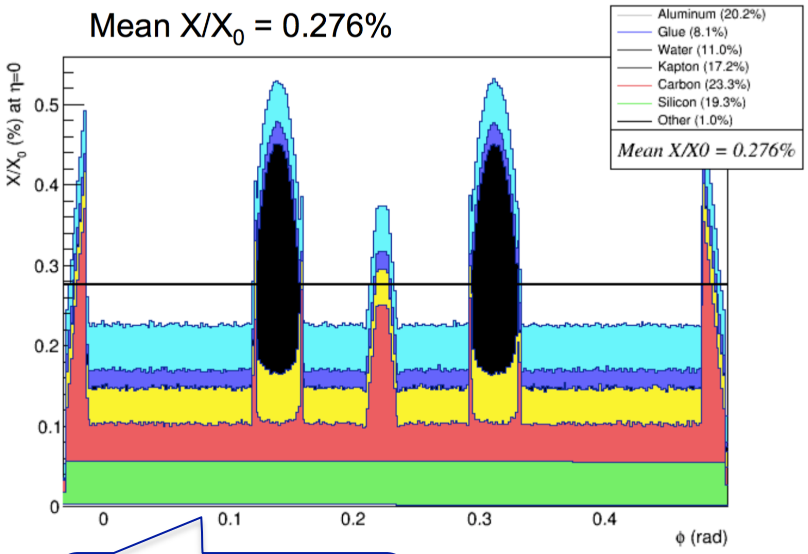
3. Future developments
   - Process modifications for enhanced depletion
   - Silicon-only vertex detector?

4. Summary

What’s up next? Ultra-light “silicon-only” vertex detector

3. Future developments





Sensor only amounts to 20% of total x/X_0

How to further reduce material thickness?

- eliminate active cooling: for a 30cm long stave possible for power densities below 20mW/cm^2
- eliminate electrical substrate (flexible FPCs): possible if power density is sufficiently low (voltage drops on supply and biasing) and the (monolithic) sensor covers the full stave length

ALPIDE Chip: pixel matrix power density ~7mW/cm^2, the rest is dissipated in the periphery!

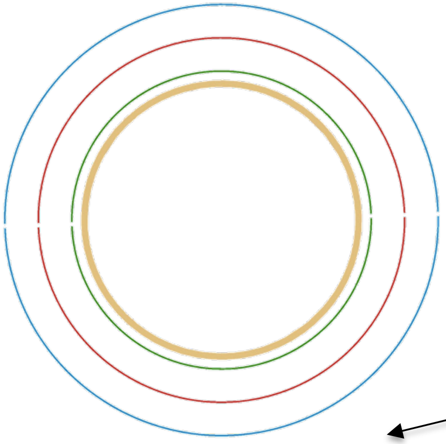
➔ Can the circuit periphery be put at the periphery of the detector?

Silicon-only vertex detector study for ALICE

3. Future developments

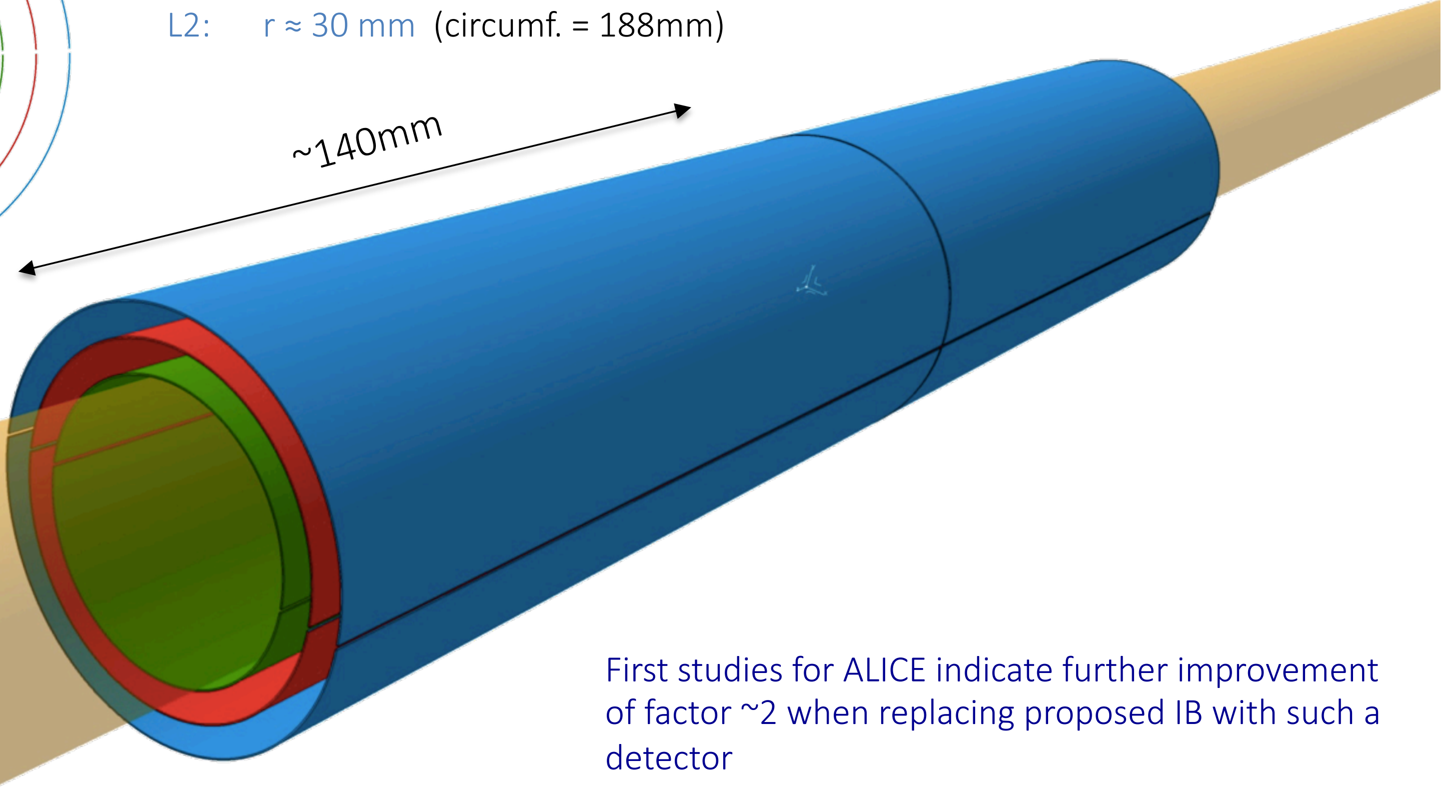
One layer built out of 4 pixel chips, with periphery at outside edge:

- chip dimensions: 140 x 56 (94) mm^2 -> fits on 200mm wafer!



Layer 0, 1, 2

L0:	r ≈ 18mm	(circumf. = 113mm)
L1:	r ≈ 24mm	(circumf. = 151mm)
L2:	r ≈ 30 mm	(circumf. = 188mm)



Beam pipe r = 16mm

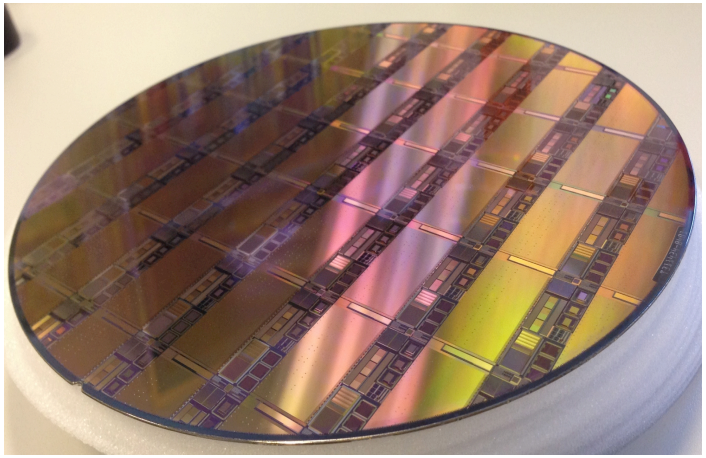
First studies for ALICE indicate further improvement of factor ~2 when replacing proposed IB with such a detector

Limits of dimensions of a CMOS chip?

3. Future developments

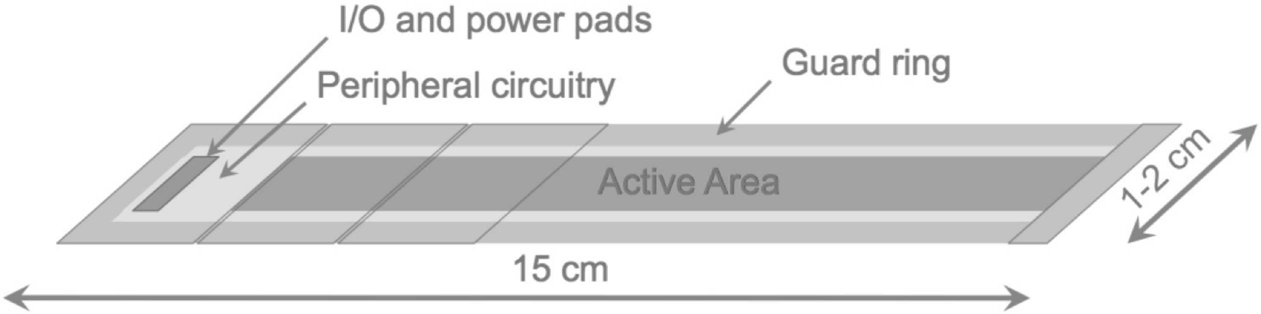
Limit: reticle mask

- typically of the order of 2 x 2 cm^2
- IC industry demands small-size reticles for fabrication yield and to facilitate system integration
- for chips larger than reticle size -> stitching



Stitching: allows building circuits as large as the entire wafers

- Stitching is combining part of the reticle to obtain a chip with an area larger than the reticle (e.g. done for large professional CCDs)
- Example in one dimension:



- All connections to the exterior on one side
- All routing using on-chip metal layers, all functions integrated

Outline

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4. Summary

Summary

4. Summary

- New ALICE ITS with 7 layers of Monolithic Active Pixel Sensor (MAPS) will be installed during LS2 of the LHC in 2019/2020

- A dedicated monolithic pixel chip – the ALPIDE – has been developed
    - Represents significant advancement of the technology of MAPS regarding power consumption, readout speed, charge collection time and radiation hardness
    - Results from ALPIDEs in module assemblies comparable to results from single chips
    - ✓ Production Readiness Review (PRR) in November 2016 -> got go ahead for production

- With the modified process, a dependency of the signal rise time on the relative signal is no longer observed, while retaining the very low pixel-input capacitances already achieved
    - Charge collected purely via drift
    - Very low pixel-input capacitances already achieved are retained
    - Good results sparked interest of several other groups (ATLAS, CLIC)
    - Recent test beam measurements show no change of efficiency after 1×10^{15} 1MeV n_{eq}/cm^2

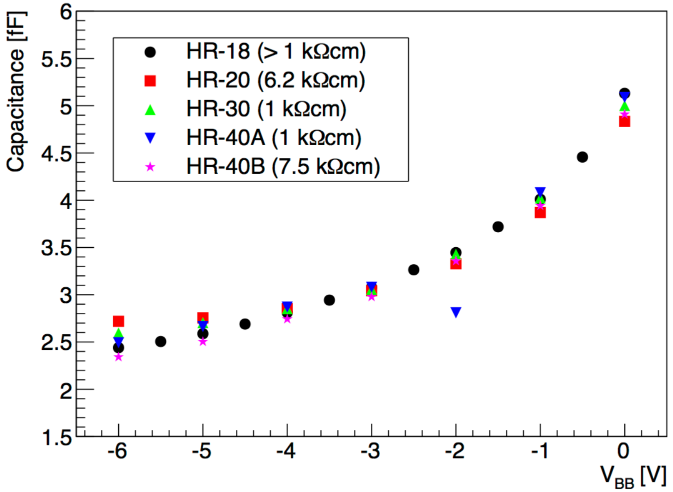
- Next step – “Silicon-only” vertex detector?
    - Technology to produce large CMOS sensors already existing
    - Yet to be verified: minimum bending radii for very thin CMOS wafers

BACKUP

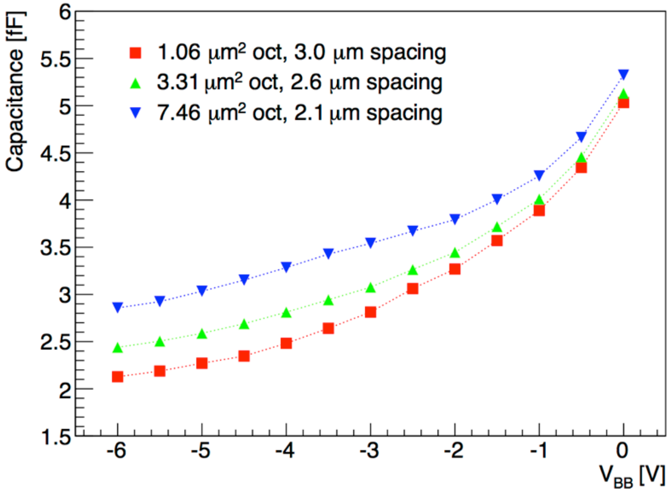
Sensor optimization – Pixel-input capacitance

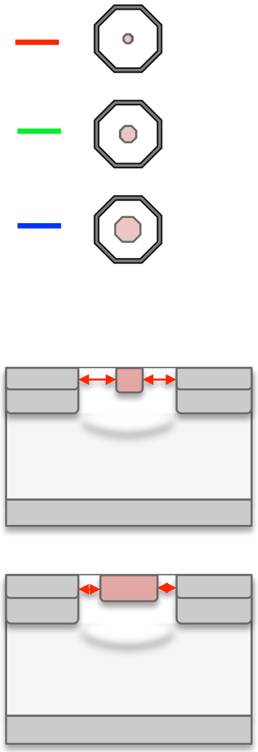
2. ALPIDE

Epitaxial layer resistivity



Collection diode geometries:





Pixel input capacitance significantly decreased with increasing $|V_{BB}|$

- ~5fF for V_{BB}=0V ➔ ~2.5fF for V_{BB}=-6V

Epitaxial layer resistivity

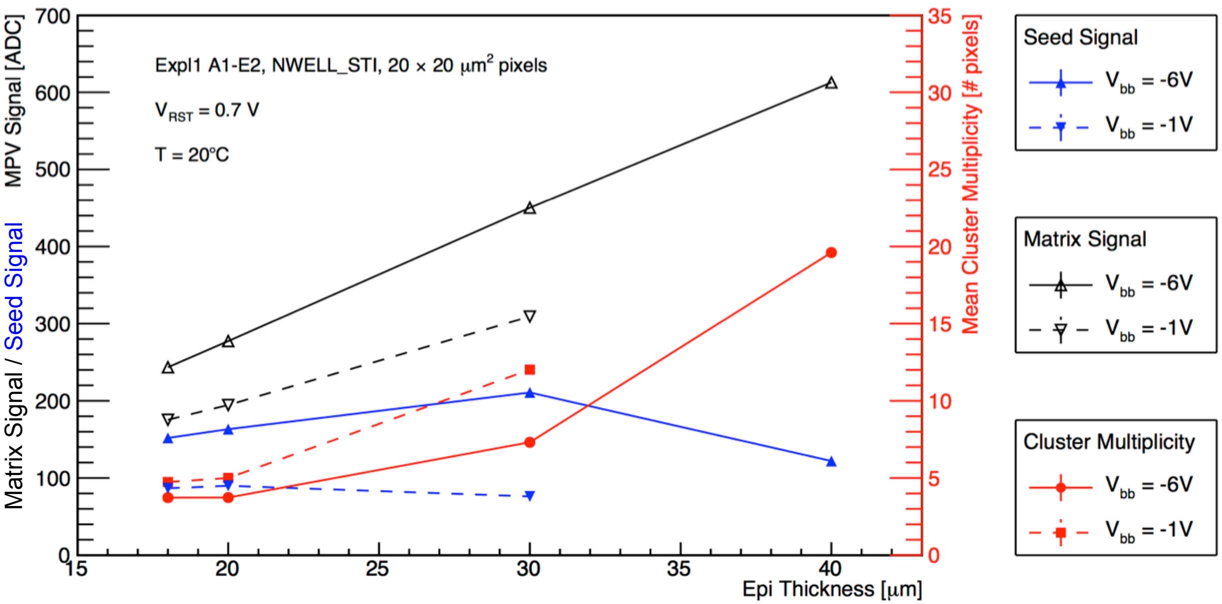
- No influence in range between 1kΩcm and 7.5kΩcm with current pixel layout

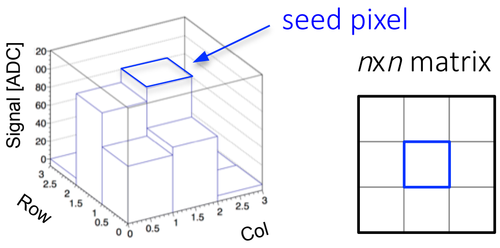
Collection diode geometry

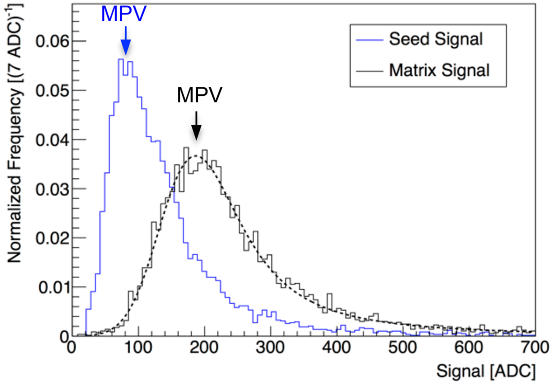
- smaller collection n-well, larger spacing ➔ smaller pixel input capacitance at large V_{BB}

Sensor optimization – Epitaxial layer thickness

2. ALPIDE







Prototypes produced on wafer with different epitaxial layer thickness and resistivity

- increasing epitaxial layer thickness:
  - generated charge (matrix signal) increases linearly
  - cluster size increases non-linearly

Optimum epitaxial layer thickness depending on achievable depletion volume

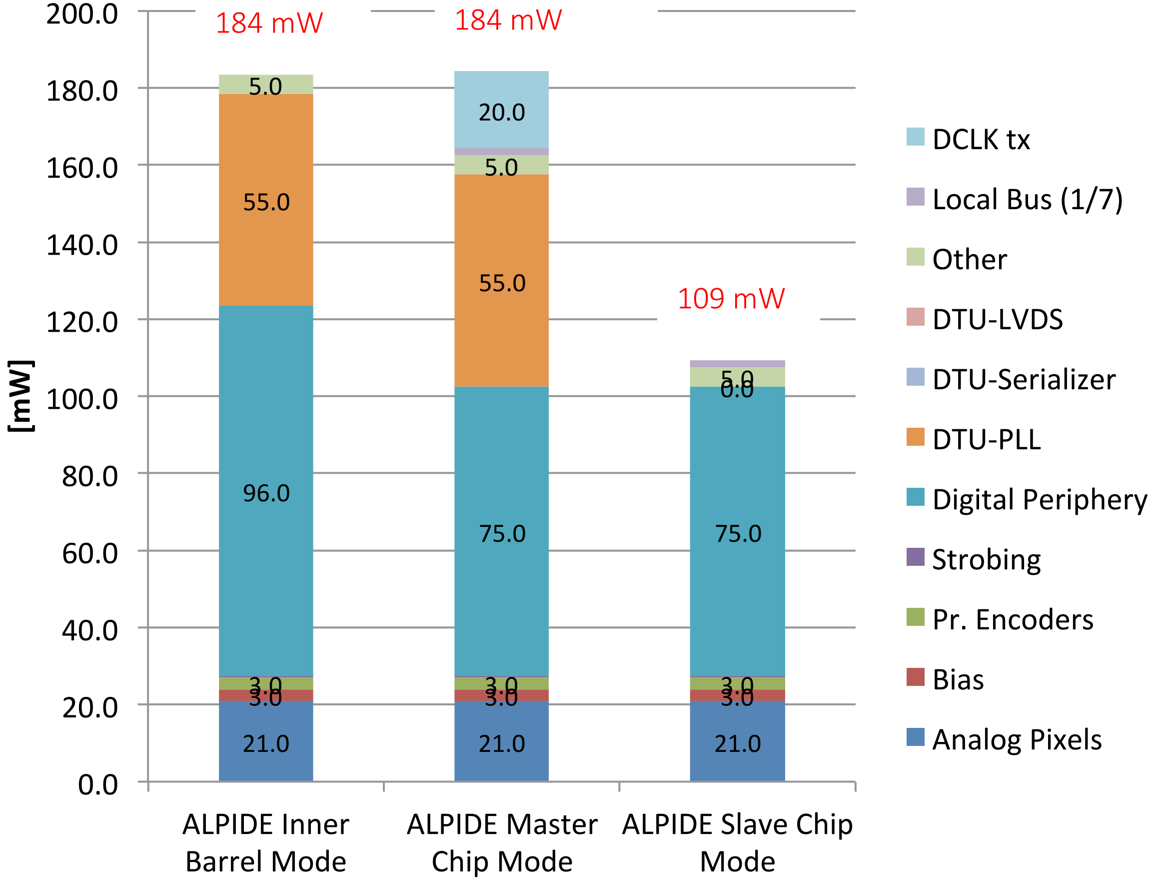
➔ depending on V_{BB} and geometry

Parameters selected for ALPIDE: 25μm epitaxial layer, 2μm n-well diameter, 3μm spacing

ALPIDE: Power consumption

Inner Barrel: 41 mW/cm^2

Outer Barrel: 27 mW/cm^2



Data: combination of available measurements and simulations

Values scaled for readout at 100 kHz rates and max occupancies

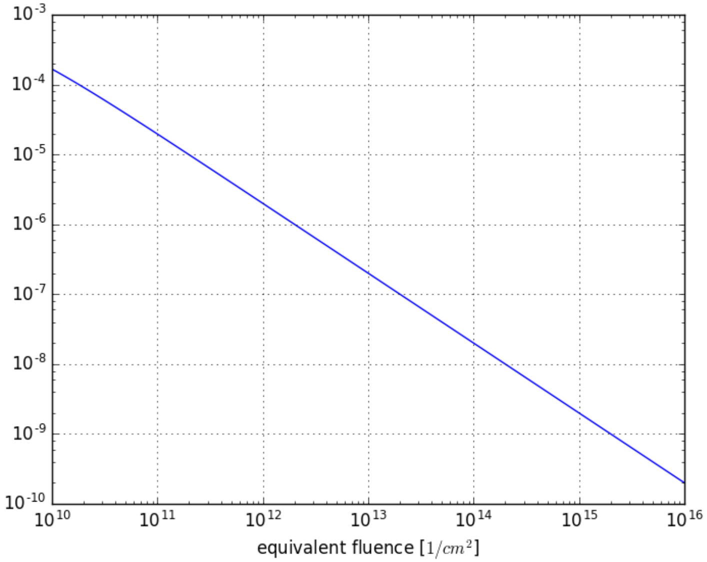
Clock gating enabled

Carrier lifetime after irradiation

- Carrier lifetime after irradiation:

$$1/\tau = 1/\tau_0 + \Phi/K$$

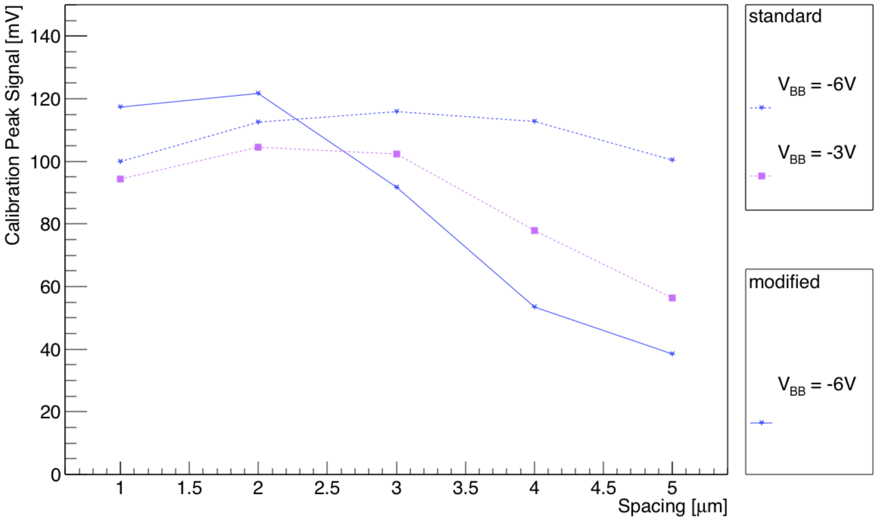
where τ is the lifetime after irradiation, τ_0 is the initial lifetime (~1ms in case of our epitaxial layers), Φ the equivalent neutron fluence, and K the silicon damage constant (~2e6 s/cm^2)

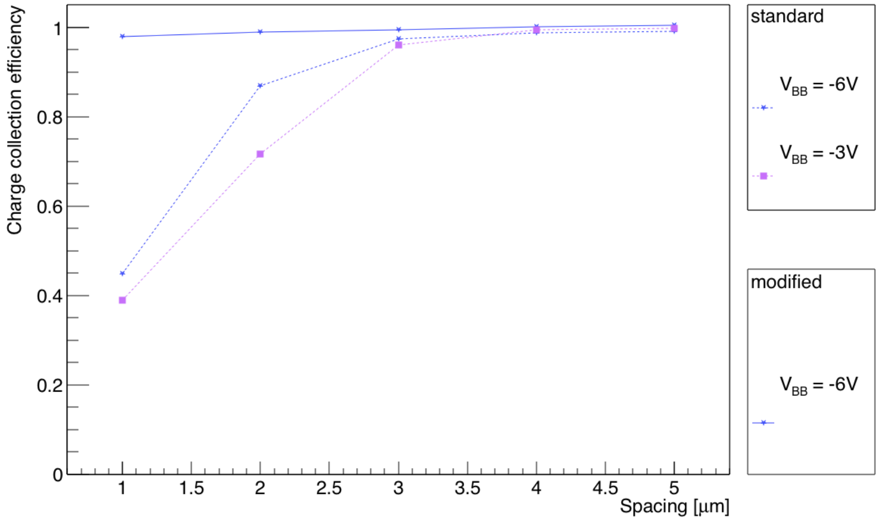


- Considering charge collection time of ~1ns, charge collection efficiency should be high up to fluence of about 1e15 n/cm^2 for modified process
  - Preliminary results pointing in this direction obtained by Heinz Pernegger, Christian Riegler et al. (ATLAS)

Charge-to-voltage conversion gain and charge-collection efficiency

- Example from scan of parameter-space: influence of spacing, at fixed n-well size (2µm), pixel pitch (28µm), and epi-layer thickness (25µm)
  - Plots only representing 5 out of 134 mini-matrices!





- Optimum spacing different for different process variants, and depending on V_{BB} applied

Charge-to-voltage conversion gain and charge-collection efficiency

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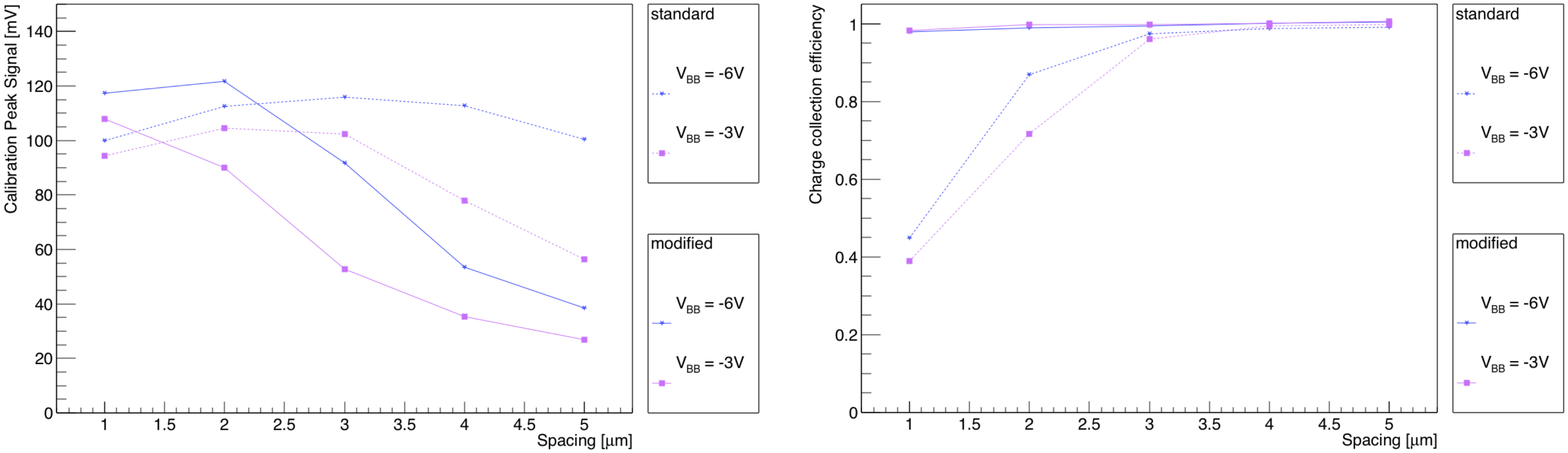
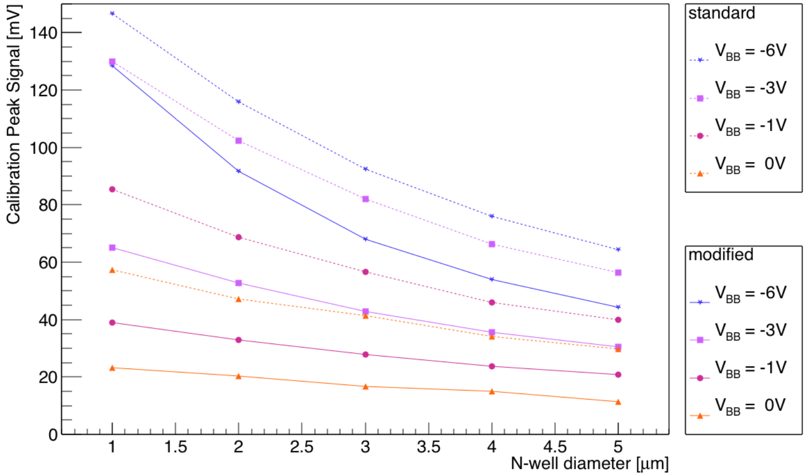


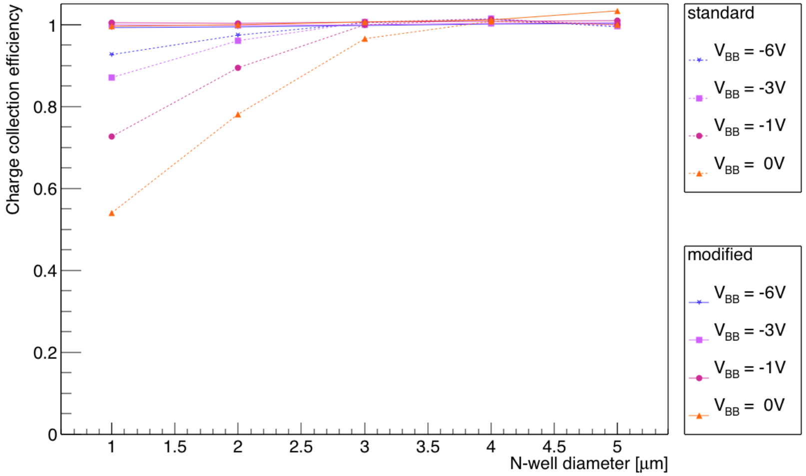
- Optimum spacing different for different process variants, and depending on V_{BB} applied

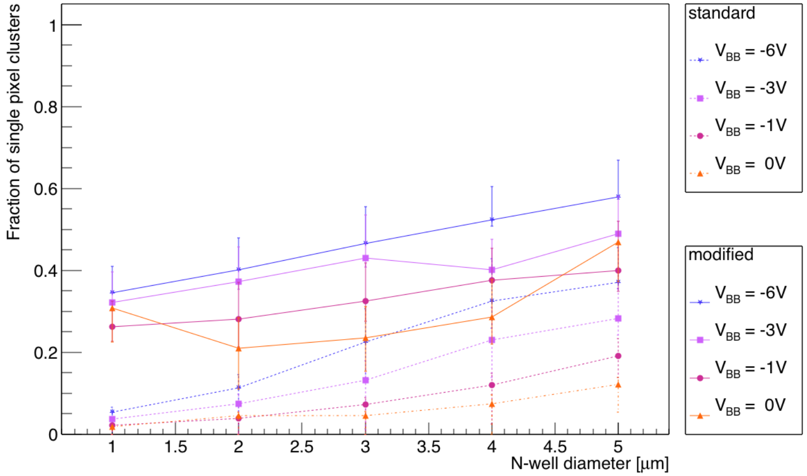
- Optimum pixel design different for different process variants
- INVESTIGATOR provides efficient tool for scanning parameter space

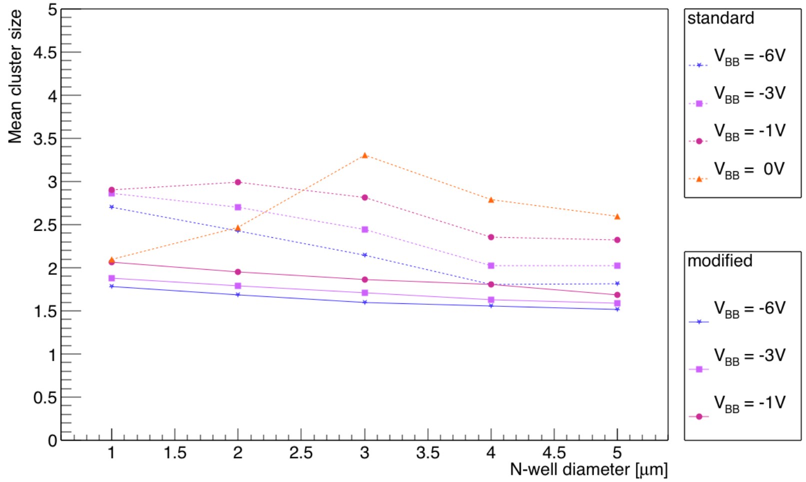
Charge-to-voltage conversion gain and charge-collection efficiency

- Example from scan of parameter-space: influence of n-well diameter, at fixed spacing (3µm), pixel pitch (28µm), and epi-layer thickness (25µm)
  - Plots again only representing 5 out of 134 mini-matrices!



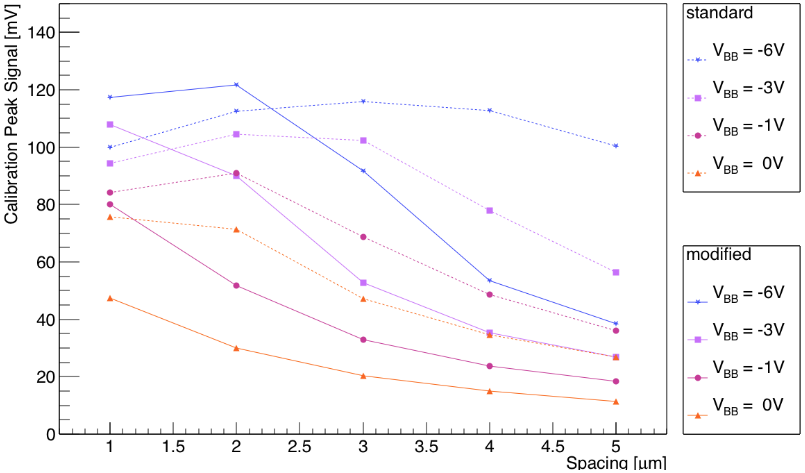


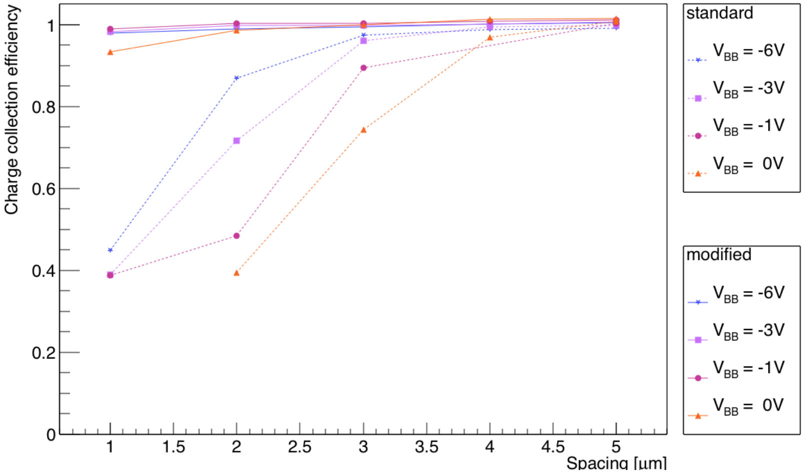


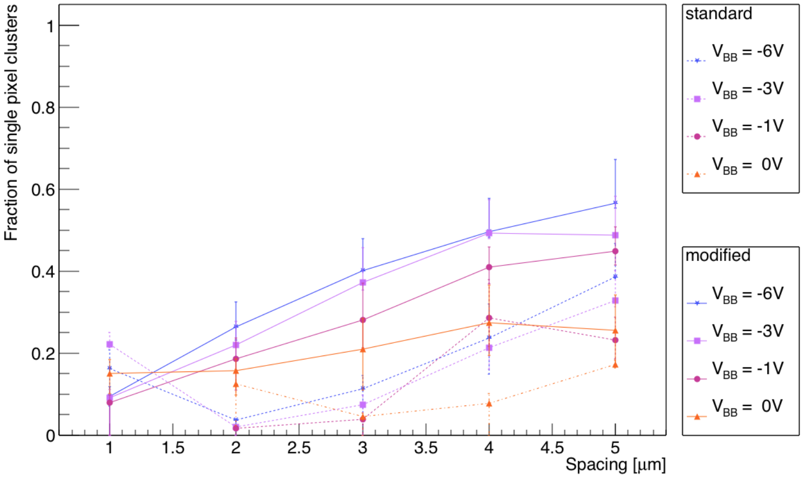


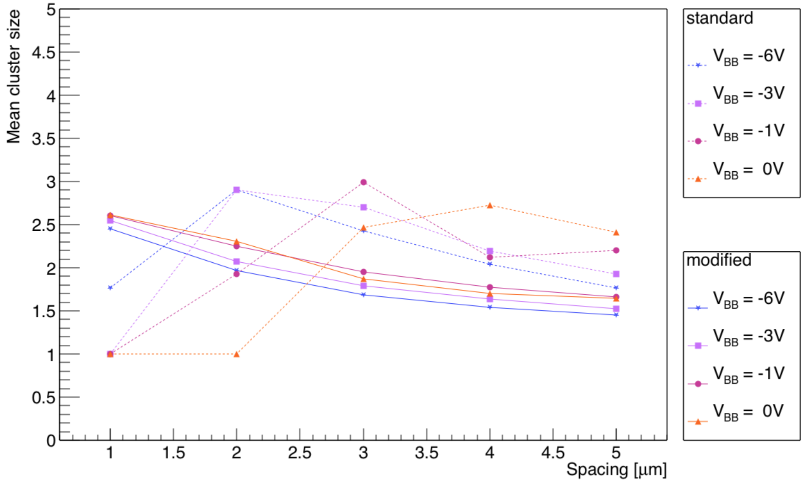
Charge-to-voltage conversion gain and charge-collection efficiency

- Example from scan of parameter-space: influence of spacing, at fixed n-well size (2µm), pixel pitch (28µm), and epi-layer thickness (25µm)
  - Plots only representing 5 out of 134 mini-matrices!



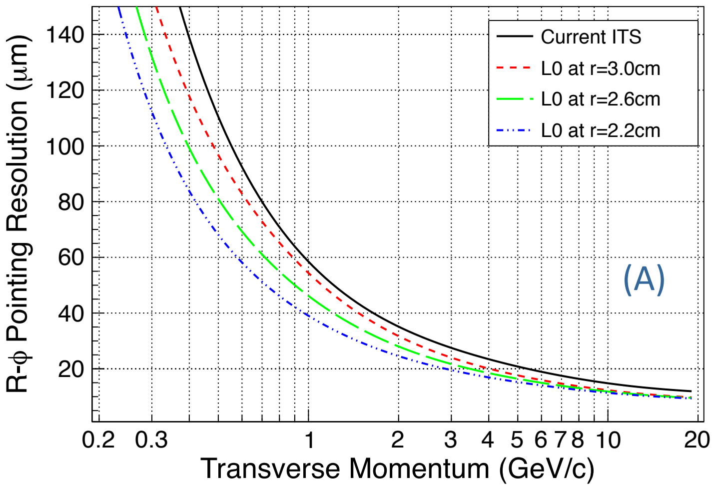




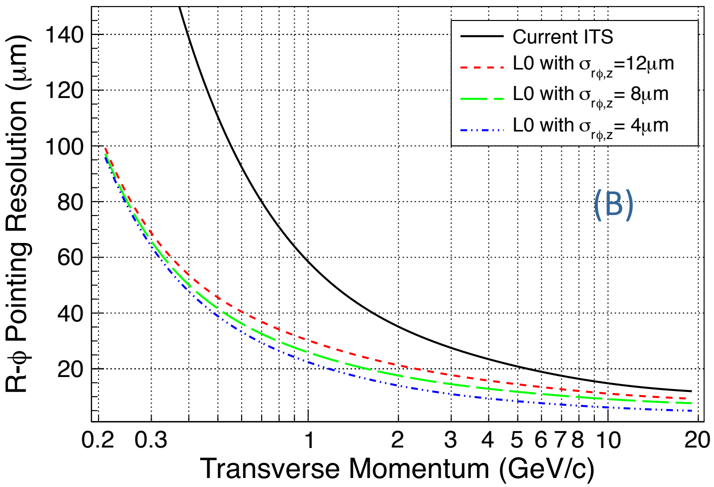


Performance of new ITS: impact parameter studies

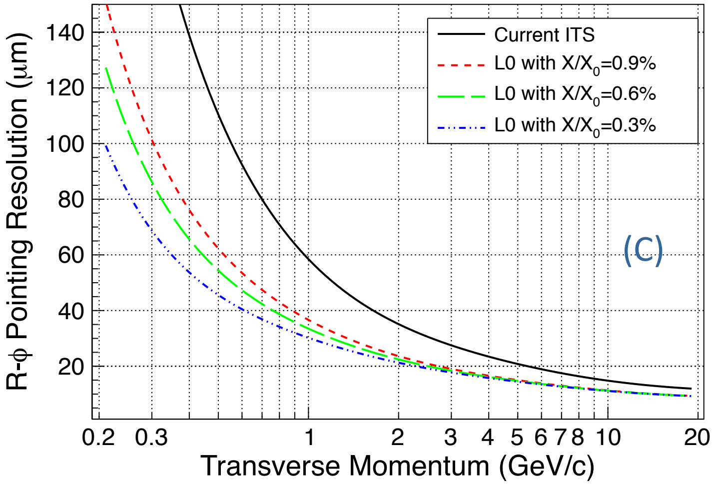
Radial distance to IP



Spatial resolution



Material budget

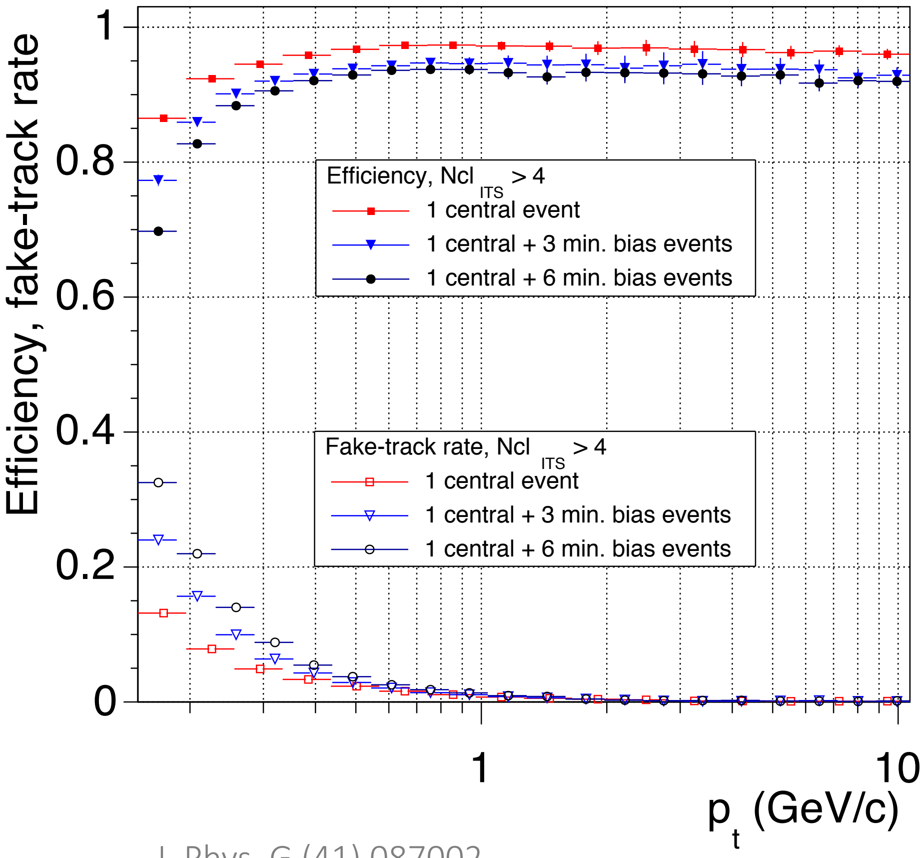


- Current ALICE ITS
  - radial position of first layer: 39mm
  - x/X_0: 1.14% per layer
  - spatial resolution (r-phi): 12 mm
- A) current ITS + L0: x/X0 = 0.3%, res.=4mm;
- B) current ITS + L0: r = 22mm, x/X_0 = 0.3%;
- C) current ITS + L0: r = 22mm, x/X_0 = 0.3%;

ALICE ITS Upgrade CDR, CERN-LHCC-2012-12

Performance of new ITS: Matching efficiency

Matching efficiency between the tracks reconstructed in the upgraded ITS and TPC for different values of event pile-up



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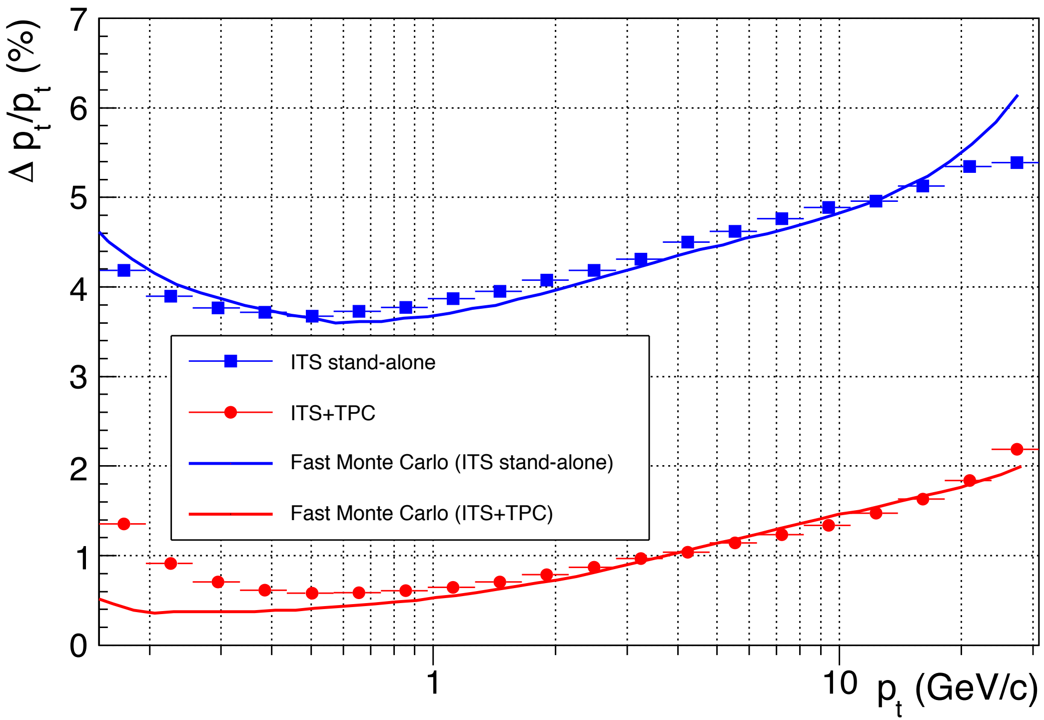
The average event pile-up depends on the interaction rate and detector integration time

interaction rate 50 kHz
integration time: 4 – 30 ms

For 30 ms integration time (worst case design):

<pile-up> = 1 central + 1.5 min. bias

Performance of new ITS (MC): Momentum resolution



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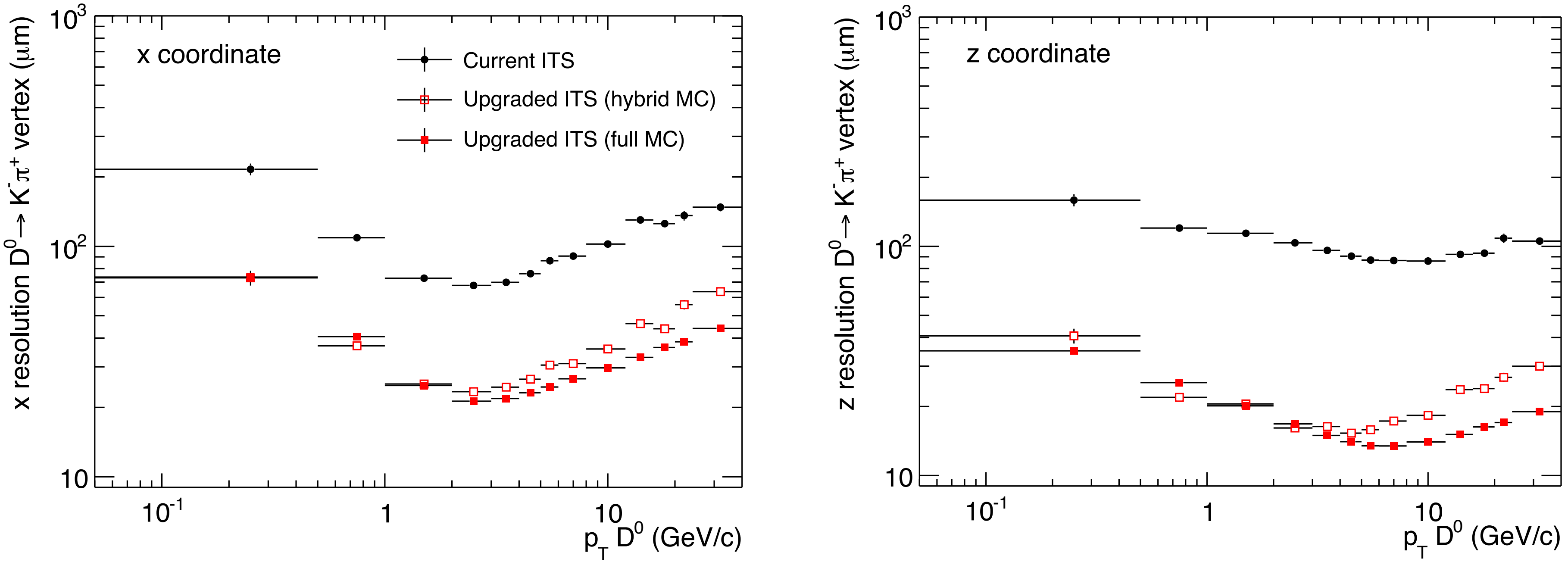
Transverse momentum resolution as function of p_T for primary charged pions for the upgraded ITS and current ITS. The results are shown for ITS standalone and ITS-TPC combined tracking.

Performance of new ITS (MC):

D^0 ➔ K^-p^+ secondary vertex position resolution



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