

FPGAs for next gen DAQ and Computing systems at CERN

Wednesday, 14 September 2016 15:00 (20 minutes)

The need for FPGAs in DAQ is a given, but newer systems needed to be designed to meet the substantial increase in data rate and the challenges that it brings. FPGAs are also power efficient computing devices. So the work also looks at accelerating HEP algorithms and integration of FPGAs with CPUs taking advantage of programming models like OpenCL. Other explorations involved using OpenCL to model a DAQ system.

Presenter: SRIDHARAN, Srikanth (CERN)

Session Classification: Public session