

# Data transfer on manycore processors for high throughput applications

› 14/09/2016

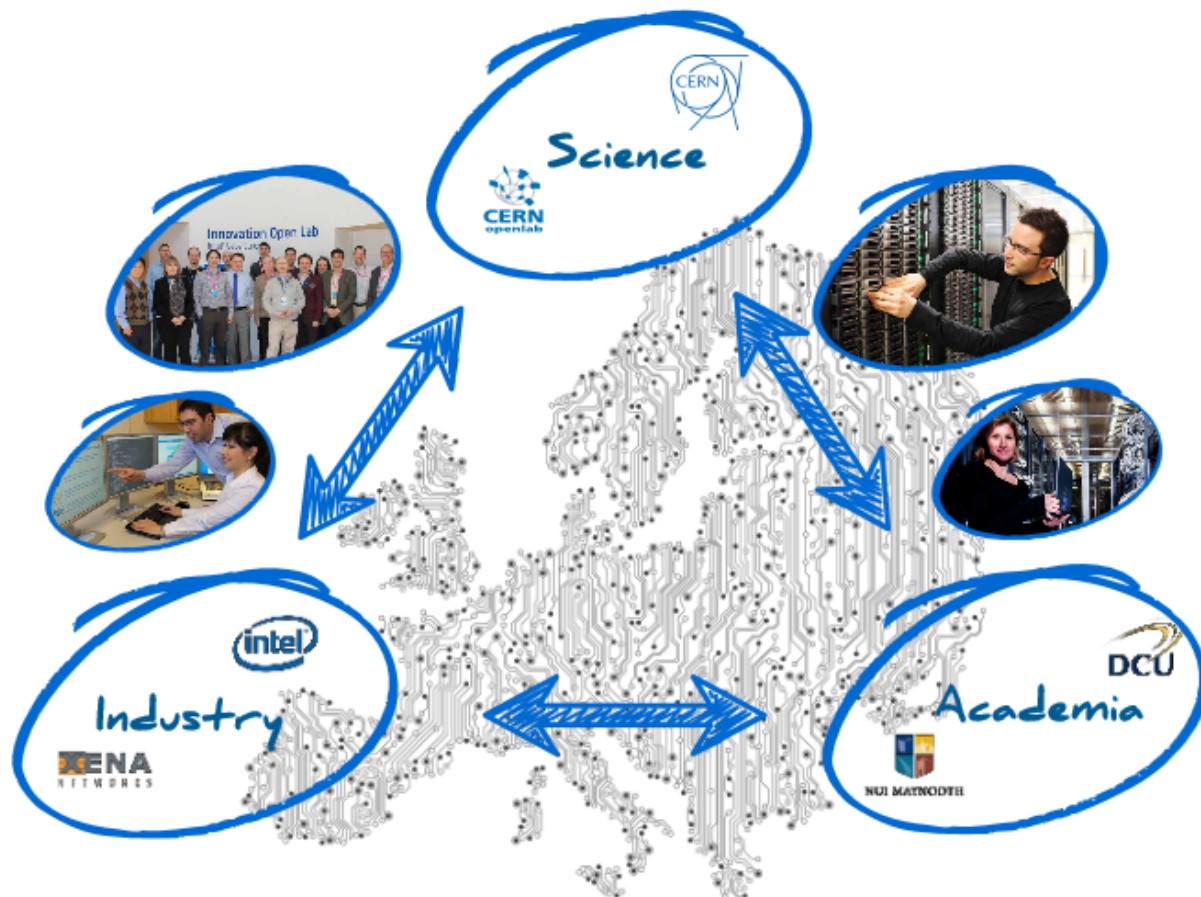
ICE-DIP WP4a - ESR4  
Aram Santogidis



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# ICE-DIP 2013-2017: The Intel-CERN European Doctorate Industrial Program

» A public-private partnership to research solutions for next generation data acquisition networks, offering research training to five Early Stage Researchers in ICT

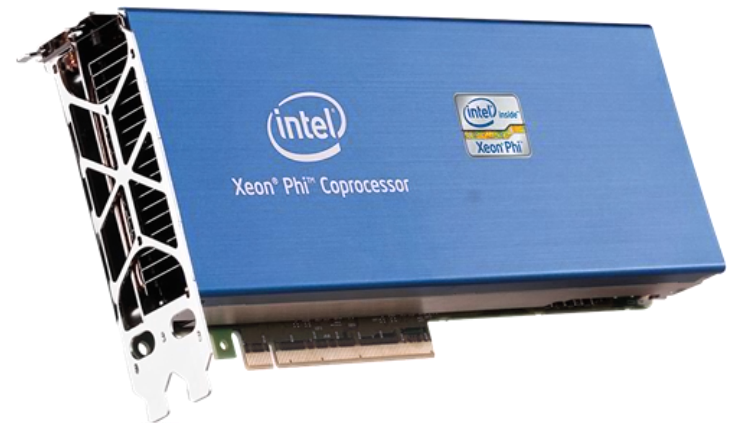


## Research topics:

- ▶ Silicon photonics systems
- ▶ Next generation data acquisition networks
- ▶ High speed configurable logic
- ▶ Computing solutions for high performance data filtering

# Intel Xeon Phi Coprocessor

- › Up to 61 Cores
- › PCIe gen2 Peripheral
- › Different computation modes
  - Offloading
  - Symmetric



# Online processing overview and my focus

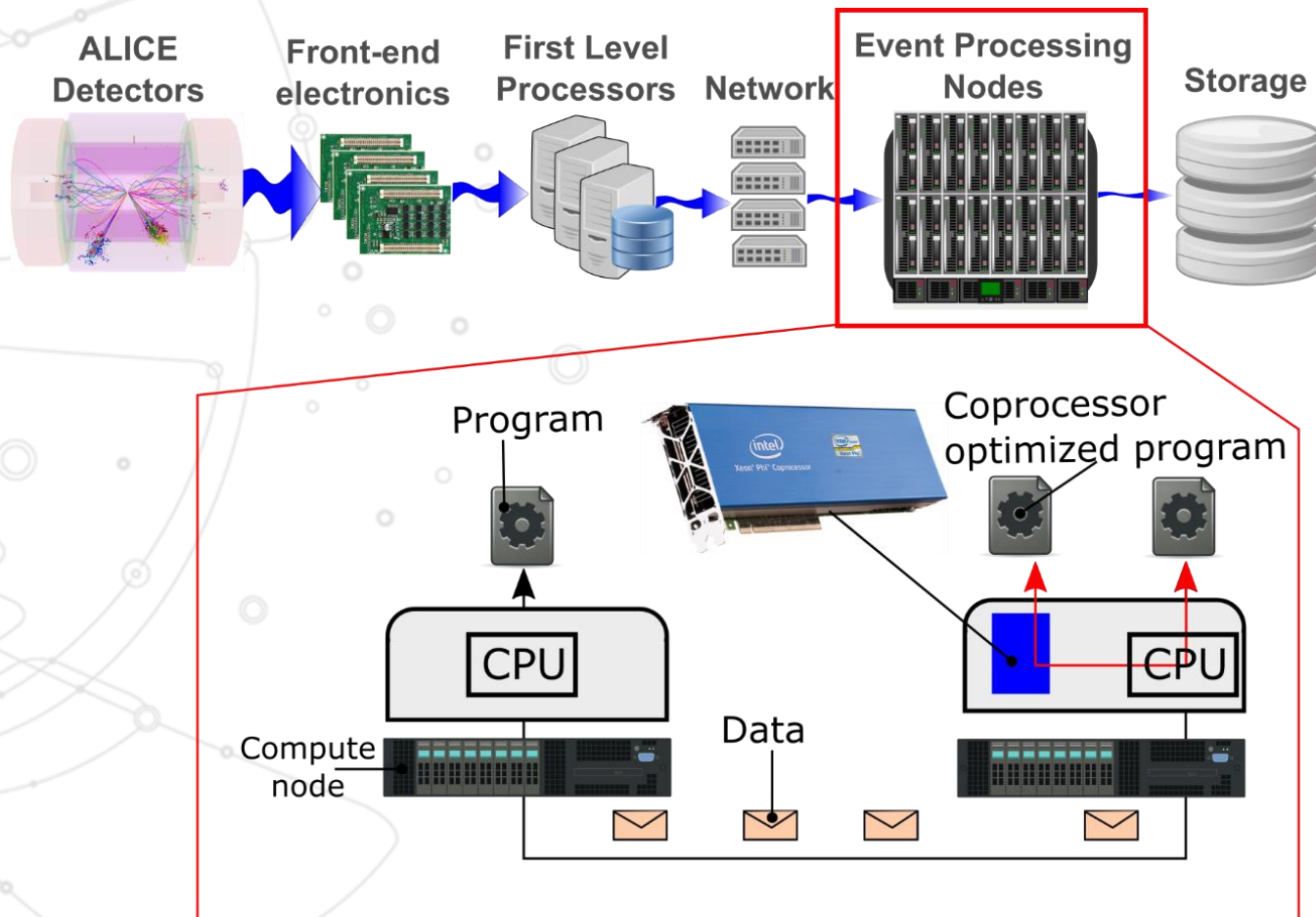
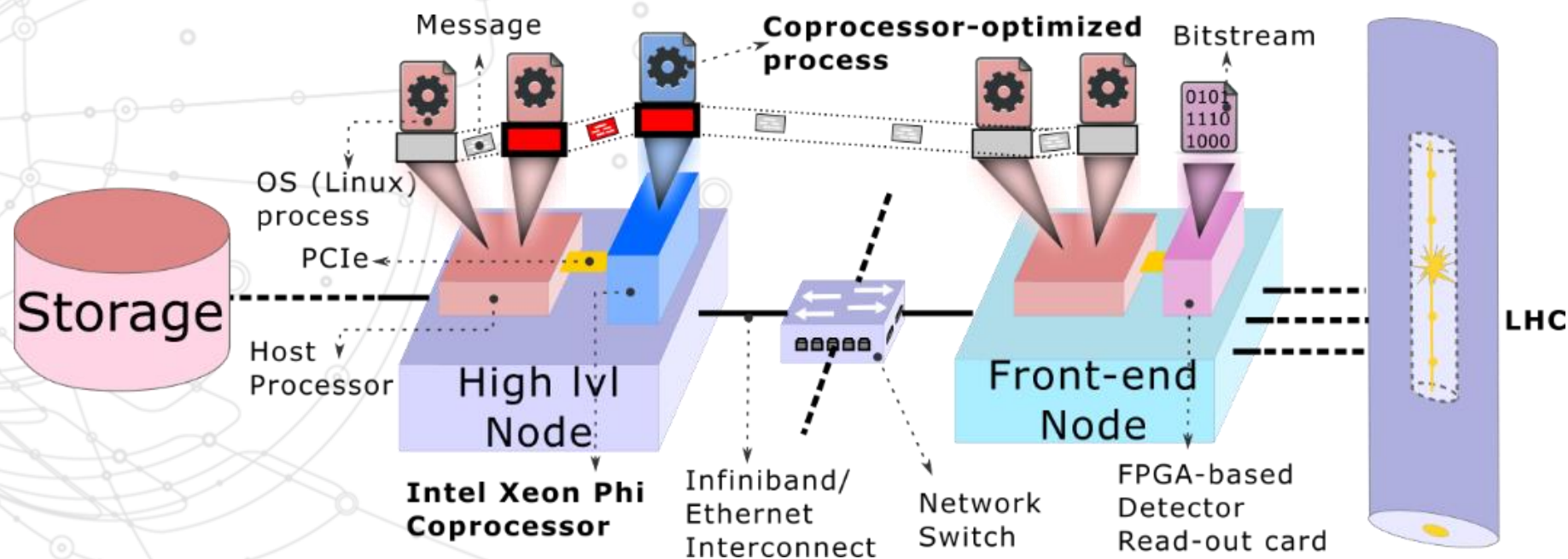


Figure 1. An overview of the ALICE data acquisition process with emphasis on the Event Processing Nodes.



# Coprocessor-Host communication in the online processing system



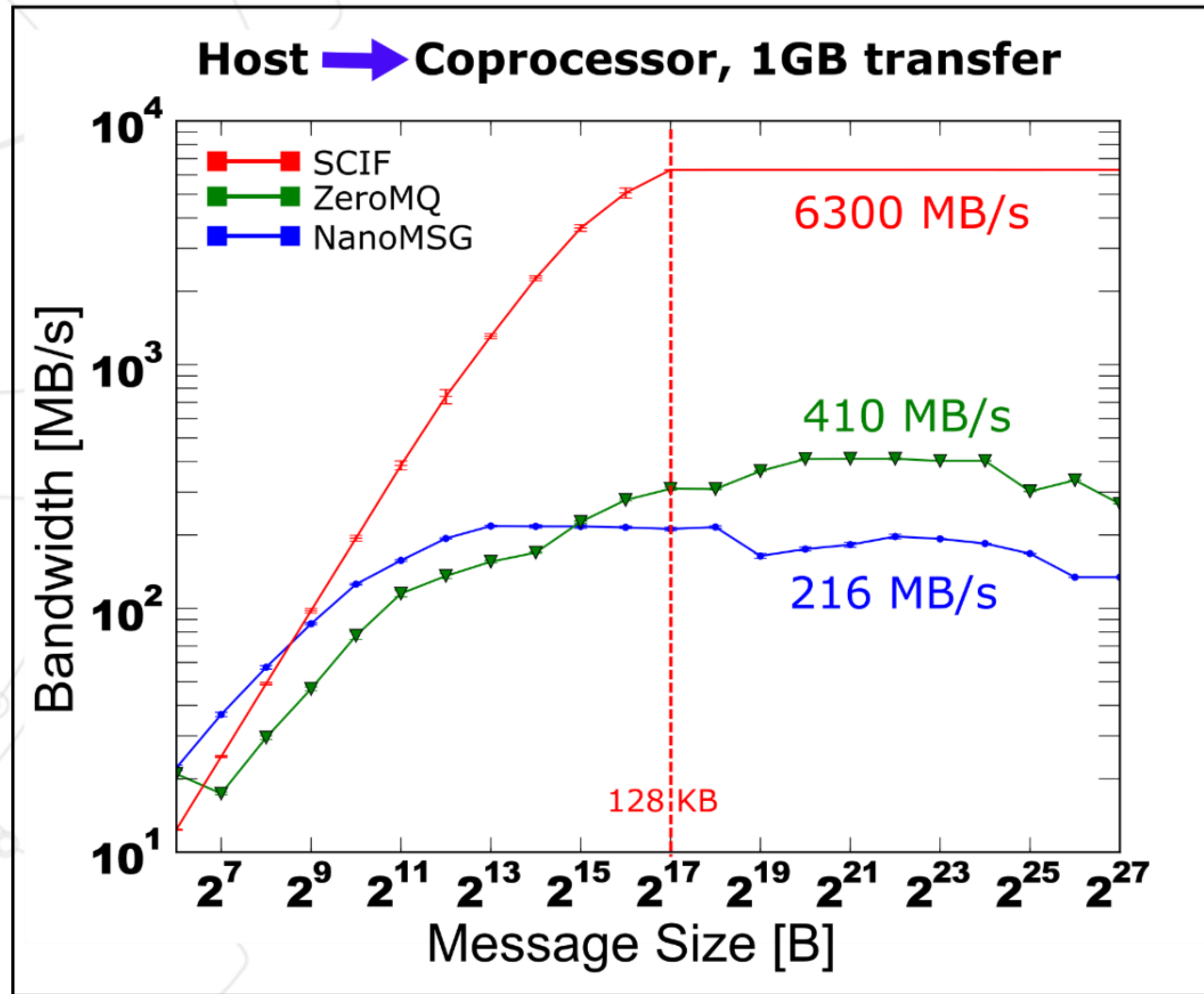
# Data transfer libraries for the data acquisition system of the ALICE experiment

# ØMQ

## nanomsg

- › Instant messaging for computers
- › Helps to create distributed systems
- › Provides good performance
- › Easy to program from non-expert programmers

# An opportunity for improvement



**Figure 2 .** This plot corresponds to a performance test of transferring 1GB payload in chunks from 4KB to 128MB[1].

# CHEP'15 poster contest award





# The Trans4SCIF library the Intel Xeon Phi Coprocessor

- › **Easy-to-use socket-like interface**
  - Send/Recv
- › **E.g. up to 3 GB/s data throughput (4x improvement with the cost of 32 MB of memory space)**
- › **Exploits cache-aligned RDMA transfers over PCIe**
- › **ZeroMQ extension for SCIF**
- › **In principle can be re-used by other RDMA based transports (e.g OmniPath)**

# Outreach and dissemination

## › Publication

- A. Santogidis, A. Hirstius, and S. Lalis. “Optimizing the transport layer of the ALFA framework for the Intel Xeon PhiCoprocesor” Proceedings of the 21st International Conference on Computing in High Energy and Nuclear Physics, April 2015, Okinawa, Japan, 2015.

## › Many talks were given to diverse audiences and places

- CHEP’15, Okinawa, Japan
- Augmented reality lab, Hong Kong
- inverted CERN School of Computing, Geneva
- thematic CERN School of Computing, Split

## › Some more are planned for the immediate future

- Huawei Labs, Paris
- Undergraduate students of University of Thessaly, Volos, Greece

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