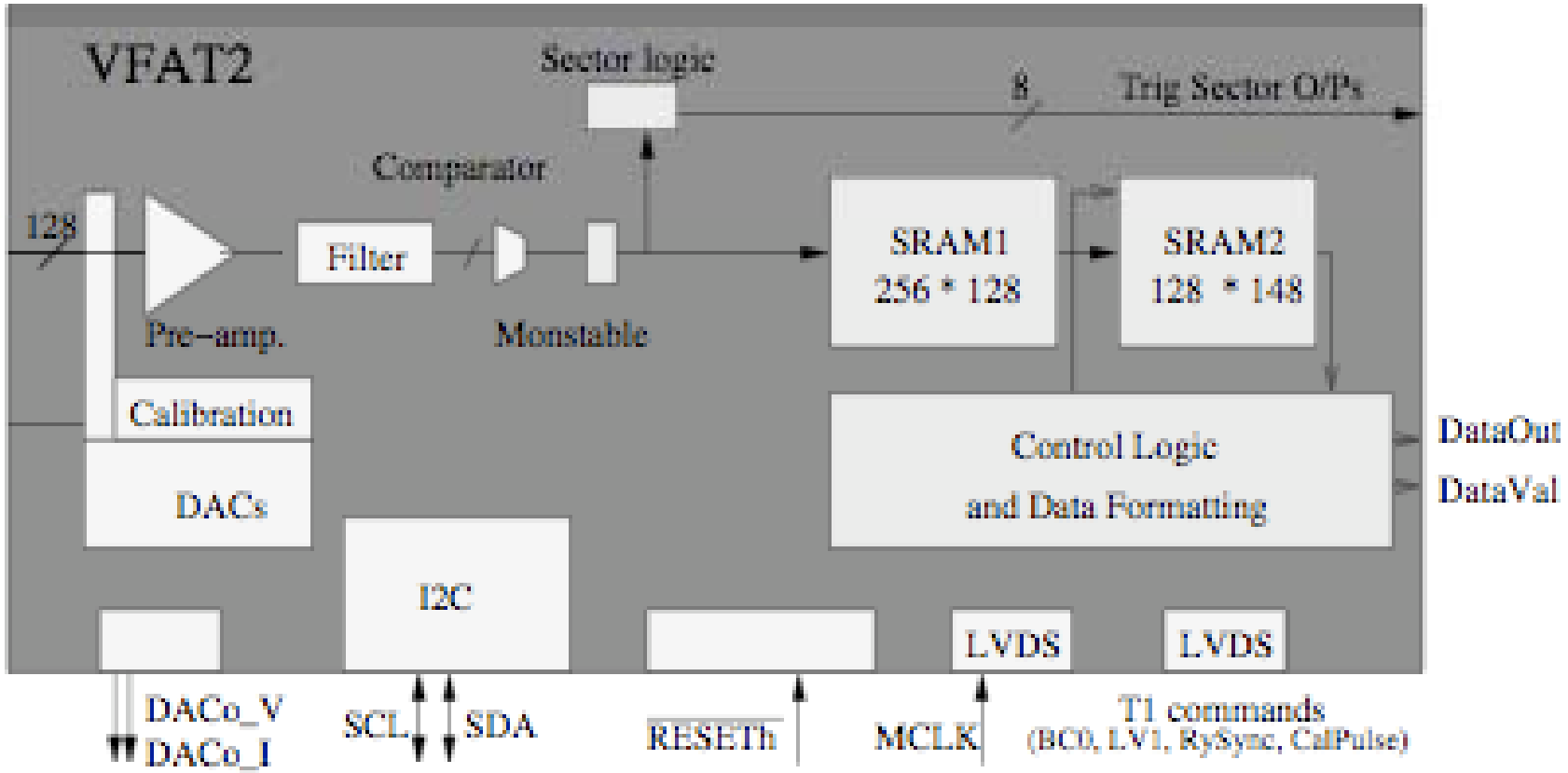
THE VFAT

What is the VFAT

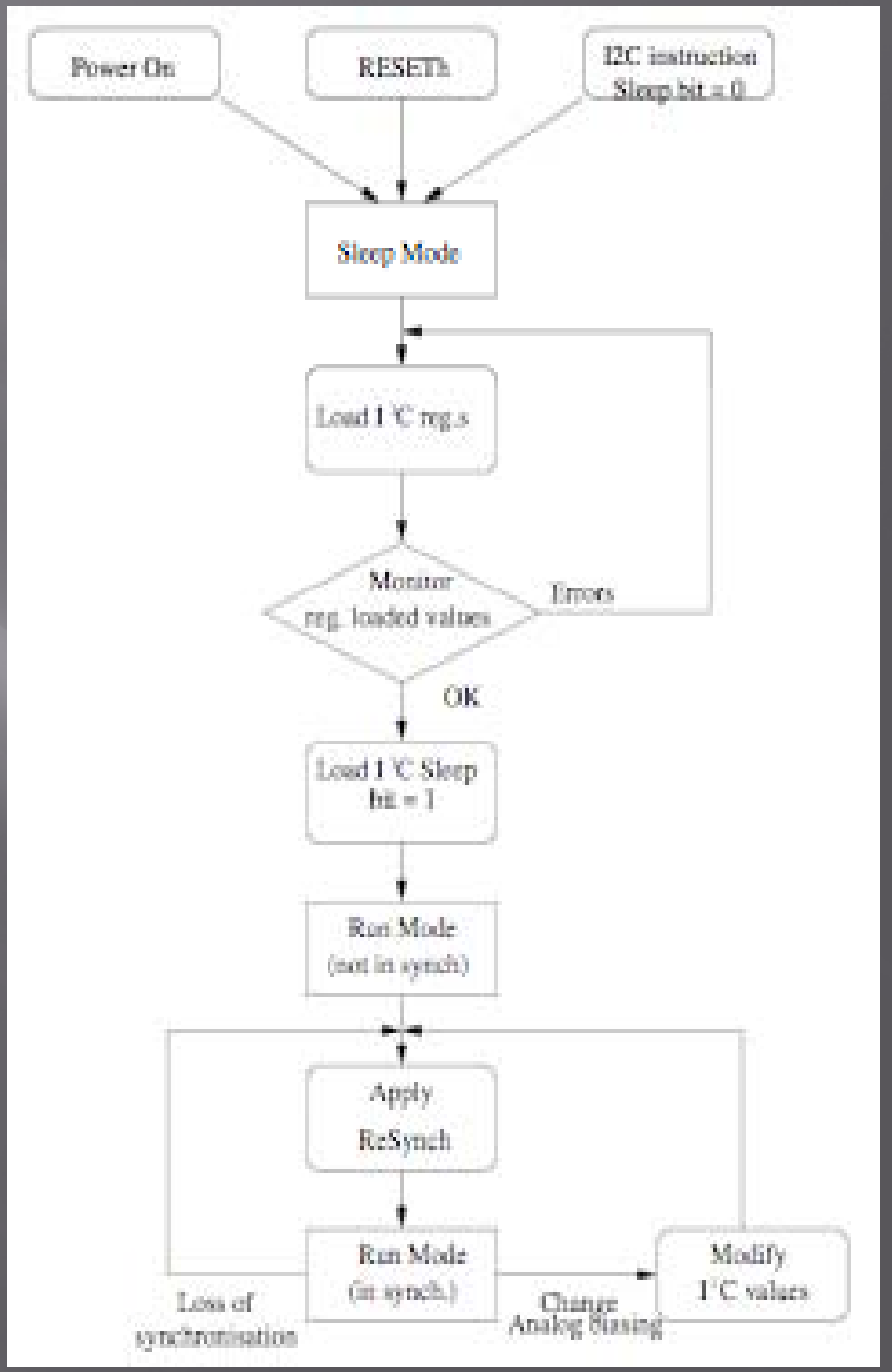
- VFAT is a front-end chip designed specifically to read out the Roman Pot silicon detectors of the Totem experiment
- It is a digital on/off chip, with an adjustable threshold for each of the 128 channels.
- It was decided to use it in all the Totem detectors, the GEMs and the CSCs to simplify the DAQ and trigger design
- For the gas detectors a special version has been developed with an internal protection diode network for each of the 128 input channels.

VFAT block diagram

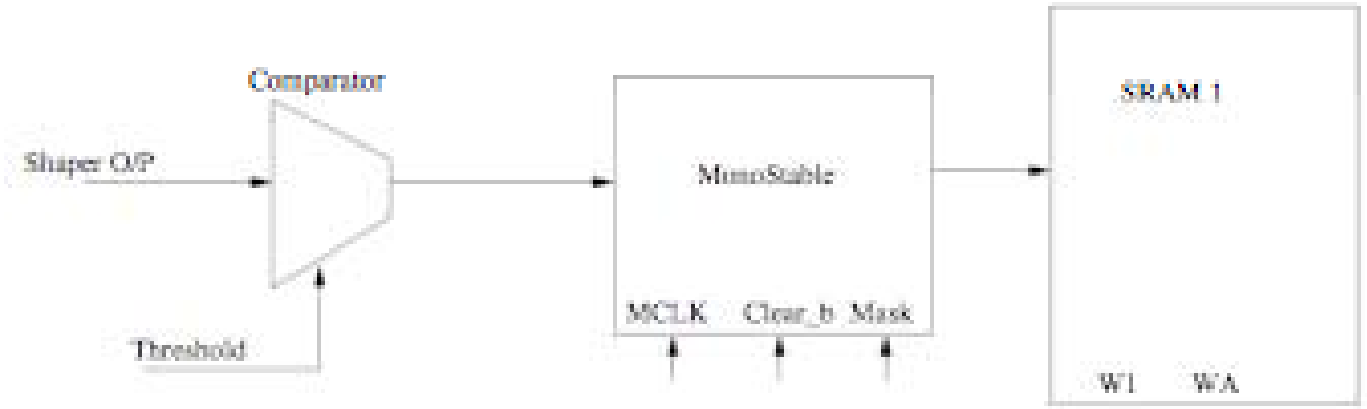


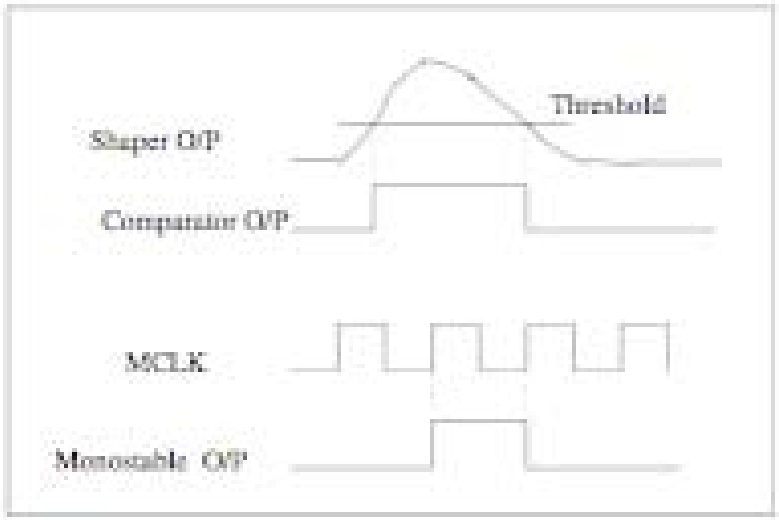
Internal registers

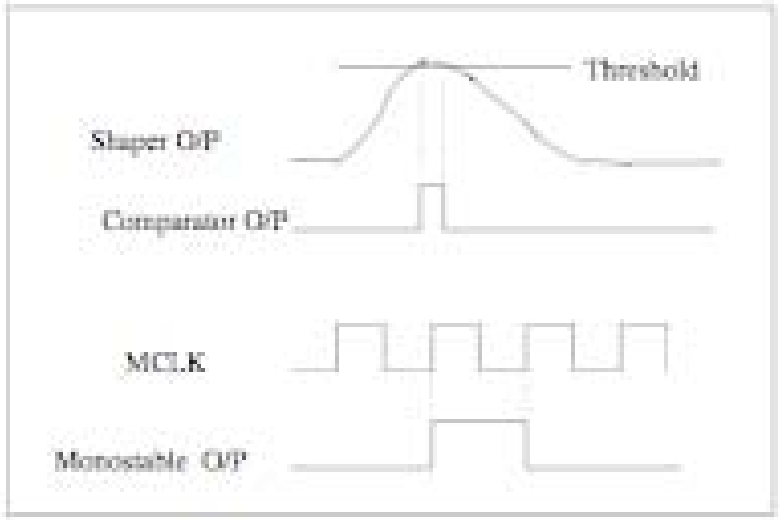
- The internal registers to set up are 128.
- An I2C line with 2 serial signals, SCL/SDA, allows read nad write operations of all the registers
- The power cycle is described in this flow chart.



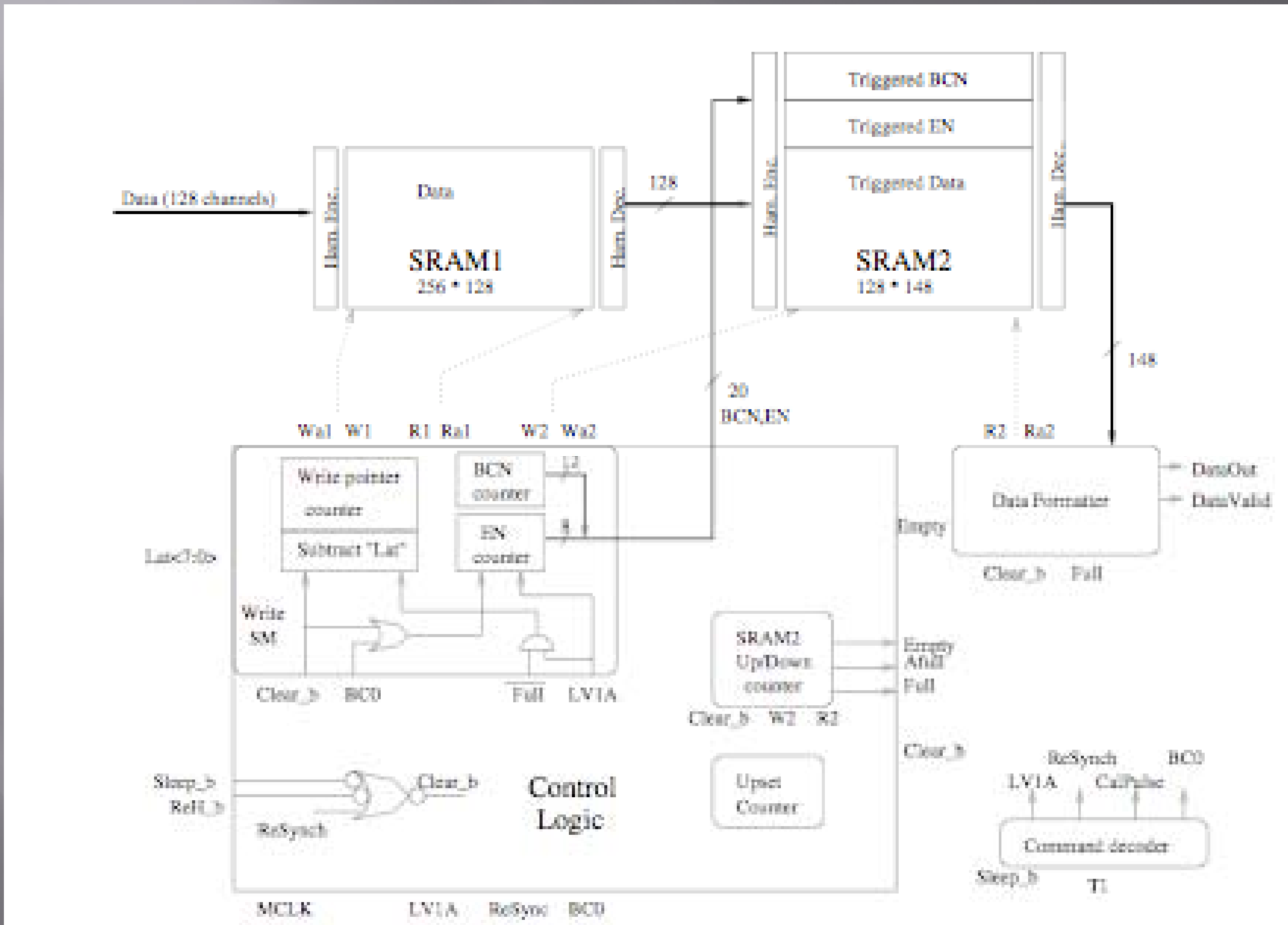
The input stage





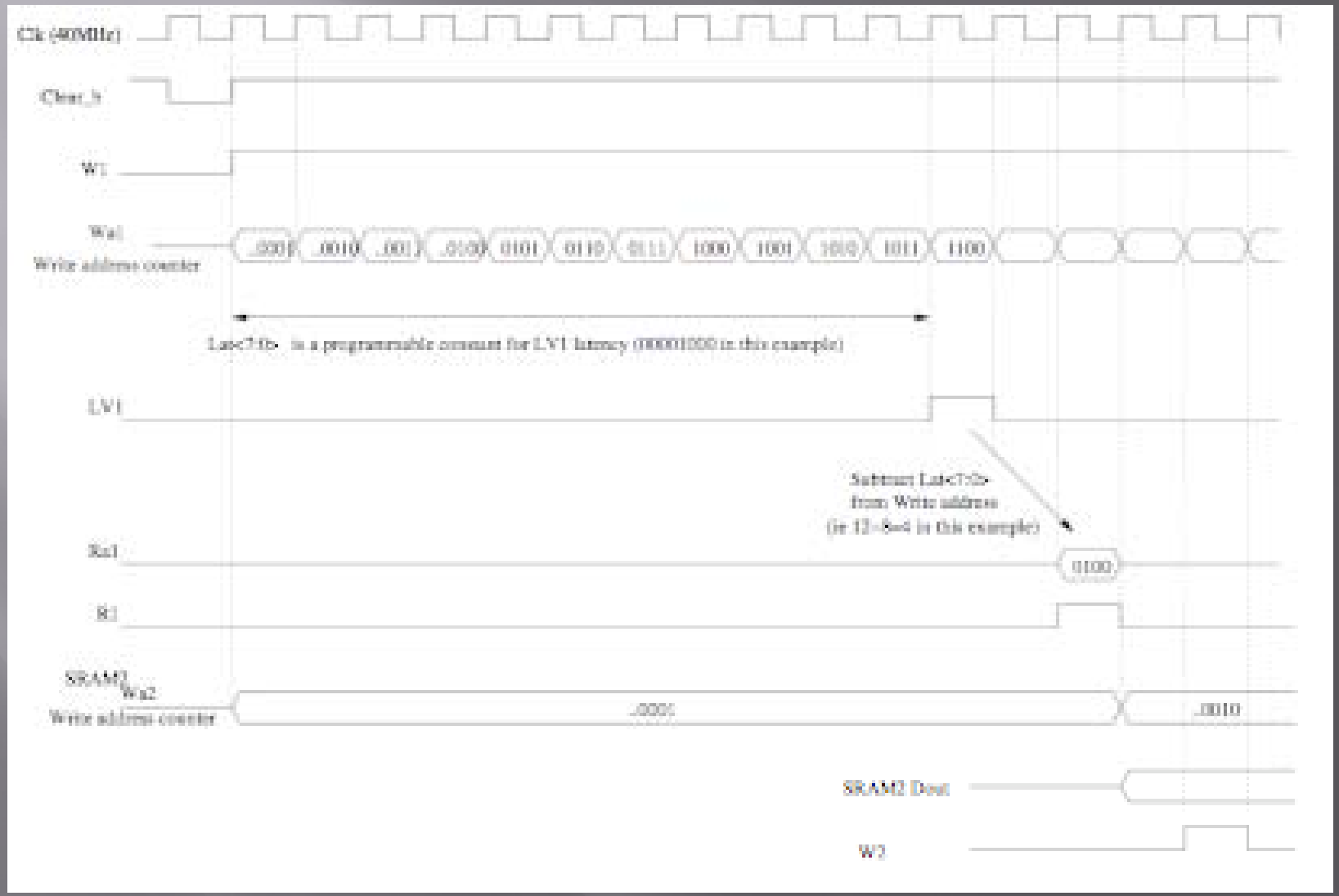


R/O



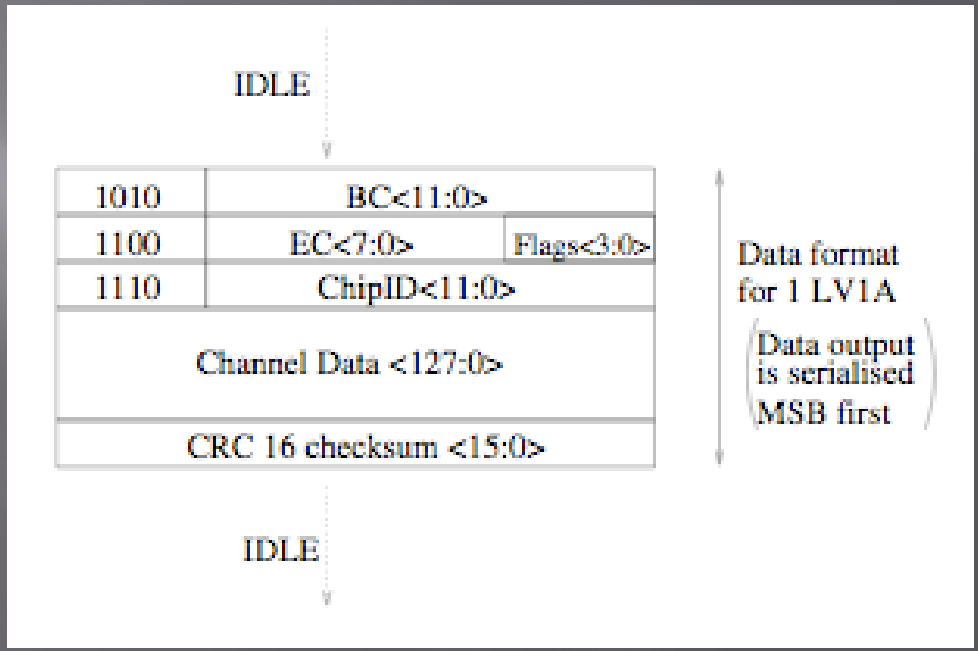
Triggered BCN
Triggered EN
Triggered Data
SRAM2
128 * 148
Data (128 channels)
Data
SRAM1
256 * 128
128
148
20
BCN,EN
Wa1 W1 R1 Ra1 W2 Wa2
R2 Ra2
Write pointer counter
Subtract "Lat"
BCN counter
EN counter
Data Formatter
DataOut
DataValid
Empty
Clear_b Full
Write SM
Clear_b BC0
Full LV1A
SRAM2 Up/Down counter
Empty
Afull
Full
Clear_b W2 R2
Clear_b
Sleep_b
ReSynch
Control Logic
Upset Counter
ReSynch BC0
LV1A CalPulse
Command decoder
Sleep_b
T1
MCLK LV1A ReSync BC0

The R/O latency



The R/O serial frame

The data out is serial, an LVDS DATA_OUT signal and a DATA_VALID synchronization signal are used to readout the frame. The frame is 192 bits long and is read at 40 MHz speed.



Trigger sectors

Self triggering operations are foreseen, and there are 8 output bits hat can be programmed as described in the tables below.

TrigMode⟨2⟩	TrigMode⟨1⟩	TrigMode⟨0⟩	Function
0	0	0	No Trigger (default)
0	0	1	One sector (S1)
0	1	0	Four sectors (S1 to S4)
0	1	1	Eight sectors (S1 to S8)
1	X	X	GEM mode (S1 to S8 as defined in table 10)

GEM mode channel assignment					
Sector	Channel assignment to sector				
S1	4	28	52	76	100
	5	29	53	77	101
	6	30	54	78	102
S2	7	31	55	79	103
	8	32	56	80	104
	9	33	57	81	105
S3	10	34	58	82	106
	11	35	59	83	107
	12	36	60	84	108
S4	13	37	61	85	109
	14	38	62	86	110
	15	39	63	87	111
S5	16	40	64	88	112
	17	41	65	89	113
	18	42	66	90	114
S6	19	43	67	91	115
	20	44	68	92	116
	21	45	69	93	117
S7	22	46	70	94	118
	23	47	71	95	119
	24	48	72	96	120
S8	25	49	73	97	121
	26	50	74	98	122
	27	51	75	99	123

The readout electronics

- For the Totem experiment a CMS-like chain has been developed in order to be compatible with the larger hosting experiment.
- Rad hard chips are used to withstand the large radiation foreseen on all the detectors areas.
- The chain is connected to the counting room through fiber optic lines using the same hardware developed by CMS experiment.

Test Beam operations

- We are developing a simple board, hosting 8 separate Hybrids with one VFAT each.
- The board is connected through 50 pins ERNI connectors to the Hybrids
- One single FPGA (Altera StratixII) is responsible for all the operations, generating the I2C protocol and controls the trigger and readout of the chips.
- The communication with the computer is dome via USB2 connection

Extension of TB board

- The TB board has the possibility to daisy chain with other boards, for a total of 8 of them, in order to control up to 64 chips, for a total of 8320 input channels with one USB line
- More USB connections can be added to expand the system to larger objects
- The Board is foreseen for the summer Test Beam.